

# AUXILIARY LOGIC RELAY TYPE SLA54K



# GEK-86672

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## AUXILIARY LOGIC UNIT

#### TYPE SLA54K

#### DESCRIPTION

The SLA54K is an auxiliary logic relay designed for use in a directional comparison blocking scheme. The relay contains the necessary logic to interpret output signals from associated measuring functions and translate them to an appropriate auxiliary output and tripping relay. In addition to the SLA54K relay, proper phase and ground relays, a power supply, and auxiliary tripping relay are required to complete a particular relaying scheme.

The SLA54K relay is packaged in a four-rack unit enclosed metal case. The relay is suitable for mounting in a 19-inch rack; the outline and mounting dimensions are shown in Figure 1. Internal connections for the SLA54K relay are shown in Figure 2, and the component location drawing is shown in Figure 3.

#### **APPLICATION**

The SLA54K auxiliary logic relay is designed to operate in conjunction with appropriate phase and ground relays and a suitable communication channel to provide a permissive overreaching transferred tripping scheme for transmission line protection. For a complete description of the particular scheme, refer to the overall logic diagram and the logic description write-up supplied with the scheme.

Protection features required in a relay scheme often vary with the particular application. It is sometimes desirable to initially provide certain features in a relaying scheme and simultaneously to make provisions for adding or changing features should it later become necessary. To this end, this relay design has incorporated circuit flexibility to permit implementation of certain optional features. To implement these features the relay is equipped with matrix connection blocks designated R, Y, OR, V, W, G, BR and B. Appropriate jumper connections are made between the various points to modify the logic. A typical option chart is shown in Figure 5.

Various points in the logic can be monitored by connecting jumpers from the cable plugs 411-420 to the selected matrix points. This option is further described under the heading DATA MONITORING POINTS in the section entitled **OPERATING PRINCIPLES**.

For the specific options and the logic arrangement supplied for a particular relaying scheme, refer to the logic diagram and the logic description supplied with that scheme. If it is desired to make logic changes, the diagrams and instruction books supplied with the equipment should be studied to determine the means for implementing the changes. If further assistance is required, contact the nearest General Electric District Sales Office.

These instructions do not purport to cover all details or variations in equipment nor to provide for every possible contingency to be met in connection with installation, operation or maintenance. Should further information be desired or should particular problems arise which are not covered sufficiently for the purchaser's purposes, the matter should be referred to the General Electric Company.

To the extent required the products described herein meet applicable ANSI, IEEE and NEWA standards; but no such assurance is given with respect to local codes and ordinances because they vary greatly.

There are no measuring functions to be set in this relay but there are certain timers included that must be set in accordance with the demands of the particular protection scheme being employed and the power system on which it is being used. Refer to the section of this book entitled **SETTINGS** for a description of these timers and for suggestions to be used in making appropriate settings.

#### RATINGS

The Type SLA54K relay is designed for use in an environment where the air temperature outside the relay case does not exceed minus  $20^{\circ}\text{C}$  or plus  $65^{\circ}\text{C}$ .

The Type SLA54K relay requires a plus or minus 15 volt DC power source which can be obtained from a Type SSA power supply.

Each contact converter in this relay has a link for selecting the proper voltage for the coil circuit on the contact converter. The three possible voltages are 48, 125 and 250 volts DC.

#### **BURDENS**

The SLA54K relay presents a burden of 300 milliamperes to the plus 15 volts DC supply of the Type SSA power supply.

Each contact converter, when energized, will draw ten milliamperes from the station battery, regardless of tap setting.

#### OPERATING PRINCIPLES

# LOGIC CIRCUIT

The functions of the Type SLA54K relay involve basic logic (AND, OR, and NOT) where the presence or absence of signals, rather than their magnitude, controls the operation. Signals are measured with respect to a reference bus accessible at TP1. In general, a signal below one volts DC represents an OFF or LOGIC ZERO condition; an ON or LOGIC ONE condition is represented by a signal of approximately plus 15 volts DC.

The symbols used on the internal connection diagram (Figure 2) are explained by the legend shown in Figure 4.

The matrix block options shown in the internal connections of the SLA54K relay are prewired at the factory. The connections are shown on the associated overall logic and are listed on the associated option chart. A sample option chart for the Type SLA54K relay is shown in Figure 5.

Some logic cards contain pushbuttons which allow injection of a logic "Level-1" signal into various logic paths for testing purposes.

#### CONTACT CONVERTERS

Six contact converters are provided in the SLA54K relay. A contact converter provides an interface between the logic circuits in the SLA54K and the external signals.

CC1 through CC6 are connected to option points (see Figure 2) and can be connected as desired. To determine the connections used on a particular equipment, see the corresponding option chart drawing.

# MONITORING POINTS

Various points within the relay logic are brought out to a cable plug mounted on the back of the SLA54K relay. These plugs provide 18 monitoring points plus one point for a voltage reference. Specific points that have been preselected are shown on the logic diagram marked with a number series of 411 to 420. These points may be augmented or readily changed at the matrix boards located inside the SLA relay. To monitor these points, an additional piece of equipment called a DLA (data logging amplifier) is required. The dry contact outputs from the DLA can be fed to an oscillograph to record selected function responses. A typical selection of monitoring points is shown below:

- 413 Phase overcurrent
- 414 Ground overcurrent
- 415 Phase overcurrent
- 416 Phase distance measurement output 417 - Ground distance measurement output
- 418 Local comparer input
- 419 Remote comparer input
- 420 Comparer output

# CHANNEL INTERFACE

The logic of the Type SLA54K relay includes an isolation interface (Figure 6) between the relays in the scheme and the associated channel. The circuitry of the isolation interface provides a signal path but maintains metallic isolation. This feature makes it possible to maintain isolation between the DC supply used for the relays and that employed by the channel.

Operation of the three functions (received carrier, transmitter control and transmitter auxiliary stop) of the isolation interface can be checked without direct connection to the subassembly. External test connections are made to the pins of the C111 socket mounted on the rear of the unit (see Figure 2). Logic circuit test connections are made at the socket pins of the channel control card in position "L."

Received carrier operation test connections are shown in Figure 8A. For this test do not remove the channel control card in position "L." Closure of the normally open contact will simulate a received carrier signal and the scope will go from a logic "O" to a logic "1."

For the transmitter control and transmitter auxiliary stop checks, remove the channel control card "L" from its socket and replace it with a test card adapter and

test card to gain access to the "L" socket pins. Transmitter control test connections are shown in Figure 8B. The test contact in the open position simulates a logic '1" condition, which holds off the transmitter control output of the isolation interface. Closure of the normally open contact generates a logic "O" condition, initiating a transmitter control output producing a five to six volt DC signal across the output loading resistor. The transmitter auxiliary stop function can be tested in a similar manner using the test connections of Figure 8C, and the output will again provide a five to six volt DC signal across the output loading resistor.

#### **OUTPUT CONTACTS**

The SLA54K relay has two sets of output contacts. Each set of contacts consists of two normally open, two normally closed or one normally open and one normally closed contact(s). The contacts are wired to terminal strips on the back of the relay per internal connections diagram, Figure 2. Output contacts provide a means of converting logic level signals into external signals.

Output contacts are rated to make and carry three amperes. Interrupting ratings are 100 volt-amperes resistive and 35 volt-amperes reactive. Contacts pick up one to two milliseconds after logic level signal is applied to transistor switch, and drop out one to two milliseconds after logic level signal is removed.

#### TIMER SETTINGS

In general, when a time range is indicated on the internal connection diagram, the timer has been factory set at a mid-range value. Timers should be set for the operating or reset times indicated on the associated overall logic diagram. When a time range is indicated on the overall logic diagram, the timer should be set at the value recommended for that function in the descriptive write-up accompanying the overall logic diagram. When a setting depends upon conditions encountered on a specific application, this is so stated and the factors influencing the choice of setting are described. The procedure for checking and setting the timers is described below.

When the time-delay cards are to be adjusted or checked, an oscilloscope that can display two traces simultaneously and that has a calibrated sweep should be used.

In order to test the timer cards it is necessary (due to the "sinking logic" technique used in this equipment) to remove the card previous to the timer under test (see Table I) and to place the timer card in a card adapter. The card adapter allows access to the input and output of the timer if they are not brought out on test points. The timer test circuit is shown in Figure 7. Opening the normally closed contact causes the output to step up to plus 15 volts DC after the pickup delay of the timer. To increase the pickup time, turn the upper potentiometer on the timer card clockwise; to decrease the time, turn it counterclockwise. Closing the contact causes the timer output to drop out after the reset time-delay setting of the card. If the timer card is provided with a variable reset relay, it can be adjusted by the lower potentiometer on the timer card (clockwise increases reset time).

A timer tester card (0172C5151G-1) can be obtained to be used instead of the test circuit of Figure 7. This card is equipped with an "ON" and "OFF" push-button switch, an "ON" indicating LED, and two parallelled test jacks. This test card can be plugged into any printed circuit card socket (except the "T" location). One test jack connects, via a test lead, to the input of the timer under test. The second test jack connects to trigger the timing device used. This timer test card provides a bounceless switching action, ease of operation and consistent results.

TABLE I

TIMER UNDER TEST	POSITION	REMOVE CARD IN POSITION		
TL1 TL2 TL3 TL4 TL6 TL7 TL8 TL9	AG G R AN K AE N AS	AF SEE OPTION CHART P SEE OPTION CHART J SEE OPTION CHART SEE OPTION CHART SEE OPTION CHART		

#### OPERATIONAL CHECKS

Operation of the SLA54K unit can be checked by observing the signals at the twenty test points (TP1 to TP20) in the SLA54K, by observing the operation of the associated channel equipment, or by observing the output functions in the associated Type SLAT tripping relay. The test points are located on two test cards in positions T and AT and are numbered 1 to 20 from top to bottom. TP1 (on card AT) is at reference bus for the logic circuit; TP10 is at plus 15 volts DC. The remaining points are located at various strategic points throughout the logic as shown on the internal connection diagram (Figure 2). Test point voltages can be monitored with a portable high impedance voltmeter, the voltmeter on the test panel of the associated equipment, or an oscilloscope.

#### OVERALL EQUIPMENT TESTS

After the SLA54K relay and the associated static relay units have been individually calibrated and tested for the desired settings, a series of overall operating circuit checks is advisable.

The elementary, overall logic, and logic description for the specific job will be useful for determining the overall operation of the scheme.

Overall equipment tests can be performed by applying alternating currents and voltages to the measuring units as specified in the instruction books for the measuring units and checking that proper outputs are obtained from the associated SLAT when the measuring units operate.

#### CONSTRUCTION

The SLA54K relay is packaged in an enclosed metal case with hinged front covers and removable top cover. The outline and mounting dimensions of the case and the physical location of the components are shown in Figures 1 and 3, respectively.

The SLA54K relay contains printed circuit cards identified by a code number, such as Al20, T102, L104 where A designates auxiliary function, T designates time-delay function, and L designates logic function. The printed circuit cards plug in from the front of the unit. The sockets are marked with letter designations or "addresses" (D, E, F, etc.) which appear on the guide strips in front of each socket, on the component location drawing, on the internal connection diagram, and on the printed circuit card. The test points (TP1, TP2, etc.) shown in the internal connection diagram are connected to instrument jacks on a test card in position T or AT with TP1 at the top of the AT card. TP10 is tied to plus 15 volts DC through a 1.5K resistor. This resistor limits the current when TP10 is used to supply a logic signal to a card.

Other logic options are selected by means of taper tip jumpers and matrix blocks. These matrix blocks are located inside the unit as shown in Figure 3. The red (R), brown (BR), black (B), green (G), orange (OR), white (W) and violet (V) matrix blocks each have 20 individual points. The yellow (YA and YB) matrix blocks each have 20 matrix points which are grouped in ten common points: one to ten are tied to plus 15 volts DC, 11 to 20 are tied to reference.

#### RECEIVING, HANDLING AND STORAGE

These relays will normally be supplied as part of a static relay equipment, mounted in a rack or cabinet with other static relays and test equipment. Immediately upon receipt of a static relay equipment, it should be unpacked and examined for any damage sustained in transit. If damage resulting from rough handling is evident, file a damage claim at once with the transportation company and promptly notify the nearest General Electric Sales Office.

Reasonable care should be exercised in unpacking the equipment. If the equipment is not to be installed immediately, it should be stored indoors in a location that is free from moisture, dust, metallic chips, and severe atmospheric contaminants.

Just prior to final installation, the upper shipping support brackets should be removed from each side of all relay units, to facilitate possible future unit removal for maintenance. These shipping support brackets are approximately eight inches back from the relay front panel. STATIC RELAY EQUIPMENT, WHEN SUPPLIED IN SWING RACK CABINETS, SHOULD BE SECURELY ANCHORED TO THE FLOOR OR TO THE SHIPPING PALLET TO PREVENT THE EQUIPMENT FROM TIPPING OVER WHEN THE SWING RACK IS OPENED.

#### INSTALLATION TESTS

#### CAUTION

THE LOGIC SYSTEM SIDE OF THE DC POWER SUPPLY USED WITH MOD III STATIC RELAY EQUIPMENT IS ISOLATED FROM GROUND. IT IS A DESIGN CHARACTERISTIC OF MOST ELECTRONIC INSTRUMENTS THAT ONE OF THE SIGNAL INPUT TERMINALS IS CONNECTED TO THE INSTRUMENT CHASSIS. IF THE INSTRUMENT USED TO TEST THE RELAY EQUIPMENT IS ISOLATED FROM GROUND, ITS CHASSIS MAY HAVE AN ELECTRICAL POTENTIAL WITH RESPECT TO GROUND. THE USE OF A TEST INSTRUMENT WITH A GROUNDED CHASSIS WILL NOT AFFECT THE TESTING OF THE EQUIPMENT. HOWEVER, A SECOND GROUND CONNECTION TO THE EQUIPMENT, SUCH AS A TEST LEAD INADVERTENTLY DROPPING AGAINST THE RELAY CASE, MAY CAUSE DAMAGE TO THE LOGIC CIRCUITRY. NO EXTERNAL TEST EQUIPMENT SHOULD BE LEFT CONNECTED TO THE STATIC RELAYS WHEN THEY ARE IN PROTECTIVE SERVICE, SINCE TEST EQUIPMENT GROUNDING REDUCES THE EFFECTIVENESS OF THE ISOLATION PROVIDED.

#### GENERAL

The SLA54K relay is supplied from the factory either mounted in a static relay equipment or as a separate unit associated with measuring relays, a Type SSA power supply, and some form of channel equipment. All relay units for a given terminal of static relaying equipment are tested together at the factory, and each unit will have the same summary number stamped on its nameplate.

#### **MAINTENANCE**

# PERIODIC TESTS

It should be sufficient to check the outputs produced at test points in the SLA54K when periodic calibration tests are made on the associated measuring units, for example, the phase and ground relays in the line relaying scheme. No separate periodic tests on the SLA54K itself should be required.

## TROUBLESHOOTING

In any troubleshooting of equipment, it should first be established which unit is functioning incorrectly. The overall logic diagram supplied with the equipment shows the combined logic of the complete equipment and the various test points in each unit. By signal tracing, using the overall logic diagram and the various test points, it should be possible to quickly isolate the trouble.

A test adapter card is supplied with each static relay equipment to supplement the prewired test points on the test cards. Use of the adapter card is described in the printed circuit card instruction book GEK-34158.

A dual-trace oscilloscope is a valuable aid to detailed troubleshooting, since it can be used to determine phase-shift, operate and reset times, as well as input and output levels. A portable dual-trace oscilloscope with a calibrated sweep and trigger facility is recommended.

#### SPARE PARTS

To minimize possible outage time, a complete maintenance program should include stocking at least one spare card of each type. It is possible to replace damaged or defective components on the printed circuit cards, but great care should be taken in soldering so as not to damage or bridge-over the printed circuit buses, or overheat the semiconductor components. The repaired area should be recovered with a suitable high-dielectric plastic coating to prevent possible breakdowns across the printed buses due to moisture and dust. The wiring diagrams for the cards in the SLA54K relay are included in the printed circuit card instruction book GEK-34158.

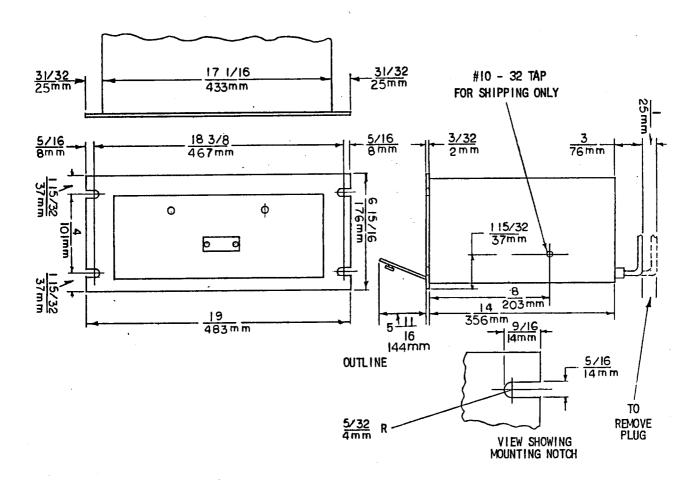


Figure 1 (0227A2037) Outline and Mounting Dimensions for the SLA54K Relay

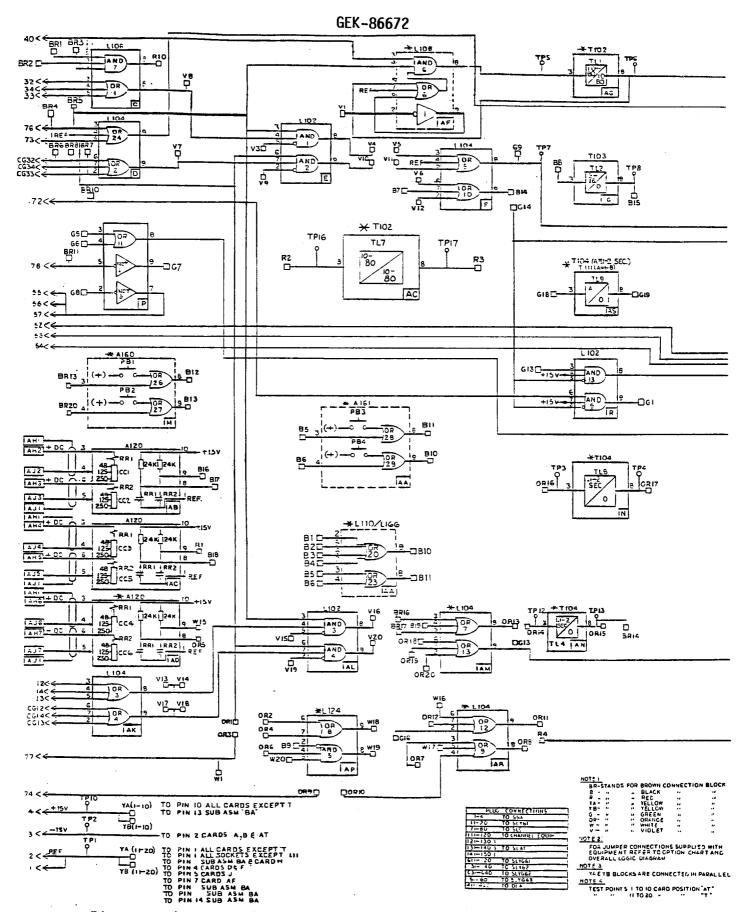


Figure 2A (0153D6706) Internal Connections for the Type SLA54K Relay

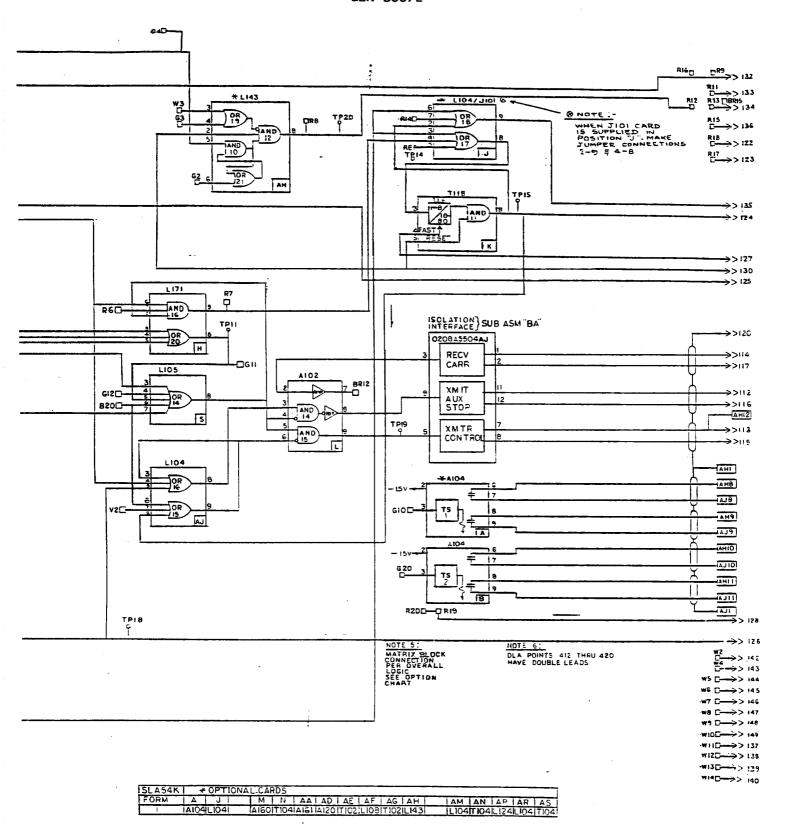


Figure 2B (0153D6706) Internal Connections for the Type SLA54K Relay

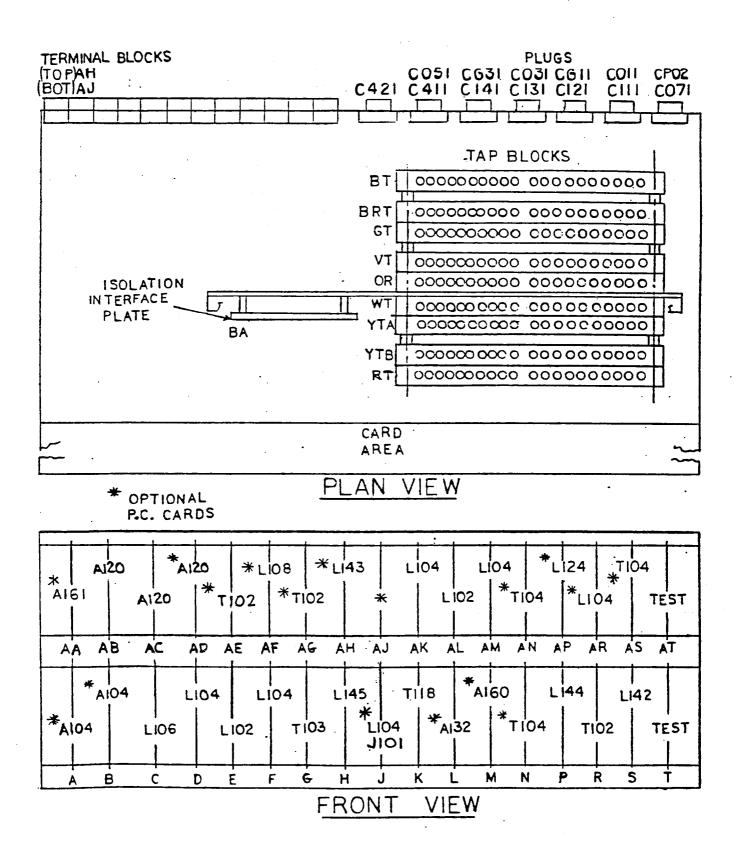


Figure 3 (0285A8935) Component Location Diagram for the Type SLA54K Relay

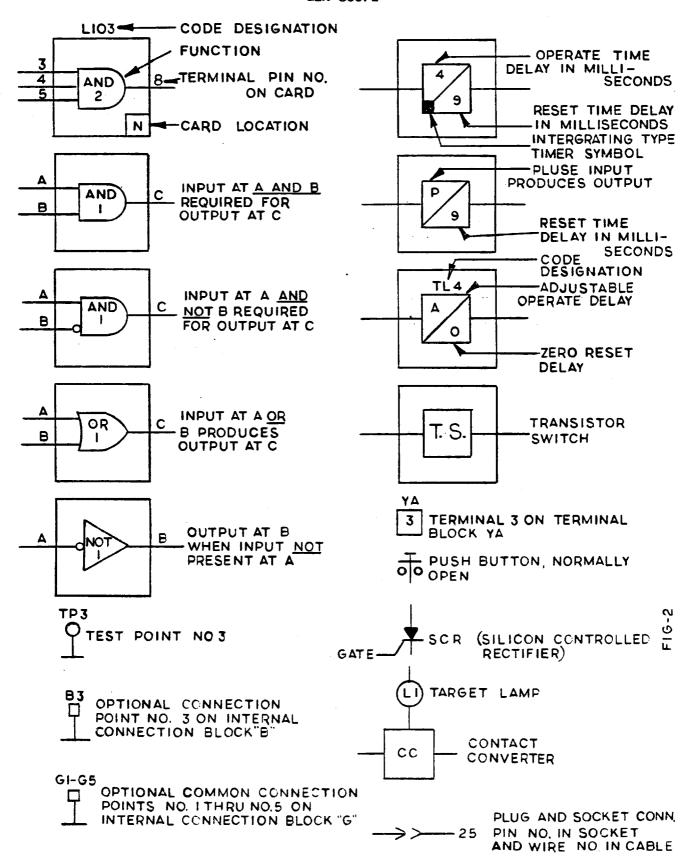


Figure 4 (0227A2047) Logic and Internal Connection Diagram Legend

THE FOLLOWING ARE FACTORY CONNECTIONS MADE AT THE MATRIX BLOCKS									
INSIDE OF THE SLA RELAY ASSOCIATED WITH THIS EQUIPMENT.									
SYMBOLS LISTED: PL=RELAY INTERCONNECTING CABLE LEAD									
(5)=LOGIC FUNCTION CARD PIN NUMBER  = 3-WAY CONNECTION									
= DLA MONITOR CONNECTION AVAILABLE BUT NOT USED									
$\Box \bullet A : \bullet \circ \circ \circ \circ \circ \circ \circ \circ \circ A = A = A = A = A = A$									
D= 4 WAY CONNECTION D=5 WAY CONNECTION (343)									
MATRIX	MATRIX BLOCK								
JUMP				JUMP	ERS	LOGIC FL	JUCTION		
FROM	TO	FROM	TO	FROM	ТО	FROM	TO		
V4	BR20		OR27(M4)		RI8	TLI (AG8)			
Δ <i>BI3</i>	V5 V1		OR5(F3)	‡ G4_	COVER	(BUT NOTCO			
Δ B/3	<del></del>		NOTI (AFZ)	RIT	Y417	PL123	REF		
4 813	OR16	OR27(M9)		‡ORI3	OR20		ORI3 (AMZ)		
A B/3	W9	OR27(M9)		‡ORI3	R4	OR7(AM8)	ORIT (13)		
A B13	COVER	(BUT NOTE	T	‡ W/9	OR19	AND5	ORI3 (AMT)		
V7	OR12		ANDIZ(ART)		W6	ANDS (APB)			
V8	W16		ANDIZ(ARG)	W18	OR18		ORI3(AMG)		
V3	YAII	ANDI (E5)	REF	W12	YA9	PL 138	+15 V		
V9	YAIZ	ANDZ (EZ)	REF	ORB	B19	OR9(ARB)	ORT (AM4)		
<i>G</i> 7	G16		ANDIZ(ARZ)	<i>‡811</i>	BRIT	OR28 (AA8)	ORT (AMS)		
V15	YA13	AND3 (ALS)		<i>‡ BII</i>	W13	OR28(AA8)	PL 139		
V19	YA14	AND4 (ALZ)		V16	BR13	AND	OR26 (M3)		
BR5	W20	PL76	AND(AP3)	# B12	BRIG	OR26 (M8)	ORT (AM3)		
V20	85	ANO4 (AL9)	OR28 (AA3)	‡B12	WII	OR26 (M8)	PL137		
D W!	OR7	PL.77		#OR5	OR6	CC4 (AD8)			
D W/	W2	PL77	PL142	IOR5	G18	CC4(AD8)			
D W/	COVER (	BUT NOT CO.	NNECTED)	G19	B9		ANDS (AP2)		
D OR9	ORIO	PL74	OR9 (AR4)	BR14	WI4	TL4(AN8)	PL140		
DOR9	W4	PL74	PL143	ORI5	OR2	TL4(AN8)	OR8 (AP6)		
OR9	COVER(	BUT NOTCOL	VNECTED)	# ORIT	OR4	TL8(N8)	OR8 (APT)		
W17	Y13	OR9(AR5)	REF	FOR17	WIO	TL8 (N8)	PL149		
Ø B10	VII	OR29 (AA9)	OR5(F5)	RT	W8	AND16 (H8)	PL147		
Ø BIO	OR 14	OR29(AA9)	TL4(AN3)	R4	YA15	OR18(J7)	REF		
Ø BIO	W7	OR29 (AA9)	PL146	RI5	YAI6	PL136	REF		
Ø BIO	COVER (	BUT NOTE		R19	WS	PLI28	PL144		
G9	88	OR5(F8)	TL2(G3)	REO	R13	PLI28	PL134		
<i>B15</i>	87	TL2 (48)	OR10(F7)	VIO	B6		OR29 (AA4)		
V6	YBII		REF	B14	G14		ANDIG(H6)		
VIZ	YB12		REF	ORII			NOT3(P2)		
≠ R16	R9		PL132	<b>IGI</b>		AND9[R9)			
#R16	RII		PL133	<b>#</b> G/	42	AND9(R9)			
R8	G20	ANDIZ(AHB)		R3	46		OR11(P4)		
G2	YA8		+ 15 VDC	45	YA17	ORII(P3)	REF		
93	YB15	OR19 (AH4)	REF	816	B20 -	CC2(AB9)			
W3	Y814	OR19/AH3)	REF	817	V2	CCI(AB8)			
		1 ////// 3/		, <b>-</b> - /	T 1		マッ・ブリグノノー		

Figure 5 (0227A2050, Sh. 343) Typical Option Chart for the Type SLA54K Relay

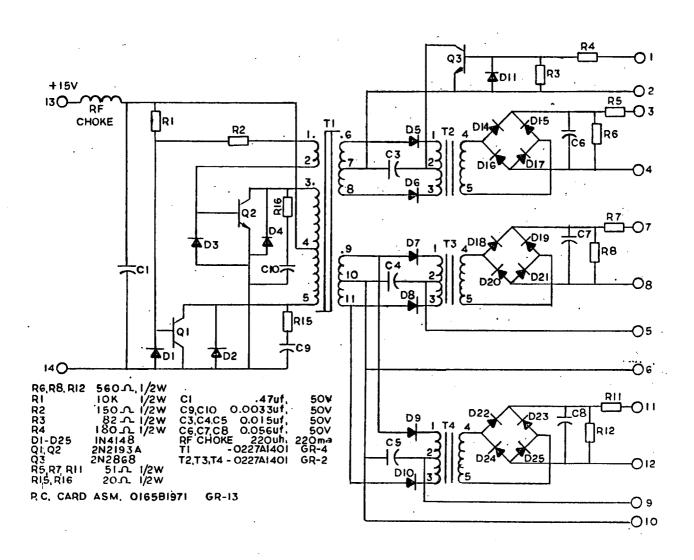
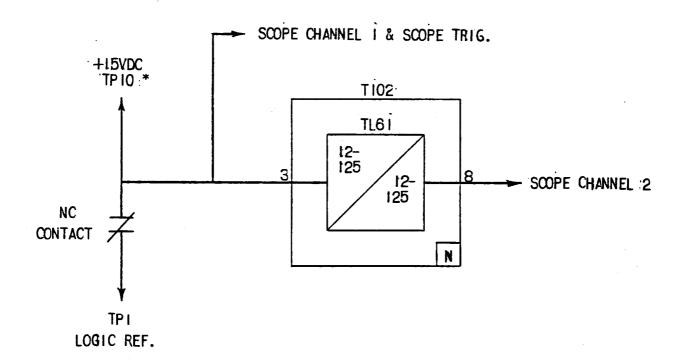
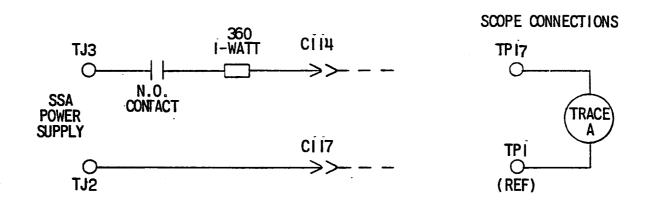


Figure 6 (0208A5504AJ) Internal Connections for the Isolation Interface Used in the Type SLA54K Relay

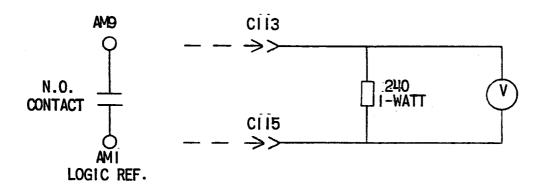


\* THE I5VDC SIGNAL AT FIN IO HAS A CURRENT LIMITING RESISTOR MOUNTED ON THE TEST CARD.

Figure 7 (0246A7987) Timer Test Circuit for Setting Timer Cards in the Type SLA54K Relay



# A-RECEIVED CARRIER TEST CONNECTIONS



# B-TRANSMITTER CONTROL TEST CONNECTIONS

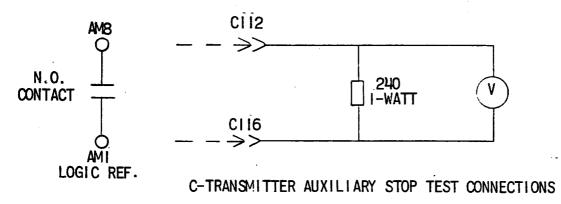


Figure 8 (0257A6244) Isolation Interface Test Circuit

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