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*GE Power Management*

# Series Compensated Line Protection Issues

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## PHILOSOPHY OF THE PROTECTION OF SERIES COMPENSATED LINES

### I. BACKGROUND

Series capacitors are almost always added to transmission lines where poor relay performance can have a significant adverse effect on the power system stability. Thus it is important to understand the relaying problems associated with series compensated lines in order to ensure that the relay systems used have an adequately high level of reliability.

It may be desirable to re-evaluate the protection philosophy to be employed on series compensated lines. Where system stability may be impacted, the protection philosophy should be selected to primarily protect the power system with the protection of the line of secondary importance. Much of the difficulty in obtaining adequate reliability of the protective systems on the initial series compensated lines was a result of using protection philosophy developed for sub-transmission line protection.

### II. RELAYING PROBLEMS

Understanding the relaying problems associated with series compensated lines is much more difficult than uncompensated line relaying for a number of reasons:

(a) It requires a better feel for the transient response of transmission lines when faulted.

(b) It requires a better understanding of transient response of protective relays.

(c) The significant problems introduced by the series capacitors will vary considerably based on system configuration, line configuration, line length, % compensation, etc.

(d) The series capacitors tend to exacerbate problems associated with some uncompensated lines such as load flow problems, of untransposed lines, mutual impedance problems, etc.

(e) The type of capacitor protection and the capacitor control can influence the significance of some problem areas.

As in all relaying, if the problem areas are anticipated and understood, the solution to the problem is achieved with comparative ease.

## A. SYSTEM TRANSIENTS

Instead of the decaying DC component of current associated with most fault incidence angles, fault current flowing through series capacitors will generate an AC transient component of current on fault inception. The frequency of the transient component of current will be approximately equal to:

fundamental * $(X_C/X_L)^{1/2}$

where $X_C$ is the total capacitive impedance in series with the total inductive impedance $X_L$. If the "voltage drops" due to the load current are small compared to the "voltage drops" due to the fault current, then in the first half cycle of voltage after the fault incidence, the voltage drop in the inductor is essentially of the same polarity as the voltage drop in the capacitor as shown in Figure 1. Thus the capacitor tends to reduce the fault current initially, and then when the capacitor voltage shifts out of phase with the inductor voltage the current is larger than the current would be if the capacitor is bypassed. It is assumed that $X_L > X_C$ in figure 1.

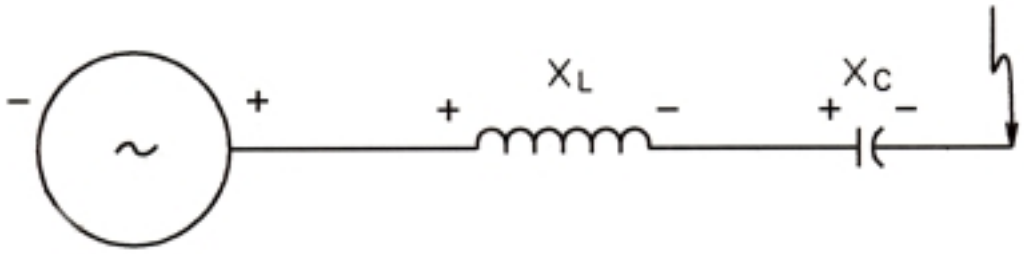


*Figure 1*

In many relays, the quantity IZ is used rather than I, so that the DC transient component of I produced a very small change in IZ. However, with the AC transient component of I, the transient component of IZ is much more significant, and thus more difficult to filter out.

Assuming that the transient frequency is somewhat less that the fundamental frequency, the voltage drop in the inductor will be much less due to the transient current compared to the fundamental frequency current. Conversely the transient voltage drop in the capacitor will be much larger due to the lower frequency of the transient current. Thus, to the low frequency transient component, the line appears to have a much higher percent compensation.

## B. CAPACITOR OVERVOLTAGE PROTECTION

Early series capacitor designs utilized a trigger gap to bypass the capacitor bank (or section) when the voltage across the bank (or section) exceeded the trigger setting (called the protection level(s) in terms of steady state current that would cause triggering because low frequency transients in the fault current increased the instantaneous voltage across the capacitor well above the steady state voltage, the capacitors would be by-passed for fault currents (or switched load currents) well below the protective level.

The capacitors were bypassed through a current limiting reactor which produced a very large transient high frequency voltage across the capacitor bank. If the fault was close to the line side of the capacitor bank, the large high frequency voltage would appear on bus side potential devices and also the shunt capacitance in adjacent lines, requiring filtering on both the voltage and current circuits in the relays.

However, despite the need for filtering, the bypass gaps operating on lower current levels provided more security for relay systems on lines adjacent to the faulted line. Unfortunately, the reliability of the power system was jeopardized by bypassing capacitors on unfaulted lines by fault (or load) currents.

More recently, instead of bypass gaps (or in addition to them) overvoltage protection is accomplished by paralleling the capacitor bank by MOV's. When the peak voltage reaches the protective level, the MOV conducts, limiting excessive voltage across the capacitor. The MOV's would also conduct transiently on over voltages as a result of the low frequency current transients, thus providing attenuation for the low frequency transients. The amount of attenuation will depend on how much conduction occurs.

If the MOV's conduct steady state then the parallel arrangement of the MOV and series capacitor will appear as a series combination of $X_C$'s and $R_C$'*. The magnitude of $X_C$/ and $R_C$' can be calculated from the ratio of the fault current $I_F$ to the protective level IPL and the prefault capacitance of the bank. The values of $X_C$' and $R_C$' can then be used in steady state analysis of relay performance. For example;

when $I_F = 2.5\ I_{PL}$, $X_C' \approx 1/3\ X_C \approx R_C'$
when $I_F = 5\ I_{PL}$, $X_C' \approx 0.1X_C$, $R_C' \approx 0.2X_C$.

The ratio of $I_F$ to $I_{PL}$ becomes the key indicator of potential problems with protection systems on series compensated systems [1].

## C. VOLTAGE REVERSALS

For the simple system shown in Figure 2, assume that the source impedance to the left of bus C is much larger than $X_C$, so that the fault current through the capacitor is less than the protective level and lags the source voltage at the left by approximately 90°. The fault current at the two ends of the line CD will have an angular difference approximately equal to the load angle across the system . The steady state voltage at C will reverse with respect to the source voltage at the left.

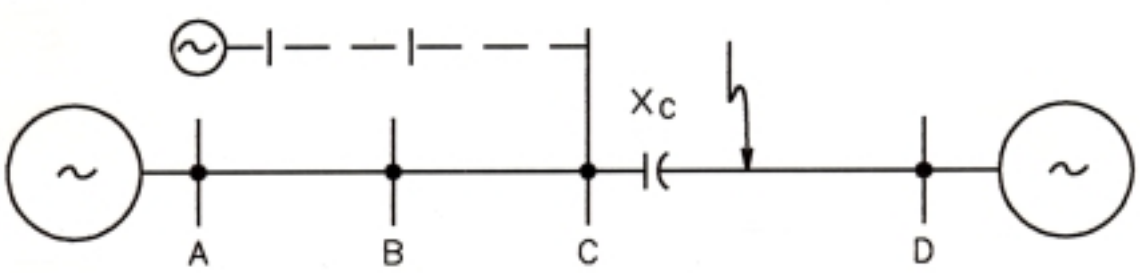


*Figure 2*

It is also possible that the voltage at bus B will also reverse if the voltage drop across the line BC is less than the voltage drop across the capacitor. This becomes increasingly likely as the fault current over the dotted line increases.

The voltage reversal does not present a concern for phase comparison systems or directional comparison systems that are designed for series compensated lines. However, if the protection on line AB for example, was not designed for series compensated lines, its performance should be checked for the fault shown.

In most power systems, the fault current is very large compared to the protective level of the series capacitor, thus minimizing any possible risk of existing relay systems misoperating. However, the relays should be evaluated under minimum system conditions that would reduce the ratio of $I_F$ to $I_{PL}$.

## CURRENT REVERSALS

In the system shown in Figure 2, the source impedance to the left of bus C is usually less than $X_C$ in normal power systems. Thus, if we ignored the capacitor overvoltage protection, the fault current at the left end of the line would reverse because the net impedance between the fault and the left source would be capacitive. Thus the fault would appear as an external fault to either a phase comparison or a directional comparison relay system. However, in this theoretical case, the leading current through inductive source would cause the voltage across the capacitor to be substantially higher than rated voltage. Normal protective levels limit capacitive voltages below rated voltage, thus insuring a lagging component of fault current to produce a voltage drop in the source impedance.

The above discussion assumes a bolted fault without fault impedance. Ground faults may have sufficient fault impedance to limit the fault current magnitude below the protective level. Phase comparison relays would see the fault as external. A well designed directional comparison relay system would see the fault as an internal fault.

If the inductive positive and negative sequence source impedances are greater than the capacitive impedance but the zero sequence source impedance was less than the capacitive impedance, there would be a fault current reversal between the zero sequence current at the right terminal and the positive and negative sequence currents at the right terminal.

Figure 2 is not as likely to occur frequently in practice since it must have a second (or third) line in parallel with line CD for system reliability when CD is faulted or out of service. A few systems with series capacitors do use path diversity for different reasons. Figure 3 illustrates the case where the lines are bussed at the same stations and either use the same right of way or different paths. For the case of Figure 3, it is more likely there will be a substantial phase angle between the currents at the two ends of the faulted line even if the source impedance behind bus C is larger than Sc1. If the fault current through Sc1 is below the protection level, then the voltage on bus C will reverse with respect to the fault point on the line. If the magnitude of the reversed voltage on bus C is greater than the positive drop in the unfaulted line CD, then the voltage on bus D will also be reversed. Thus the fault current at the remote end of the faulted line will be approximately 180° out of phase with the near end fault current. There will be a fault location near the end of the line where the voltage drop across $X_{C1}$ just equals the voltage drop across the unfaulted line CD. In this case the voltage on bus D will be zero with respect to the fault point and the fault current at the remote end of the line will be zero.

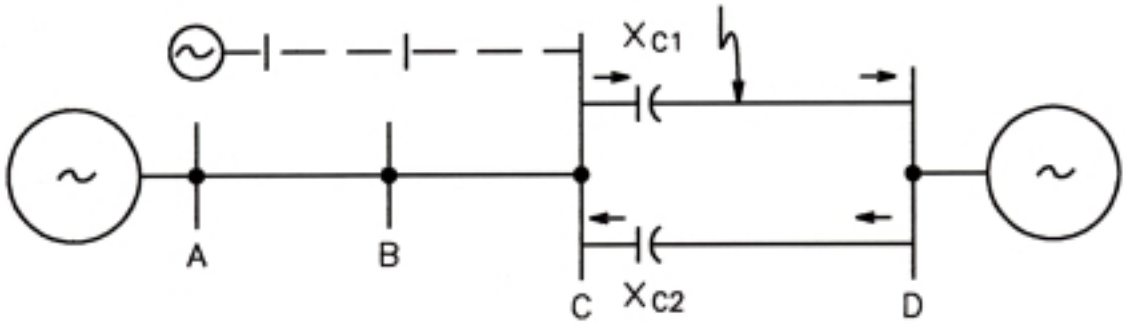


*Figure 3*

If the fault current through $X_{C1}$ is greater than the protective level, then the MOV will conduct and $X_{C1}$ in series with $R_C$' with the magnitudes roughly and inverse function of the fault current. Thus, the remote end fault current can vary in phase angle with respect to the near end fault current from approximately zero to 180°. The actual configuration in your utility has a station tapped into one of the two parallel lines that will produce some degree of modification to the analysis stated above.

## E. HIGHER LOAD FLOWS

Usually series capacitors are added to enhance system stability with higher load flows. In general, the higher load flows tend to make phase comparison systems less sensitive. This is also true of some designs of directional over current relaying in some directional comparison schemes. The general problems of distance relaying are discussed in a paper (Reference x in GE technical proposal). These problems are exacerbated by long lines, the use of distance relays designed for subtransmission systems, and the indiscriminate use of high speed reclosing.

## F. VERY LONG SERIES COMPENSATED LINES

In general, pilot schemes become less reliable for faults near one end because the current at the remote end of the fault can be indeterminate in magnitude and direction (as discussed in Section D). The pilot schemes are very effective for faults in the midsection of the lines. By contrast, direct trip functions are most effective for near end faults, and less effective for faults mid line and beyond. A later section on channeling will describe how this performance can be used to increase the overall reliability of the relay system.

## G. UNBALANCED LINE IMPEDANCE

Untransposed lines, or partially untransposed lines, cause unbalanced line impedances. Since the capacitors are usually (unless there is a failed cap) the same impedance, the impedance unbalance becomes a much higher percentage of the compensated line impedance. Thus, a higher lever of negative and zero sequence currents can be expected which may require re-evaluating ground back up relay settings. This is increasingly significant with higher percent compensation.

## H. MUTUAL IMPEDANCE

Similar to (Co) the series capacitors cancel out the lie self impedances but not the mutual impedance with a parallel line. This can be some advantage in setting a ground direct trip function if the parallel lines are reliable bussed at the two ends. Conversely it may be some disadvantage if they are not reliably bussed. However, the setting must consider the case where the parallel line is out of service and grounded at both ends. Again, the percent compensation is a very significant factor.

## I. FAULTS IN CAPACITOR BANK

The capacitor bank will have internal protection (For example, group overvoltage because of fuse blowing) that will require shorting the platform. At least in older designs, there was a delay before the other two phase platforms were bypassed. This provided a window of opportunity for a high speed sensitive ground directional comparison scheme to operate if the capacitor unbalance appeared as an internal fault.

It will appear as an internal fault if the potential location is on the bus side of the series capacitors and as an external fault with line side potential location. However, the sensitivity can be reduced when the capacitor unbalance appears as an internal fault while still retaining reasonable sensitivity to detect broken conductor faults which can pose a serious safety threat.

## J. COMPENSATION

In general, some problem areas tend to increase as the percent compensation increases. Sometimes the addition of future substations will result in shortening the line length and increasing the percent compensation.

## K. SERIES CAPACITOR LOCATION

In some of the earlier series capacitor applications the series capacitors were located at the mid line or along the line in the mistaken assumption that relaying would be easier. Most of the applications used line end series capacitors because of the prohibitive cost of developing and maintaining a separate site. However, if series capacitors are added later, the mid line site may be the lower cost. Some of the advantages of line end location are:

(a) Use of line side potential location;

- When the trigger gaps are used they produce a fairly high noise level which is partially attenuated if the wave traps are located between coupling capacitors and capacitors. This will shorten the time that power line carrier channels are out of service.
- The effectiveness of first zone hybrid distance units may be substantial improved.
- No loss in sensitivity of high resistance ground fault protection as discussed in (I).

(b) Where there is a somewhat weaker system at one end of the line compared to the other. An excellent example is the Poinsett Rice line with the Duval Rice line out of service. For this case, if the capacitor was located at Rice and the fault was closed to the capacitor, the risk of 230 kV line relaying may be substantial. Even if the fault was just beyond the point where the fault appeared inductive from Rice, the low frequency transient in the capacitor may still cause misoperation, depending on the relay design.

## L. SINGLE POLE TRIPPING AND RECLOSING (SPT&R)

It is understood that your utility will not be using SPT&R. However, the problems associated with SPT&R and series capacitors are well known as they are probably the majority of applications in the world.

## M. BACKUP PROTECTION

Backup protection must be faster than the critical switching time to be of any positive value in protecting the power system.

Often the two high speed independent relay systems are considered adequate backup protection. Some will switch in a third system with "first" and "second" zone distance relays with short time delays when one of the primary systems is out of service. Some will have a simpler third relay system in service all the time.

On very long lines, normal second zone time delays may be adequate for faults near the remote end (assuming the series capacitors will bypass fairly quickly).

Sometimes simple direct tripping overcurrent relays can be used which would also provide stub fault protection.

# III. RELAY RESPONSE CONSIDERING SERIES CAPACITORS

## A. DISTANCE RELAY THEORY

(a) The key to correct directional sensing in distance relay design is a reliable memory circuit. Thus the prefault voltage is used for the polarizing signal to avoid the obvious errors that would be due to a voltage reversal. The duration of the memory voltage is limited to ensure proper operation during load swings; for example, if the circuit breaker is reclosed onto a permanent fault. The line relaying should also work correctly in case the system swings out of step. Since the memory voltage is limited in duration, the relay operation is sealed-in as required for reliable performance on internal faults.

(b) The relay units are somewhat more sophisticated in design when designed for series capacitors. For example, the block-spike technique used in earlier designs of solid state block relaying units would be inadequate for series compensated line applications.

(c) Low Frequency Transients

The paper "Series Compensated Line Protection - A Practical Evaluation" illustrates how a low inertia relay can overreach on the low frequency transients. These low frequency transients will also occur in adjacent lines, creating the possibility of adjacent line relays operating. However, the adjacent lines will have more steady state restraint making misoperation very unlikely. If relays are available to test on a Model Power System using EMTP data, the effective inertia of the relays could be evaluated by using the currents and voltages at Thalmann for a fault on Duval Bus with the Thalman Hatch line out of service. Compare relay response with different reach settings.

(d) "Capacitive" Faults

Capacitive faults are defined as faults where the net impedance between the potential location and the fault is a net capacitive impedance. Section II A indicates that there is a transition period after fault inception before reaching steady sate values. This discussion assumes a steady state condition, and is intended to supplement the information provided in the paper "Series Compensated Line Protection: Practical Solutions". Figure 4(a) illustrates a bus with a block and trip distance function and three fault locations that can be described as "capacitive faults". For each relay and each fault, the phase relay inputs are shown, and the dynamic characteristic obtained by using the prefault voltage for polarizing. The diagrams are drawn for no load on the system.

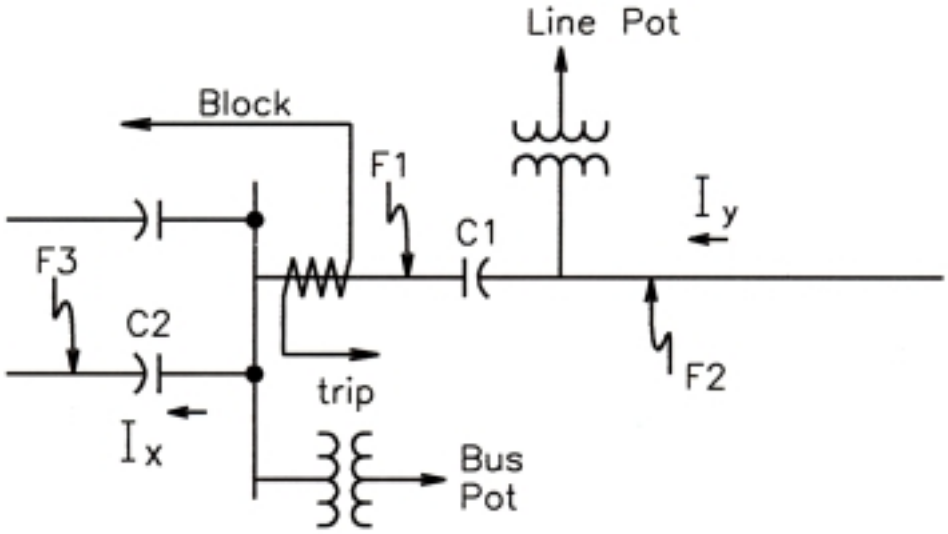


*Figure 4A*

Figure 4(b) shows the trip unit for an F2 fault and bus side Pts. Of significance is the fact that the voltage is an "operating" signal rather than a "restraining" signal. $Z_{SL}$ shown on the dynamic characteristic is the source impedance to the left of the bus. The dynamic characteristic goes through $Z_{SL}$ since relay operation ceases when $X_C$ slightly exceeds $Z_{SL}$ and the fault current reverses. If there was load flow on the system, the Iz-V signal would shift by the angle "S" where "S" is the angle between the $V_{POL}$ (prefault) and the voltage at the source on the left.

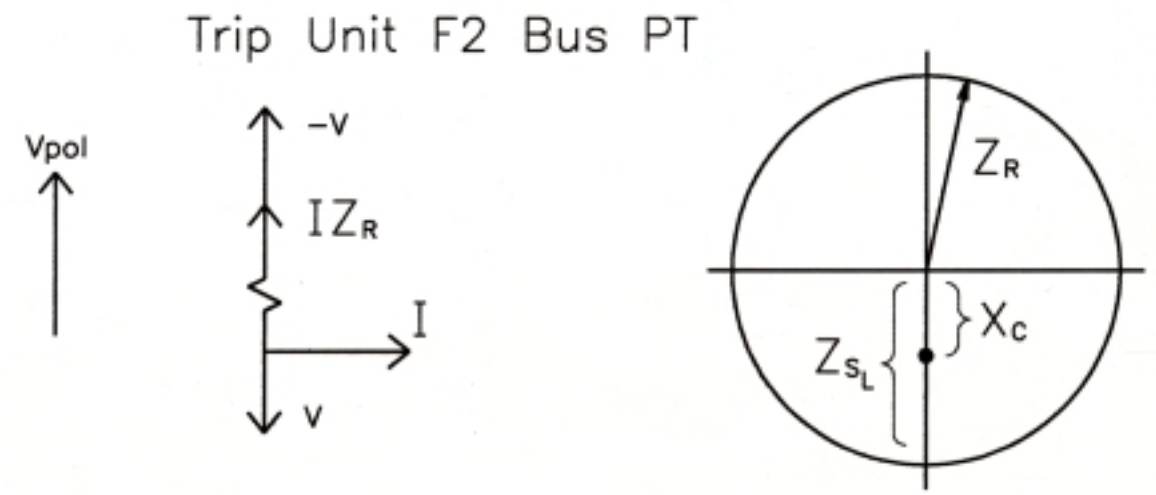


*Figure 4B*

Figure 4(c) is similar to 4(b) except an F1 fault and Line PT. The significant difference is that -V ($-I_Y X_C$) is not related to the current in the relay, but is the fault current from the other end of the line. It does determine relay operation but is doesn't have the real meaning described for $X_C$ in the Figure 4(b). Also the IZ signal will rotate the angle "s" described in conjunction with Figure 4(b) but -V will shift in accordance with the load between the bus voltage and the voltage behind the source at the right end of the line. Since the relay responds to the input quantities and the angle between them, sometimes it is easier to understand relay operation by examining the input phasors rather than the RX diagram.

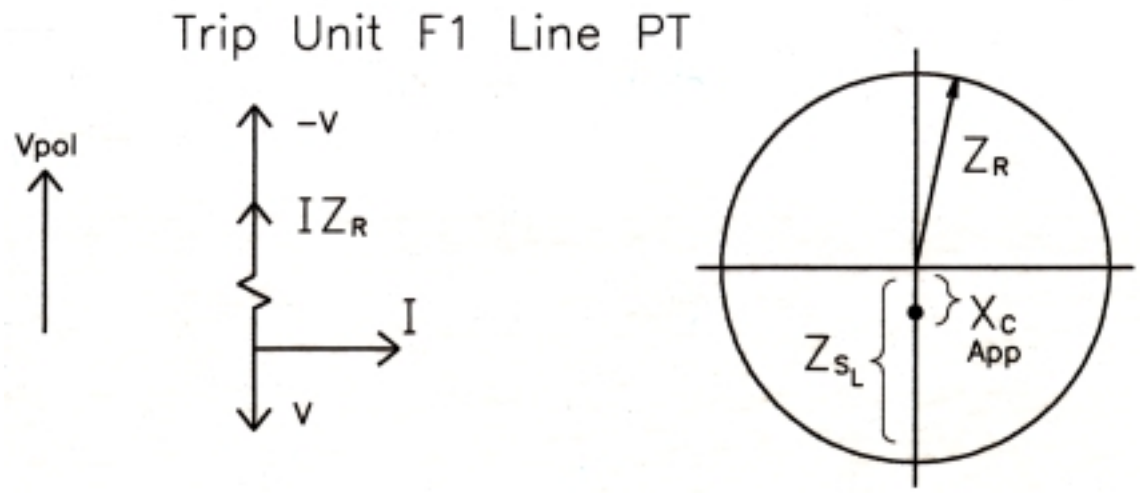


*Figure 4C*

Figure 4(d) illustrates the trip unit on the external fault F3 with Line PTs. The infeed over the unfaulted line on the left has increased the capacitive voltage drop so that -V is larger than $IZ_R$ so that the simple relay described in the aforementioned paper would operate. However, in a sophisticated transmission line relay such as the TLS, multi-input comparators are used. The $IZ_R$ signal is a separate input and is out of phase with $V_{POL}$ and $IZ_R$-V and hence the TLS trip unit would not operate for this fault. For this fault the load current effect is a little more difficult to estimate because $I_Y$ is composed of components from both the left source and the right source.

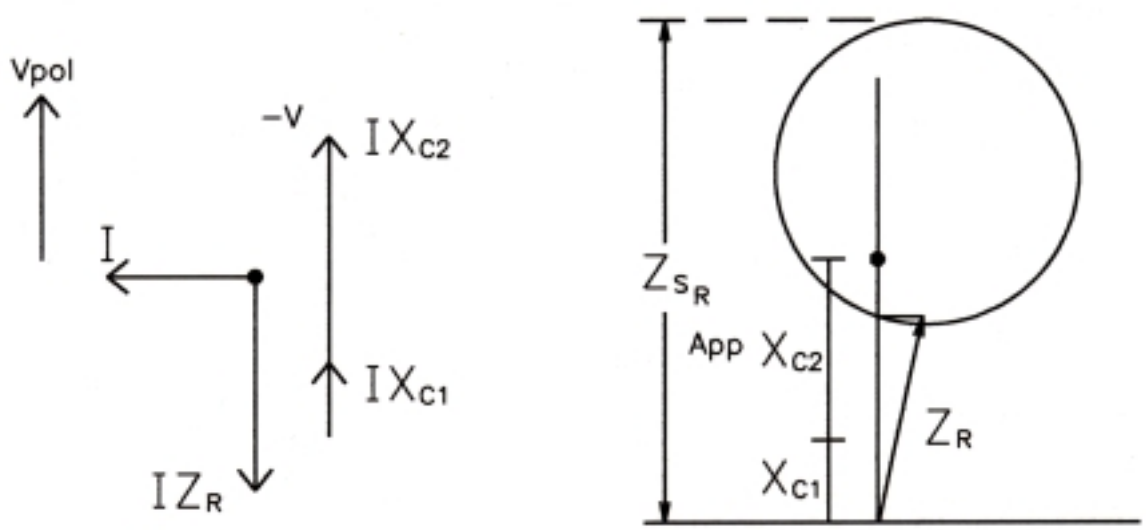


*Figure 4D*

Figure 4(e) is the block unit on an internal fault of F2 with Bus PT. Non-operation is assured if $Z_R$ is set larger than $X_C$. However consideration of coordination with the remote trip unit will require a much larger setting of $Z_R$.

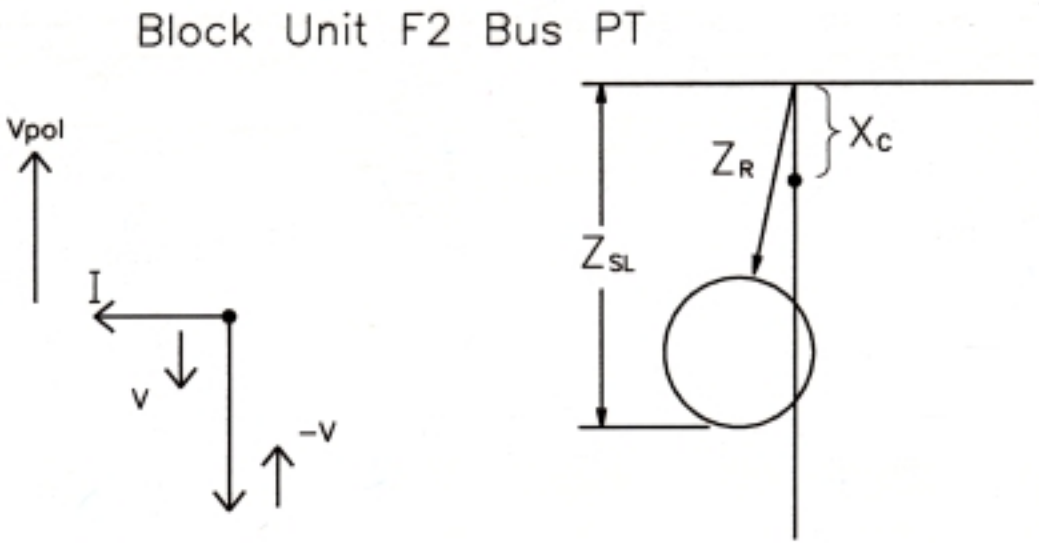


*Figure 4E*

Figure 4(f) is similar to Figure 4(e) except the fault location is F1 with the Line Pts. Of note is that the current producing -V is from the remote end of the line whereas $IZ_R$ is developed from the relay current. Since near end infeed is almost always larger than the infeed from the remote end, non-operation is more secure than in Figure 4(e). If the remote infeed is larger, it should be evaluated in the $Z_R$ setting.

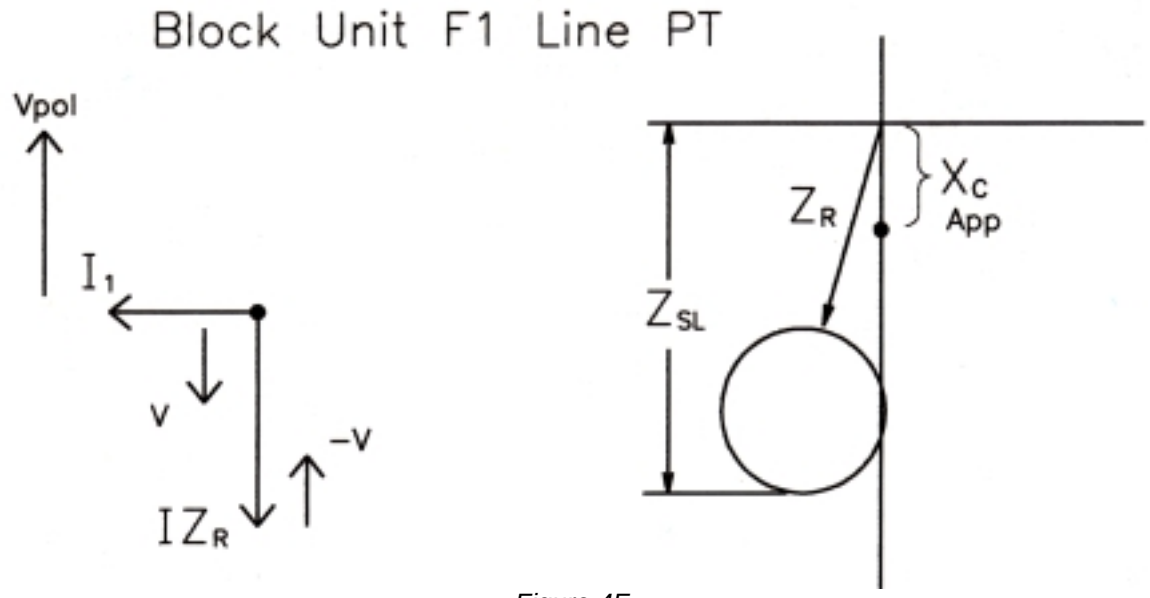


*Figure 4F*

Figure 4(g) illustrates the performance of the blocking unit on the F3 fault with Line PTs. The restraint signal (-V) and the replica voltage signal ($IZ_R$) are in phase, and in phase with the polarizing signal ($V_{POL}$). This relationship will produce correct operation. The load effect is complex to evaluate but if the source voltage at the left is leading and the source voltage at the right is lagging, there will be a tendency to cancel the effect of load angle.

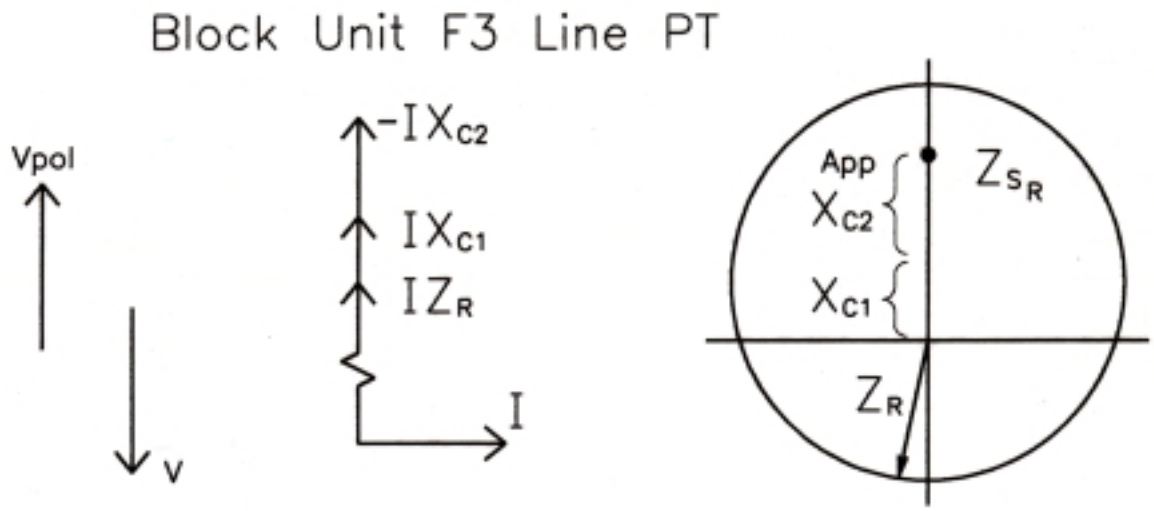


*Figure 4G*

Figure 4(h) is similar to Figure 4(b) except that the MOV- is conducting so that $X_C$ is replaced by $X_C' + R_C'$. Fault current is twice the protective level and $Z_R$ is twice $X_C$ (no conduction in MOV). It will be noted that $-IR_C'$ causes a very minimal phase shift in the IZ-V input signal.

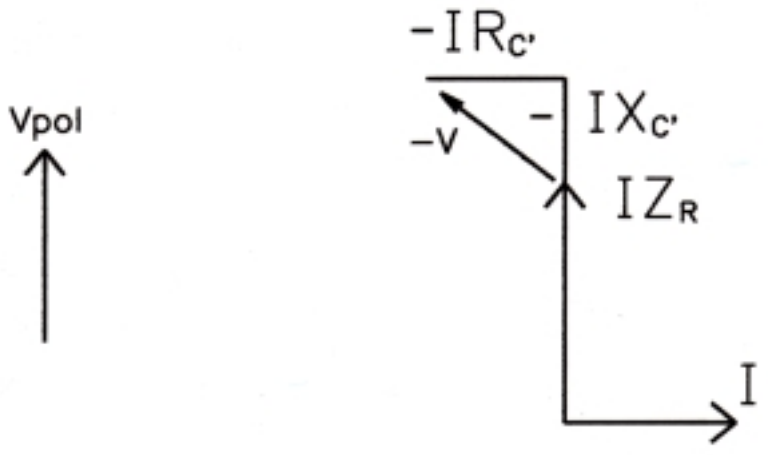


*Figure 4H*

## B. ELECTRO-MECHANICAL RELAYS

Although they are unlikely to be used on series compensated lines, they may be very likely to be on lower voltage lines adjacent to series compensated lines and be included in the "sphere of influence" of the series capacitors.

(1) E/M relays have significant inertia. Thus it would seem unlikely that they would respond to low frequency transients with some reasonable level of steady sate restraint.

(2) The inertia "effect" can be significantly increased by increasing the contact spacing, lowering the reach tap, and increasing the spring restraint.

(3) The dynamic characteristics of self polarized mho trip relays is only marginally larger than the steady state characteristic. However, the blocking units have excellent dynamic characteristics because they only need to open a NC contact.

(4) The phase to phase unit (in a KD for example) theoretically has a steady state characteristic equal to the dynamic which gives it more coverage of the magnified Rc' component of a series capacitor with MOV conducting.

(5) It is assumed that a fault on the compensated line at a point where the line impedance is equal to capacitive impedance will result in some conduction of the MOV. Thus there will not be a case where the reversed capacitive voltage on the bus behind the capacitor where the $IR_C'$ drop is zero. Because the infeed to the fault in the lower lines is small compared to the total fault current, the capacitive impedance will be magnified to the point where it may cause voltage reversals two or more line sections away. Thus if $IR_C'$ was zero, there would be a risk of wide spread tripping in a fairly large area around the station with the capacitive fault.

However, for your utility, it is expected that the minimum fault capacity on the bus adjacent to the series capacitor (with worst outage scenario) will still produce fault currents above the protective level when the capacitive impedance is cancelled out by the line impedance to the fault.

The Aspen program can check fault locations near the capacitor and determine the magnitude of $X_C'$ and $R_C'$. The magnified $X_C'$ tends to bring the opponent impedance seen by remote relays into the characteristic, whereas the magnified $R_C'$s will tend to drive it out of the characteristic along a line parallel to the R axis. Load flow ill cause a "tilt" to both the $X_C'$ drop and the $R_C'$ drop.

Auxiliary programs can modify the voltages and currents at each terminal to determine if the fault appears inside or outside of the relay characteristic.

## C. SOPHISTICATED DIRECTIONAL COMPARISON SCHEMES

For lines with series capacitors or adjacent to series compensated lines there are transmission line relays such as the TLS or PLS relay systems that incorporate techniques developed in over 30 years of testing directional comparison schemes on series compensated lines. Besides the multi-input comparators for excellent directional sensing, the last referenced paper on "Practical Solutions" describes; the Special hybrid distance unit that provides very high speed operation on severe faults while retaining complete security from overreaching due to the series capacitors, the direction units that are compensated to provide correct directional sensing even with the potential location on the line sides of the capacitors, the use of positive sequence restrained zero and/or negative sequence overcurrent relay for maximum reliability by optimizing the balance between security and dependability, and the optimizing of distance relay characteristics.

## D. PHASE COMPARISON SCHEMES

The primary improvement in phase comparison schemes for series compensated lines was the addition of signal conditioning. A phase comparison system designed for lower voltage sub transmission lines averaged one false trip for each correct trip until it was re-designed for EHV series compensated lines. Another improvement was the development of segregated phase comparison that eliminated any errors in mixing the signals and was particularly advantageous in providing phase selection for single pole tripping and reclosing.

E. Other schemes have been proposed for series compensated lines but they either lack confirming experience or have demonstrated poor performance.

Comparison of Phase Comparison and Directional Comparison

Historically, phase comparison was selected over directional comparison in the United States in the initial application of series compensated line protection.
In the absence of an adequate model power system to check the relay response, a simplistic evaluation based on consideration of voltage reversals primarily favored phase comparison. By contrast, in Canada where an adequate model power system was available, the decision was made to use directional comparison relaying based on the significant tendency of the phase comparison to false trip during model power system tests. The feasibility of using directional comparison relaying on series compensated lines was established by two basic concepts:

(a) The dynamic characteristic of distance relays with memory action provides excellent directional integrity in the presence of voltage reversals for the duration of the memory signal.

(b) Reversing the initial priority of the tripping and blocking units so that if the blocking units operated first, transient blocking was set up to block the tripping unit after the fault was cleared.

In the development and testing of directional comparison relaying in Canada, (and later in the United States when model power systems became available), many design innovations were incorporated to significantly enhance the performance on series compensated lines.

Based on reports of relaying experience on series compensated lines, these innovations have significantly improved the performance of directional comparison relaying over the phase comparison. For example, an unpublished report on five years experience on 500 kV series compensated lines indicated that over 14% of the operations of the phase comparison relaying were incorrect compared to 0% incorrect operations of a directional comparison scheme designed for high performance on series compensated lines.

(c) It should be noted;

- The phase comparison relays were provided by two manufacturers and includes a few different models from each manufacturer.
- The total operations on each manufacturers relays was in the ratio of 4 to 5.
- The total incorrect trips were about equal, giving one manufacturer a small edge. However, the false trip rates are both sufficiently close so as to provide a reasonable indication of the false trip rate of phase comparison.
- The high performance directional comparison scheme included direct transfer trip capability and used the positive sequence current restrained zero sequence overcurrent relay for sensitive ground fault protection. This directional comparison scheme was not available when most of the lines went into service and thus there were fewer relays in the survey. The total operations of the directional comparison schemes were 9% of total operations of the phase comparison schemes, 10.7% of the current operations of the phase comparison schemes.

The reason for the substantial discrepancies in performance appear to be the inherent difficulty in providing security in the design of phase comparison relaying. Phase comparison relaying requires the comparatively precise measurement of current signals for each end of the line. The timer measuring the coincidence or anti-coincidence of the two signals discriminates between internal faults based on timer settings in the order of a few milliseconds.

This timer setting must ensure the combination of errors between the signal and the primary line current does not cause misoperation. Some of these "errors" are:

(1) Distortion of the secondary current because of saturation in the current transformers. This error can cause misoperation all by itself under worst conditions.

(1a) By contrast, a directional comparison scheme equipped with blocking units and transient blocking circuits will largely eliminate any possibility of false tripping due to CT saturation.

It is interesting to note that this is a much more significant problem in North America than it would be in Europe, for example. Station design in Europe is usually a single breaker per line where as North American practice is largely breaker and one half schemes. European relay literature points out that CT saturation is not a significant factor because the CT currents are the same at the two ends of the line. This is reasonable when considering European station design practice. However, considering long lines and North American station design and a worst cast scenario with a breaker open as shown in Fig. 5, the ratio of currents at the two ends of the line can be 40 or more. Also the two CT's at different experience with adverse residual flux in each. For example, if there had been a severe fault on the protected line with offset fault currents.

Another consideration is that if a zero sequence phase comparison is used, for 00 or 30 faults there is no "real" zero sequence current in the fault. Thus the only zero sequence current seen by the phase comparison relay is the CT error current.

(2) Travelling waves on fault inception can result in apparent phase shifts of the current half cycles at the two ends, tending to reduce the security margin on long lines.

(2a) Travelling waves can also impact the security of distance relays but in high performance transmission line relays the circuit design ensures the travelling waves cannot cause misoperation.

The maximum reliability of a relay system is obtained by the optimum balance of dependability and security. Because a directional comparison scheme is comparing relay decisions rather than instantaneous current quantities, the operating time of the different functions in a directional comparison scheme can be modified to increase both the dependability and the security of the relay system.

To increase dependability, very fast relay operation is desirable when fault currents are large enough to saturate CT's quickly. One very long line that included a direct transfer trip capability achieved 1 1/2 cycle clearing time for near end faults with nominal 2 cycle breakers. Typical clearing time at the remote terminal was 2 cycles with nominal 2 cycle breakers. The fault was typically angle fault and occurred about 100 miles from one end.

By contrast, fault currents in the order of the surge impedance loading require much slower operating times if reasonable levels of security are to be achieved. For example, there was a power system blackout when two, parallel, series compensated 500 kV lines were tripped incorrectly. There was no fault on the system. The first line tripped as a result of a component failure (the fact that it was a phase comparison system is believed to be irrelevant).

The phase comparison system on the parallel line responded to the staggered pole clearing on the first line and initiated a trip. The blocking channel failed to respond initially, resulting in the tripping of the second line and the subsequent power system failure.

The channel errors may be a result of human error. In a different system to that covered by the report mentioned above, a long line was protected in part by a phase comparison scheme that did not respond to load current. Each end of the line was owned and operated by different companies. When the scheme started false tripping, each company tested their own terminal several times without determining the cause. It was almost 2 years before both companies could schedule simultaneous testing at both ends to check the channel delay timers that proved to be incorrectly set. By contrast, a directional comparison terminal could be tested independently by each company.

(3) Any positive or negative variation in channel time and/or any error in setting the phase delay to compensate for the channel results in a reduction of inherent security.

. (3a) In a directional comparison tripping scheme, a variation in channel time does not impact security. In a blocking scheme, a time delay greater than the maximum channel time can be used to provide a margin to ensure security.

In practice, the phase comparison relaying is very much more likely to see an external fault than a directional comparison scheme using distance relays, and thus, on a statistical basis, is very much more likely to trip on external faults due to channel errors. This tendency is borne out by experience. An illustration of how far a phase comparison system can see was emphasized when a human error in setting fault detectors caused a 500 kV series compensated line in California to trip incorrectly for a SLG fault on a 69 kV in Nevada.

It should be noted that if directional overcurrent relaying is used in the directional comparison scheme instead of ground distance relays, then some reduction in security will result. The amount of the reduction in security will vary considerably with different designs of directional and overcurrent units. The positive sequence restrained zero sequence overcurrent has excellent security.

In contrast with the wide disparity of security between phase comparison and directional comparison schemes, there appears to be no diminution in dependability of either scheme because of the series capacitors.

However, since series compensated lines tend to be long to very long, both the phase comparison schemes and directional comparison schemes tended to be supplemented by direct trip functions. Thus, the high level of dependability indicated by experience is attributable to both the direct trip functions and the pilot functions and hence does not indicate the dependability of either pilot function by itself. The five year report mentioned earlier does not mention failure to operate.

The previous comparison is specifically related to transmission line relaying, and particularly to long series compensated lines. In subtransmission systems where false tripping is unlikely to cause a major system blackout, the disadvantage of phase comparison is less significant.

Some cases of short, double-circuit lines with single pole tripping to increase the reliability of double circuits tend to favor the use of segregated phase comparison or segregated current differential schemes. Studies and some field data has indicated that intercircuit fault may exceed single line to ground faults on double circuit lines.

PT LOCATION

When tappets series capacitors are used, and the relaying channel is over power line carrier, it is generally recommended that the potential source be located on the line side of the series capacitors. The wave traps are located between the series capacitors and the potential location to provide some attenuation of the carrier frequency noise generated when the gaps flash.

With the potential location on the line side of the series capacitors, the effective reach of direct tripping distance relays can be increased. Line side potential may require the use of "compensated" directional units if directional overcurrent relaying is employed. In negative or zero sequence, directional units without compensation the directional units may maloperate on forward faults if the capacitor impedance is larger than the source impedance behind the bus.

If bus side potential is used with sensitive directional overcurrent relaying, then there is a possibility that the directional overcurrent relaying could operate on heavy load swings or 3 phase faults if capacitor bypassing is permitted on an unsymetrical basis. This may require desensitizing the overcurrent relay if it is set to detect very high resistance ground faults.

In general, where there is a free choice of line side or bus side potential location, the line side potential location is a logical choice for the improved relaying performance of direct tripping hybrid distance units. However, when series capacitors are added to an existing line, the cost and difficulty of moving the potential location should be evaluated against the benefits of the improved relaying, In general, the use of high percentage compensation, high protective levels, high speed gap protection, and power line carrier will tend to provide a higher justification for line side potential.

CHANNEL CONSIDERATIONS

On very important lines where relaying performance is important to the reliability of the power system, the choice of both the relays and channels should be based on their impact on system reliability. The following philosophical concepts should be considered:

(a) The clearing times should be significantly less than the critical switching times, and increase at a slower note than the critical switching time. However, faster relay operating times should not be used at the expense of security if the clearing time is substantially less than the critical switching time.

(b) The relaying system should be selected with an optimum balance between the relays and channels. On very long lines, and particularly series compensated lines, the optimum relaying system for maximum reliability tends to vary with different fault locations, As discussed previously, for faults near one end, the fault current at the other end can be very small, or zero, or even in the wrong direction (fault current reversal with series caps). For the near end faults, a direct under reaching transfer trip scheme is ideal for this case. However, for mid line faults the direct underreaching transfer trip scheme is very poor if the series capacitors have caused a significant reduction in line coverage of the direct trip functions. For the mid line faults a permissive overreaching type of scheme is ideal. Thus, for maximum performance a combined scheme using two channels is recommended with the receipt of either channel providing a permissive trip signal and the receipt of both channels producing a direct transfer trip. Some of the advantages of the combined scheme are:

(1) greater dependability is achieved by providing a channel only means of tripping the remote end

(2) greater dependability is achieved in the case of a single channel failure since the second channel assures a pilot channel is still in service.

(3) greater security can be achieved since the remote end relays on a near end fault do not have to operate to achieve remote end tripping and then can be designed and set to emphasize security

(4) since the combined scheme provides double channel direct transfer trip, it can be used for breaker failure or other equipment failure. In the Southwest Region of the United States, the combined scheme is implemented by using one channel for the permissive relay channel and two separate channels for direct transfer trip (which are keyed by the line channels). They also use path diversity by putting the three channels associated with one relay system over power line carrier and the other three channels over microwave. It is believed the justification of using three channels provides greater separation of the channels to lessen human errors. However, there are hundreds of applications of the two channel approach.

In either the two or three channel arrangement provision must be made to initiate reclosing when the direct trip is keyed by the relays and blocked by the direct trip when it is keyed by equipment failure. This provision is often achieved by the duration of the direct trip; ceases with fault clearance when keyed by the line relays but maintained by equipment failure keying for a predetermined time that either locks out reclosing or cancels any local initiation of reclosing.

So as not to delay reclosing the direct trip blocks reclosing after the reclosing timer. In addition, local reclose blocking (for example fault serverity) must be arranged to take priority over the reclose initiation of the direct transfer trip.

The report previously referred to covering 5 years relaying experience is no longer available for dissemination.

There was an English paper covering statistical performance of phase comparison with directional comparison but the reference has been lost. It is unlikely that it is relevant to series compensated lines.

The discussion relates in general to phase and directional comparison schemes designed for series compensated lines. It should be emphasized the extremely high fake trip rate of the phase comparison scheme that was not designed for series capacitors. It seems very likely that a direction comparison scheme not designed for series compensated lines will have acceptable performance without testing and modification. It may be noted that EM relays were tested for one application of sub transmission lines adjacent to a series compensated transmission line. The tentative conclusion was that adequate performance could be obtained with scheme modifications.

Some brief references have been made to relaying philosophy as it pertains to transmission lines and sub transmission lines. This is a very broad subject and is well beyond the scope of this report. Never the less, it is possibly the most significant factor in achieving maximum reliability of the power system based on relay performance.