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Digital Low-Impedance Bus Differential Protection: Principles and Approaches

DIGITAL LOW-IMPEDANCE BUS DIFFERENTIAL PROTECTION – REVIEW OF PRINCIPLES AND APPROACHES

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1. Introduction

Protection of power system busbars is one of the most critical relaying applications. Busbars are areas in power systems where fault current levels may be very high. In spite of that, some of the circuits connected to the bus may have their Current Transformers (CTs) insufficiently rated. This creates a danger of significant CT saturation and jeopardizes security of the busbar protection system.

A false trip of a distribution bus can cause outages to a large number of customers as numerous feeders and/or subtransmission lines may get disconnected. A false trip of a transmission busbar may drastically change system topology and jeopardize power system stability. Hence, the requirement of a maximum security of busbar protection.

On the other hand, bus faults generate large fault currents. If not cleared promptly, they endanger the entire substation due to both dynamic forces and thermal effects. Hence, the requirement of high-speed operation of busbar protection.

With both security and dependability being very important for busbar protection, the preference is always given to security.

Techniques commonly applied for protection of busbars are reviewed in Section 2.

Recently, microprocessor-based low-impedance relays have gained more trust due to advances in technology (fast processors, fiber optic communications) and sophisticated algorithms making them immune to CT saturation.

This paper presents a new algorithm for microprocessor-based low-impedance differential relay (Section 3) that combines the differential (Section 4) and current directional (Section 5) protection principles within a frame of an adaptive algorithm controlled by a dedicated CT saturation detection module (Section 6). Implementation of the algorithm is briefly presented (Section 7). The results of extensive testing with the use of the Real-Time Digital Simulator – RTDS (Section 8) prove excellent performance in terms of both speed and security.

2. Busbar Protection Techniques

Power system busbars vary significantly as to the size (number of circuits connected), complexity (number of sections, tie-breakers, disconnectors, etc.) and voltage level (transmission, distribution).

The above technical aspects combined with economic factors yield a number of solutions for busbar protection.

2.1. Interlocking Schemes

A simple protection for distribution busbars can be accomplished as an interlocking scheme. Overcurrent (OC) relays are placed on an incoming circuit and at all outgoing feeders. The feeder OCs are set to sense the fault currents on the feeders. The OC on the incoming circuit is set to trip the busbar unless blocked by any of the feeder OC relays (Figure 1). A short coordination timer is typically required to avoid race conditions.

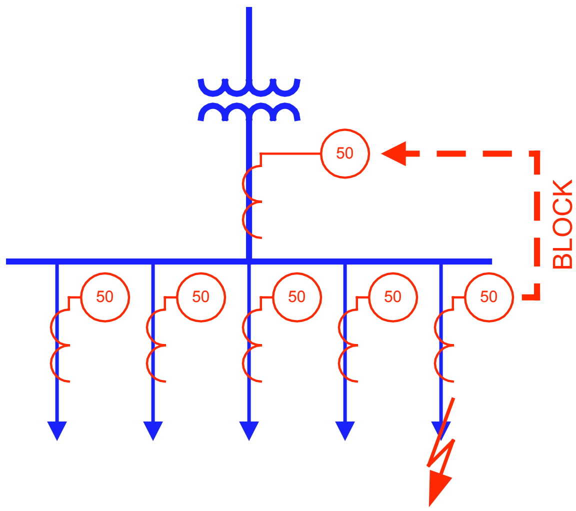

Fig.1. Illustration of the interlocking scheme.

When using microprocessor-based multi-functional relays it becomes possible to integrate all the required OC functions in one or few relays. This allows not only to reduce the wiring but also to shorten the coordination time and speed-up operation of the scheme.

Modern relays provide for fast peer-to-peer communications using protocols such as the UCA with the GOOSE mechanism [1]. This allows eliminating wiring and sending the blocking signals over the communications.

The scheme although easy to apply and economical is limited to specific busbar configurations.

2.2. Overcurrent Differential

Typically a differential current is created externally to a current sensor by summation of all the circuit currents (Figure 2). Preferably the CTs should be of the same ratio. If they are not, matching CT (or several CTs) is needed. This in turn may increase the burden for the main CTs and make the saturation problem even more serious.

Historically, means to deal with the CT saturation problem include definite time or inverse-time overcurrent characteristics.

Although economical and applicable to distribution busbars, this solution does not match performance of more advanced schemes and should not be applied to transmission-level busbars.

The principle, however, may be available as a protection function in an integrated microprocessor-based busbar relay. If this is the case, such unrestrained differential element should be set above the maximum spurious differential current and may give a chance to speed up operation on heavy internal faults as compared to a percent (restrained) bus differential element.

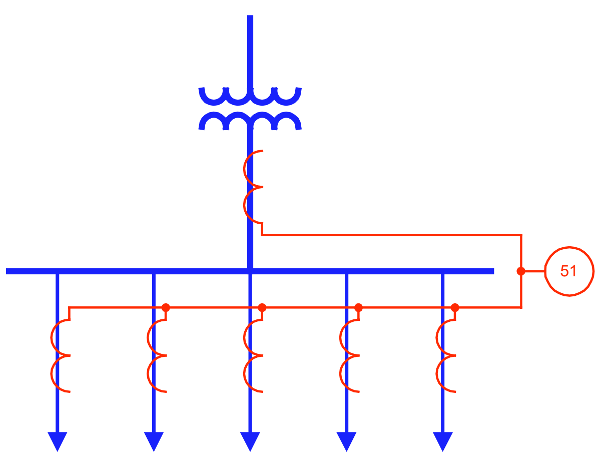

Fig.2. Overcurrent differential protection.

2.3. Percent Differential

Percent differential relays create a restraining signal in addition to the differential signal and apply a percent (restrained) characteristic. The choices of the restraining signal include “sum”, “average” and “maximum” of the bus currents. The choices of the characteristic include typically single-slope and double-slope characteristics.

This *low-impedance* approach does not require dedicated CTs, can tolerate substantial CT saturation and provides for high-speed tripping.

Many integrated relays perform CT ratio compensation eliminating the need for matching CTs.

This principle became really attractive with the advent of microprocessor-based relays because of the following:

- Advanced algorithms supplement the percent differential protection function making the relay very secure.
- Protection of re-configurable busbars becomes easier as the dynamic bus replica (bus image) can be accomplished without switching current secondary circuits.
- Integrated Breaker Fail (BF) function can provide optimal tripping strategy depending on the actual configuration of a busbar.
- Distributed architectures are proposed that place Data Acquisition Units (DAU) in bays and replace current wires by fiber optic communications.

2.4. High-Impedance Protection

High-impedance protection responds to a voltage across the differential junction points. The CTs are required to have a low secondary leakage impedance (completely distributed windings or toroidal coils). During external faults, even with severe saturation of some of the CTs, the voltage does not rise above certain level, because the other CTs will provide a lower-impedance path as compared with the relay input impedance. The principle has been used for more than half a century because is robust, secure and fast.

The technique, however, is not free from disadvantages. The most important ones are:

- The high-impedance approach requires dedicated CTs (significant cost associated).
- It cannot be easily applied to re-configurable buses (current switching using bistable auxiliary relays endangers the CTs, jeopardizes security and adds an extra cost).
- It requires a voltage limiting varistor capable of absorbing significant energy during busbar faults.
- The scheme requires only a simple voltage level sensor. From this perspective the high-impedance protection *scheme* is not a *relay*. If BF, event recording, oscillography, communications, and other benefits of microprocessor-based relaying are of interest, then extra equipment is needed (such as a Digital Fault Recorder or dedicated BF relays).

2.5. Busbar Protection using Linear Couplers

A linear coupler (air core mutual reactor) produces its output voltage proportional to the derivative of the input current. Because they are using air cores, linear couplers do not saturate.

During internal faults the sum of the busbar currents, and thus their derivatives, is zero. Based on that, a simple busbar protection is thus achieved by connecting the secondary windings of the linear couplers in series (in order to respond to the sum of the primary currents) and attaching a low-energy voltage sensor (Figure 3).

Disadvantages of this approach are similar to those of the high-impedance scheme.

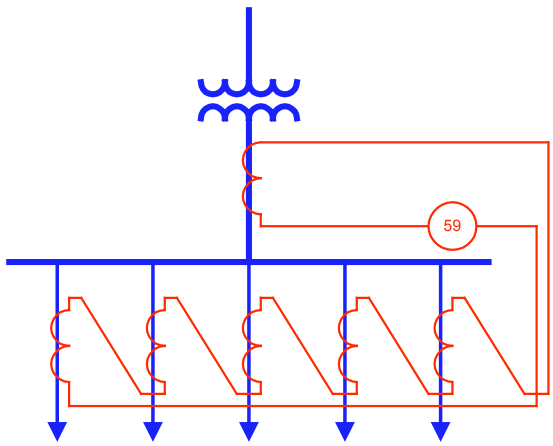

Fig.3. Busbar protection with linear couplers.

2.6. Microprocessor-based Relays and Multi-Criteria Solutions

The low-impedance approach used to be perceived as less secure when compared with the high-impedance protection. This is no longer true as microprocessor-based relays apply sophisticated algorithms to match the performance of high-impedance schemes [2-6], and at the same time, the cost considerations make the high-impedance scheme less attractive [7]. This is particularly relevant for large (cost of extra CTs) and complex (dynamic bus replica) buses that cannot be handled well by high-impedance schemes.

Microprocessor-based low-impedance busbar relays are developed in one of the two architectures:

- Distributed busbar protection uses DAUs installed in each bay to sample and pre-process the signals and provide trip rated output contacts (Figure 4). It uses a separate Central Unit (CU) for gathering and processing all the information and fiber-optic communications between the CU and DAUs to deliver the data. Sampling synchronization and/or time-stamping mechanisms are required. This solution brings advantages of reduced wiring and increased computational power allowing for additional functions such as back-up OC protection or BF per circuit.
- Centralized busbar protection requires wiring all the signals to a central location, where a single relay does the entire processing (Figure 5). The wiring cannot be reduced and the calculations cannot be distributed between a number of DAUs imposing more computational demand for the central unit. On the other hand, this architecture is perceived as more reliable and suits better retrofit applications.

Algorithms for low-impedance relays are aimed at [2,4]:

(a) Improving the main differential algorithm by providing better filtering, faster response, better restraining technique, robust switch-off transient blocking, etc.

(b) Incorporating a saturation detection mechanism that would recognize CT saturation on external faults in a fast and reliable manner.

(c) Applying a second protection principle such as phase directional (phase comparison) for better security.

This paper describes an algorithm that successfully addresses the aforementioned objectives.

3. Overview of the New Algorithm

The presented solution incorporates: enhanced percent differential characteristic, fast and robust saturation detection and current directional principle.

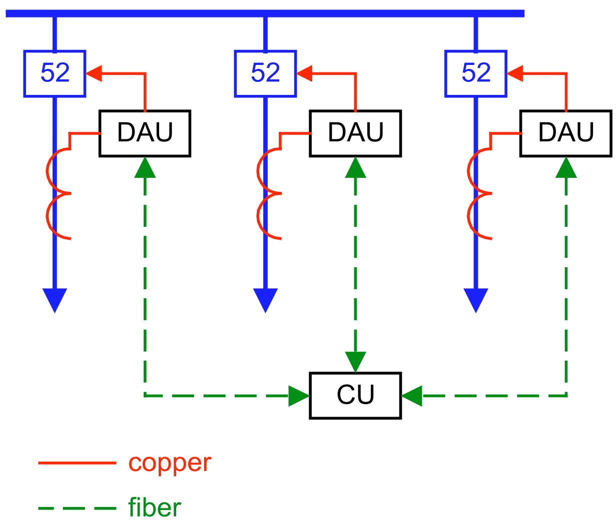

Fig.4. Distributed busbar protection.

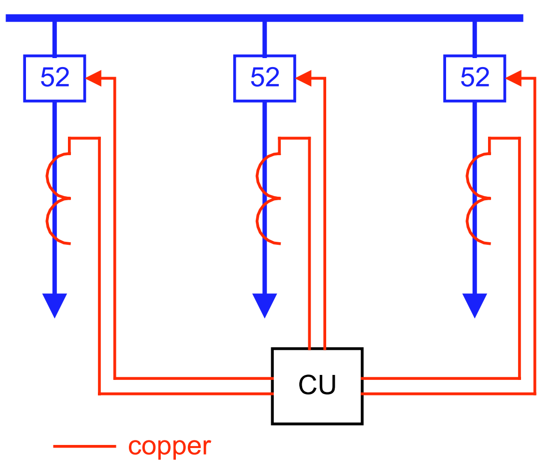

Fig.5. Centralized busbar protection.

The differential protection function uses a double-slope double-breakpoint characteristic. In order to enhance the security, the operating region of the characteristic is divided into two areas (Figure 6) having diverse operating modes.

The bottom portion of the characteristic applies to comparatively low differential currents and has been introduced to deal with CT saturation on low-current external faults. Certain distant external faults may cause CT saturation due to extremely long time constants of the d.c. components or due to multiple autoreclosure shots. The saturation, however, is difficult to detect in such cases. Additional security is permanently applied to this region without regard to the saturation detector.

The top region includes the remaining portion of the differential characteristic and applies to comparatively high differential currents. If, during an external fault, the spurious differential current is high enough so that the differential–restraining current trajectory enters the top region, then such CT saturation is guaranteed to be detected by the saturation detector.

The relay operates in the 2-out-of-2 mode in the first region of the differential characteristic. Both differential (Section 4) and current directional (Section 5) principles must confirm an internal fault in order for the relay to operate (Figure 7).

The relay operates in the dynamic 1-out-of-2 / 2-out-of-2 mode in the second region of the differential characteristic. If the saturation detector (Section 6) does not detect CT saturation, the differential protection principle alone is capable of tripping the busbar. If CT saturation is detected, both differential and directional principles must confirm an internal fault in order for the relay to operate.

Because of diverse operating modes in the first and second regions of the differential characteristic, the user gains double control over dependability and security. The first level includes slopes and breakpoints of the characteristic with regard to the amount of the restraint. The second level involves control over the split between the bottom (biased towards security) and top (biased towards speed) regions of the characteristic.

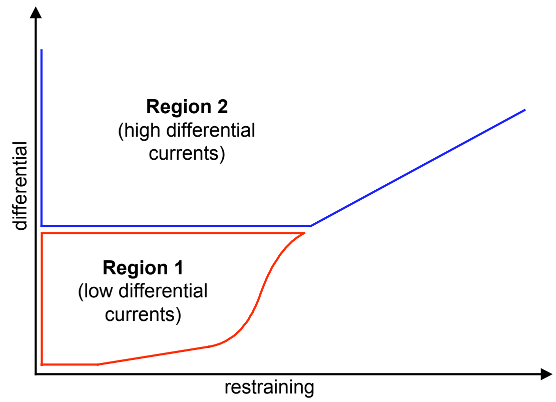

Fig.6. Two regions of the differential characteristic.

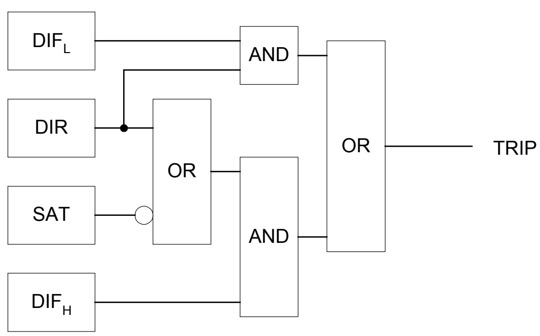

Fig.7. Adaptive trip logic.

4. Differential Principle

4.1. Differential and Restraining Currents

The algorithm uses an enhanced digital mimic filter to remove the decaying d.c. component (-s) and provide band-pass filtering. The filter is a Finite Impulse Response (FIR) filter having the data window of 1/3rd of the power system cycle. The full-cycle Fourier algorithm is used for phasor estimation. The combination of the pre-filter and phasor estimator reduces transient overshoot errors to less than 2%.

The differential current is produced as a sum of the phasors of the input currents of a differential bus zone taking into account the connection status of the currents, i.e. applying the dynamic bus replica of the protected bus zone. The CT ratio matching is performed before forming the differential and restraining currents.

The restraining current is produced as a maximum of the magnitudes of the phasors of the bus zone input currents taking into account the connection status of the currents.

The "maximum of" definition of the restraining signal biases the relay toward dependability without jeopardizing security as the relay uses additional means to cope with CT saturation on external faults. An additional benefit of this approach is that the restraining signal always represents a physical – compared to the "average" and "sum of" approaches – current flowing through the CT which is most likely to saturate during a given external fault. This brings more meaning to the breakpoint settings of the operating characteristic.

4.2. Differential Characteristic

The relay uses a double-slope double-breakpoint operating characteristic shown in Figure 8.

The PICKUP setting is provided to cope with spurious differential signals when the bus carries a light load and there is not any effective restraining signal.

The first breakpoint (LOW BPNT) is provided to specify the limit of guaranteed linear operation of the CTs in the most unfavorable conditions such as high residual magnetism left in the magnetic cores or multiple autoreclosure shots. This value defines the upper limit for the application of the first, lower slope (LOW SLOPE).

The second breakpoint (HIGH BPNT) is provided to specify the limits of operation of the CTs with substantial saturation. This point defines the lower limit for the application of the second slope (HIGH SLOPE).

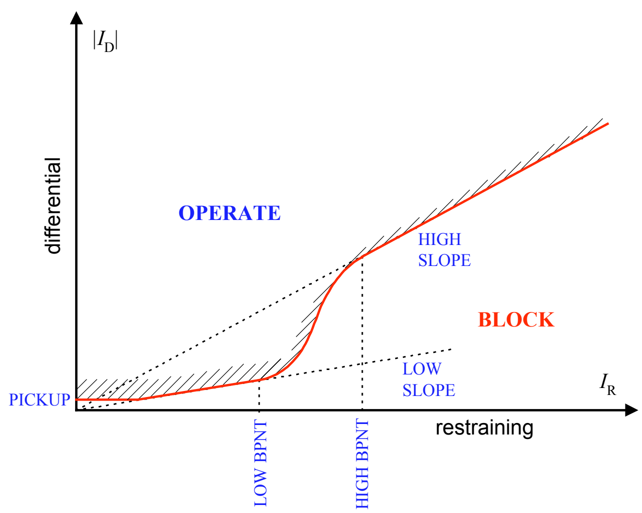

Fig.8. Percent characteristic and its settings.

The higher slope used by the relay acts as an actual percent restraint regardless of the value of the restraining signal. This is so because the boundary of the operating characteristic in the higher slope region is a straight line intersecting the origin of the differential – restraining plane. The advantage of having a constant percent restraint specified by the HIGH SLOPE setting creates an obstacle of a discontinuity between the first and second slopes. This is overcome by using a smooth (cubic spline) approximation of the characteristic between the lower and higher breakpoints.

The adopted characteristic ensures:

- a constant percent restraint of LOW SLOPE for restraining currents below the lower breakpoint of LOW BPNT;
- a constant percent restraint of HIGH SLOPE for restraining currents above the higher breakpoint of HIGH BPNT; and
- a smooth transition from the restraint of LOW SLOPE to HIGH SLOPE between the breakpoints.

The characteristic allows more precise setting of the differential element regarding performance of the CTs.

5. Directional Principle

For better security, the relay uses the current directional protection principle to dynamically supervise the main current differential function. The directional principle is applied permanently for low differential currents (region 1 in Figure 6) and is switched-on dynamically for large differential currents (region 2 in Figure 1) by the saturation detector (Figure 7) upon detecting CT saturation.

The directional principle responds to a relative direction of the fault currents. This means that a reference signal, such as a bus voltage, is not required. The directional principle declares that:

- either all of the fault currents flow in one direction, and thus, the fault is internal;
- or at least one fault current flows in an opposite direction as compared with the sum of the remaining currents, and thus, the fault is external.

The directional principle is implemented in two stages.

First, based on the magnitude of a given current, it is determined whether a given CT current is a fault current. If so, its relative phase relation must be considered in the next step. The angle

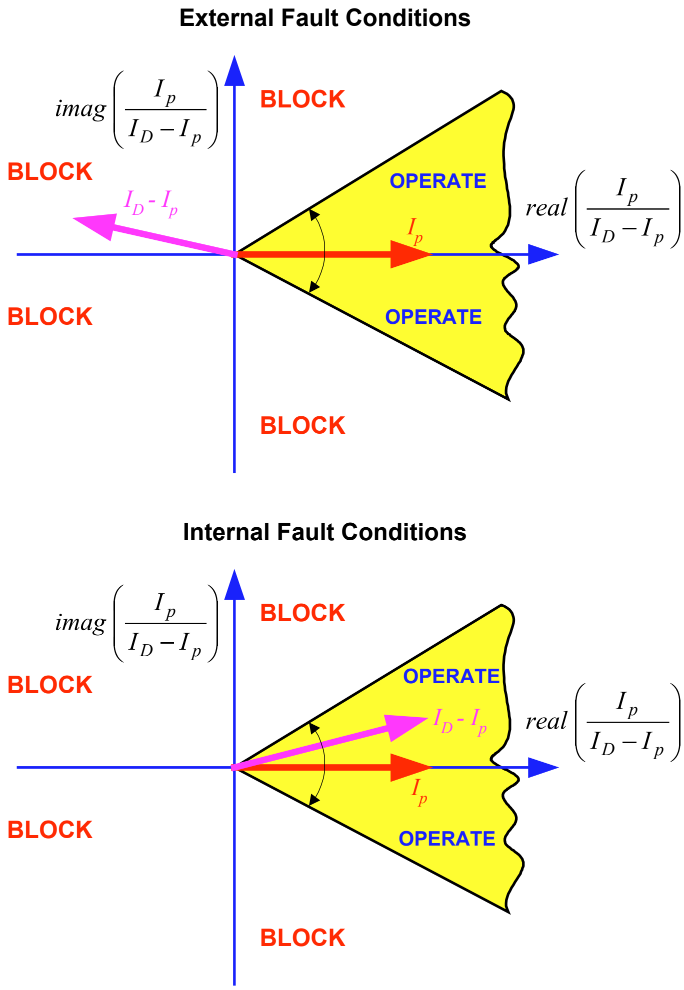

Fig.9. Illustration of the directional principle.

check must not be initiated for the load currents, as the direction will be out of the bus even during internal faults.

The auxiliary comparator of this stage applies an adaptable threshold. The threshold is the lower of the low breakpoint and certain fraction of the restraining current.

Second, for – and only for – the fault currents selected in the first stage the phase angle between a given current and the sum of all the remaining currents is checked. The sum of all the remaining currents is the differential current less the current under consideration. Therefore, for each, say p-th, current to be considered the angle between the phasors I_{p} and I_{D}-I_{p} is to be checked.

Ideally, during external faults the said angle is close to 180 degrees; and during internal faults – close to 0 degrees (Figure 9).

The limit (threshold) angle applied is 90 degrees. Analyzing the waveform of a saturated current one would conclude that it is physically impossible for the phasor of a current supplied by a saturated CT to display an angle error greater than 90 degrees. Thus, the selected limit angle.

The directional principle must have some short intentional delay (“security count”) added in order to cope with unfavorable transients. Because of that and the natural response speed resulting from the applied phasor estimators, the directional principle – although very secure – is slightly slower as compared with the differential principle. In order to gain some speed the directional check is not applied permanently – like in some approaches [2] – but switched on and off dynamically as requested by the saturation detector.

6. CT Saturation Detection

The saturation detector of the relay takes advantage of the fact that any CT operates correctly for a short period of time even under very large primary currents that would subsequently cause a very deep saturation. As a result of that, in the case of an external fault the differential current stays very low during the initial period of linear operation of the CTs, while the restraining signal

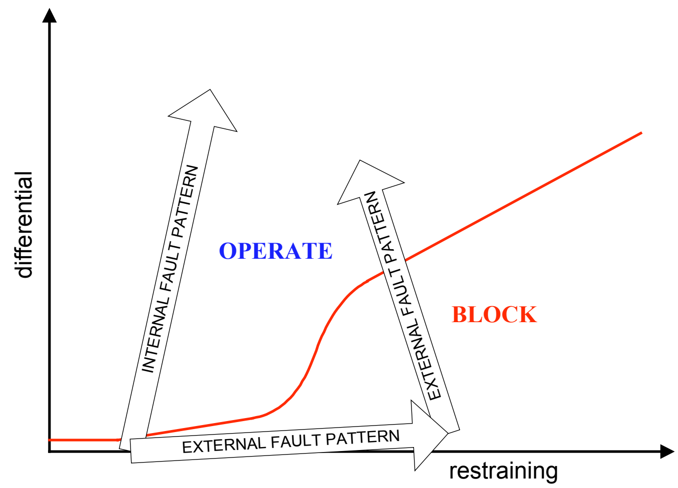

Fig.10. Saturation detection: internal and external fault patterns.

develops rapidly. Once one or more CTs saturate, the differential current will increase. The restraining signal, however, precedes by at least few milliseconds. During internal faults both the differential and restraining currents develop simultaneously. This creates characteristic patterns for the differential – restraining trajectory as depicted in Figure 10.

The CT saturation condition is declared by the saturation detector when the magnitude of the restraining signal becomes larger than the higher breakpoint (HIGH BPNT) and at the same time the differential current is below the first slope (LOW SLOPE). This condition is of the transient nature and requires "sealing". A special logic in the form of a state machine is used for this purpose as depicted in Figure 11.

As the phasor estimator introduces a delay into the measurement process, the aforementioned saturation test would fail to detect CT saturation that occurs very fast. In order to cope with very fast CT saturation, another condition is checked that uses relations between the signals at the waveform-sample level. The basic principle is similar to that described above. Additionally, the sample-based path of the saturation detector uses the time derivative of the restraining signal (di/dt) to trace better the saturation pattern shown in Figure 10.

7. Implementation

The described algorithm has been implemented using the concept of a "universal relay" — a modular, scaleable and upgradable engine for protective relaying [1].

The relay is built as a centralized architecture. It samples its input signals at 64 samples per cycle. The phasors, although calculated using all 64 samples, are refreshed 8 times a cycle. The algorithm's logic is evaluated 8 times per cycle. The dynamic bus replica is refreshed 8 times per cycle.

The architecture incorporates all the commonly available features of a digital relay including metering, oscillography, event recording, self-monitoring, multiple setting groups, trip-coil monitoring, communications, etc.

8. Testing

Initial verification of the algorithm has been performed using Real-Time Digital Simulator (RTDS) generated waveforms and MATLAB simulations.

Several thousand cases have been analyzed at this stage. This included variety of bus configuration, variety of circuits connected (transformers, equivalent systems, loads), various CT

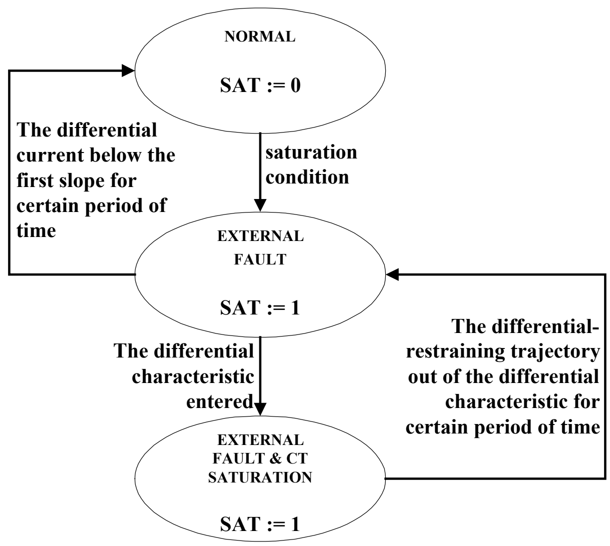

Fig.11. CT saturation detector: the state machine.

characteristics, internal and external faults, multiple autoreclosure actions, switching onto an internal faults, switching onto an external fault, and many others.

The final stage of testing has been performed using actual hardware, RTDS and high accuracy, high-power voltage and current amplifiers. The targeted sub-cycle operating times and enhanced security have been successfully validated.

Two examples have been included in this paper. In both examples a six-circuit bus is considered. The connected circuits are of different nature including lines, transformers of various connection types, and loads.

The measured currents are referenced as F1, F5, M1, M5, U1 and U5, respectively. The F1, F5, M1, M5 and U5 circuits are capable of feeding the fault current; the U1 circuit supplies a load. The F1, F5 and U5 circuits are significantly stronger than the F5 and M1.

The M5 circuit contains the weakest CT of the bus.

8.1. External Fault Example

Figure 12 presents the bus currents and the most important logic signals for a sample external fault. Despite very fast and severe CT saturation the relay remains stable.

8.2. Internal Fault Example

Figure 13 presents the same signals but for an internal fault. The relay operates in 10ms in a 60 Hz system.

9. Conclusions

The paper presents a new algorithm for low-impedance busbar protection. The algorithm combines restrained differential and current directional protection principles. An adaptive logic controlled by the saturation detector is used for optimum performance.

The presented algorithm has been implemented on a "universal relay" platform. The extensive RTDS tests have proven both the algorithm and its implementation extremely secure and fast. The relay operates typically with a sub-cycle time. This includes a trip-rated output contact.

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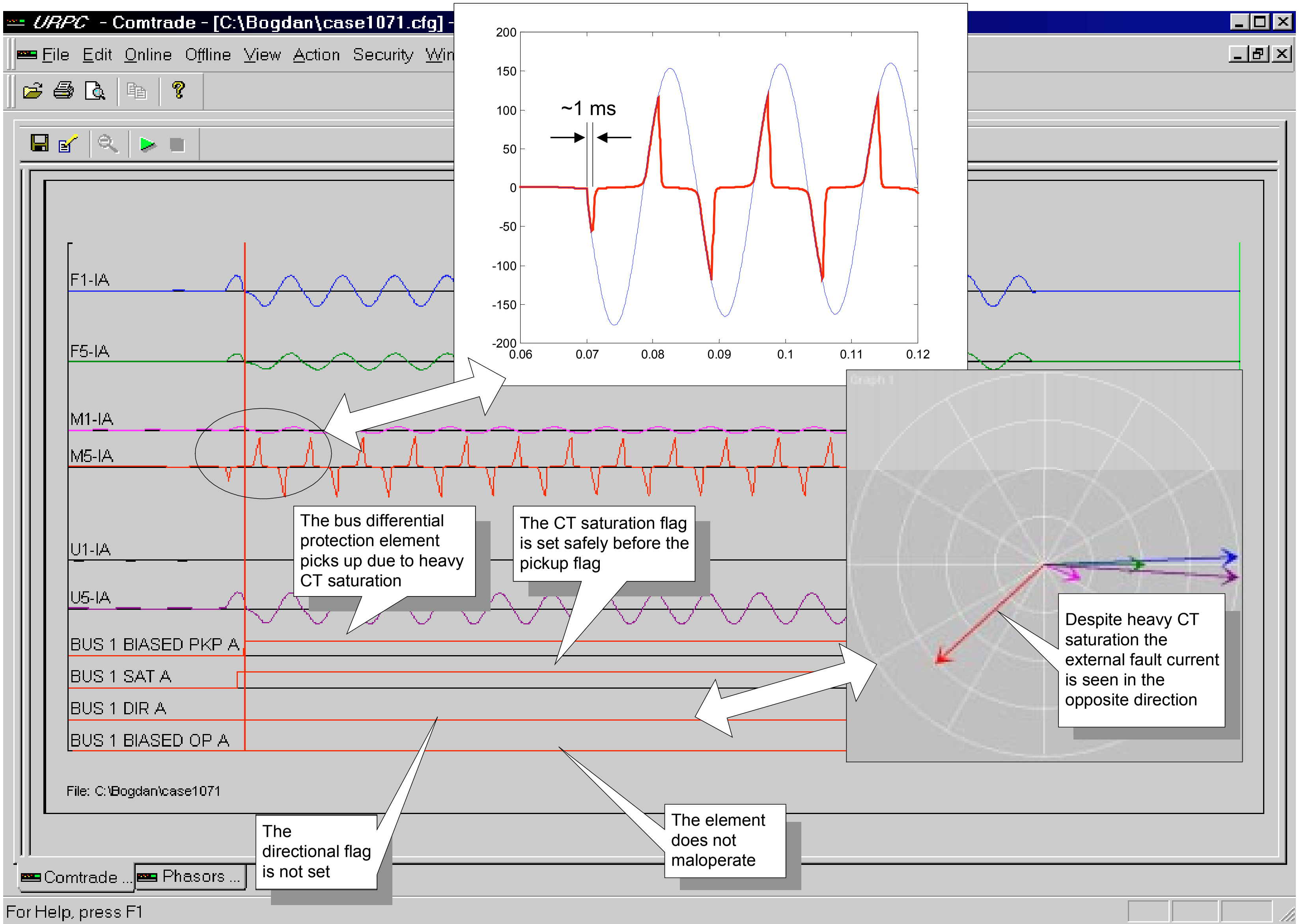

Fig.12. External fault example.

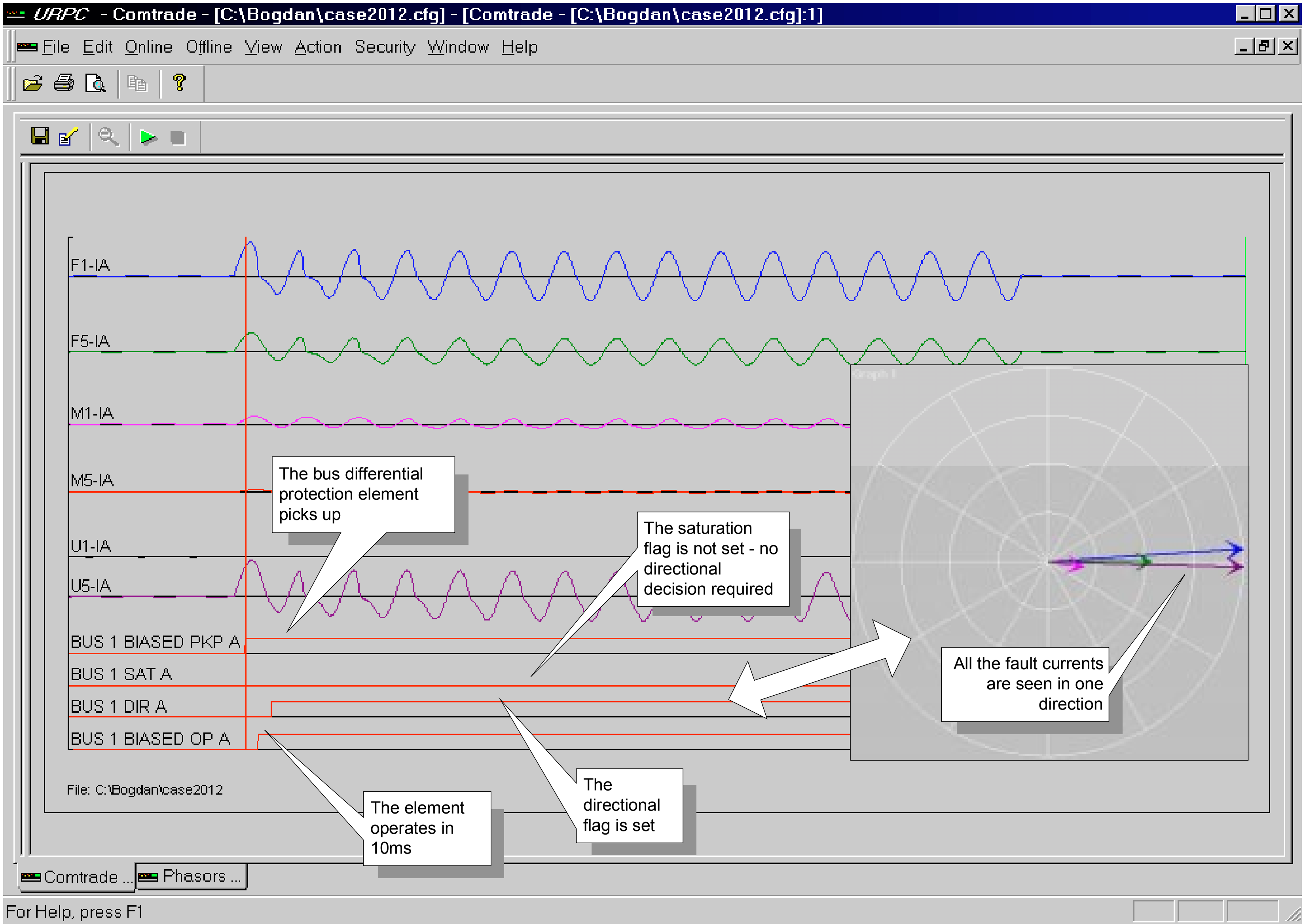

Fig.13. Internal fault example