GE Industrial Systems

Bridge Interface Controller Board
IS200BICIH_A_ _

These instructions do not purport to cover all details or variations in equipment, nor to provide every possible contingency to be met during installation, operation, and maintenance. If further information is desired, or if particular problems arise that are not covered sufficiently for the purchaser's purpose, the matter should be referred to GE Industrial Systems.

Safety Symbol Legend

WARNING — Indicates a procedure, practice, condition, or statement that, if not strictly observed, could result in personal injury or death.

CAUTION — Indicates a procedure, practice, condition, or statement that, if not strictly observed, could result in damage to or destruction of equipment.

Note — Indicates an essential or important procedure, practice, condition, or statement.

Contents

Functional Description

The IS200BICI Bridge Interface Controller Board (BICI) is a controller board for bridges using Integrated Gate Commutated Thyristor (IGCT) switching devices. The BICI board mounts in an Innovation Series™ board rack and interfaces to the IS200CABP Control Assembly Back-Plane Board (CABP) through its P1 and P2 backplane connectors (CABP connectors J15 and J20). Input power for the BICI board is provided by the DS200RAPA Rack Power Supply Board (RAPA) and comes from the CABP board through BICI board backplane connectors P1 and P2. The BICI board does not provide power to any other boards or assemblies. Gate control and status feedback signals from the IS200BPII Bridge Power Interface Board (BPII) are conditioned and sent to the BICI board via the P1 and P2 backplane connectors (see Figure 1).

Three connectors are located on the front panel of the BICI board, PFBK1, PFBK2, and PSRC.

- **PFBK1:** Feedback signals from the first full bridge or first half of the cells in a series bridge are brought back to the BICI board from the IS200GGXI Expander Load/Source Board (GGXI) through connector PFBK1 (44-pin high density and special twisted pair).

- **PFBK2:** Feedback signals from the optional second full bridge or the second half of the cells in a series bridge are brought back to the BICI board from the IS200GGXI Expander Load/Source Board (GGXI) through connector PFBK2 (44-pin high density and special twisted pair).
- **PSRC:** Feedback signals from the IS200GGXD Expander Diode Source Board (GGXD) and gate control signals for DB IGCT switches are brought back to BICI board through connector PSRC (50-pin high density using standard shielded twisted pair cable).

Voltage feedback isolation (by attenuation) is provided from the DS200NATO Voltage Feedback Scaling Board (NATO).

The BICI board has provisions for control of up to 28 IGCT devices, and produces a three-level inverter control. The BICI board also supports control of a diode source and DB (dynamic braking.)

Daughterboards

Nineteen daughterboards are soldered onto the BICI board. These daughterboards are the:

- IS205AOCA Analog Comparator Modules (AOCA)
- IS205DVAA Dual Voltage Controlled Oscillator (VCO) Modules (DVAA)

Eleven AOCA daughterboards are mounted on, and draw their power from, the BICI board. Each AOCA daughterboard provides eight independent identical comparator circuits. Each circuit compares an input voltage signal against an input reference voltage (total 8 comparator circuits against 8 references per AOCA daughterboard).

Eight DVAA daughterboards are also mounted on, and draw power and input clock sources from, the BICI board. Each DVAA daughterboard provides two identical VCO circuits and a pulse-train compatible output.

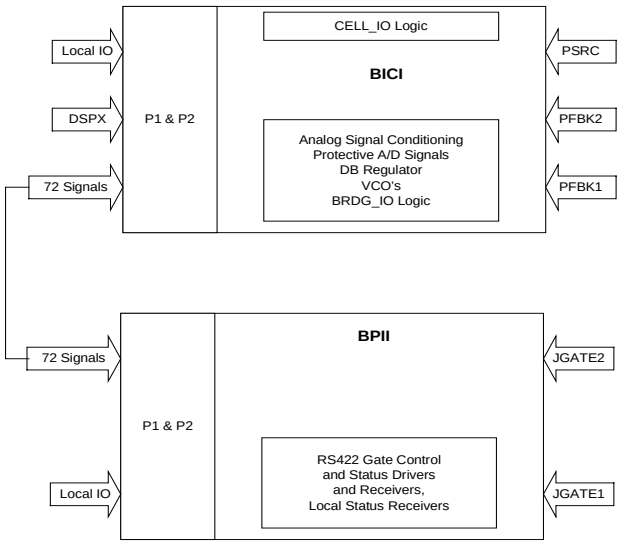

Figure 1. BICI Board and BPII Board Interface Connections

Electronic Board Identification

The BICI board incorporates a serial prom ID chip. The board identification (BRDID) net is extended to the GGXI boards through BICI board connectors PFBK1 and PFBK2. To verify that GGXI boards are connected properly, a pair of wires in the PFBK_ cable (from the BICI board to the GGXI boards) and in the JGATE cable (from the GGXI boards to the BPII board) are dedicated. To verify that the cables are not crossed, current is passed in opposite directions for the first and second GGXI boards. A signal showing that the current(s) have been detected in the correct direction is passed back to the BICI board (through the CABP board) from the BPII board. See Figure 2 for a diagram of this arrangement.

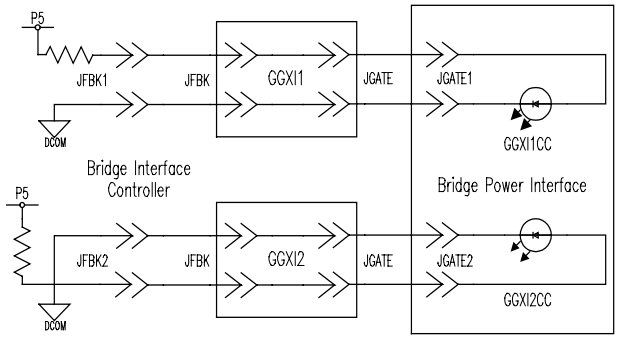

Figure 2. Board Identification Signals

Local DSP

The BICI board contains a local digital signal processor (DSP) that serves as a coprocessor for the DSPX board.

Boot Process

The local DSP is held in reset by default until the host DSPX board configures all logic devices and loads a boot table image for a bootstrap loader function into the DPRAM. The DSPX board then releases the reset so that the local DSP may boot the image in DPRAM. Boot up of the local DSP then continues under DSPX board control until complete. The local DSP will then begin executing the loaded code

Coordination

Coordination between the DSPX board and the local DSP is performed by a combination of software and firmware. Access to the local hardware register set is shared between the DSPX board and the local DSP with arbitration built into the BICI board register logic. Only one processor has write access to the register set at a time, and has to pass control to the other processor. At RESET, the DSPX board's processor has write access. Read access is arbitrated on a first come-first served basis.

Memory Map

The local DSP memory map is a subset of the DSPX memory map. It includes SRAM, DPRAM, and bridge interface controller registers.

DSP Hardware Access

The BICI board incorporates a connector header for emulator access to the local DSP. A ground pin in this connector is used to detect the emulator and release the RESET pin, even while the logic is not yet configured so that the emulator may function. A connector header is also provided for access to the high-speed serial port for monitor access supported by a software implemented UART.

Current Feedback Signals

Analog signals from active current transformer current sensor burden resistors are brought back to the BICI board on twisted pairs within shielded cables.

These signals are received differentially and are used to produce protective logic signals for hardware action and software inputs for control functions. (The logic signals are created by comparing the analog input signals against various programmable values.)

Protective Turnoff (Overcurrent) Signals: When these signals indicate that the current is excessive, the associated device is turned OFF immediately. The CELL_IO FPGA processes these to turnoff the victim cell(s) in an appropriate manner relative to other bridge conditions. A protective turnoff (PTO) may be initiated by a Load Fault (latched), an overcurrent condition (transient), or a gate driver fault (latched).

Load Fault (di/dt) Turnoff Signals: When these signals indicate that current is out of control due to a load fault, the associated device is turned OFF while it is still possible. The CELL_IO FPGA processes these to turnoff the victim cell(s) in an appropriate manner relative to other bridge conditions.

Current Freeze Faults Signals: When these signals indicate that the current is too large to be turned off safely at the present rate of change, the CELL_IO FPGA processes them and prevents the victim cell(s) from being turned OFF because they are at risk. This allows the fuses an opportunity to protect the bridge. These events set report latches in the status registers that are cleared when read by the processor. If the cell test mode is not active, and the events last longer than the programmable freeze fault latch filter time, a fault latch is set and the drive is tripped. The freeze fault latch is RESET by the fault RESET command.

Current Present Detection (Current Not Low): These signals are monitored to detect when current is flowing in the reverse parallel diode in the bridge in order to preserve bridge IGCT, gate driver, and power supply ratings. The signals are processed by the CELL_IO FPGA to optionally skip turn-on commands when they would produce no useful contribution to load current.

Software Feedbacks: Each analog current feedback is passed through a synchronous VCO to produce a frequency that is representative of the voltage value of the feedback signal.

The output of each VCO goes to 2 MHz for a full scale positive input (+5 V) and to 0 Hz for a full scale negative input (–5 V). These frequencies drive counters in the BRDG_IO FPGA logic that are read by the active DSP to produce current feedback values.

Voltage Feedback Signals

Analog signals from voltage attenuator burden resistors are brought back to the BICI board on twisted pairs within shielded cables. These signals are received differentially and are used to produce protective logic signals for hardware action and software inputs for control functions. (The logic signals are created by comparing the analog input signals against various programmable values.)

Overvoltage Signals: Voltage feedbacks representing dc link voltage levels are monitored to detect an overvoltage condition. These are processed by the CELL_IO FPGA to alert the drive of the condition.

Shoot-Through Fault Signals: Voltage feedbacks representing the voltage across the link reactor are monitored to detect excessive di/dt in the dc link. If the condition lasts longer than the fault filter time, a shoot-through fault latch is set causing the drive to trip. This is a major fault and the exact path of the fault current cannot be determined from available signals, so a freeze action is initiated for all phases. The freeze action continues until the duration counter expires. This provides a delay for the fuses in the faulting phase to clear before allowing all cells to turnoff where able. This is done to prevent the freeze action from blowing fuses in other phases. The shoot-through fault latch must be RESET by a general fault RESET command.

DB Regulator: Voltage feedbacks representing dc link voltages from uncontrolled rectifier source bridges are monitored for maximum and minimum ripple peak values. These are processed by the BRDG_IO FPGA to activate a ripple driven DB regulator. The regulator commands are used to properly control the DB Bridge IGCT switches.

Software Feedbacks: Each analog voltage feedback is passed through a synchronous VCO to produce a frequency that is representative of the voltage value of the feedback signal.

The output of each VCO goes to 2 MHz for a full scale positive input (+5 V) and to 0 Hz for a full scale negative input (–5 V). VCOs that are fed by unipolar voltage signals are scaled for 0 – 5 V full scale and produce an output frequency of 0 Hz for 0 V and 2 MHz for 5 V. Negative unipolar signals are inverted so that they also drive 0 – 5 V into a VCO. These frequencies drive counters in the BRDG_IO FPGA logic that are read by the active DSP to produce voltage feedback values.

Gating Command Timing Requirements

All gating commands issued by the BICI board to the IS200IGPA Gate Driver Power Supply Board (IGPA) have **minimum on** and **minimum off** time restraints.

- A **minimum on** time is the time after the IGCT is turned on during which it cannot be turned off without risking damage to the device.
- A **minimum off** time is the time after the IGCT is turned off that it may not be turned on without risking damage to the device.

The following are some of the gating commands issued by the BICI board to the IGPA board:

Inner–Outer Timing: The BICI board acts to delay the turn-on of any outer cells in a phase by the skew time defined in firmware. The BICI board also delays the turn-off of an outer cell by the same skew time.

Timing Concurrence: Minimum On and Minimum Off times are cell specific. When other timing is correct, a cell may be turned on while another cell is enduring its minimum off time.

Phase Underlap: When a phase changes its output state, a timer on the BICI board is started that momentarily freezes all phase states until the commutation reactor has had time to reset. If changes are pending for two phases when the timer expires, only one will be allowed to complete its state change forcing the other to wait until the next opportunity.

Gate Driver Fault Detection: Each IGCT gate driver module provides feedback to the BICI board informing the board of its health and the health of the connected cell. As long as the cell is not shorted and the gate driver is ready to respond to commands, the status is asserted. If a problem occurs the status is de-asserted. When the drive is enabled, the status feedbacks are monitored by the BICI board in the form of counters that increment whenever the status report is negative and are reset at each load pulse. If a counter expires, a source report latch and a gate driver fault latch are set by the BICI board that trips the drive.

Programmable Logic

Two Field Programmable Gate Arrays (FPGA), the BRDG_IO FPGA and the CELL_IO FPGA provide the logic functions on the BICI board. These SRAM based logic devices provide the interface between the DSPX board, the local DSP, and the bridge control signals. Both FPGAs are configured by the DSPX board during powerup. Verification of configuration completion is performed by reading a version register in each FPGA. Figure 3 shows an overview of the logic architecture of the BICI board.

Reset Management

A hardware RESET places an FPGA in an unconfigured state so that it may be reconfigured. Non-volatile logic manages the RESET access to the FPGA. This logic blocks hardware resets from the FPGA's 0PROGRAM pin when the DONE output is high, until the logic reaches a safe state. The BRDG_IO logic initiates a bridge disable when the RESET input signal is detected and responds with a RESET permissive when the OFF state is achieved. If a latched freeze occurs to block the disable, the logic will withhold the permissive and allow the time limit to prevail.

Processor Interfaces

The DSPX board and the local DSP are presented very similar interfaces to the logic function. Each data bus in 16-bits wide and each address bus is 6-bits wide. Each may use the same memory map for similar resources.

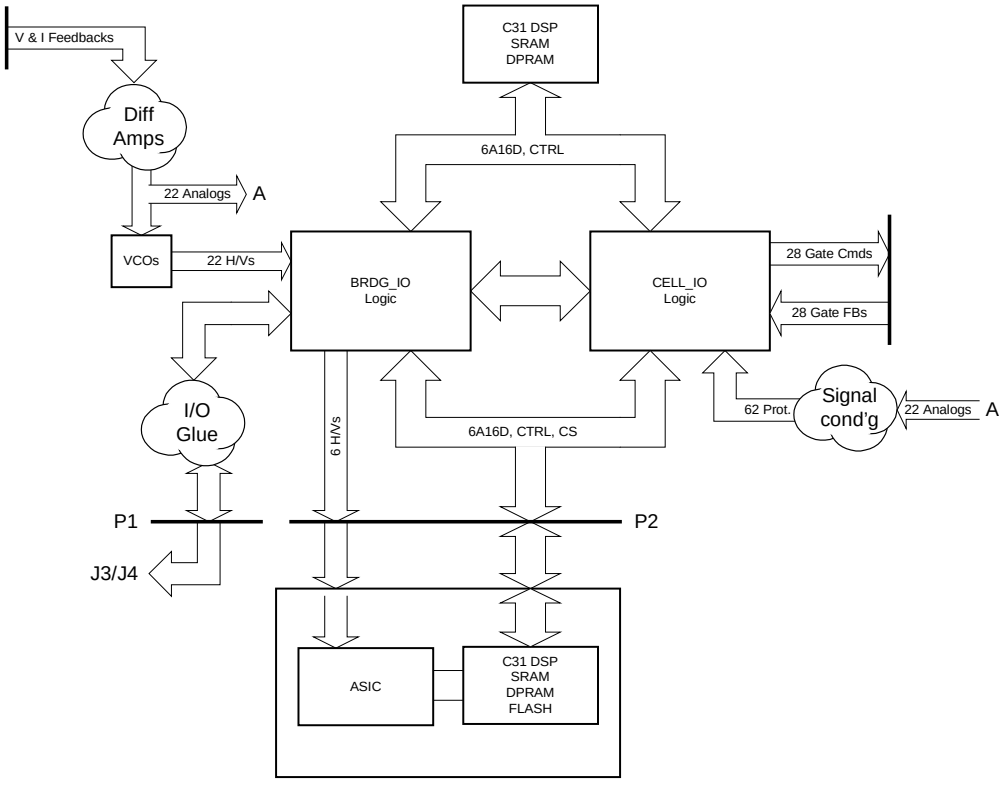

Figure 3. BICI Board Logic Architecture

DSPX Board Interface: Before the logic is configured, the only devices accessible to the DSPX board are the configuration ports of the FPGAs. Once the FPGAs are configured, the BRDG_IO FPGA provides coordination and control over access to all local resources, including DPRAM and the registers in the BRDG_IO and CELL_IO FPGAs. It also controls the DSPX board 0BUS_BSY line to insure adequate timing for each access cycle. The local DSP remains in RESET until released by the DSPX board via a register in BRDG_IO logic. BRDG_IO logic will control the interrupt line to cause the local DSP to boot from an address that is mapped to DPRAM by the BRDG_IO logic. Access to SRAM is controlled directly from the DSP signals to allow zero wait state read and write access without involving the logic device.

Register Access Lock Out: Certain command registers or bits of command registers ignore write accesses when the power electronics enable (PE_ENABLE) flag is set. This lockout condition protects hardware operating parameters that may affect the operational integrity when the drive is running.

CELL_IO FPGA

The CELL_IO FPGA manages the discrete controls and protective feedbacks direct to the IGCT gate drivers. It provides the timing for PWM cycles as well as the timing constraints imposed by the IGCT devices or their gate driver modules. It monitors the protective feedbacks and takes immediate and independent action to respond to fault conditions in the bridge to prevent cell damage and assure best performance. Fault events and any associated action are recorded and made available in registers for processor action. See Table 3 for register descriptions.

Initial State Register: An initial state register is used to establish the state at the beginning of the next task interval (initiated by a load pulse). The register contains 7 individual 2-bit state variables; one for each of the possible six bridge legs that may be controlled and another for the DB assembly. The initial state register is double buffered so that updates written during a task interval are loaded into the active register at the load pulse that initiates the next task interval.

PWM Timers: Each bridge phase is controlled by a PWM timer that is written to by the processor with timing and next state data to be implemented in the next task interval. The timer registers each contain a 13-bit time delay value and a 2-bit value as a next state to be activated after the time delay has expired. The PWM timing registers are double buffered so that updates written during a task interval are loaded into the active register at the load pulse that initiates the next task interval. At the beginning of each task interval, a counter is loaded with the time delay value. The counter is then decremented to zero, at which time the active phase state variable is updated to the next state value in the PWM timing register. A PWM timer register is also provided that may optionally be used to control the DB assembly.

Control and Status Registers: Status register 3 is contiguous with status registers 1 and 2 in the BRDG_IO FPGA for access via repeat block processor instructions. Registers with latched fault clear when read unless the fault condition is still present.

BRDG_IO FPGA

The BRDG_IO FPGA provides all logic for discrete I/O and control signals, fault reporting, VCO counters, tach encoder interface with fractional tach pulse values, second identification tag access port, and analog inputs/outputs. (See Table 6.)

VCO Counters: There are 22 VCO inputs to the BRDG_IO FPGA. Six of these are passed through to the VCO counters on the DSPX board while the remaining 16 are counted in this FPGA. The six VCO inputs passed to DSPX board may also be counted in the FPGA when needed by the BICI board's DSP. The counter values are latched on the load pulse without missing counts (latch may be read by either processor). See Table 4 for VCO signal assignments.

Tach Interface: The tach input is driven from the same input that drives the tach interface on the DSPX board to add partial tach pulse capability. The encoder is 16-bits and has marker pulse latch, command event latch, and a tick since last tach pulse register.

Free Running Time Counter: A 16-bit counter that increments once every microsecond is readable by both processors. It does not miss counts when read and provides a common time reference between the two processors. The value of this counter is latched into two registers.

One of these registers is driven by the load pulse from each processor. This provides time stamp information for all latched input registers.

Analog I/O: There is a 12-bit data port through the logic to access analog I/O resources. There are three 12-bit analog inputs:

- One for a thermistor on the BICI board for local ambient temperature
- A second for an external thermistor through connector J4 of the CABP board
- A third for self test loop-back of protective thresholds voltages selected through a multiplexer.

There are four diagnostic D/A converters and seven other analog outputs for setting the protective logic thresholds. Logic controls access to these ports for both processors. A lockout bit protects the analog threshold outputs from being accessed when the bridge is enabled. See Table 5 for a summary of the analog I/O usage.

Discrete Digital I/O: The discrete inputs and outputs on the BICI board preserve the definitions from the BICM board. Additions include a command bit to latch the tach encoder value. A bit to designate when the local DSP has write access to the logic and bits to control reset and interrupt of the local DSP. See Table 4 for details of the register set in the BRDG_IO FPGA.

Table 3. CELL_IO FPGA Register Descriptions

Register type	R/W	Description
PWM initial states	W	Initial state upon load pulse
PWM timer (1 – 7)	W	PWM timer delay count and next state
BRDG_IO/CELL_IO (Command Word 1)	W	PWM configuration & control bits; power electronics enable register, reset of BICI fault latch, register to force DC over voltage trip from software (CELL_IO), register to enable BIC_ fault on LOCAL_FLT, register to enable BIC_ fault on SYSTEM_FLT, register watchdog toggle bit (BRDG_IO), latch tach encoder (BRDG_IO/MC)
BRDG_IO / CELL_IO (Command Word 2)	W	BRDG_IO & CELL_IO command bits; DSPX board write access (both), local DSP 0RESET pin (BRDG_IO), local DSP INT0 pin (BRDG_IO), Green LED on (BRDG_IO), lDPLS_EQ_W_ACCESS (both), clear BICI DSP MCBL mode MC (BRDG_IO), Tach encoder latch on LDPLS (BRDG_IO), Disable source bridge faults (BRDG_IO), Disable bridge 2 faults (BRDG_IO)
CELL_IO (Status Word 4)	R	IOC faults, Load faults
CELL_IO (Command Word 3)	W	DB mode, OC trip count, Shoot-through fault filter
CELL_IO (Status Word 5)	R	CELL_IO phase fault latches; Freeze faults, Bridge Freeze faults, Dc overvoltage
CELL_IO (Command Word 4)	W	Control register 4 (gate control functions); Minimum on time, Minimum off time, Disable skipping of optional firings
Phase event latches	R	IOC PTOs, di/dt Freezes, Fault reset executed flag
CELL_IO (Command Word 5)	W	Control register 5 (gate control functions); Inner IGCT skew time, Phase underlap delay, Freeze latch delay
CELL_IO (Command Word 6)	W	Control register 6 (gate control functions); Shoot-Through freeze duration (0 disables freeze action)
Cell test mask register	W	Individual cell mask bits for bridge test
Bridge 1 gate fault latches	R	Bridge 1 gate driver fault latches
Bridge 2 gate fault latches	R	Bridge 2 gate driver fault latches
CELL_IO Version	R	CELL_IO FPGA version

Table 4. VCO Signal Assignments

VCO#	Counter Location	Signal Description
VCO_1	DSPX board	Phase A1 current
VCO_2	DSPX board	Phase B1 current
VCO_3	DSPX board	Phase C1 current
VCO_4	DSPX board	Phase A2 current
VCO_5	DSPX board	Phase B2 current
VCO_6	DSPX board	Phase C2 current
VCO_7	BICI board BRDG_IO FPGA	Line to Line Voltage AB (source)
VCO_8	BICI board BRDG_IO FPGA	Line to Line Voltage BC (source)
VCO_9	BICI board BRDG_IO FPGA	DB Resistor Voltage
VCO_10	BICI board BRDG_IO FPGA	Line to Line Voltage AB (1)
VCO_11	BICI board BRDG_IO FPGA	Line to Line Voltage BC (1)
VCO_12	BICI board BRDG_IO FPGA	Positive Half Link Voltage (1)
VCO_13	BICI board BRDG_IO FPGA	Mid Point Voltage (1)
VCO_14	BICI board BRDG_IO FPGA	Negative Half Link Voltage (1)
VCO_15	BICI board BRDG_IO FPGA	Line to Line Voltage AB (2)
VCO_16	BICI board BRDG_IO FPGA	Line to Line Voltage BC (2)
VCO_17	BICI board BRDG_IO FPGA	Positive Half Link Voltage (2)
VCO_18	BICI board BRDG_IO FPGA	Mid Point Voltage (2)
VCO_19	BICI board BRDG_IO FPGA	Negative Half Link Voltage (2)
VCO_20	BICI board BRDG_IO FPGA	Source Phase A Current (3)
VCO_21	BICI board BRDG_IO FPGA	Source Phase B Current (3)
VCO_22	BICI board BRDG_IO FPGA	Source Phase C Current (3)

Table 5. Analog I/O Summary

Port	Signal	Port	Signal
A/D 1	Bridge Interface Controller Ambient Temperature	Analog 3 *	Load Fault Threshold
A/D 2	External Temperature	Analog 4 *	Freeze Phase Threshold
A/D 3	Test loop-back input *	Analog 5 *	L (di/dt) Freeze Threshold
D/A 1	DIAG1	Analog 6 *	DB Turn-on Threshold
D/A 2	DIAG2	Analog 7 *	DB Turn-off Threshold
D/A 3	DIAG3	Analog 8 *	DC Over Voltage Threshold
D/A 4	DIAG4	Offset check *	For Loop-back input calibration
Analog 1 *	Protective Turnoff Threshold	Calibration Ref *	For loop-back input calibration
Analog 2 *	Low Current Threshold		

*Readable via loop-back input

Table 6. BRDG_IO FPGA Register Descriptions

Register type	R/W	Description
BRDG_IO Version	R	Major, minor, patch, release (4-bits each)
VCO (1 – 22)	R	16-bit pulse counter with clock controlled to prevent count loss during reads
DAC output 1	W	Active DAC Channel 1 output
DAC output 2	W	Active DAC Channel 2 output
DAC output 3	W	Active DAC Channel 3 output
DAC output 4	W	Active DAC Channel 4 output
TAMB ATOD	R/W	Ambient Temperature D/A converter
Analog IO control register	W	Select DAC for output access, default AOCA address for loop-back ATOD multiplexer
Loop-back ATOD data	R	Data register of Loop-back A/D converter; 2 comp of analog value (+/-5V range), Read 0, A/D busy (conversion)
Loop-back ATOD convert	W	Write here to start Loop-back conversion
Fault mask and dig in force	W	Fault enable bits for digital inputs to allow them to set bits of the fault register, Bits ORed with digital inputs to force input to appear true
Digital Outs	W	Register holding state of digital outputs
Time Counter	R	16-bit free running count of 1microsecond time ticks
DSPX LDPLS time	R	Time count at DSPX load pulse
BICI LDPLS time	R	Time count at Bridge Interface Controller load pulse
Tach latch time	R	Time count at last tach encoder latch
Tach encoder latch	R	Value of tach encoder at latch cmd
Tach marker latch	R	[Value of tach encoder at marker pulse.
Tach pulse length	R	Time (1 – 8 microseconds) since last tach pulse.
BRDG_IO (Status Word 1)	R	Read back of power electronics enable register, drive fault latch state, BICI board fault latch state (not reset on read), feedback of main contractor state (spare), digital input bits
BRDG_IO (Status Word 2)	R	BIC_DABL input latch state, BICI board power supply fault latch state, isolated 24V supply fault latch state, local panel fault string latch state, system panel fault string latch state, digital input fault present, 8 MHz clock fault latch state, 30 MHz clock fault latch state, rack power converter fault latch state, watchdog fault, watchdog echo bit
BRDG_IO/CELL_IO (Command Word 1)	W	PWM configuration and control bits; Power electronics enable register (BRDG_IO), reset of BICI card fault latch (both), register to force DC over voltage trip from software (CELL_IO), register to enable BIC_ fault on LOCAL_FLT, register to enable BIC_ fault on SYSTEM_FLT, register watchdog toggle bit (BRDG_IO), latch tach encoder (BRDG_IO)
BRDG_IO/CELL_IO (Command Word 2)	W	BRDG_IO and CELL_IO command bits; DSPX board write access (both), local DSP 0RESET pin (BRDG_IO), local DSP INT0 pin (BRDG_IO), Green LED on (BRDG_IO), IDPLS_EQ_W_ACCESS (both), BICI board MCBL mode (BRDG_IO), tach encoder latch on LDPLS (BRDG_IO), disable source bridge faults (BRDG_IO), disable bridge 2 faults (BRDG_IO)
BRDG_IO (Status Word 3)	R	BRDG_IO status bits; NATO board cable missing (source, bridge 2, bridge 1), fuse fault (bridge 2, bridge 1), HFPA board power fault (source, bridge 2, bridge 1), P5 fault (source, bridge 2, bridge 1), 115 V ac fault (source, bridge 2, bridge 1), feedback cable wrong (bridge 2, bridge 1)

Application Data

The BICI board includes one LED indicator, three plug connectors, two backplane connectors, and eight user testpoints as part of the board. There are no fuses or adjustable hardware devices included on the BICI Board. Refer to the following figures for the locations of these items:

- See Figure 4 for a BICI board front panel diagram
- See Figure 5 for a BICI board layout diagram
- See Figure 6 for an AOCA daughterboard layout diagram
- See Figure 7 for a DVAA daughterboard layout diagram.

Connectors

The BICI board interfaces to other boards through the two backplane connectors, P1 and P2, and the three front panel connectors, PFBK1, PFBK2, and PSRC. See Figures 4 and 5 for the connector locations. See the following tables for pin signal descriptions of these connectors: (also see Note)

- See Table 7 for P1 and P2 backplane signal descriptions
- See Table 8 for PFBK1, GGXI board to BICI board feedback signal descriptions
- See Table 9 for PFBK2, GGXI board to BICI board feedback signal descriptions
- See Table 10 for PSRC, GGXD board to BICI board feedback and gate control signal descriptions

Testpoints

Eight testpoints are accessible via a port in the board front panel that provides analog signals for system diagnostics. See Figures 4 and 5 for the testpoint locations. Refer to Table 11 for the testpoint signal descriptions.

Note

The connectors and testpoints located on the BICI board surface provide access to signals for test and development use only.

LED Indicator

A single IMOK LED is visible from the board front. If the LED fails to come on, a fault condition is indicated.

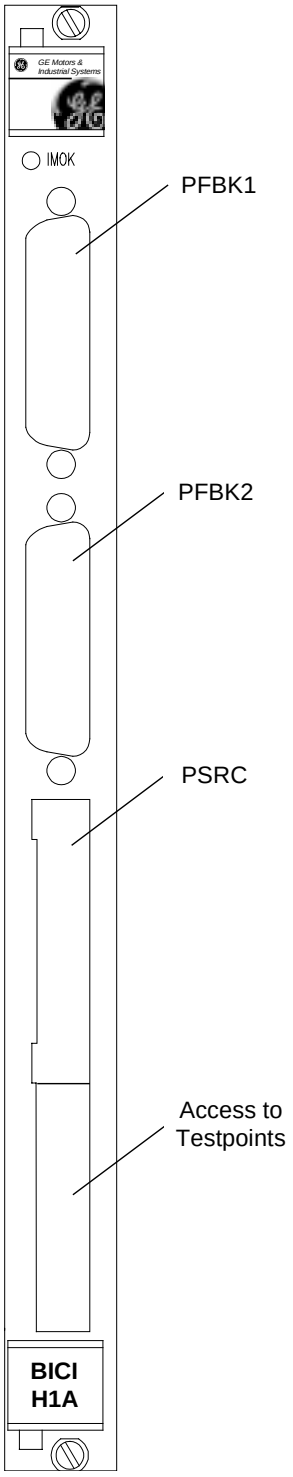

Figure 4. BICI Board Front Panel

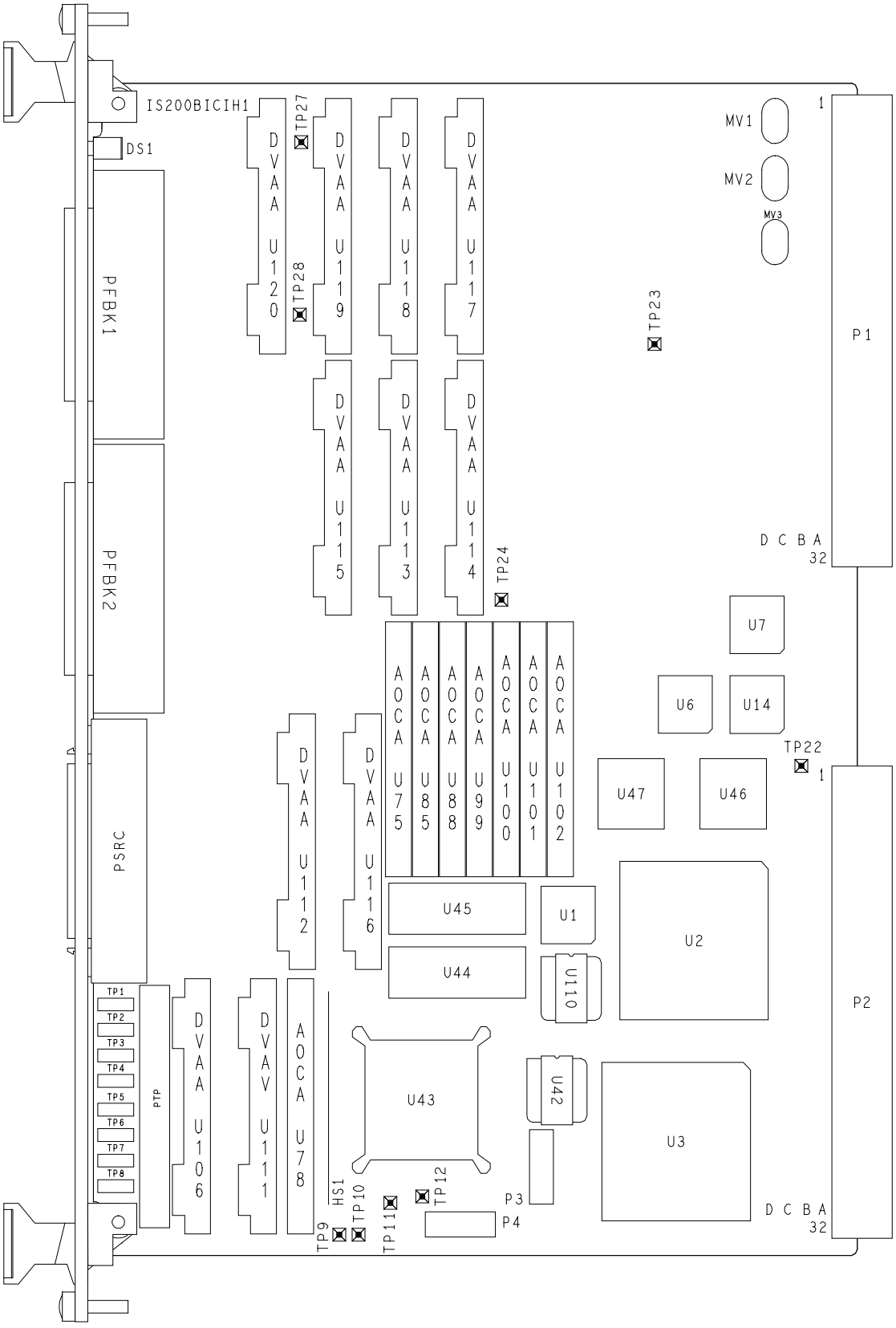

Figure 5. BICI Board Layout Diagram

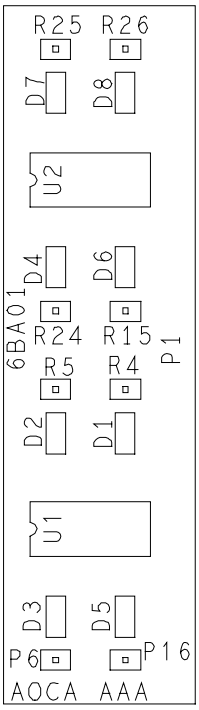

Figure 6. AOCA Daughterboard Layout Diagram

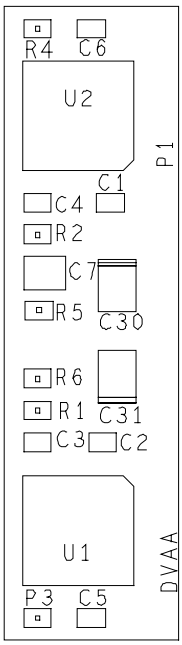

Figure 7. DVAA Daughterboard Layout Diagram

Table 7. P1 and P2 Backplane Connector Pin Signal Descriptions

Pin#	Description
P1-A18	Gate Status Bridge 1 cell G4B
P1-A19	Gate Status Bridge 1 cell G3C
P1-A20	Gate Status Bridge 1 cell G4C
P1-A21	Bridge 1 Fuse Status
P1-B10	Gate Command Bridge 1 cell G1A
P1-B13	Gate Command Bridge 1 cell G2A
P1-B14	Gate Command Bridge 1 cell G3A
P1-B15	Gate Command Bridge 1 cell G4A
P1-B17	Gate Command Bridge 1 cell G1B
P1-B18	Gate Command Bridge 1 cell G2B
P1-B20	Gate Command Bridge 1 cell G3B
P1-B22	Gate Command Bridge 1 cell G4B
P1-B23	Gate Command Bridge 1 cell G1C
P1-B24	Gate Command Bridge 1 cell G2C
P1-B26	Gate Command Bridge 1 cell G3C
P1-B28	Gate Command Bridge 1 cell G4C
P1-B29	Buffered Tach 1A Signals
P1-B31	Buffered Tach 1B Signals
P1-C10	Gate Status Bridge 1 cell G1A
P1-C14	Gate Status Bridge 1 cell G2A
P1-C15	Gate Status Bridge 1 cell G3A
P1-C16	Gate Status Bridge 1 cell G1B
P1-C18	Gate Status Bridge 1 cell G1C
P1-C20	Bridge 1 GDPA Board Status
P1-C21	Bridge 1 115 V Ac Status
P1-C22	Bridge 1 GGXI Board P5 Status
P1-C24	Bridge 1 NATO Board Cable Check Status
P1-C26	Bridge 1 GATE/FBK Cable Check Status
P1-C27	Buffered Tach 2A Signals
P1-C28	Buffered Tach 2B Signals
P1-C30	Buffered Tach 3A Signals
P1-C32	Buffered Tach 3B Signals
P1-C7	RAPA Board CVOK
P1-D15	Gate Status Bridge 1 cell G4A
P1-D16	Gate Status Bridge 1 cell G2B
P1-D17	Gate Status Bridge 1 cell G3B

Table 7. P1 and P2 Backplane Connector Pin Signal Descriptions – Continued

Pin#	Description
P1-D18	Gate Status Bridge 1 cell G2C
P2-A17	Gate Command Bridge 2 cell G1A
P2-A18	Gate Command Bridge 2 cell G3A
P2-A19	Gate Command Bridge 2 cell G4A
P2-A23	Gate Command Bridge 2 cell G2B
P2-A24	Gate Command Bridge 2 cell G4B
P2-A25	Gate Command Bridge 2 cell G1C
P2-A29	Bridge 2 GDPA Board Status
P2-A31	Chassis
P2-B16	Gate Status Bridge 2 cell G1A
P2-B22	Gate Command Bridge 2 cell G1B
P2-B23	Gate Status Bridge 2 cell G2B
P2-B28	Gate Status Bridge 2 cell G3C
P2-B29	Gate Status Bridge 2 cell G4C
P2-B30	Bridge 2 GGXI Board P5 Status
P2-C17	Gate Command Bridge 2 cell G2A
P2-C20	Gate Status Bridge 2 cell G4A
P2-C22	Gate Status Bridge 2 cell G1B
P2-C23	Gate Command Bridge 2 cell G3B
P2-C25	Gate Status Bridge 2 cell G1C
P2-C27	Gate Status Bridge 2 cell G2C
P2-C28	Gate Command Bridge 2 cell G4C
P2-C29	Bridge 2 Fuse Status
P2-C30	Bridge 2 NATO Board Cable Check Status
P2-D17	Gate Status Bridge 2 cell G2A
P2-D18	Gate Status Bridge 2 cell G3A
P2-D23	Gate Status Bridge 2 cell G3B
P2-D24	Gate Status Bridge 2 cell G4B
P2-D25	Gate Command Bridge 2 cell G2C
P2-D27	Gate Command Bridge 2 cell G3C
P2-D29	Bridge 2 115 V Ac Status
P2-D31	Bridge 2 GATE/FBK Cable Check Status

Table 8. PFBK1 Connector Pin Signal Descriptions

Pin#	Signal Function
PFBK1-1	Bridge 1 Phase A Active Current Transformer Burden (+)
PFBK1-2	Bridge 1 Phase A Active Current Transformer Burden (–)
PFBK1-3	Bridge 1 Phase B Active Current Transformer Burden (+)
PFBK1-4	Bridge 1 Phase B Active Current Transformer Burden (–)
PFBK1-5	Bridge 1 Phase C Active Current Transformer Burden (+)
PFBK1-6	Bridge 1 Phase C Active Current Transformer Burden (–)
PFBK1-7	Bridge 1 Phase A Vphase Burden (+)
PFBK1-8	Bridge 1 Phase A Vphase Burden (guard)
PFBK1-9	Bridge 1 Phase B Vphase Burden (+)
PFBK1-10	Bridge 1 Phase B Vphase Burden (guard)
PFBK1-11	Bridge 1 Phase C Vphase Burden (+)
PFBK1-12	Bridge 1 Phase C Vphase Burden (guard)
PFBK1-13	Bridge 1 PDC Link Volts Burden (+)
PFBK1-14	Bridge 1 PDC Link Volts Burden (guard)
PFBK1-16	Bridge 1 NDC Link Volts Burden (+)
PFBK1-17	Bridge 1 NDC Link Volts Burden (guard)
PFBK1-18	Bridge 1 P Reactor Volts Burden (+)
PFBK1-19	Bridge 1 P Reactor Volts Burden (guard)
PFBK1-20	Bridge 1 N Reactor Volts Burden (+)
PFBK1-21	Bridge 1 N Reactor Volts Burden (guard)
PFBK1-22	Bridge 1 0 V Dc Link Volts Burden (+)
PFBK1-23	Bridge 1 0 V Dc Link Volts Burden (guard)
PFBK1-24	Bridge 1 GATE/FBK Cable Check (+)
PFBK1-25	Bridge 1 GATE/FBK Cable Check (return)
PFBK1-26	Bridge 1 BRDID
PFBK1-27	Bridge 1 BRDID Return

Table 9. PFBK2 Connector Pin Signal Descriptions

Pin#	Signal Function
PFBK2-1	Bridge 2 Phase A Active Current Transformer Burden (+)
PFBK2-2	Bridge 2 Phase A Active Current Transformer Burden (–)
PFBK2-3	Bridge 2 Phase B Active Current Transformer Burden (+)
PFBK2-4	Bridge 2 Phase B Active Current Transformer Burden (–)
PFBK2-5	Bridge 2 Phase C Active Current Transformer Burden (+)
PFBK2-6	Bridge 2 Phase C Active Current Transformer Burden (–)
PFBK2-7	Bridge 2 Phase A Vphase Burden (+)
PFBK2-8	Bridge 2 Phase A Vphase Burden (guard)
PFBK2-9	Bridge 2 Phase B Vphase Burden (+)
PFBK2-10	Bridge 2 Phase B Vphase Burden (guard)
PFBK2-11	Bridge 2 Phase C Vphase Burden (+)
PFBK2-12	Bridge 2 Phase C Vphase Burden (guard)
PFBK2-13	Bridge 2 PDC Link Volts Burden (+)
PFBK2-14	Bridge 2 PDC Link Volts Burden (guard)
PFBK2-16	Bridge 2 NDC Link Volts Burden (+)
PFBK2-17	Bridge 2 NDC Link Volts Burden (guard)
PFBK2-18	Bridge 2 P Reactor Volts Burden (+)
PFBK2-19	Bridge 2 P Reactor Volts Burden (guard)
PFBK2-20	Bridge 2 N Reactor Volts Burden (+)
PFBK2-21	Bridge 2 N Reactor Volts Burden (guard)
PFBK2-22	Bridge 2 0 V Dc Link Volts Burden (+)
PFBK2-23	Bridge 2 0 V Dc Link Volts Burden (guard)
PFBK2-24	Bridge 2 GATE/FBK Cable Check (+)
PFBK2-25	Bridge 2 GATE/FBK Cable Check (return)
PFBK2-26	Bridge 2 BRDID
PFBK2-27	Bridge 2 BRDID Return

Table 10. PSRC Connector Pin Signal Descriptions

Pin#	Signal Function
PSRC-1	Source NATO Board Cable Check Status
PSRC-2	Source Phase A CT Burden (+)
PSRC-3	Source Phase B CT Burden (+)
PSRC-4	Source Phase C CT Burden (+)
PSRC-5	Source 1 Phase A Vline Burden (+)
PSRC-6	Source 1 Phase B Vline Burden (+)
PSRC-7	Source 1 Phase C Vline Burden (+)
PSRC-8	DB Resistor 1 Volts Burden (+)
PSRC-9	DB Resistor 2 Volts Burden (+)
PSRC-10	Not Connected
PSRC-11	Not Connected
PSRC-12	DB Gate Firing Command 1 (A)
PSRC-13	DB Gate Firing Command 2 (A)
PSRC-14	DB Gate Firing Command 3 (A)
PSRC-15	DB Gate Firing Command 4 (A)
PSRC-16	DB Gate Status Feedback 1 (A)
PSRC-17	DB Gate Status Feedback 2 (A)
PSRC-18	DB Gate Status Feedback 3 (A)
PSRC-19	DB Gate Status Feedback 4 (A)
PSRC-20	Not Connected
PSRC-21	Not Connected
PSRC-22	Source GDPA Status
PSRC-23	Source 115 V Ac Status
PSRC-24	Source GGXI Board P5 Status
PSRC-25	Source BRGD_ID
PSRC-26	Source Voltage Feedback Scaling Board Cable Check Status Return
PSRC-27	Source Phase A CT Burden (–)
PSRC-28	Source Phase B CT Burden (–)
PSRC-29	Source Phase C CT Burden (–)
PSRC-30	Source 1 Phase A Vline Burden (guard)
PSRC-31	Source 1 Phase B Vline Burden (guard)
PSRC-32	Source 1 Phase C Vline Burden (guard)
PSRC-33	DB Resistor 1 Volts Burden (guard)

Table 10. PSRC Connector Pin Signal Descriptions – Continued

Pin#	Signal Function
PSRC-34	DB Resistor 2 Volts Burden (guard)
PSRC-35	Not Connected
PSRC-36	Not Connected
PSRC-37	DB Gate Firing Command 1 (B)
PSRC-38	DB Gate Firing Command 2 (B)
PSRC-39	DB Gate Firing Command 3 (B)
PSRC-40	DB Gate Firing Command 4 (B)
PSRC-41	DB Gate Status Feedback 1 (B)
PSRC-42	DB Gate Status Feedback 2 (B)
PSRC-43	DB Gate Status Feedback 3 (B)
PSRC-44	DB Gate Status Feedback 4 (B)
PSRC-45	Not Connected
PSRC-46	Not Connected
PSRC-47	Source GDPA Board Status Return
PSRC-48	Source 115 V Ac Status Return
PSRC-49	Source GGXI Board P5 Status Return
PSRC-50	Source BRGD_ID Return

Table 11. User Testpoints (Located On Board Front Panel)

Testpoint	Nomenclature	Description
TP1	IA1	Phase A1 Current
TP2	IB1	Phase B1 Current
TP3	IC1	Phase C1 Current
TP4	VAB1	Line-to-line Voltage (A1–B1)
TP5	VBC1	Line-to-line Voltage (B1–C1)
TP6	VPDC1	Positive DC Link 1 Rail Voltage
TP7	VNDC1	Negative DC Link 1 Rail Voltage
TP8	ACOM	Analog Common

Renewal/Warranty Replacement

How to Order a Board

When ordering a replacement board for a GE drive, you need to know:

- How to accurately identify the part
- If the part is under warranty
- How to place the order

This information helps ensure that GE can process the order accurately and as soon as possible.

Board Identification

A printed wiring board is identified by an alphanumeric **part (catalog) number** located near its edge. Figure 8 explains the structure of the part number.

The board's functional acronym, shown in Figure 8, normally is based on the **board description**, or name. For example, the *BICI* board is described as the *Bridge Interface Controller Board*.

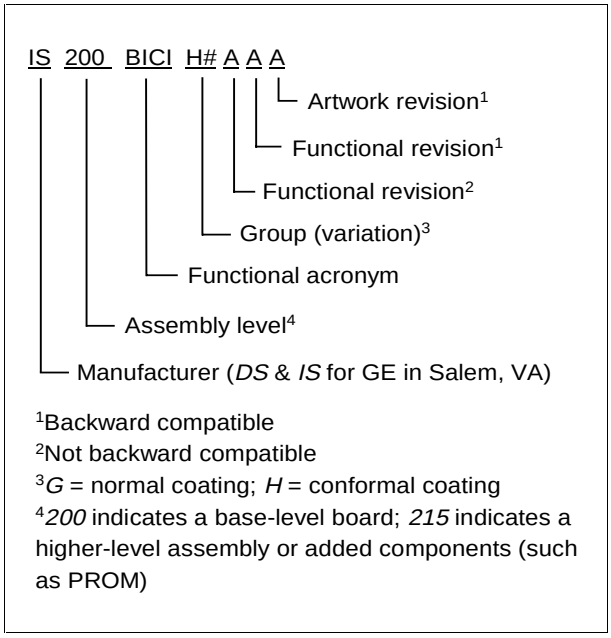

Figure 8. Board Part Number Conventions

Warranty Terms

The GE *Terms and Conditions* brochure details product warranty information, including **warranty period** and **parts and service coverage**. The brochure is included with customer documentation. It may be obtained separately from the nearest GE Sales Office or authorized GE Sales Representative.

Placing the Order

Parts still under **warranty** may be obtained directly from the factory:

GE Industrial Systems
Product Service Engineering
1501 Roanoke Blvd.
Salem, VA 24153-6492 USA
Phone: +1-540-387-7595
Fax: +1-540-387-8606
("+" indicates the international access code required when calling from outside of the USA.)

Renewals (spares or those not under warranty) should be ordered by contacting the nearest GE Sales or Service Office. Be sure to include:

- Complete part number and description
- Drive serial number
- Drive Material List (ML) number

Note

All digits are important when ordering or replacing any board.

The factory may substitute later versions of boards based on availability and design enhancements. However, GE Industrial Systems ensures backward compatibility of replacement boards.

Onboard Firmware

Each new BICI board is shipped with the applicable firmware already installed. The onboard EEPROM containing this firmware is not intended for removal or programming in the field. If the BICI board fails because of firmware or EEPROM problems, or if an upgrade is needed, the board must be replaced.

How to Replace the Board

Handling Precautions

CAUTION

To prevent component damage caused by static electricity, treat all boards with static sensitive handling techniques.

Printed wiring boards may contain static-sensitive components. Therefore, GE ships all replacement boards in antistatic bags. Use the following guidelines when handling boards:

- Store boards in antistatic bags or boxes.
- Use a grounding strap when handling boards or board components.

Replacement Procedures

WARNING

To prevent electric shock, turn off power to the board, then test to verify that no power exists in the board before touching it or any connected circuits.

CAUTION

To prevent equipment damage, do not remove, insert, or adjust board connections while power is applied to the equipment.

Remove the board from the rack as follows:

1. Make sure that the drive in which the board resides has been deenergized.
2. Open the drive's cabinet door, and using equipment designed for high voltages, test any electrical circuits **before touching them** to ensure that power is off.
3. Carefully remove the board from the rack, as follows:
   a. Loosen the screws at the top and bottom of the board, near the board ejector tabs. (The screws are captive in the board front and should not be removed.)
   b. Unseat the board by raising the ejector tabs.
   c. Using both hands, gently pull the board from the rack.

Install the new (replacement) board in the rack as follows:

1. Slide the board into the **correct slot** in the rack.

CAUTION

Because boards are designed to fit specific rack slots, inserting the board into the wrong slot can damage the electronics or the rack.

2. Begin seating the board by firmly pressing the top and bottom of the board at the same time with your thumbs.
3. Finish seating the board in the slot by starting and then tightening the screws at the top and bottom of the board. **Tighten the screws evenly** to ensure that the board is seated squarely.

GE Industrial Systems

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