

CB10A
AUTOMATIC CHECK-BACK SYSTEM



**Meter and Control
Business Department**

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These instructions do not purport to cover all details or variations in equipment nor provide for every possible contingency to be met in connection with installation, operation or maintenance. Should further information be desired or should particular problems arise which are not covered sufficiently for the purchaser's purposes, the matter should be referred to the General Electric Company.

To the extent required the products described herein meet applicable ANSI, IEEE and NEMA standards; but no such assurance is given with respect to local codes and ordinances because they vary greatly.

TYPE CB10A CHECKBACK EQUIPMENT

CB10A_P1

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Master Checkback	GEK-90706
Auxiliary Relay	GEK-99322

MASTER CHECKBACK EQUIPMENT TYPE CB10A_P1

GENERAL

The automatic MASTER CHECKBACK equipment Type CB10A_P1, when used in conjunction with the REMOTE CHECKBACK equipment, provides the means for automatically testing equipment such as the G. E. AUDIO TONE EQUIPMENT TYPES NN40A AND NS40A, to verify proper equipment operation.

The equipment consists of a SHELF, a POWER SUPPLY, a MASTER CHECKBACK, and an AUXILIARY RELAY module. Detailed descriptions of these modules are included in subsequent sections of this INSTRUCTION BOOK.

This equipment was originally designed for use with CS26/27A/B BLOCKING CARRIER, therefore some of the labeling of indicators is not directly related to this application. For example, the indicator LED'S and the ALARMS are labeled "FULL POWER" and "REDUCED POWER" whereas they are used for CHANNEL 1 and CHANNEL 2 respectively when used with NN40A or NS40A TONE EQUIPMENT.

SHELF

The SHELF serves to mount the modules, provide the necessary interconnections between the modules, and provide customer connection points.

The 3 Rack-Unit high (5.25") steel shelf is designed for flush mounting in standard EIA 19-inch racks or cabinets. Auxiliary brackets (19B218789P008, Qty 2) are available for semi-flush mounting in shallow racks. The front door is removable. Barrier-type terminal boards, similar to GE EB-25 boards, which will accommodate wire sizes AWG 22 through AWG 10, are mounted on the printed-circuit mother-board backplane.

POWER SUPPLY

The POWER SUPPLY module occupies slot J1 in the shelf and is a DC-DC Converter. Power supplies are available for use with station batteries of 48, 110, 125, 220, and 250 Volts DC. This Converter, with battery surge and transient protection, provides +/-12VDC to operate the other modules in the shelf. A power ON-OFF switch, short-circuit protection, alarm relay and a fuse are part of this module. Test points on the front of the module can be used to monitor the +/-12VDC outputs.

MASTER CHECKBACK

The MASTER CHECKBACK module occupies slot J3 in the shelf.

Automatic testing of the system is provided by the timing and memory circuits of the MASTER CHECKBACK module. The time interval between tests is programmable from 1 to 255 hours in one-hour steps. The number of failed or successful tests can be recorded by a counter located on the module.

Remote supervision of the MASTER CHECKBACK module is available for CLOCK RESETTING, REMOTE TEST INITIATION, and REMOTE ALARM CLEARING. These supervisory functions can be optionally strapped to prevent automatic test initiation, or to disable one or two remote alarms. The remote supervision relays operate from Station Battery.

When applied with the TYPES NN40A or NS40A TONE EQUIPMENTS, the "FULL POWER" tests are used to verify CHANNEL ONE and the "REDUCED POWER" tests are used to verify CHANNEL TWO operation. Up to three remote terminals can be tested, and six LED'S mounted on the front panel indicate failures of either CHANNEL ONE or CHANNEL TWO for each remote.

Alarm contacts are also provided for remote indication of failures; however, before a failed test is alarmed, the test is automatically repeated up to three times to assure the user that a valid system failure has occurred. Nuisance alarms from temporary system disturbances are thus eliminated. This REPEAT TEST feature is field programmable to repeat the test after time intervals between 0 and 17 minutes.

AUXILIARY RELAY

The AUXILIARY RELAY module, located in slot J2 of the shelf, contains three mercury-wetted relays with separate inputs and outputs. The relays provide isolation between the CHECKBACK EQUIPMENT and the TONE EQUIPMENT. Front-mounted LED'S indicate which relays are energized.

APPLICATION

As the CHECKBACK EQUIPMENT actually sends a single-channel TRIP signal to verify proper channel operation, it should be applied only with DUAL channel DIRECT TRIP, or with PERMISSIVE relaying schemes.

Tone OPTIONS such as "REVERT TO SINGLE CHANNEL" or "TRIP WINDOW" cannot be used in conjunction with the CHECKBACK system.

If "TRIP HOLD" is used in the optional tone LOGIC MODULE, the tone "TRIP RECEIVED" signal used as the CHECKBACK "RECEIVE" input must be taken directly from the tone RECEIVER, rather than from the output of the LOGIC circuit.

The TONE EQUIPMENT must be equipped with the AUXILIARY RELAY module. Two of the relays on this module are employed to supply the "TRIP RECEIVED" signals to the CHECKBACK. This is necessary because the TONE EQUIPMENT heavy-duty output relays are not fast enough to follow the CHECKBACK signals.

OPERATION

The MASTER CHECKBACK test cycle can be initiated by the BUILT-IN CLOCK, by the front-panel "TEST INITIATE" push-button, by the operation of the supervisory "TEST INITIATE" relay, or by receipt of a "REQUEST FOR TEST" signal from a REMOTE CHECKBACK module.

The test cycle is composed of nine segments of one second each, as follows:

1. During the first segment, the MASTER CHECKBACK sends eight pulses of 32 msec. width at 16 cps on channel one.
2. During the second, third and fourth segments, the MASTER CHECKBACK "listens" for a response on channel one from the first, second, and third REMOTE CHECKBACK(s) respectively. Any of these segments that are not used can be disabled.
3. During the fifth segment, the MASTER CHECKBACK sends four pulses of 32 msec. width at 16 cps on channel two.
4. During the sixth, seventh, and eighth segments, the MASTER CHECKBACK "listens" for a response on channel two from the first, second, and third REMOTE CHECKBACK(s) respectively. Any of these segments that are not used can be disabled.
5. The ninth and final segment is used to initiate alarms, initiate the automatic re-test function, or (in the event of a successful test) reset all circuits.

NOMENCLATURE SELECTION GUIDE

CHECKBACK SHELF

CB10A 04 P 1

TYPE

- 1 MASTER CHECKBACK-STANDARD
- 2 MASTER CHECKBACK-CS26/27B
- 3 REMOTE CHECKBACK-STANDARD
- 4 REMOTE CHECKBACK-CS26/27B
- 5 DUAL REMOTE-STANDARD
- 6 DUAL REMOTE-CS26/27B
- 7 MASTER CHECKBACK-CS26/27A
- 8 REMOTE CHECKBACK-CS26/27A
- 9 DUAL REMOTE-CS26/27A

POWER SUPPLY

N NONE (NOTE 1)

P BUILT-IN POWER SUPPLY

NOTES:

1. POWER SUPPLY "N" CAN BE USED ONLY WITH TYPES 1, 3, AND 5 WHEN USED IN CONJUNCTION WITH GE TYPE 40 TONE EQUIPMENT.

STATION BATTERY

04 48VDC

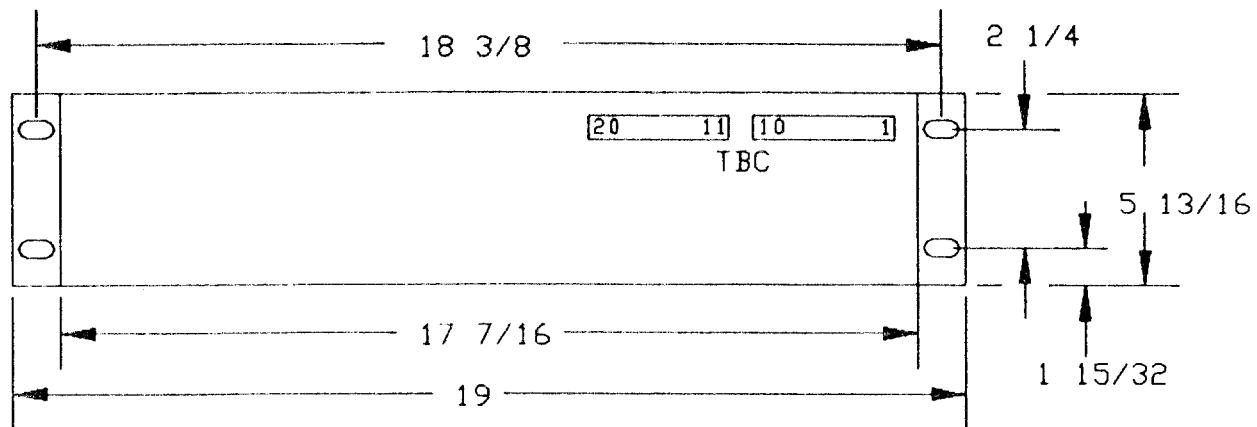
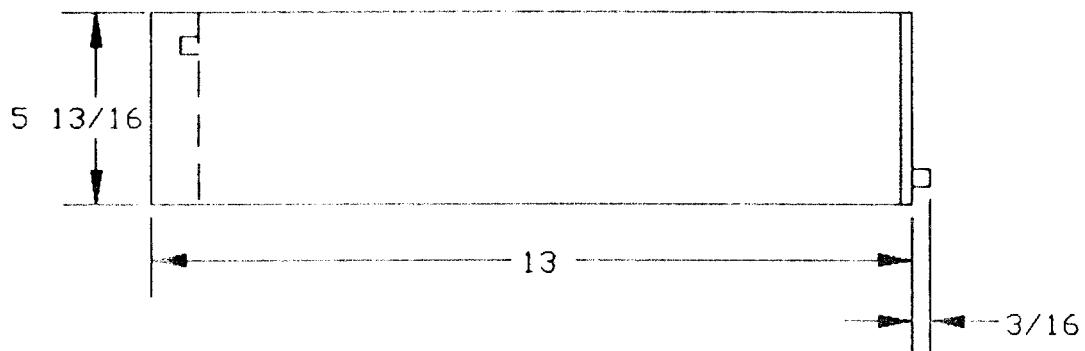
11 110VDC

12 125VDC

22 220VDC

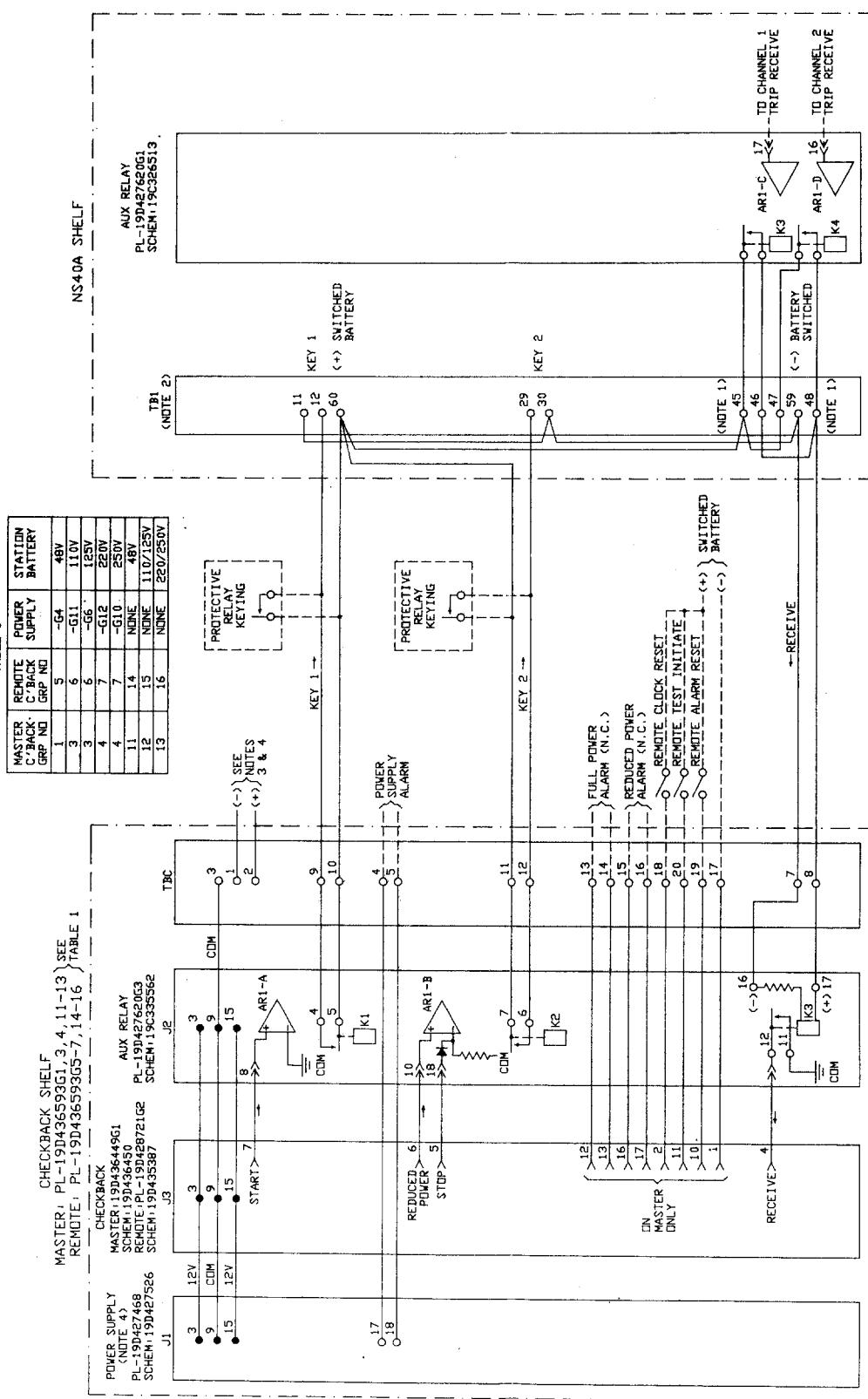
25 250VDC

CHECKBACK EQUIPMENT

REAR VIEWSIDE VIEW

OUTLINE DIAGRAM-0286A2941

TABLE 1



JUMPER CONNECTION CHART

BOARD LOCATION	A	B	C	D	E	F	G	H	I	J	K	L	M	N	O	P	Q	R	S	T	U	V	W	X	Y	Z	AUX RELAY
JUMPER CONNECTION	2-3	2-3	1-2	1-2	1-2	1-2	1-2	1-2	1-2	1-2	1-2	1-2	1-2	1-2	1-2	1-2	1-2	1-2	1-2	1-2	1-2	1-2	1-2	1-2	1-2	1-2	
(FUNCTION ARRAY) F#	4	2	9	11	13	15	17	OFF	ON	ON	OFF	ON	ON	4	5	7	2	3	4	5	6	2-3	2-3	1-2	1-2	1-2	1-2

SHELF ASSEMBLY Master Checkback

Assembly Drawing No:

19C335803G1 48 VDC
19C335803G3 110/125 VDC
19C335803G4 220/250 VDC

Consists of:

Backplane Asm.-19D436577G1 48 VDC
-G3 110/125 VDC
-G4 220/250 VDC

Case Asm.-19C335651G3
Door Asm.-19B230622G2

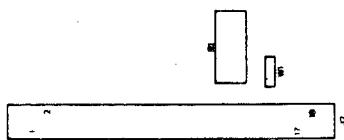
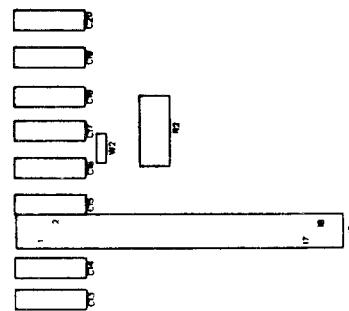
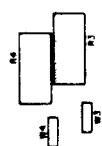
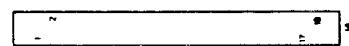
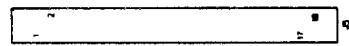
The Master Checkback Shelf consists of a keyed, slotted chassis that holds three plug-in card-type modules, each equipped with 18 contacts that mate with contacts mounted on the backplane on the rear of the chassis.

All groups of the backplane contain two 10-point barrier-type terminal boards, similar to GE EB-25 boards, which will accomodate wire sizes AWG 22 through AWG 10, and the SWC capacitors (C1, C2 and C13-C20).

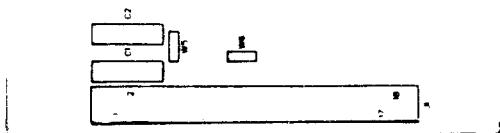
The 48 VDC version (-G1) contains components W1-W4, which are zero-ohm resistors. In the 110/125 VDC version (-G3), W1 is replaced by resistor R1. In the 220/250 VDC version (-G4), W1-W4 are replaced by R1-R4.

<u>ITEM</u>	<u>IDENTIFICATION NUMBER</u>	<u>DESCRIPTION</u>	<u>COMMENTS</u>
C1,C2 C13-C20	0246A9028P472	CAP., 4700PF, 3KV	
W1-W4	0246A9141P001	RESISTOR, 0 OHM	
R1	0246A9125P302	RESISTOR, 3.0K OHM, 2W	(IN -G3 ONLY)
R1	0246A9125P622	RESISTOR, 6.2K OHM, 2W	(IN -G4 ONLY)
R2-R4	0246A9125P203	RESISTOR, 20K OHM, 2W	(IN -G4 ONLY)

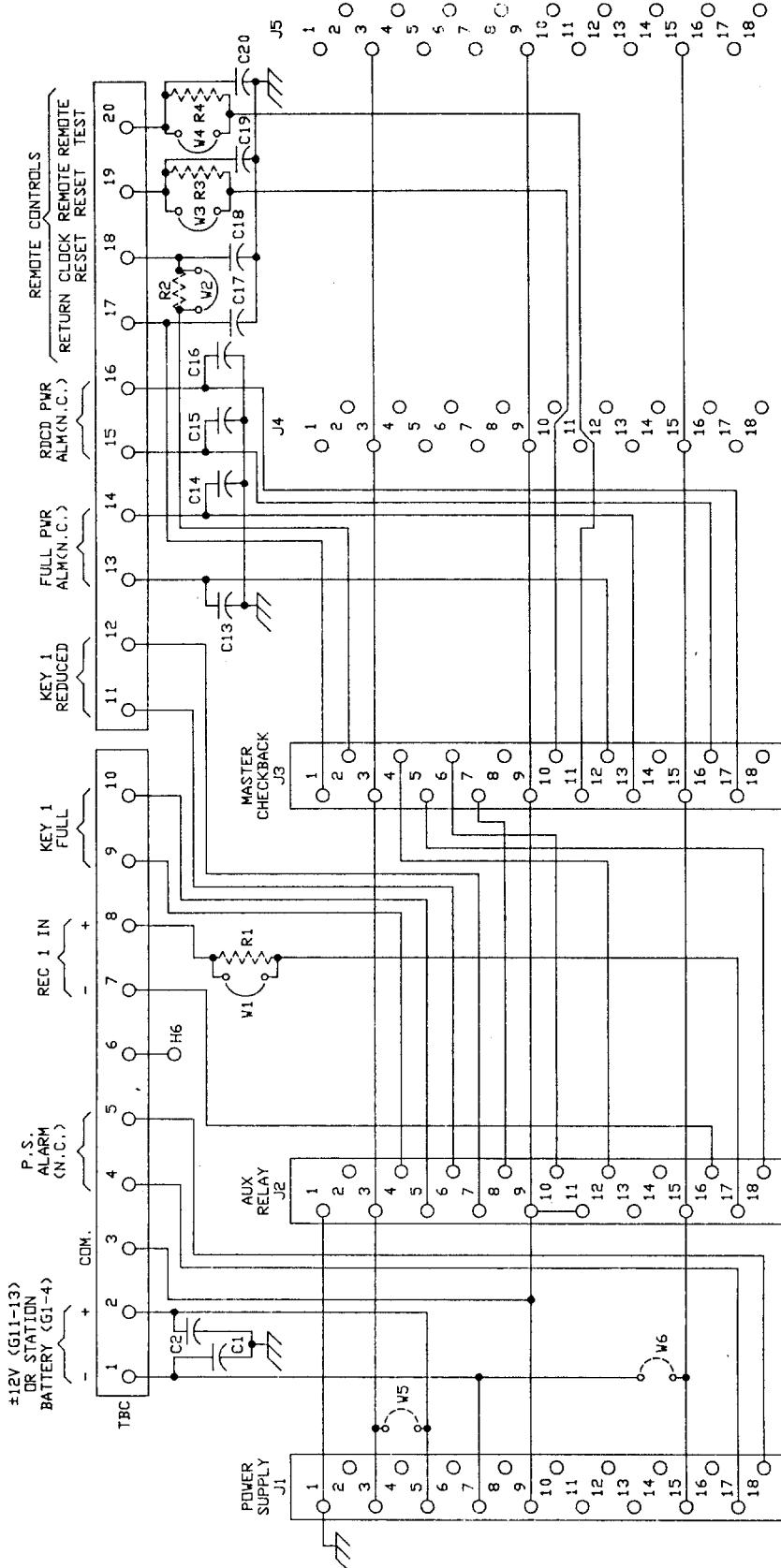
PARTS LIST-19D436577G1, -G3, -G4



OY



BACKPLANE OUTLINE-19D436576



GROUP	R1	R2	R3	R4	V1	V2	V3	V4	V5	V6	APPLICATION
1					0.1	0.1	0.1	0.1	0.1	0.1	C326/27B, 48-125V, STD 48V
2	20K	20K	20K	20K	0.1	0.1	0.1	0.1	0.1	0.1	C326/27B, 220/250V
3	3.0K	20K	20K	20K	0.1	0.1	0.1	0.1	0.1	0.1	STD 110/125V
4	6.2K	20K	20K	20K	0.1	0.1	0.1	0.1	0.1	0.1	STD 220/250V
11					0.1	0.1	0.1	0.1	0.1	0.1	STD 48V NO POWER SUPPLY
12	3.0K	20K	20K	20K	0.1	0.1	0.1	0.1	0.1	0.1	STD 110/125V, NO POWER SUPPLY
13	6.2K	20K	20K	20K	0.1	0.1	0.1	0.1	0.1	0.1	STD 220/250V, NO POWER SUPPLY

MASTER CHECKBACK
19D436577

SCHEMATIC DIAGRAM-19B230657 Sh. 1

**TYPE NS40A
POWER SUPPLY
PL-19D427468G 2, 4,
10-12**

DESCRIPTION

The Power Supply module provides the conversion from the DC battery voltage to the regulated +12 VDC. Different Group Numbers are used for different battery voltages:

<u>Group</u>	<u>Battery Voltage</u>
2	24 VDC
4	48
6	125
10	250
11	110
12	220 VDC

OPERATION

Refer to Schematic Diagram 19D427526 which is included in this instruction.

The input voltage is applied to the converter through a 2-pole switch S1. This switch also provides a switched battery output. The positive input is fused (F1) and the negative input includes a reverse voltage protection diode (D54). An input filter (T2, C9, C11 and C12) attenuates noise from the power source to the power supply and vice-versa.

The DC-DC converter (A1) is a fixed frequency (20 kHz) variable pulse width regulator. Integrated circuit AR3 generates a 20 kHz square-wave with a duty cycle of 90%. Flip-flop U2 alternates the power pulse between power transistors Q6 and Q11. Transistors Q2 through Q5 and Q7 through Q10 interface the CMOS gates U1-C and U1-D with the power transistors.

Secondary winding 9 and 10 of T1 provides the supply voltage for the control circuits plus the voltage control loop. These secondary voltage pulses are rectified by diodes D4 and D5, and integrated by resistor R47 and capacitor C3. Integrated circuit AR2 senses when this voltage has reached a predetermined level and switches the output pulse OFF.

Integrated circuit AR1 provides short circuit protection by sensing the emitter current of Q6 and Q11 through resistor R24, and switching the output pulse OFF when the emitter current exceeds a predetermined level. This circuit also limits the in-rush current when the power supply is first turned ON.

Transistor Q12 prevents gate U1-A from switching ON until the supply voltage for the control circuits reaches its normal level through resistor R31.

Secondary winding 4 and 5 of T1 provides the negative bias voltage to switch power transistors Q6 and Q11 OFF.

Variable resistor R8, ±12 VDC OUTPUT LEVEL ADJ, is used for adjusting the output to ±12 VDC.

The ±12 VDC output is rectified by diodes D9 through D12 and filtered by inductors L1 and L2 and capacitors C14, C18 and C19.

The alarm circuit switches ON when the output voltage (3/C - 15/S) reaches 23 VDC and OFF if the output voltage drops to 17 VDC. Form C alarm contacts are provided.

NOMINAL OPERATING CHARACTERISTICS

1. Input Voltage:

- a. Group 2 21 VDC to 28 VDC at 600 mA max.
- b. Group 4 42 VDC to 56 VDC at 300 mA max.
- c. Group 6 103 VDC to 142 VDC at 125 mA max.
- d. Group 10 210 VDC to 280 VDC at 10 mA max.
- e. Group 11 96 VDC to 124 VDC at 125 mA max.
- f. Group 12 192 VDC to 248 VDC at 80 mA max.

2. Output voltage:

- a. $+12 \pm 1$ VDC, 500 mA max.
- b. -12 ± 1 VDC, 500 mA max.

3. Low Voltage Alarm: form C contacts, 100 VA

- a. Pick-up 23 VDC max.
- b. Drop-out 17 VDC min.

ITEM NO.	IDENTIFICATION NUMBER	DESCRIPTION	GROUP NUMBER AND QUANTITY					
			1	2	3	5	6	7
R26	0246A9105P513	RES 51K OHM 1/4W 5% CRN	1	1	1	1	1	1
R27	0246A9105P103	RES 10K OHM 1/4W 5% CRN	1	1	1	1	1	1
R28	0246A9105P512	RES 5.1K OHM 1/4W 5% CRN	1	1	1	1	1	1
R29	0246A9102P101	RES 100 OHM .5W 5%	1	1	1	1	1	1
R30	0246A9102P201	RES 2000OHM .5W 5%	1	1	1	1	1	1
R31	19A116479P2152K	RES 1.5KOHM 10% 2W FLPRF	1		1		1	
R31	19A116479P2153K	RES 15KOHM 10% 2W FLPRF		1		1		1
R31	19A116479P2512K	RES 5.1KOHM 10% 2W FLPRF			1			1
R31	19A116479P4303K	RES 30.0KOHM 10%4W FLPRF				1		1
R32	19A116559P109	POT 250KOHM 1/2W LIN	1	1	1	1	1	1
R42	0246A9134P1002	RES 10K OHM 1/4W 1% MTL	1	1	1	1	1	1
R43	0246A9105P103	RES 10K OHM 1/4W 5% CRN	1	1	1	1	1	1
R44	19A116479P2131K	RES 1300HM 10% 2W FLPRF		1			1	
R44	19A116479P2331K	RES 3300HM 10% 2W FLPRF			1			1
R44	19A116479P2680K	RES 68 OHM 2W 10%	1			1		1
R44	19A116479P2681K	RES 6800HM 10% 2W FLPRF				1		1
R45	19A116479P2131K	RES 1300HM 10% 2W FLPRF		1			1	
R45	19A116479P2331K	RES 3300HM 10% 2W FLPRF			1			1
R45	19A116479P2680K	RES 68 OHM 2W 10%	1				1	
R45	19A116479P2681K	RES 6800HM 10% 2W FLPRF				1		1
R46	0246A9105P103	RES 10K OHM 1/4W 5% CRN	1	1	1	1	1	1
R47	0246A9134P1002	RES 10K OHM 1/4W 1% MTL	1	1	1	1	1	1
R48	0246A9134P1782	RES 17.8KOHM 1/4W 1% MTL	1	1	1	1	1	1
R49	0246A9134P2432	RES 24.3KOHM 1/4W 1% MTL						
R49	0246A9134P2942	RES 29.4KOHM 1/4W 1% MTL	1					
R49	0246A9134P3242	RES 32.4KOHM 1/4W 1% MTL			1			
R49	0246A9134P3482	RES 34.8KOHM 1/4W 1% MTL				1		
R50	0246A9134P5112	RES 51.1KOHM 1/4W 1% MTL	1	1	1	1	1	1
T1	19B229227G001	COIL	1					
T1	19B229227G002	COIL		1				
T1	19B229227G003	COIL			1			1
T1	19B229227G010	COIL						
T1	19B229227G011	COIL						
T1	19B229227G014	COIL						
T2	19B221725G001	CHOKE	1	1	1	1	1	1
U1	19A134097P302	INT. CKT CMOS			BI	1	1	1
U2	19A134097P323	INT. CKT	1	1	1	1	1	1
VR1	0246A9403P6R2	ZENER 6.2V 5% 400MW	1	1	1	1	1	1

Figure 1 (PL-19D427383)
DC/DC Converter Parts List, continued

ITEM NO.	IDENTIFICATION NUMBER	DESCRIPTION	GROUP NUMBER AND QUANTITY					
			2	4	6	10	11	12
	19D427468G002 REV#03	POWER SUPPLY						
	19D427468G004 REV#04	POWER SUPPLY						
	19D427468G006 REV#04	POWER SUPPLY	PCB ASM					
	19D427468G010 REV#03	POWER SUPPLY						
	19D427468G011 REV#01	POWER SUPPLY	PCB ASM					
	19D427468G012 REV#01	POWER SUPPLY						
A1	19D427383G001	DC-DC CONVERTER	RV#B	1				
A2	19D427383G002	DC-DC CONVERTER	RV#C		1			
A3	19D427383G003	DC-DC CONVERTER	RV#C			1		
A3	19D427383G006	DC-DC CONVERTER						
A5	19D427383G005	DC-DC CONVERTER	RV#C				1	
A5	19D427383G007	DC-DC CONVERTER						1
C51	0246A9028P682	CAP 6800PF CERAMIC	RV#1	1	1	1	1	1
C52	0246A9028P682	CAP 6800PF CERAMIC	RV#1	1	1	1	1	1
D51	0246A9418P206	LED, GREEN		1	1	1	1	1
D53	0246A9427P350A	TRANSORB 300V						
D53	0246A9427P5654A	TRANSORB 64V		1	1			
D53	0246A9427P5663A	TRANSORB 145V						
D54	0246A9407P5626	DIODE		1	1	1	1	1
F1	1R16P001	FUSE SIM/312.500						
F1	1R16P003	FUSE SIM/312001 (1 A)						
F1	1R16P005	FUSE (2 A)			1			
F1	1R16P007	FUSE		1				
K51	19B209598P001	REL 24VDC 600 OHMS 10%		1	1	1	1	1
Q51	19A115300P002	TSTR NPN 60V 2N3053		1	1	1	1	1
R51	19A116479P2221K	RES 2200HM 10% 2W FLPRF		1	1	1	1	1
R52	0246A9103P131	RESISTOR		1	1	1	1	1
R53	0246A9105P102	RES 1K OHM 1/4W 5% CRN		1	1	1	1	1
R54	0246A9134P86R6	RES		1	1	1	1	1
R56	0246A9134P1002	RES 10K OHM 1/4W 1% MTL		1	1	1	1	1
R57	0246A9134P1002	RES 10K OHM 1/4W 1% MTL		1	1	1	1	1
S1	0246A9987P001	SW DPST		1	1	1	1	1
VR51	0246A9403P6R2	ZENER 6.2V 5% 400MW		1	1	1	1	1

Figure 2 (PL-19D427468)
NS40A Power Supply Parts List

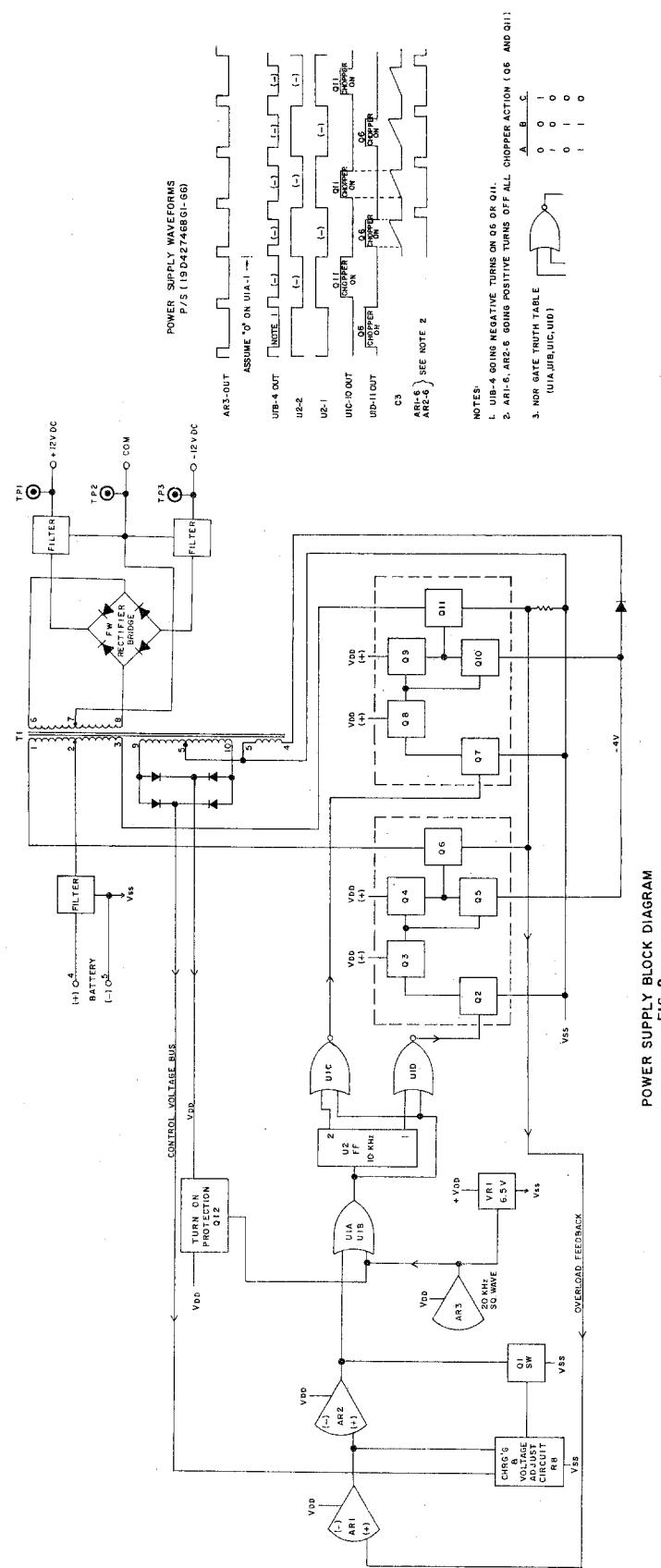
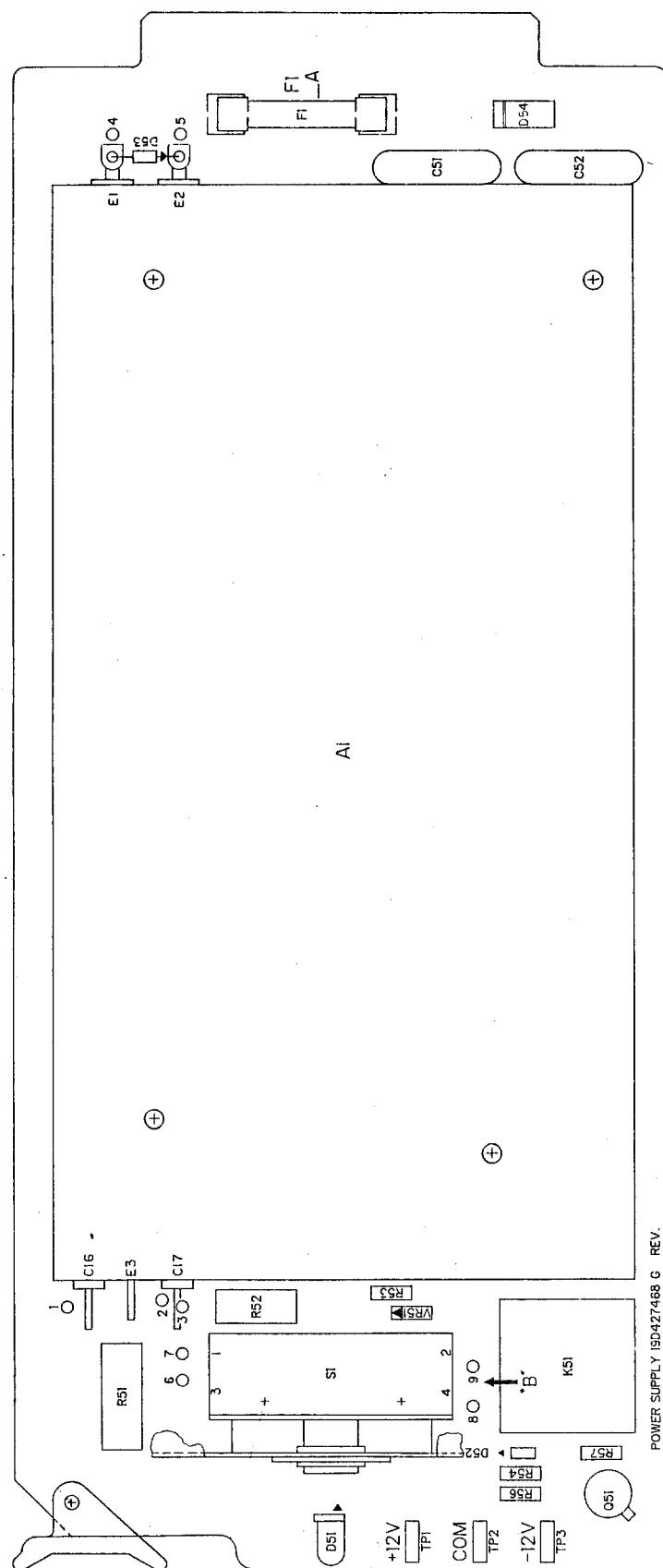


Figure 3 (19D434354 [1]) Functional Block Diagram
Type NS40A Power Supply



* Figure 4 (19D427468, Sh.2 [2]) Pictorial Diagram
Type NS40A Power Supply

* Revised since last issue

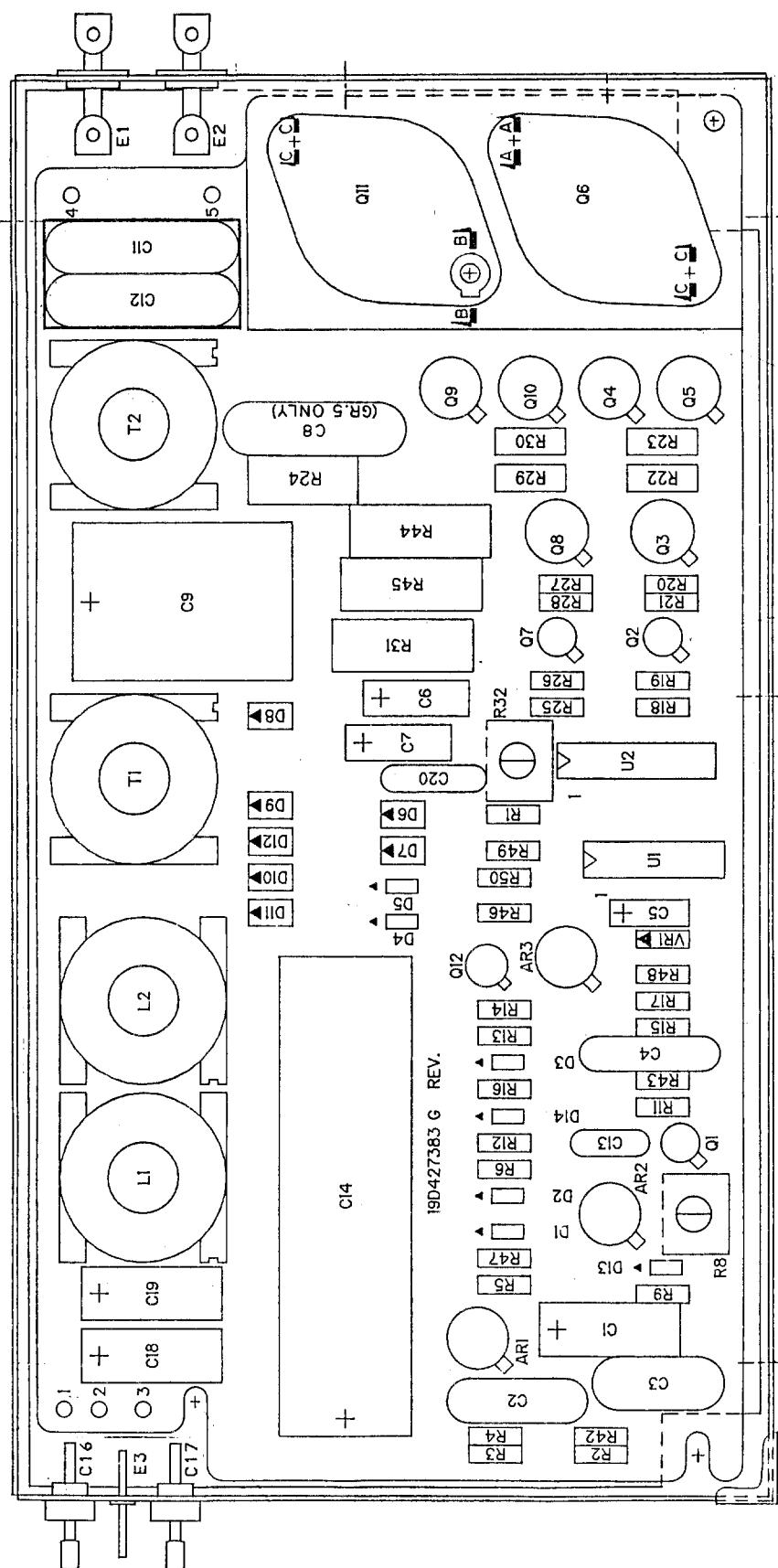


Figure 5 (19D427383 Sh.1 [13]) Pictorial Diagram
DC-DC Converter PL-19D427383G

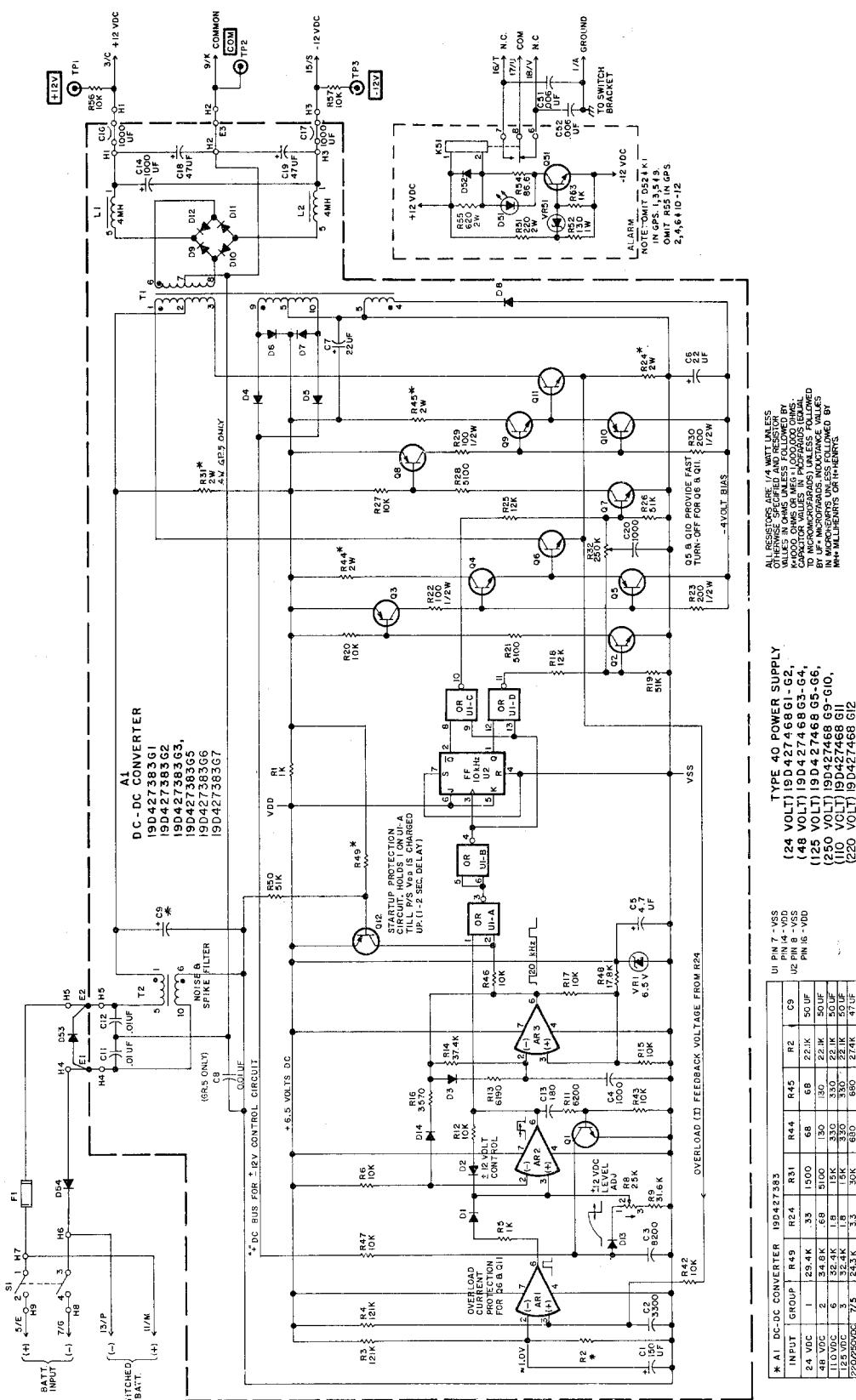


Figure 6 (19D427526 [14]) Schematic Diagram
Type 40 Power Supply PL-19D427468G

TYPE CS28A CHECKBACK (MASTER)

PL-19D436449G1

Schematic 19D436450

The Master Checkback module produces the keying pulses, timing sequences, display lights and alarms to check and monitor the carrier system, either manually or automatically. Up to three "remotes" may be checked for full and reduced power by the Master module. In special applications requiring testing of more than three remotes (up to six), the equipment can be programmed to check some or all remotes in either the full power or the reduced power mode. See the SPECIAL APPLICATION section which follows. The counter can be strapped to count the number of good tests or the number of failed tests. The counter may also be strapped to count only (1) full power or (2) full power and reduced power tests. Automatic checkback cycles are programmable from 1 hour to 255 hours in 1 hour intervals. Automatic retest cycles may be programmed for from 0 to 17 minutes delay.

A full power alarm relay and a reduced power alarm relay are provided with Form "C" contacts. Alarm lights on the front panel of the module identify which remote failed and whether it was a full or reduced power failure. Provision is made (by built-in relays) for remotely initiating a test, resetting alarms and resetting the program clock or, alternately, disabling the checkback, disabling remote #1 alarms, and disabling remote #2 alarms.

Also, a checkback test may be manually initiated at any remote location, but only when the Master module is not in the test mode (interrogating the remotes).

OPERATION

The entire interrogation and response sequence takes place in a nine (9) second interval. A master clock divides the total interval into nine (9) individual one second periods with the first period for master interrogation (8 pulses @ 16 Hz in 1/2 sec.) of the entire system. Then it "listens" during periods 2, 3, and 4 for each remote's

respective response on full power. It interrogates again in period 5 (different code; 4 pulses @ 16 Hz in 1/4 sec.) and similarly waits for the sequential response of each remote in periods 6, 7 and 8 on reduced power. During clock period 9, the clock and alarms are reset and the entire interrogation/response sequence is ready to repeat as programmed by "dip" switch S1 on the module. The timing of the nine intervals is controlled by counter U12 which, when activated produces nine sequenced outputs at one second intervals.

Refer to the Schematic Diagram located in this section of this manual. The 32,768 Hz frequency at the output of the crystal oscillator AR1 is divided down to 16 Hz at Pin 15 of counter U1 and down to 1 Hz at Pin 6 of counter U2. At Pin 3 of counter U3, the frequency has been counted down to 1 Hz per hour. Programmable counters U5 and U6 set the automatic test output at Pin 3 of U6 in hour steps from 1 to 255 hours. Switch S1 is used to program the counters in straight binary. Examples are given in Table I.

The checkback test sequence may be initiated in several ways, namely:

- ▶ Automatically, by the local master programmed clock (U6).
- ▶ Automatically, by the retest timer (U30)
- ▶ Manually, by depressing the Manual Test Switch on the front panel at either the master or remote locations.
- ▶ By energizing the remote test relay coil (K4) at the master station.

When initiated U78 sets, Pin 13 switches positive and applies a 1 to the Data Input of Flip-Flop U7A, and switches AR3-A positive lighting the TEST LED (D10). This inhibits AR3-B, C & D, on the next positive edge of the 1 Hz clock. Flip-Flop U7A sets and Pin 2 of U7A switches to 0 and applies a 0 to NOR gate U8D, Pin 13. This allows a 1 Hz clock signal to be applied to counter U12, Pin 14 through inverter U8A and NOR gate U8D. On the first count U12-Q1 (Pin 2) switches to 1. This sets Flip-Flop U10A and Pin 1 of U10A switches to 1. NOR gate U9A switches to 0 allowing the 16 Hz clock to be

TABLE I

TYPICAL TEST INTERVALS (Switch S1 Settings)

TEST INTERVAL	SWITCH POSITION							
	1 1Hr	2 2Hr	3 4Hr	4 8Hr	5 16Hr	6 32Hr	7 64Hr	8 128Hr
1 Hour	C							
2 Hours		C						
4 Hours			C					
8 Hours				C				
12 Hours			C	C				
24 Hours (1 Day)				C	C			
48 Hours (2 Days)					C	C		
72 hours (3 Days)				C			C	
168 Hours (1 Week)				C		C		C
240 Hours (10 Days)					C	C	C	C
255 Hours (max.)	C	C	C	C	C	C	C	C

C = SWITCH CLOSED WITH OTHERS OPEN

gated through NOR gate U9B to the STOP output. With jumper K in the 1-2 position, the START output is switched ON through inverters U9B and C by Flip-Flop U10A. With jumper K in the 2-3 position, the START output is switched ON each time the STOP is switched OFF. Counter U11 counts the output pulses (16 Hz) at the STOP output. When the count reaches 8, Flip-Flop U10 is reset by a 1 output from U11, Pin 11. Counter U11 is also reset by NOR gate U9A.

These 8 pulses at a 16 Hz rate from the Master Checkback Module are recognized at the remote Checkback Modules as a command to switch to the test mode.

Flip-Flop U21A is set on the second 1 Hz clock period and U12 switches to a 1 on Q2 (Pin 4), the full power alarm light is turned ON for remote #1, and the 1 is applied to Pin 1 of NAND gate U20A. Remote #1 must send back 8 pulses at a 16 Hz rate during this clock period. These input pulses switch AR2. The output of AR2 is connected to bandpass filter AR4-A and transistor switch Q5. As the pulses are received, Q5 causes the alarm lights to flash at a 16 Hz rate.

The 16 Hz pulses are detected by AR4-D and applied to the clock input of counter U16

through inverter AR4-B. Timing circuit AR4-C is switched LOW by the first pulse and allows U16 to count the pulses. If a pulse is delayed or missing, AR4-C will switch positive, resetting counter U16. This prevents random pulses from counting up to the desired number. When counter U16 reaches 8, Pin 9 switches to a 1, setting Flip-Flop U17-B. This starts counter U19 and when it reaches its predetermined count, Pin 1 momentarily switches to a 1 and this switches NAND gate U20-A to 0 and inverter U20-B to 1, resetting Flip-Flop U21A and turning OFF alarm light #1.

If an additional pulse had been received, AR4-D would have reset U17A, which in turn would have reset U18 before an output was produced. If the 8 pulses are not received within the second period of the 1 Hz clock, Flip-Flop U21A is left set and full power alarm light #1 is left ON.

The sequence described above is repeated for remotes 2 and 3 in the 3rd and 4th 1 Hz clock periods. At the start of 1 Hz clock period 5, Q5 (Pin 1) of U12 switches to a 1, setting Flip-Flop U10B. NOR gate U9A switches to 0, allowing the 16 Hz clock to be gated through NOR gate U9B to the STOP output. When U11 counts up to 4, Pin 1 switches to a

1, resetting Flip-Flop U10B. REDUCED POWER was switched ON when U10B was set and the START output was held OFF by U10A. The 4 pulses from the Master command the remotes to switch to reduced power and return 4 pulses in their respective time slots.

At the start of 1 Hz clock period 6, Q6 (Pin 5) of U12 switches to a 1, setting Flip-Flop U25A, turning ON the reduced power alarm light for remote #1, and applying the 1 to Pin 1 of NAND gate U24A. During this clock period, remote #1 must send back 4 pulses at a 16 Hz rate. The four input pulses are detected as explained above for the eight pulses, except counter U16 sets Flip-Flop U17A and counter U18 is started and, when its count is reached, it applies a 1 to Pin 2 of U24A. This causes a 1 to be applied to Pin 4 of U25A, resetting that Flip-Flop and turning OFF reduced power alarm light #1. The circuits for the reduced power alarms are identical to the full power alarm circuits. The sequence described above is repeated for remotes 2 and 3, in the 7th and 8th 1 Hz clock periods. If any of the remotes (1, 2, or 3) do not exist, the appropriate segments of switch SS are closed to prevent an alarm.

During 1 Hz clock period 9, Pin 11 of U12 switches to a 1, resetting Flip-Flop U7B and preventing Flip-Flop U7A from resetting. U7B switches AR3-A OFF, turning the test light OFF and removing the inhibit from AR3-B & D. If any of the alarms are ON at the end of the test, AR3-D (for full power) or AR3-C (for reduced power) are switched OFF. The output of AR3-D or AR3-C is connected to Test Failure counters U27 and U28 respectively through U26A and U26B. The output from U27 or U28 caused by the first (or second) test failure will start timer U30. When U30 counts to the output selected by jumper 'G' its output will reset the alarm lights and restart the Checkback cycle. After a failure of three test cycles U29C or U29D will turn off transistor Q3 or Q4, de-energizing alarm relay K1 or K2 and closing the alarm contacts. If either AR3-C or AR3-D are switched OFF (Jumper L to 2-3), NAND gate U13C switches to a 1, which applies a reset to Flip-Flop U7A & B (Jumper M connected to 1-2), preventing the unit from going into the test mode until the alarms have been cleared. Under normal

conditions Flip-Flop U7A is reset at the beginning of the 1 Hz clock period 10.

If counter (M1) is strapped to count good tests (Jumper B to 1-2), NAND gate U13B remains at 0 during period 9 (if no alarms are ON) and the 1 output from Pin 11 of U12 is switched through to the counter. An alarm causes U13B to switch to a 1 during period 9 and this blocks the pulse at U13D. Connecting jumper B to 2-3 permits each failed test to be counted, since each time U13B switches to a 1 the counter is advanced one count. If jumper L is connected to 1-2, the reduced power tests are also included in the count. Jumper M connected to 1-2 latches the checkback in a "no-test" mode until the alarms are reset.

The automatic timing sequence is started by operating CLOCK RESET switch S2. When this switch is operated, a test is started and the test will automatically be repeated in the number of hours programmed into the clock by switch S1.

A test may be manually initiated at any time, without affecting the automatic timing, by operating MANUAL TEST switch S3. When a test is not in progress, the Master Checkback will recognize the 4 pulse at 16 Hz as a command to switch into the test mode. The output of 4 pulse detector U18, Pin 1, is OR connected by diode CR33 into the test start circuit.

A positive voltage applied to Pin 8 of the checkback disables the output, and therefore stops any test in progress and resets all circuits. It also prevents the unit from switching to the test mode.

SPECIAL APPLICATIONS

Although the Checkback system was designed for a maximum of four stations (one Master and three Remotes) situations may arise where it is desirable to test more than four equipments in a line section or over a system of multiple line sections. In the normal configuration the second through fourth test time slots of the Master Checkback are used for receiving Full Power signals of eight pulses from each of three remote checkbacks, and time slots six through eight (6-8) are used to receive

REDUCED POWER signals of four pulses from each of the same three remote checkbacks.

The number of stations tested can be increased beyond three (to four, five or six) by having some (or all) remote checkbacks respond in only one time slot rather than two as shown in Table II.

One Checkback system can be used on two or more adjacent line sections by connecting the interposing stations in a 'repeater' configuration as shown in the diagram below.

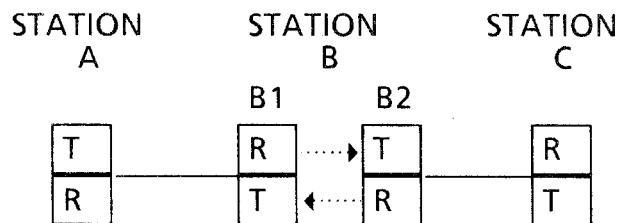
TABLE II

	FULL POWER			REDUCED POWER		
Alarm Indicator	1	2	3	1	2	3
Time Slot	2	3	4	6	7	8
RESPONDING STATION						
Normal (3 remotes)	#1	#2	#3	#1	#2	#3
4 Remotes	#1	#2	#3†	#1	#2	#4††
5 Remotes	#1	#2†	#3†	#1	#4††	#5††
6 Remotes	#1	#2†	#3†	#4††	#5††	#6††

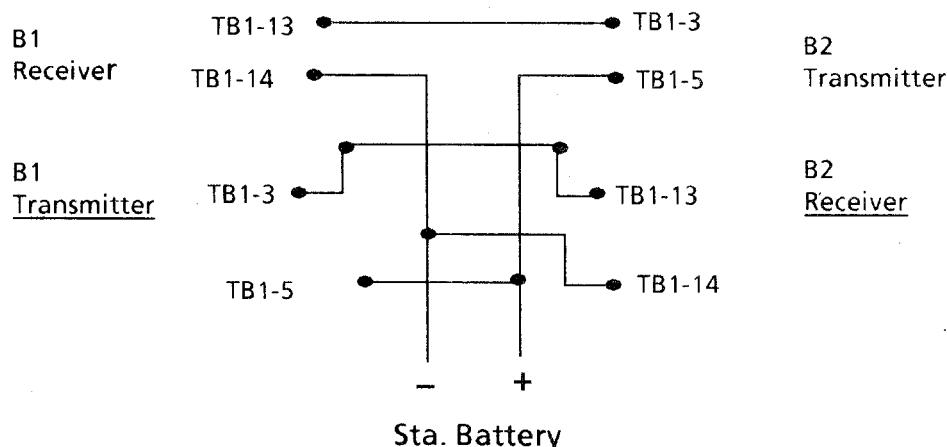
† Remote strapped for FULL POWER response only.

†† Remote strapped for REDUCED POWER response only. See Remote Checkback module description for strapping

In this example the signals from a Master Checkback at station A will be received at station B, and repeated to station C. Station B1 will respond in its assigned time slot and will repeat the signals of the stations B2 and station C in their assigned time slots. In case of an alarm, the alarm lights at the Master will indicate which remote station (B1, B2, or C), failed to respond.



Connections at Station B:



Note that the transmitters must be strapped for STOP priority to assure proper functioning during operation of the protective relays.

NOMINAL OPERATING
CHARACTERISTICS

1. Power Requirements:

+12 VDC, 95 mA
-12 VDC, 95 mA

2. Outputs:

Stop, Start and Reduced Power:

- a) OFF: -6 VDC
- b) ON: +6 VDC

3. Inputs:

a) Checkback Disable:

- (1) OFF: -6 VDC
- (2) ON: +6 VDC

b) Receive Input:

- (1) OFF: Open Circuit
- (2) ON: Connect to Common

4. Remote Controls:

Clock Reset, Test and ALarm Reset

- a) ON: 30 - 150V
- b) OFF: 0 VDC

5. Oscillator Frequency (TP1):

32,768 Hz

6. Pulse Frequency (TP2 - During Test):

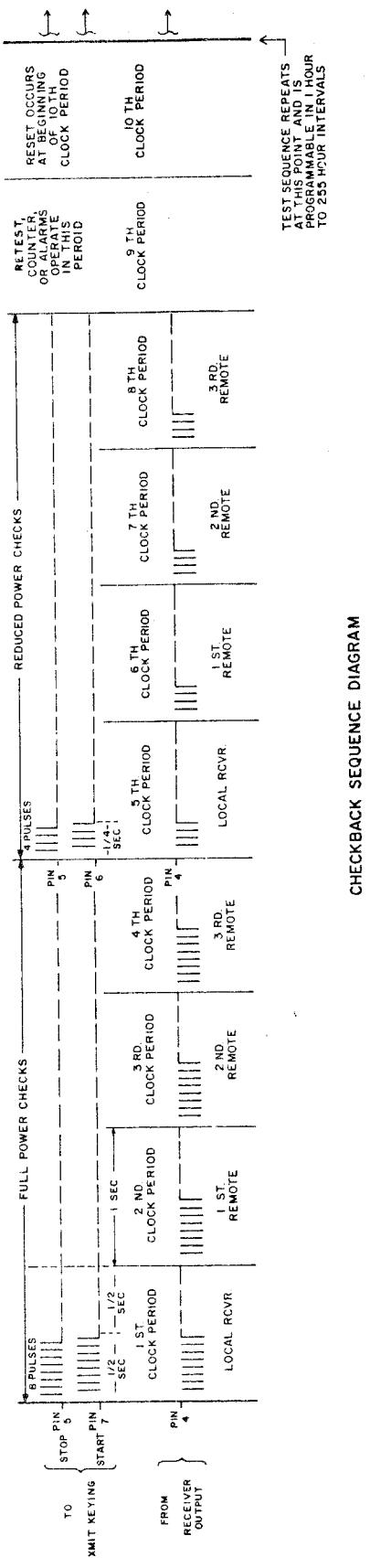
16 Hz

7. Time Slots:

1 sec.

CHECKBACK MASTER TEST POINT
READINGS

TP1	Square wave	32.768 Hz
	Amplitude approx.	15. V pk. to pk.
TP2	Square wave	16 Hz
	Amplitude approx.	15. V pk. to pk.
TP3	Square wave	1 Hz
	Amplitude approx.	15. V pk. to pk.



CHECKBACK SEQUENCE DIAGRAM

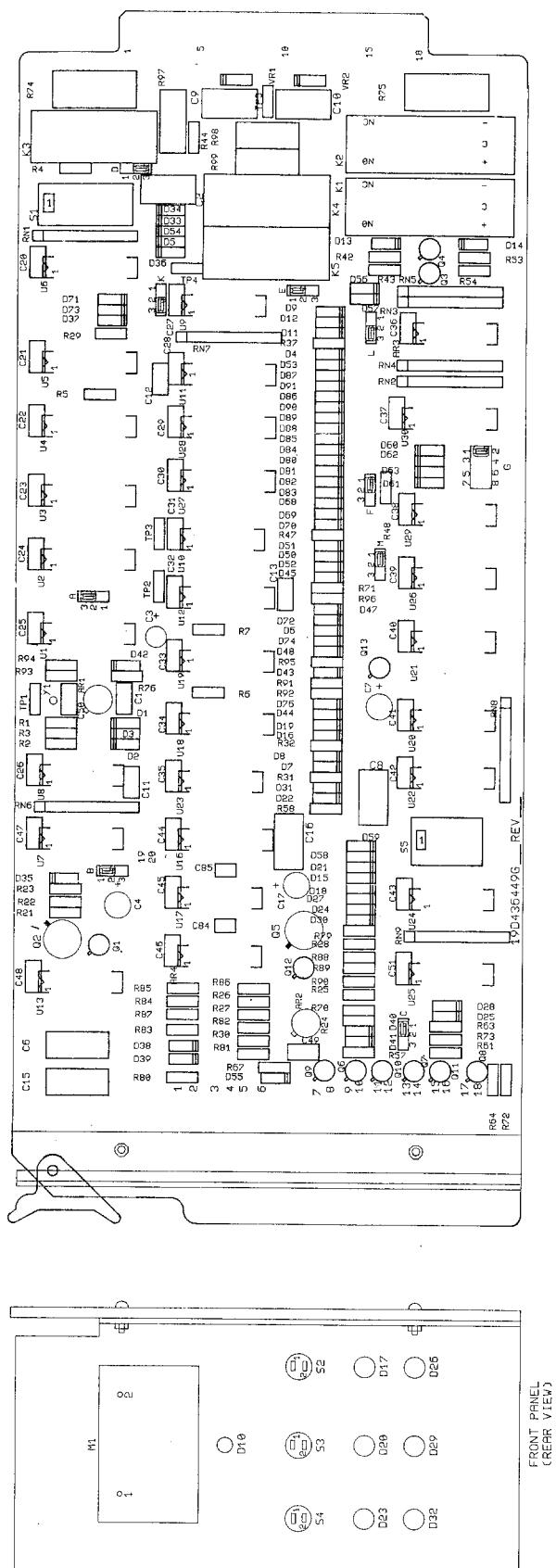
Figure 1 (19D426755-2) Master Checkback Sequence Diagram

ITEM NO.	IDENTIFICATION NUMBER	DESCRIPTION	GROUP NUMBER AND QUANTITY				
			1	2	3	4	5
D18	0246A9401P4148	DIODE JAN 1N4148	1				
D19	0246A9401P4148	DIODE JAN 1N4148	1				
D20	0246A9958P001	RED LED 12V LEDCO 4100-2	1				
D21	0246A9401P4148	DIODE JAN 1N4148	1				
D22	0246A9401P4148	DIODE JAN 1N4148	1				
D23	0246A9958P001	RED LED 12V LEDCO 4100-2	1				
D24	0246A9401P4148	DIODE JAN 1N4148	1				
D25	0246A9401P4148	DIODE JAN 1N4148	1				
D26	0246A9958P001	RED LED 12V LEDCO 4100-2	1				
D27	0246A9401P4148	DIODE JAN 1N4148	1				
D28	0246A9401P4148	DIODE JAN 1N4148	1				
D29	0246A9958P001	RED LED 12V LEDCO 4100-2	1				
D30	0246A9401P4148	DIODE JAN 1N4148	1				
D31	0246A9401P4148	DIODE JAN 1N4148	1				
D32	0246A9958P001	RED LED 12V LEDCO 4100-2	1				
D33	0246A9401P4148	DIODE JAN 1N4148	1				
D34	0246A9401P4148	DIODE JAN 1N4148	1				
D35	0246A9401P4148	DIODE JAN 1N4148	1				
D36	0246A9401P4148	DIODE JAN 1N4148	1				
D37	0246A9401P4148	DIODE JAN 1N4148	1				
D38	0246A9401P4148	DIODE JAN 1N4148	1				
D39	0246A9401P4148	DIODE JAN 1N4148	1				
D40	0246A9401P4148	DIODE JAN 1N4148	1				
D41	0246A9401P4148	DIODE JAN 1N4148	1				
D42	0246A9401P4148	DIODE JAN 1N4148	1				
D43	0246A9401P4148	DIODE JAN 1N4148	1				
D44	0246A9401P4148	DIODE JAN 1N4148	1				
D45	0246A9401P4148	DIODE JAN 1N4148	1				
D47	0246A9401P4148	DIODE JAN 1N4148	1				
D48	0246A9401P4148	DIODE JAN 1N4148	1				
D50	0246A9401P4148	DIODE JAN 1N4148	1				
D51	0246A9401P4148	DIODE JAN 1N4148	1				
D52	0246A9401P4148	DIODE JAN 1N4148	1				
D53	0246A9401P4148	DIODE JAN 1N4148	1				
D54	0246A9401P4148	DIODE JAN 1N4148	1				
D55	0246A9401P4148	DIODE JAN 1N4148	1				
D56	0246A9401P4148	DIODE JAN 1N4148	1				
D57	0246A9401P4148	DIODE JAN 1N4148	1				
D58	0246A9401P4148	DIODE JAN 1N4148	1				
D59	0246A9401P4148	DIODE JAN 1N4148	1				
D60	0246A9401P4148	DIODE JAN 1N4148	1				
D61	0246A9401P4148	DIODE JAN 1N4148	1				
D62	0246A9401P4148	DIODE JAN 1N4148	1				
D63	0246A9401P4148	DIODE JAN 1N4148	1				
D68	0246A9401P4148	DIODE JAN 1N4148	1				
D69	0246A9401P4148	DIODE JAN 1N4148	1				
D70	0246A9401P4148	DIODE JAN 1N4148	1				
D71	0246A9401P4148	DIODE JAN 1N4148	1				
D72	0246A9401P4148	DIODE JAN 1N4148	1				
D73	0246A9401P4148	DIODE JAN 1N4148	1				
D74	0246A9401P4148	DIODE JAN 1N4148	1				
D76	0246A9401P4148	DIODE JAN 1N4148	1				
D80	0246A9401P4148	DIODE JAN 1N4148	1				
D81	0246A9401P4148	DIODE JAN 1N4148	1				
D82	0246A9401P4148	DIODE JAN 1N4148	1				
D83	0246A9401P4148	DIODE JAN 1N4148	1				
D84	0246A9401P4148	DIODE JAN 1N4148	1				
D85	0246A9401P4148	DIODE JAN 1N4148	1				
D86	0246A9401P4148	DIODE JAN 1N4148	1				
D87	0246A9401P4148	DIODE JAN 1N4148	1				
D88	0246A9401P4148	DIODE JAN 1N4148	1				
D89	0246A9401P4148	DIODE JAN 1N4148	1				
D90	0246A9401P4148	DIODE JAN 1N4148	1				
D91	0246A9401P4148	DIODE JAN 1N4148	1				
K1	19B209439P003	REL MERC. 24V 1 FORM C	1				
K2	19B209439P003	REL MERC. 24V 1 FORM C	1				
K3	0367A0602G001	COIL	1				
K4	0367A0602G001	COIL	1				
K5	0367A0602G001	COIL	1				
M1	19A144612P002	COUNT ELEC 5 DIGIT 24VDC	1				

Figure 2 (19D436449 G1 [3]) Master Checkback Parts List

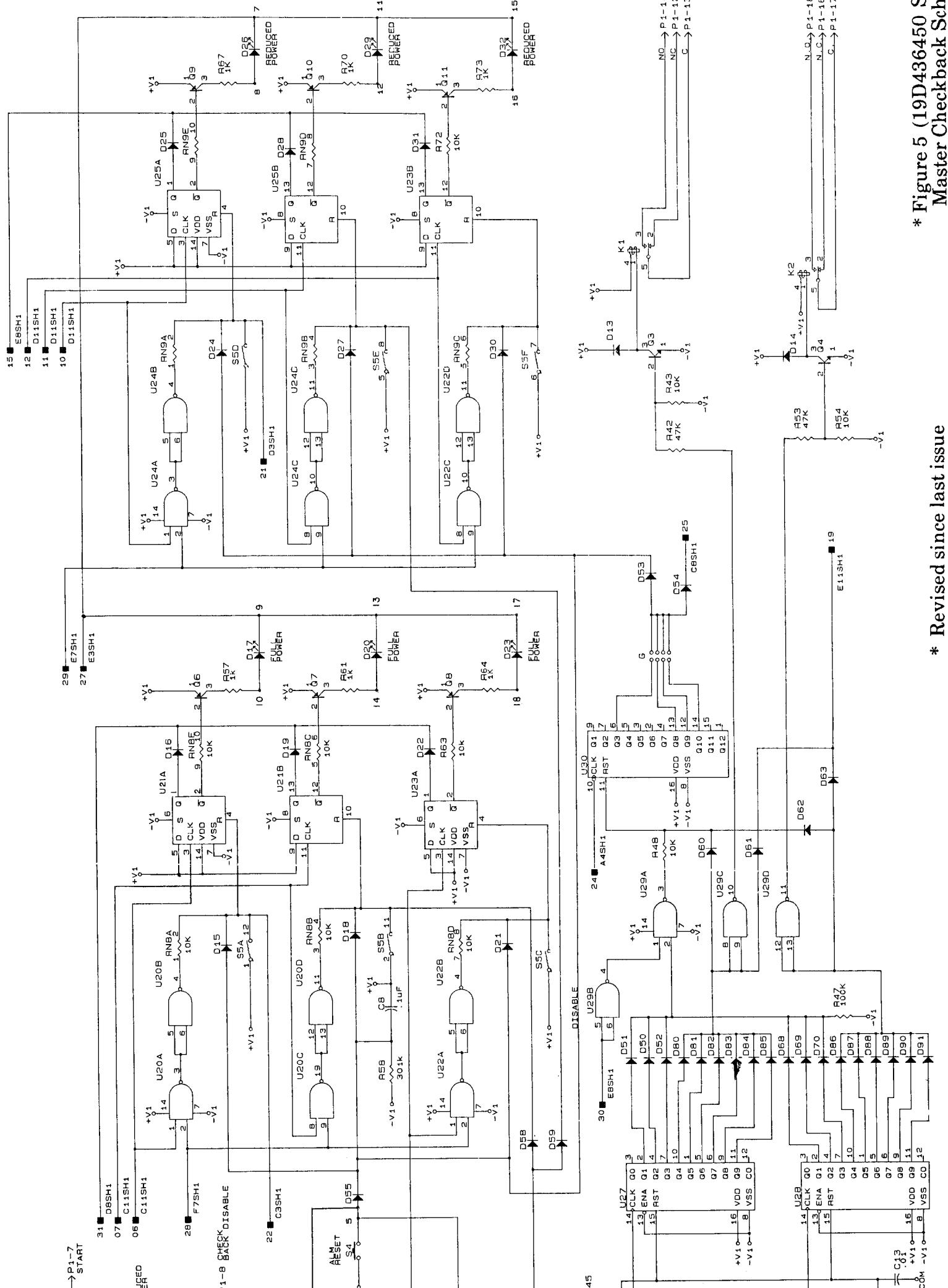
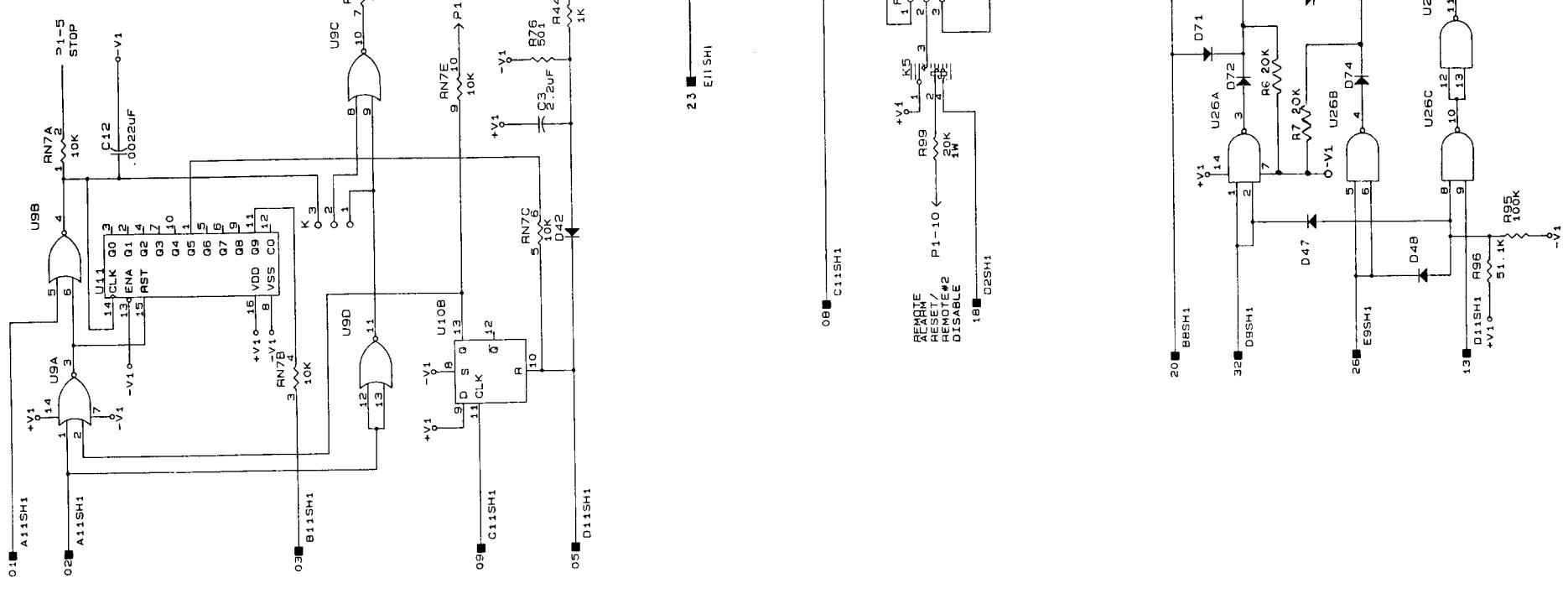
ITEM NO.	IDENTIFICATION NUMBER	DESCRIPTION	GROUP NUMBER AND QUANTITY				
			1	2	3	4	5
R98	0246A9103P203	RES.CARC 5% ,1W 20K	1				
R99	0246A9103P203	RES.CARC 5% ,1W 20K	1				
RN1	0246A9132P104C	RESNET 10-PIN 9X100K 2%	1				
RN2	0246A9133P104C	RESNET 10-PIN 5X100K 2%	1				
RN3	0246A9133P104C	RESNET 10-PIN 5X100K 2%	1				
RN4	0246A9133P104C	RESNET 10-PIN 5X100K 2%	1				
RN5	0246A9133P104C	RESNET 10-PIN 5X100K 2%	1				
RN6	0246A9133P103C	RESNET 10-PIN 5X10K 2%	1				
RN7	0246A9133P103C	RESNET 10-PIN 5X10K 2%	1				
RN8	0246A9133P103C	RESNET 10-PIN 5X10K 2%	1				
RN9	0246A9133P103C	RESNET 10-PIN 5X10K 2%	1				
S1	0246A9957P003	DIP SWITCH	1				
S2	7481654P006	SW.PUSH,SPNO,RED	1				
S5	0246A9957P002	DIP SWITCH	1				
U1	0246A9502P4040	I.C. 4040 CMOS	1				
U2	0246A9502P4040	I.C. 4040 CMOS	1				
U3	0246A9502P4526	I.C. 4526 CMOS	1				
U4	0246A9502P4526	I.C. 4526 CMOS	1				
U5	0246A9502P4526	I.C. 4526 CMOS	1				
U6	0246A9502P4526	I.C. 4526 CMOS	1				
U7	0246A9502P4013	I.C. 4013 CMOS	1				
U8	0246A9502P4001	I.C. 4001 CMOS	1				
U9	0246A9502P4001	I.C. 4001 CMOS	1				
U10	0246A9502P4013	I.C. 4013 CMOS	1				
U11	0246A9502P4017	I.C. 4017 CMOS	1				
U12	0246A9502P4017	I.C. 4017 CMOS	1				
U13	0246A9502P4011	I.C. 4011 CMOS	1				
U16	0246A9502P4017	I.C. 4017 CMOS	1				
U17	0246A9502P4013	I.C. 4013 CMOS	1				
U18	0246A9502P4040	I.C. 4040 CMOS	1				
U19	0246A9502P4040	I.C. 4040 CMOS	1				
U20	0246A9502P4011	I.C. 4011 CMOS	1				
U21	0246A9502P4013	I.C. 4013 CMOS	1				
U22	0246A9502P4011	I.C. 4011 CMOS	1				
U23	0246A9502P4013	I.C. 4013 CMOS	1				
U24	0246A9502P4011	I.C. 4011 CMOS	1				
U25	0246A9502P4013	I.C. 4013 CMOS	1				
U26	0246A9502P4011	I.C. 4011 CMOS	1				
U27	0246A9502P4017	I.C. 4017 CMOS	1				
U28	0246A9502P4017	I.C. 4017 CMOS	1				
U29	0246A9502P4011	I.C. 4011 CMOS	1				
U30	0246A9502P4040	I.C. 4040 CMOS	1				
VR1	0246A9403P6R2	ZENER 6.2V 5% 400MW	1				
VR2	0246A9403P6R2	ZENER 6.2V 5% 400MW	1				
Y1	19A701383P001	XTAL 32.768 KHZ	1				

Figure 2 (19D436449 G1 [3]) Master Checkback Parts List



* Figure 3 (19D436449 Sh.1 [4]) Master Checkback Outline

* Revised since last issue



* Revised since last issue

* Figure 5 (19D436450 Sh 2 [3])
Master Checkback Schematic

AUXILIARY RELAY 19D427620G3

DESCRIPTION

The Auxiliary Relay, 19D427620G3, is used in conjunction with the CB10A Checkback Equipment. It provides isolation between the Checkback shelf and the associated PLC equipment through use of three mercury-wetted relays. These relays have separate inputs and outputs. Three LED indicators show which relay is energized.

OPERATION

Refer to the Schematic Diagram located in this instruction. A positive input signal applied to the INPUT of relay #1 or to INPUT #1 of relay #2 will switch the associated input amplifier ON. This switches on the relay driver Q1 or Q2, energizing K1 or K2. A positive input to INPUT #2 of relay #2 will override an INPUT #1 of relay #2 and lock the relay #2 input amplifier in the OFF position.

Relay K3 is energized directly by application of 125 VDC (Jumper "A" in the 1-2 position) or 48 VDC (Jumper "A" in the 2-3 position) to relay #3 INPUT #1 (+) and INPUT #2 (-). An external resistor is used for 250 VDC applications.

NOMINAL OPERATING CHARACTERISTICS

1. Input level

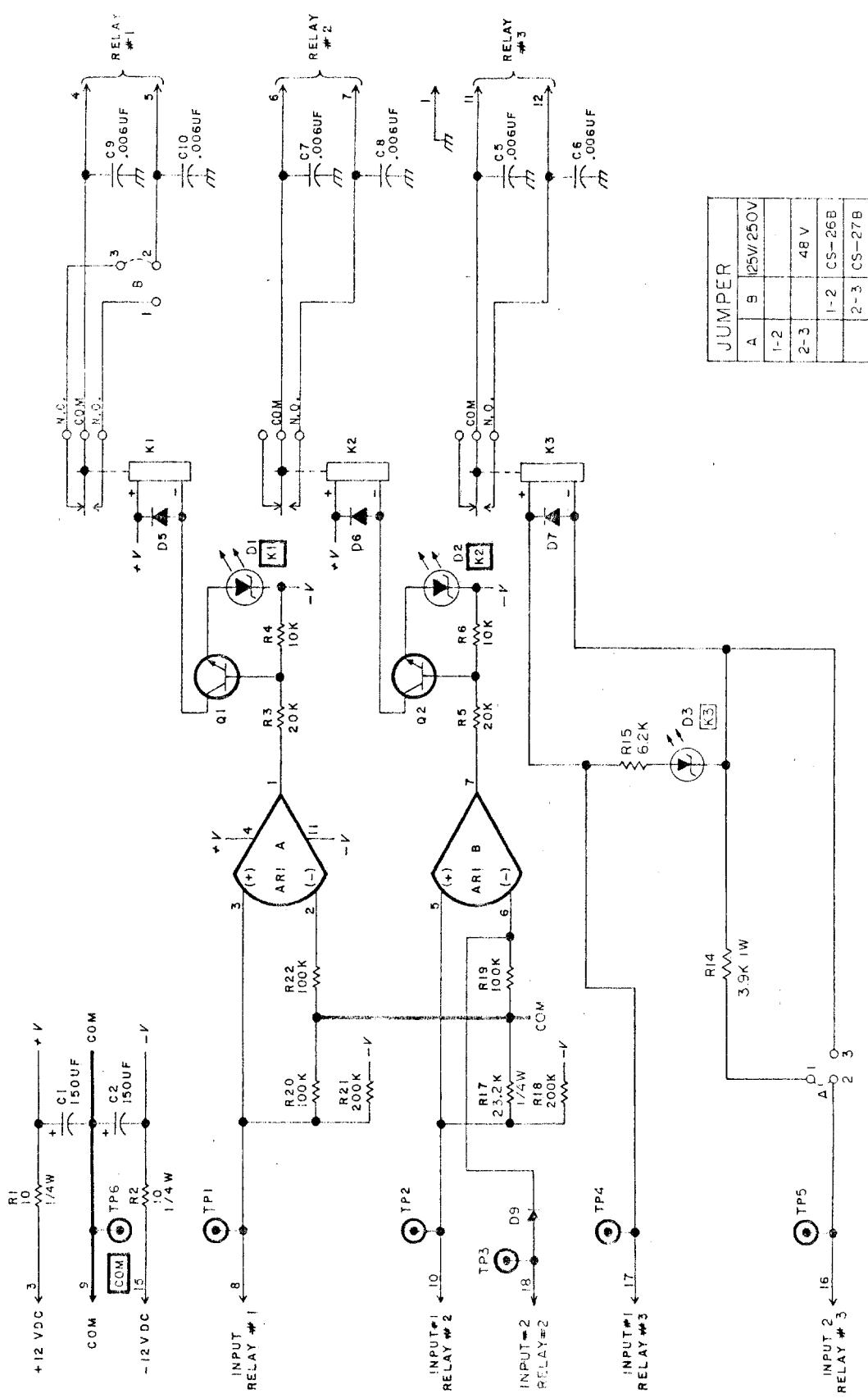
a.	Relay #1 INPUT,	Relay #2 INPUT #1,	+ 10 VDC = ON
b.		Relay #2 INPUT #2,	+ 10 VDC = OFF
c.	Relay #3	Jumper "A" 1-2	125 VDC
		Jumper "A" 2-3	48 VDC

2. Output contacts: 100 VA

3. Relay operate time: 2 milliseconds max.

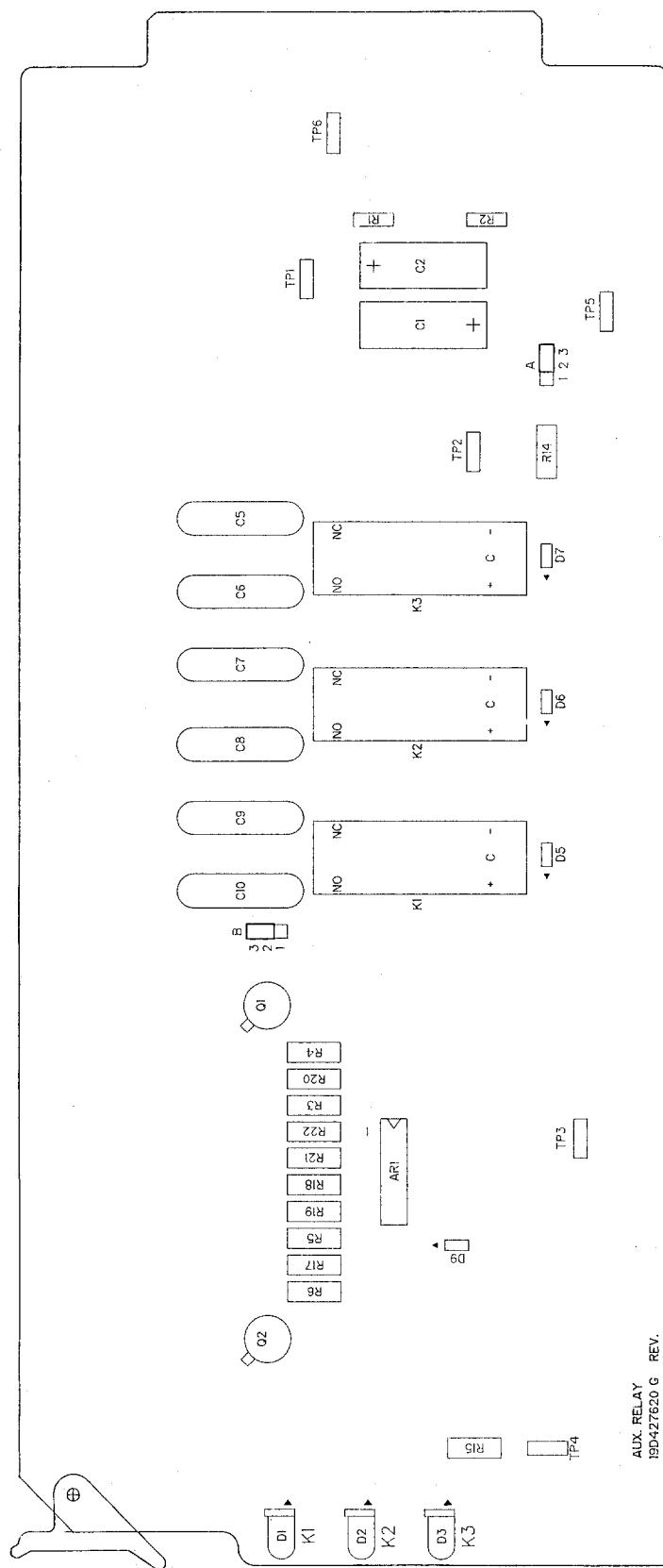
ITEM NO.	IDENTIFICATION NUMBER	DESCRIPTION			
			1	2	3
	19D427620G003 REV#02	CHK-BACK AUX.			
AR1	0246A9351P224	OP AMP LM224	1		
C1	5496267P012	CAPACITOR	1		
C2	5496267P012	CAPACITOR	1		
C5	0246A9028P682	CAP 6800PF CERAMIC RV#1	1		
C6	0246A9028P682	CAP 6800PF CERAMIC RV#1	1		
C7	0246A9028P682	CAP 6800PF CERAMIC RV#1	1		
C8	0246A9028P682	CAP 6800PF CERAMIC RV#1	1		
C9	0246A9028P682	CAP 6800PF CERAMIC RV#1	1		
C10	0246A9028P682	CAP 6800PF CERAMIC RV#1	1		
D1	0246A9418P406	LED,RED	1		
D2	0246A9418P406	LED,RED	1		
D3	0246A9418P406	LED,RED	1		
D5	0246A9401P4148	DIODE JAN 1N4148	1		
D6	0246A9401P4148	DIODE JAN 1N4148	1		
D7	4037822P001	RECTIFIER - 1N4004G	1		
D9	0246A9401P4148	DIODE JAN 1N4148	1		
K1	19B209439P001	REL	1		
K2	19B209439P001	REL	1		
K3	19B209439P001	REL	1		
Q1	19A115300P002	TSTR NPN 60V 2N3053	1		
Q2	19A115300P002	TSTR NPN 60V 2N3053	1		
R1	0246A9134P10R0	RES 10 OHM 1/4W 1% MTL	1		
R2	0246A9134P10R0	RES 10 OHM 1/4W 1% MTL	1		
R3	0246A9102P203	RES 20K .5W 5%	1		
R4	0246A9102P103	RES 10KOHM .5W 5%	1		
R5	0246A9102P203	RES 20K .5W 5%	1		
R6	0246A9102P103	RES 10KOHM .5W 5%	1		
R14	19A116479P2392K	RES 3.9KOHM 10% 2W FLPRF	1		
R15	0246A9103P622	RES 6.2K 1W 5%	1		
R17	0246A9134P2322	RES 23.2KOHM 1/4W 1% MTL	1		
R18	0246A9102P204	RESISTOR	1		
R19	0246A9102P104	RES 100K .5W 5%	1		
R20	0246A9102P104	RES 100K .5W 5%	1		
R21	0246A9102P204	RESISTOR	1		
R22	0246A9102P104	RES 100K .5W 5%	1		

AUXILIARY RELAY-PARTS LIST - 19D427620G3



SCHEMATIC DIAGRAM-19C335562 [2]

AUX RELAY
19D427620 G3,G103



AUXILIARY RELAY OUTLINE - 19D427620 SH.3 [1]