



INSTRUCTIONS

GEK-65567

DATA LOGGING AMPLIFIER

TYPE DLA52D

GENERAL  ELECTRIC

DATA LOGGING AMPLIFIER

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DESCRIPTION

The Type DLA52D is a transistorized data logging amplifier used for oscillograph monitoring of up to twelve points in a MOD III type static relaying scheme. These points are shown on the overall logic diagram of the relaying scheme. The DLA52D has contact outputs to operate an oscillograph. All twelve DLA contact outputs are supervised by one input. The DLA amplifier prevents undue loading and possible malfunctioning of the relay circuitry that is monitored. The DLA52D amplifier requires a DC power source and bias voltages which may be obtained from a Type SSA power supply.

The internal connections for the DLA52D are given in Fig. 1. This relay is built into a two rack unit case whose outline and mounting dimensions are given in Fig. 2. The component locations for the Type DLA52D are shown in Fig. 3.

RATINGS

The DLA52D is designed for use in an environment where the ambient temperature outside the case does not exceed -20°C or $+65^{\circ}$.

The DLA52D is designed to operate on bias voltages of plus 15 VDC and minus 15 VDC, these voltages may be obtained from a Type SSA power supply.

The contact outputs of the DLA52D are rated for a maximum load of 10 volt amperes. Maximum current is 500 milliamperes (resistive) and maximum voltage is 250 VDC.

BURDENS

The DLA52D presents a burden of ten milliamperes per channel to the positive DC power supply when ON (Logic 1). It presents a burden of one milliampere per channel to the positive DC power supply when OFF (Logic Zero).

CIRCUIT DESCRIPTION

The DLA52D is used when monitoring relay circuitry functions involving current-sinking type logic, where the presence or absence of signals, rather than their magnitudes, controls the operation. Therefore, with respect to the reference bus,

These instructions do not purport to cover all details or variations in equipment nor to provide for every possible contingency to be met in connection with installation, operation or maintenance. Should further information be desired or should particular problems arise which are not covered sufficiently for the purchaser's purposes, the matter should be referred to the General Electric Company.

To the extent required the products described herein meet applicable ANSI, IEEE and NEMA standards; but no such assurance is given with respect to local codes and ordinances because they vary greatly.

signals below one volt represent an OFF condition (Logic Zero), while signals resulting in an ON condition (Logic 1) are generally in the range of plus 12 to plus 15 volts. Current-sinking type logic is a logic system where the output stage that is OFF actually draws current from the stage driven to prevent it from turning ON.

The internal of one printed circuit card is shown in Fig. 4. Pins 3 and 4 are inputs, pins 7 and 8 are outputs. For a Logic 1 at both pins 3 and 4, both diodes D1 and D2 are reversed biased, allowing transistor Q1 to turn on. This energizes reed relay RR, which closes the two "A" type contacts. Connecting pin 2 to reference will seal the reed relay. This feature is not used in the DLA52D. The purpose of the series resistor in the contact circuit is to limit the contact current due to load and line capacitance. Excessive momentary current can cause contact welding.

For a Logic Zero (current sinking) at either, or both inputs, transistor Q1 is prevented from turning on, due to the 6.8V zener diode.

Both pin 3 and 4 inputs can be monitored at the orange (OTJ) and the green (GTS) test jacks respectively. These jacks are located on the A133 printed circuit card.

Pin 4 of each card is tied to pin 2 of the C411 input cable. This input is used to supervise all other inputs by means of the AND function included on each card. A typical supervising function is the trip bus in the static relay.

CONSTRUCTION

The DLA52D is packaged in a metal enclosed case which is suitable for mounting one standard 19 inch rack. The outline and mounting dimensions of this case and the physical location of the components are included in this instruction book.

It will be noted that the internal connection diagram of this DLA gives a block diagram of one of the twelve printed circuit cards included in the DLA. A table is also provided on this diagram. The second column of this table gives the letters that correspond to the card addresses shown on the component location diagram. The remaining columns give the connection entering or leaving the unit.

TESTING

GENERAL

The DLA52D is usually supplied from the factory mounted in a static relay equipment. All units for a given terminal of static relaying are tested together at the factory and each has the same summary number stamped on its nameplate. When the DLA is furnished as a separate unit, it should be interconnected with the associated relay equipment via the shielded plug-in cables prior to testing.

INSTALLATION TESTS

WARNING: THE LOGIC SYSTEM SIDE OF THE DC POWER SUPPLY USED WITH MOD III STATIC RELAY EQUIPMENT IS ISOLATED FROM GROUND. IT IS A DESIGN CHARACTERISTIC OF MOST ELECTRONIC INSTRUMENTS THAT ONE OF THE SIGNAL INPUT TERMINALS IS CONNECTED TO THE INSTRUMENT

CHASSIS. IF THE INSTRUMENT USED TO TEST THE RELAY EQUIPMENT IS ISOLATED FROM GROUND, ITS CHASSIS MAY HAVE AN ELECTRICAL POTENTIAL WITH RESPECT TO GROUND. THE USE OF A TEST INSTRUMENT WITH A GROUNDED CHASSIS WILL NOT AFFECT THE TESTING OF THE EQUIPMENT. A SECOND GROUND CONNECTION TO THE EQUIPMENT, SUCH AS A TEST LEAD INADVERTENTLY DROPPING AGAINST THE RELAY CASE, MAY CAUSE DAMAGE TO THE LOGIC CIRCUITRY. NO EXTERNAL TEST EQUIPMENT SHOULD BE LEFT CONNECTED TO THE STATIC RELAYS WHEN THEY ARE IN PROTECTIVE SERVICE, SINCE TEST EQUIPMENT GROUNDING REDUCES THE EFFECTIVENESS OF THE ISOLATION PROVIDED.

Since the DLA52D logic sections are basically transistor switches which energize a reed relay, adjustments are neither provided nor required. The various functions that are monitored and therefore serve as inputs to the DLA are covered in the overall logic diagram and descriptive writeup furnished with each equipment.

MAINTENANCE

PERIODIC TESTS

It should be sufficient to check the DLA outputs by observing oscillograph operation during periodic calibration tests made on the associated measuring units of the relaying scheme. No separate periodic tests of the DLA itself should be required.

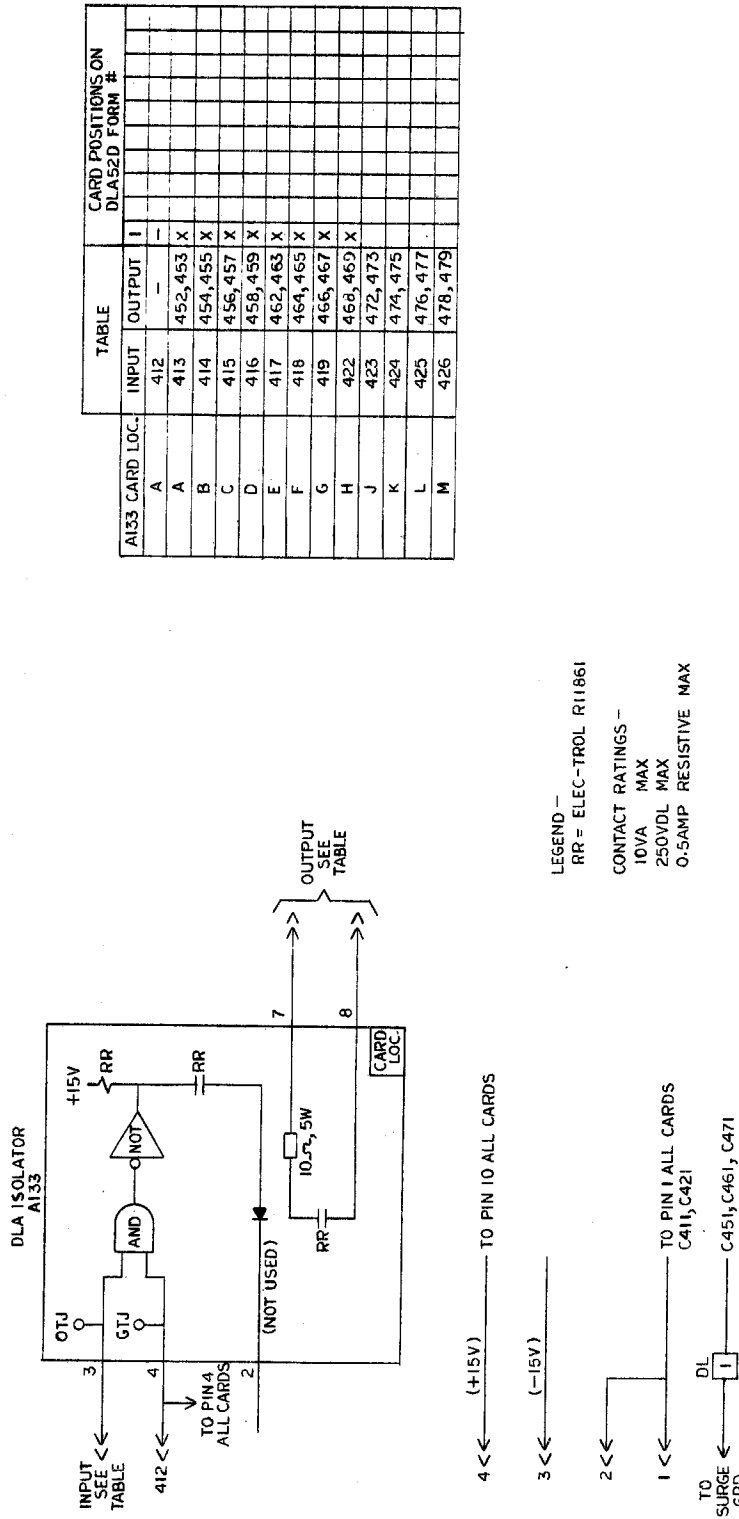
TROUBLESHOOTING

By signal tracing using the overall logic diagram and the various equipment test points, it should be possible to quickly isolate a DLA malfunction. A test adapter card, 0108B9643G2, is supplied with each static relay equipment to supplement the prewired equipment test points. Use of the adapter card is described in the card instruction book GEK-34158.

SPARE CARDS

The number of spare cards to be stocked depends on the total number of similar cards used at the same location or serviced by the same test group. For each type of card (different code designation) a suggested minimum number of spare cards would be:

- 1 spare for one to 25 cards
- 2 spares for 26 to 75 cards
- 3 spares for 76 to 150 cards.



AI33 CARD LOC.	TABLE		CARD POSITIONS ON DLA52D FORM #											
	INPUT	OUTPUT	1	2	3	4	5	6	7	8	9	10	11	12
A	412	-												
B	413	452, 453	X											
C	414	454, 455	X											
D	415	456, 457	X											
E	416	458, 459	X											
F	417	462, 463	X											
G	418	464, 465	X											
H	419	466, 467	X											
I	422	468, 469	X											
J	423	472, 473	X											
K	424	474, 475												
L	425	476, 477												
M	426	478, 479												

Fig. 1 (0138B7338-0) Internal Connections Diagram for the DLA52D Relay.

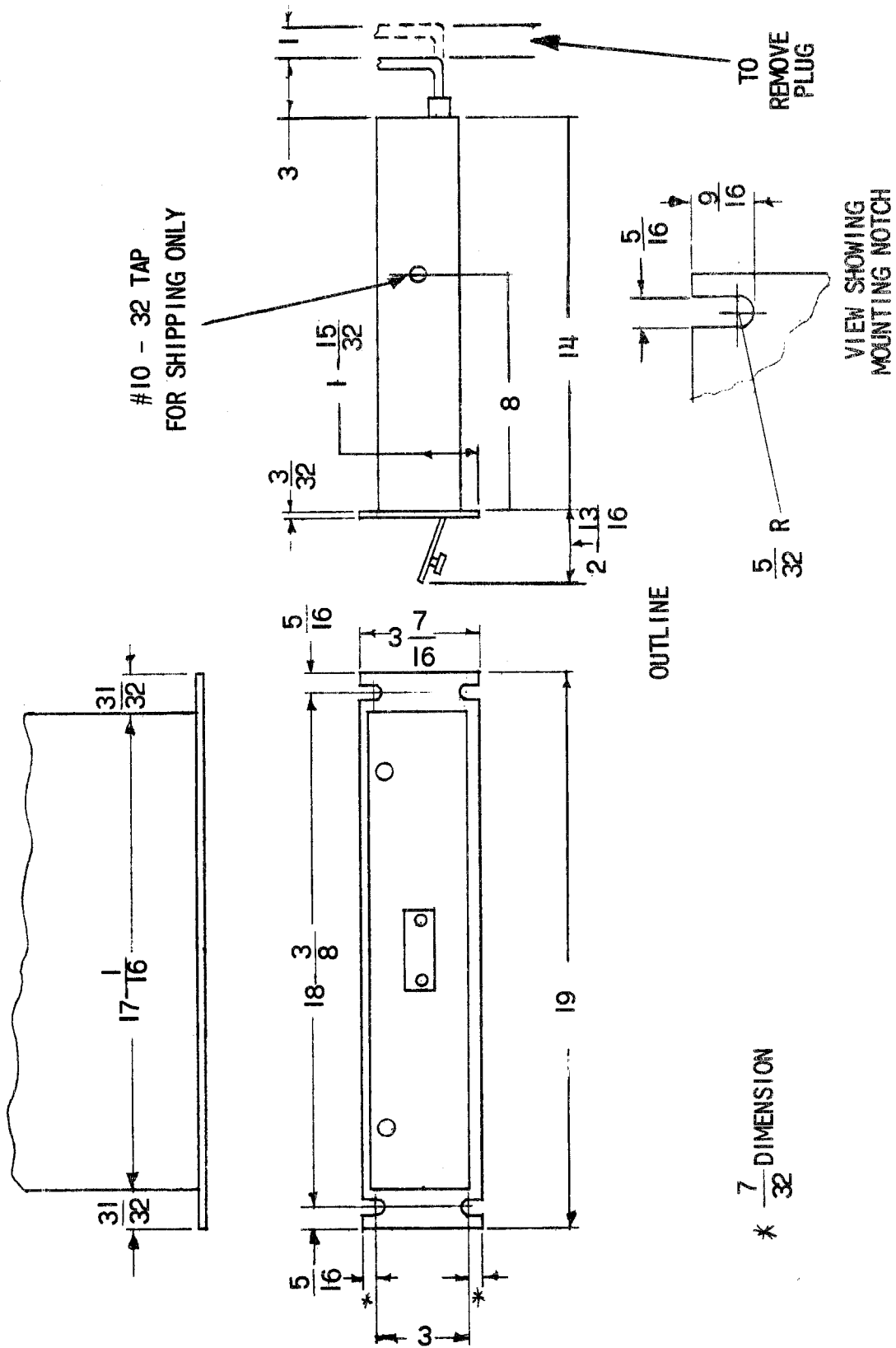
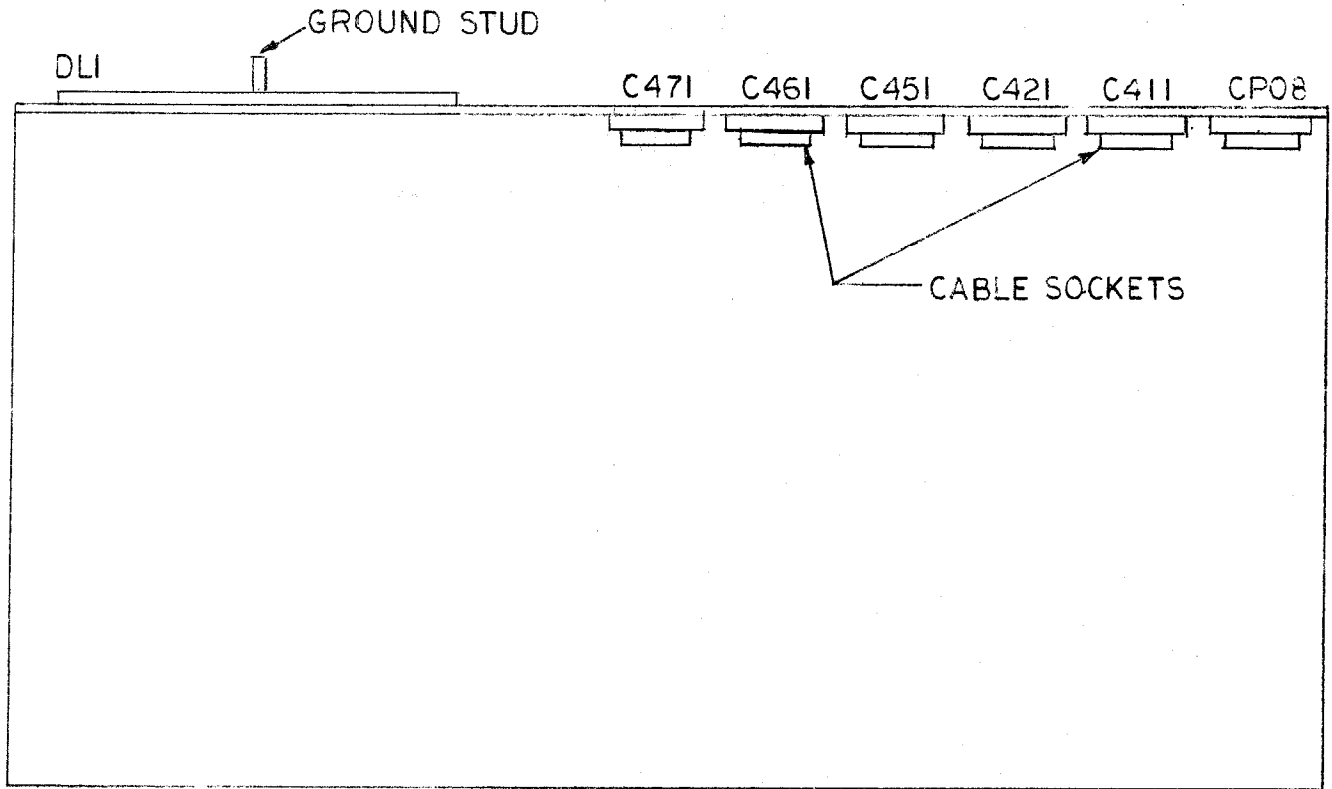
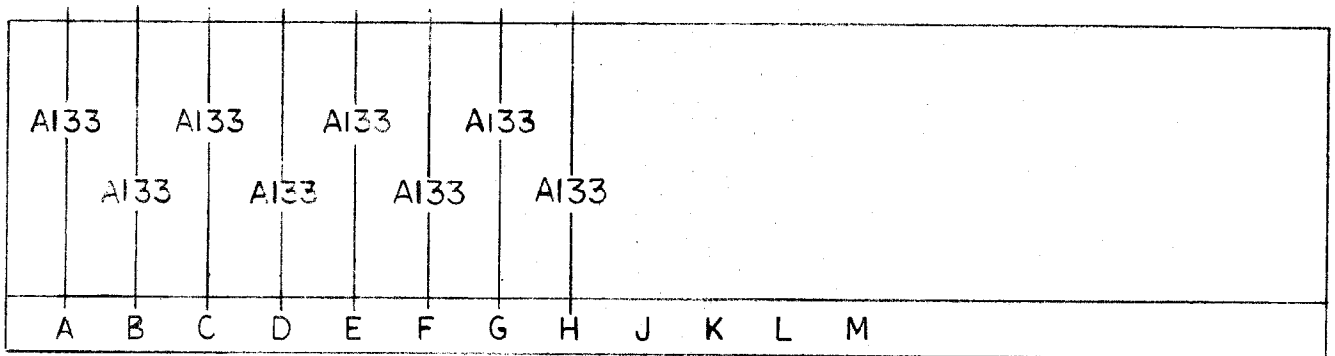


Fig. 2 (0227A2036-0) Outline and Mounting Dimensions for the DLA52D Relay



PLAN VIEW



FRONT VIEW
COVER REMOVED

Fig. 3 (0275A4581-0) Component Location Diagram for the DLA52D Relay

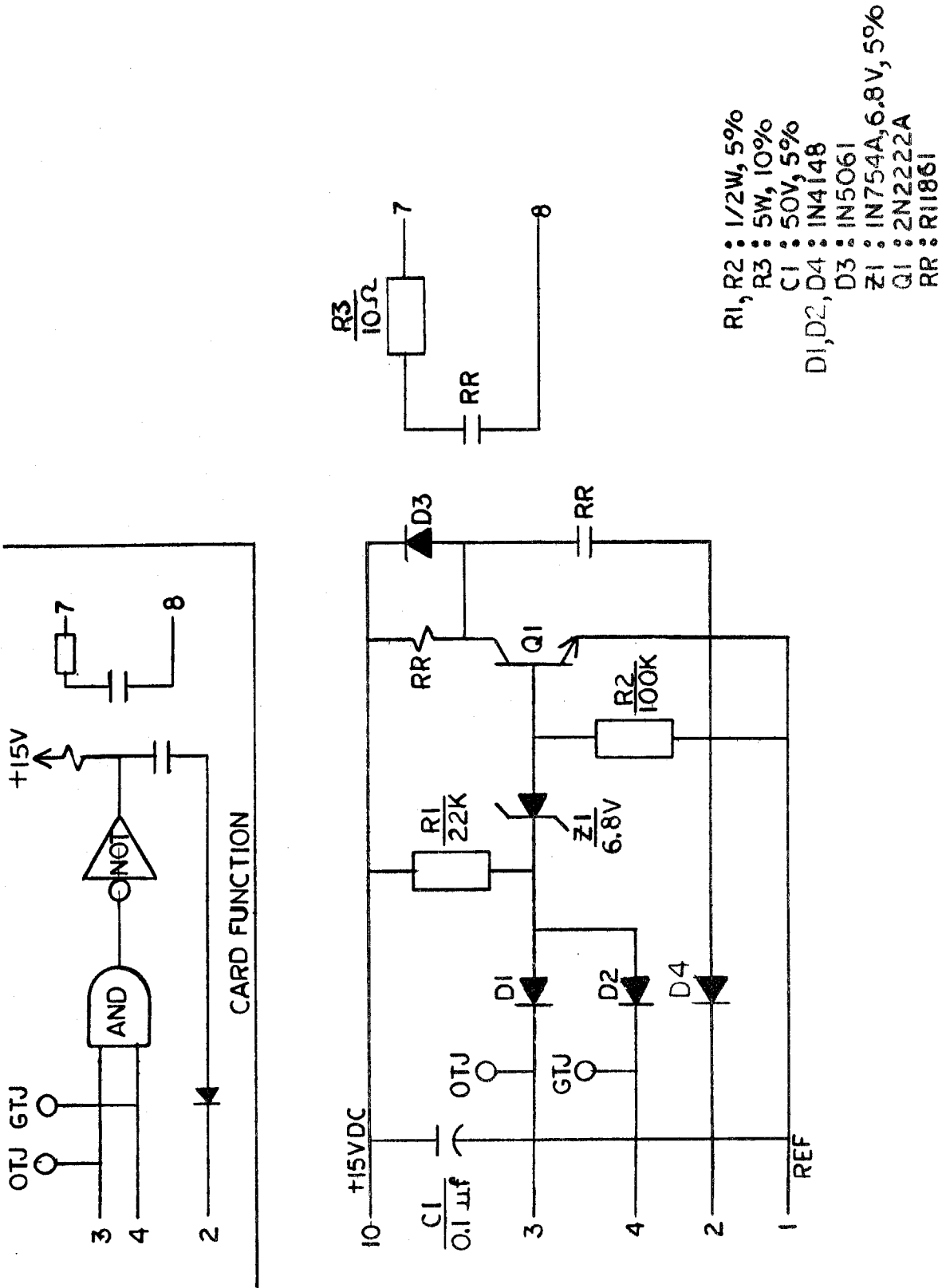


Fig. 4 (0148A3903PF-0) One Section of the DLA52D Circuitry.
 A133 Printed Circuit Card Internal

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