GE Motors & Industrial Systems

GATE DISTRIBUTION AND STATUS BOARD

DS200FCGD1A_ _

These instructions do not purport to cover all details or variations in equipment, nor to provide every possible contingency to be met during installation, operation, and maintenance. If further information is desired or if particular problems arise that are not covered sufficiently for the purchaser's purpose, the matter should be referred to GE Motors & Industrial Systems.

CONTENTS

SAFETY SYMBOL LEGEND

WARNING Indicates a procedure, practice, condition, or statement that, if not strictly observed, could result in personal injury or death.

CAUTION Indicates a procedure, practice, condition, or statement that, if not strictly observed, could result in damage to or destruction of equipment

NOTE Indicates an essential or important procedure, practice, condition, or statement.

FUNCTIONAL DESCRIPTION

INTRODUCTION

The Gate Distribution and Status Card (FCGD) is an interface board for a 6-pulse phase-controlled non-reversing bridge. It receives SCR firing information from the DS200DSPC (DSPC – the VME processor) board and returns feedback and diagnostic information via the VME backplane. The FCGD decodes and distributes cell gating signals for each bridge leg and receives a multiplexed cell status signals from each bridge leg. It also receives and scales bridge feedback signals then sends this voltage, frequency, and current status information back to the DSPC board.

The FCGD board is 6U VME size (9.2x6.3 inches), with six layers and surface-mounted devices (SMDs) on both sides. The FCGD mounts in the same VME rack that houses the Digital Signal Processing Card (DSPC).

BOARD FUNCTIONS

System Clock

To generate firing commands and time stamping feedback values, the FCGD has a **system clock register**. This is a 16-bit up-counter that rolls over to 0 when it reaches the hexadecimal number 0FFFFH.

LEM is a registered trademark of LEM USA Incorporated.

System Reset

The system reset signal sets all of the registers on the board to their initial values during power up or hardware resets.

System Heartbeat

The **heartbeat** is a periodic signal generated by an electronic component to announce that the component is still functional. The system heartbeat register on the FCGD supports this function. When written to by the VME host CPU the first time, the board-level heartbeat begins to count at the same rate as the system clock, and a green board-front LED labeled **IMOK** (I am okay) is lit.

If the number (≈ 8 msec) in the heartbeat register exceeds its design limit, the board front IMOK light and the gating are both turned off. A hard reset is required to exit this condition.

Firing Commands

The fiber-optic firing signal transmitters are controlled by a **firing mask register** containing six entries corresponding to the six cell strings in a bridge. The FCGD can turn-on up to six fiber-optic transmitters at one time. The contents of the firing mask register may be written directly by the host CPU over the VME bus connection.

Cell Status Feedback

The FCGD receives feedback signals through fiber-optic connections from three FGPA boards. The feedback consists of two sets of leg cell status signals plus the power supply status signals combined into a single 16-bit value. This information is stored in a cell status register.

Zero-crossing Time Detection

Three zero-crossing signals are developed in analog / digital hardware on the FCGD. Each of the three signals controls a digital latch. At each edge of a zero-crossing signal, the value of the system time clock is written into its respective 16-bit register.

VCO Feedback Count Accumulation

Eight voltage-controlled oscillator (VCO) signals are generated on the FCDG. Each of these signals feeds into a 16-bit up-counter. Upon receipt of a command from the VME host CPU the VCO accumulator values are written into eight registers. Also the value of the system time clock is written into the **feedback time register**.

Voltage Feedback From NATO

The FCGD accepts input signals from the Voltage Feedback Scaling (NATO) board over a 20-pin ribbon cable (see Table 5). These signals include five attenuated analog voltage signals which correspond to plus / minus dc, and three ac voltages all referenced to ground through a local resistor. The input range is rescaled using the jumpers on NATO to keep the resulting signals within the ± 10 V range of the signal electronics. Testpoints for the Va, Vb, Vc, Vp, and Vn signals are available on the VME backplane.

Current Feedback

Current feedback is provided by two Current Transformers (source side) or two LEM® modules (load side) located on phases A and C of the power bridge. Conditioning of the current signals yields IA, IB, and IC signals with IA and IC feeding VCO feedback circuits. The circuit minimizes offset drift over time and temperature. IA and IC current signals feed board-front testpoints.

Hardware Overcurrent

The three current signals, combined to form an IFB signal, drive a hardware overcurrent detector. The overcurrent level is set with potentiometer OC_SP on the front of the board (see Figure 2). The IFB signal is compared against this overcurrent level. If IFB is greater than the overcurrent setting for approximately 26 milliseconds, the FCGD causes an overcurrent signal that can only be cleared by a hardware reset.

The IFB signal level can be read at the board front testpoint (OCSP). The red LED lamp on the board front labeled **OC** indicates operation of the overcurrent protection when lighted.

The hardware overcurrent signal drives an open circuit bussed line on the P2 connector. There are separate bus lines from source and load FCGDs to a processor board (such as the DSPC) because load and source isolators do not necessarily have same sequencing. This signal is also used by the processor board for trip relay. On some processor boards, it is possible to select by means of a

jumper whether the relay or driver energizes or de-energizes when a fault condition occurs. This is necessary to satisfy the diverse fail-safe requirements of varying components.

Hardware Flux Calculation

Reconstructed flux signals (FBAR, FCBR, FACR) are generated in hardware. Though only two go through the VCO, all three are needed for the zero-crossing detection.

Analog/Digital Conditioning

Voltage controlled oscillators are used for analog feedback of voltage, current, and flux. The VA, VB, VC, VDC, IA, IC, FLUXBAR, FLUXCBR signals (see Table 1) drive the VCOs. The voltage and current signals also feed into six Sigma-Delta converters which operate in parallel with the VCOs.

Commutation Failure Signals

The hardware signals for detecting current in a leg are compared against the actual legs being asked to fire from the firing mask. Leg current should only be present during its gating interval plus the commutation overlap time. A commutation failure circuit checks that the leg current is not on during other parts of the cycle.

A load-side commutation circuit checks for a positive di/dt leg current after the end of its gating interval.

Both of these commutation circuits are combined for each leg and sent to the FPGA where they increment a counter. The software can read this counter for excessive time counts and take any necessary action. The goal is to detect and correct any problem within 15 degrees, thereby minimizing the effect on the dc link reactor and load. The counter is reset to zero on each new firing mask.

Groundfault Protection Signals

The groundfault detection function is implemented in software.

Difference Current Detection

The source-to-source or load-to-source current difference function is implemented in software.

Board Selftest

Most of the board functions can be tested on command from the VME host CPU. The selftests include loopback tests and the injection of test signals into analog signal paths.

APPLICATION DATA

CTLN1

Existing drive products have a 24 V dc hardware loop (CTLN1) to block gating of cells independent of the host CPU. These signals are translated into 5 V dc signal-level voltage and brought into the FCGD through bussed lines on the P2 VME connector (see Table 5). If 24 V dc on CTLN1 is not present firing is inhibited.

VME Bus Interface

The FCGD board is compatible with the VME (A24/D16) bus specification both electrically and physically. The FCGD environment consists of up to four FCGD boards and a VME bus host CPU. All bus signals are contained on the P1 connector and the board decodes most of the 24 address bits for internal addressing. The P2 connector is available as an I/O signal expansion path and as a means to connect signals between FCGD boards. The VME bus address of each FCGD board is set automatically using data provided through the pins on connector P2. If FCGD boards are relocated on the bus, each can discover its new address without operator intervention.

Hardware OC Setpoint Potentiometer

Set the overcurrent level manually for each FCGD board using potentiometer OC_SP on the board front (see Figure 2). If the position of a FCGD board in the VME rack is changed, its overcurrent level needs to be manually re-adjusted. Compute the OC_SP voltage level setpoint as follows:

T.L. – P.U. overcurrent **Trip** level
Im – Rated motor current
CT – CT primary (for 1 Amp secondary)
LEM – LEM primary (for 20 mA output)

Source-side : OC_SP = (T.L. * 1.2825 * Im * 0.6)/CT

Load-side : OC_SP = (T.L. * 1.2825 * Im * 0.605)/LEM

Table 1. Testpoints

Name	Nomenclature	Description
TP1	VDC	Bridge DC link voltage – attenuated
TP4	VBA	Bridge line-to-line voltage feedback – attenuated & scaled
TP5	VCB	Bridge line-to-line voltage feedback – attenuated & scaled
TP6	VAC	Bridge line-to-line voltage feedback – attenuated & scaled
TP7	FBAR	Scaled, reconstructed flux. 4.75 V = 1 P.U.
TP8	FCBR	Scaled, reconstructed flux. 4.75 V = 1 P.U.
TP9	FACR	Scaled, reconstructed flux. 4.75 V = 1 P.U.
TP11	IFB	Pseudo -dc link current – unscaled
TP12	OC_SP	Overcurrent setpoint (26 msec filter) – compared to IFB
TP19	IA	Phase line current feedback – scaled. 3 V pk = 1 P.U.
TP20	IC	Phase line current feedback – scaled. 3 V pk = 1 P.U.
TP21	0FC1	0 = fire cells in leg 1
TP27	ACOM	Analog signal common (ground)
TP33	0FC3	0 = fire cells in leg 2
TP35	0FC5	0 = fire cells in leg 3

Table 2. Fiber-optic Connectors

Name (Color)	Nomenclature	Description
U56 (Blue)	STAT1 IN	FIber-optic receiver; cell status feedback from FGPA board
U57 (Blue)	STAT2 IN	FIber-optic receiver; cell status feedback from FGPA board
U67 (Blue)	STAT3 IN	FIber-optic receiver; cell status feedback from FGPA board
U71 – U76 (Gray)	LEG1 – 6	Fiber-optic transmitters; firing signals to FGPA board

Table 3. LED Functions

Name	Nomenclature	Description
DS1	OC FLT	Red LED indicates when lighted that overcurrent protection is active
DS2	IMOK(T) ACTIVE	Green LED indicates when lighted that board is functional

Table 4. Removable Programmable Parts

Name	Nomenclature	Description
U7	EPROM	Serial configuration XC17256D

Table 5. Onboard Connectors

Name	Description
P1	96-pin board-edge connector. See ***ANSI/VITA 1-1994*** manual for details on VME interfacing.
P2	96-pin board-edge connector. Used to set board VME address and for I/O signal routing.
TSTP1	Connector for 20-pin ribbon cable. **Not intended for customer use.**
TSTP2	Connector for 20-pin ribbon cable. **Not intended for customer use.**

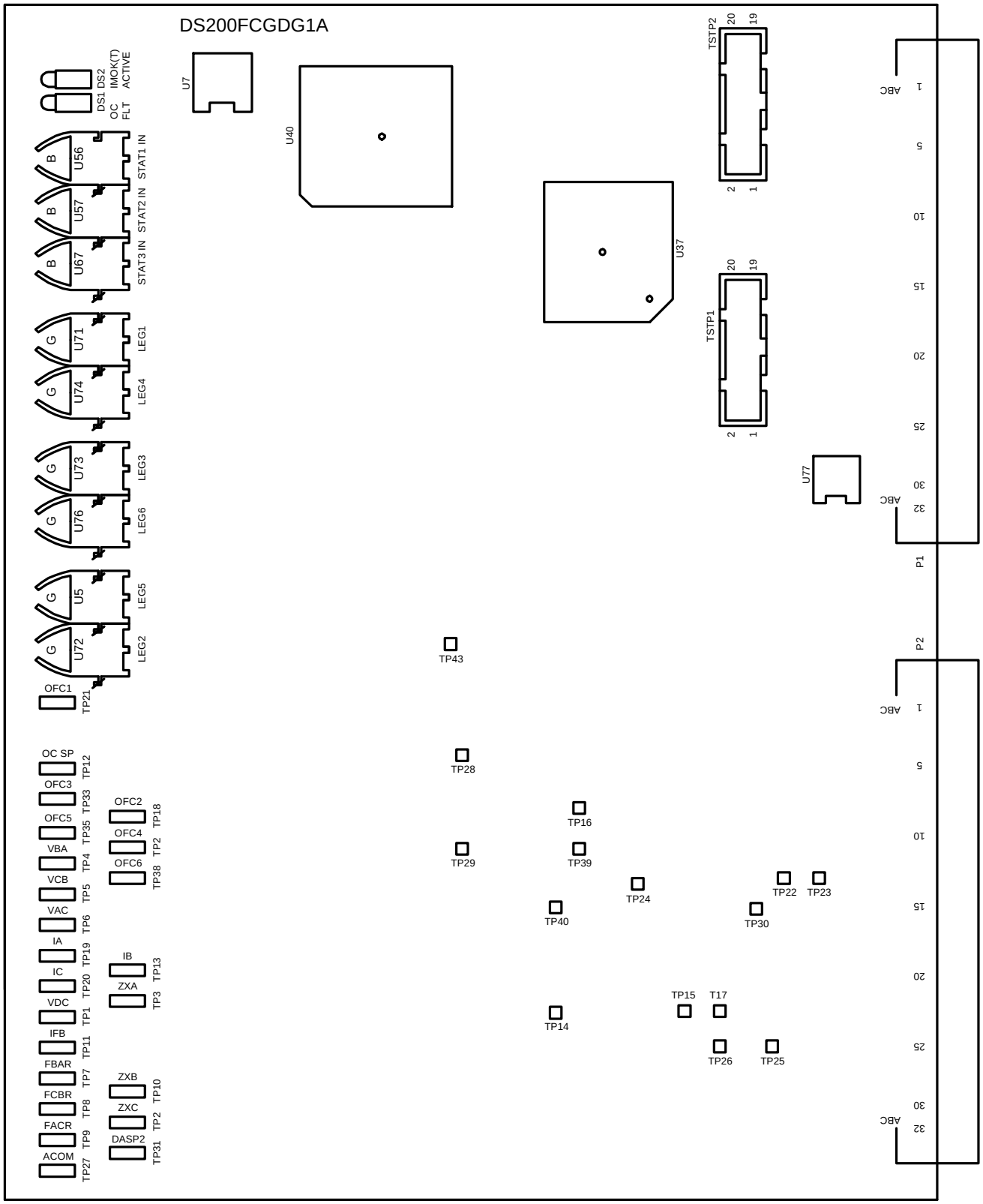

Figure 1. FCGD Board Layout

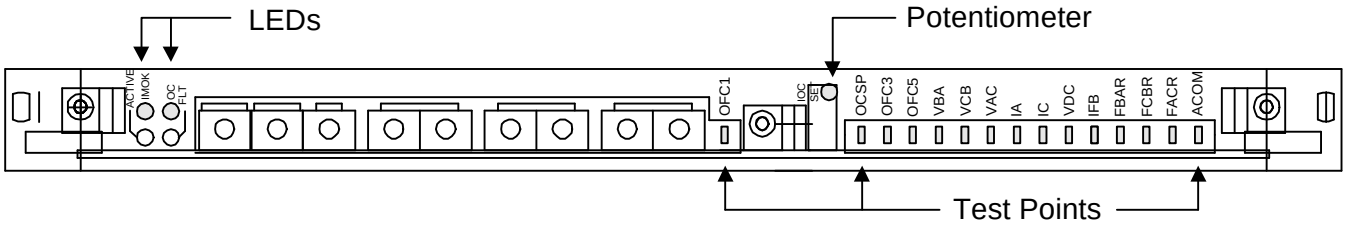

Figure 2. FCGD Board Front Panel

RENEWAL/WARRANTY REPLACEMENT

NOTE

All digits are important when ordering or replacing any board.

BOARD IDENTIFICATION

A printed wiring board is identified by an alphanumeric part (catalog) number stamped on its edge. For example, the FCGD is identified by part number DS200FCGDG#. Figure 3 describes each digit in the part number.

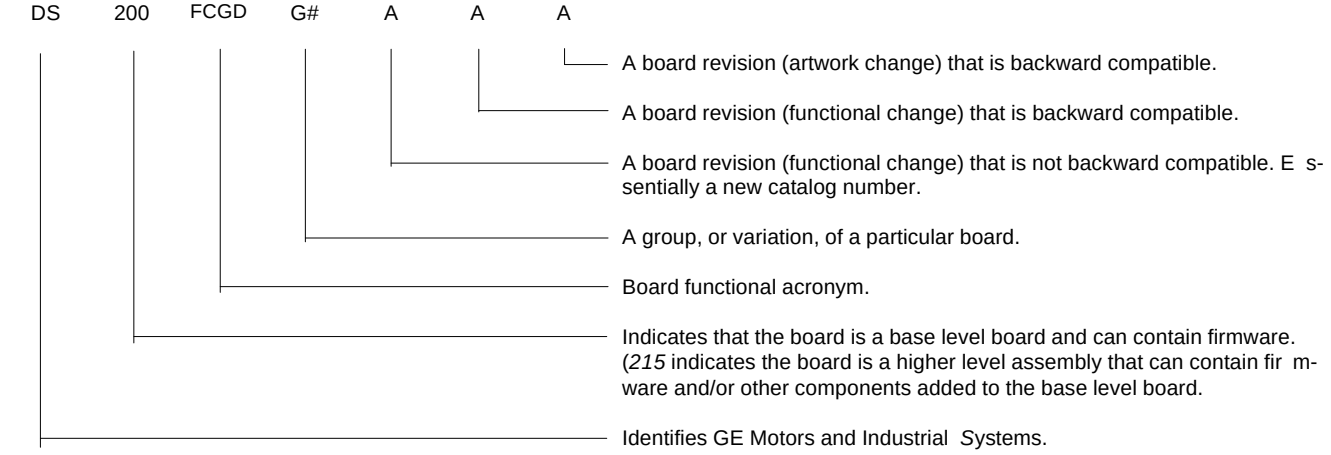

Figure 3. Sample Board Part Number, DS Series

WARRANTY TERMS

The GE Motors & Industrial Systems Terms and Conditions brochure details product warranty information, including the **warranty period** and **parts and service** coverage.

The brochure is included with customer documentation. It may also be obtained separately from the nearest GE Sales Office or authorized GE Sales Representative.

WARRANTY PARTS AND SERVICE

This board has no fuses or other end-user serviceable parts. If it fails, it needs to be replaced as a unit.

To obtain a replacement board, or service assistance, contact the nearest GE Service Office. Please have the following information ready to exactly identify the **part** and **application**:

- GE requisition or shop order number
- LCI serial number and model number
- Board number and description

PROCEDURE FOR REPLACING BOARDS

WARNING

To prevent electric shock, turn off power to the board, then test to verify that no power exists in the board before touching it or any connected circuits.

CAUTION

To prevent equipment damage, do not remove boards or connections, or re-insert them, while power is applied to the drive.

Treat all boards as static-sensitive. Use a grounding strap when changing boards and always store boards in anti-static bags or boxes they were shipped in.

To replace an FCGD board:

1. **Turn off power**.
2. To remove the FCGD board, carefully disconnect all cables, as follows:
   – For fiber-optic connectors, press the latch on the mating cable connector. Pull the connector only; do not pull the fiber-optic cable.
3. Install the new FCGD board.
4. Reconnect all cables, ensuring that each connector is properly seated at both ends.

NOTE

Because of upgrades, boards of different revision levels may not contain identical hardware. However, GE Motors & Industrial Systems ensures backward compatibility of replacement boards.

Notes:

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