TYPE CS28A CHECKBACK (MASTER) PL-19D436449G1

Schematic 19D436450

The Master Checkback module produces the keying pulses, timing sequences, display lights and alarms to check and monitor the carrier system, either manually or automatically. Up to three "remotes" may be checked for full and reduced power by the Master module. In special applications requiring testing of more than three remotes (up to six), the equipment can be programmed to check some or all remotes in either the full power or the reduced power mode. See the SPECIAL APPLICATION section which follows. The counter can be strapped to count the number of good tests or the number of failed tests. The counter may also be strapped to count only (1) full power or (2) full power and reduced power tests. Automatic checkback cycles are programmable from 1 hour to 255 hours in 1 hour intervals. Automatic retest cycles may be programmed for from 0 to 17 minutes delay.

A full power alarm relay and a reduced power alarm relay are provided with Form "C" contacts. Alarm lights on the front panel of the module identify which remote failed and whether it was a full or reduced power failure. Provision is made (by built-in relays) for remotely initiating a test, resetting alarms and resetting the program clock or, alternately, disabling the checkback, disabling remote #1 alarms, and disabling remote #2 alarms.

Also, a checkback test may be manually initiated at any remote location, but only when the Master module is not in the test mode (interrogating the remotes).

OPERATION

The entire interrogation and response sequence takes place in a nine (9) second interval. A master clock divides the total interval into nine (9) individual one second periods with the first period for master interrogation (8 pulses @ 16 Hz in 1/2 sec.) of the entire system. Then it "listens" during periods 2, 3, and 4 for each remote's respective response on full power. It interrogates again in period 5 (different code; 4 pulses @ 16 Hz in 1/4 sec.) and similarly waits for the sequential response of each remote in periods 6, 7 and 8 on reduced power. During clock period 9, the clock and alarms are reset and the entire interrogation/response sequence is ready to repeat as programmed by "dip" switch S1 on the module. The timing of the nine intervals is controlled by counter U12 which, when activated produces nine sequenced outputs at one second intervals.

Refer to the Schematic Diagram located in this section of this manual. The 32,768 Hz frequency at the output of the crystal oscillator AR1 is divided down to 16 Hz at Pin 15 of counter U1 and down to 1 Hz at Pin 6 of counter U2. At Pin 3 of counter U3, the frequency has been counted down to 1 Hz per hour. Programmable counters U5 and U6 set the automatic test output at Pin 3 of U6 in hour steps from 1 to 255 hours. Switch S1 is used to program the counters in straight binary. Examples are given in Table I.

The checkback test sequence may be initiated in several ways, namely:

- Automatically, by the local master programmed clock (U6).
- Automatically, by the retest timer (U30)
- Manually, by depressing the Manual Test Switch on the front panel at either the master or remote locations.
- By energizing the remote test relay coil (K4) at the master station.

When initiated U78 sets, Pin 13 switches positive and applies a 1 to the Data Input of Flip-Flop U7A, and switches AR3-A positive lighting the 'TEST' LED (D10). This inhibits AR3-B, C & D, on the next positive edge of the 1 Hz clock. Flip-Flop U7A sets and Pin 2 of U7A switches to 0 and applies a 0 to NOR gate U8D, Pin 13. This allows a 1 Hz clock signal to be applied to counter U12, Pin 14 through inverter U8A and NOR gate U8D. On the first count U12-Q1 (Pin 2) switches to 1. This sets Flip-Flop U10A and Pin 1 of U10A switches to 1. NOR gate U9A switches to 0 allowing the 16 Hz clock to be

TABLE I

TYPICAL TEST INTERVALS (Switch S1 Settings)

TEST INTERVAL	SWITCH POSITION 1 1Hr	2 2Hr	3 4Hr	4 8Hr	5 16Hr	6 32Hr	7 64Hr	8 128Hr
1 Hour		C						
2 Hours			C					
4 Hours				C				
8 Hours					C			
12 Hours			C	C				
24 Hours (1 Day)				C	C			
48 Hours (2 Days)					C	C		
72 hours (3 Days)				C			C	
168 Hours (1 Week)				C		C		C
240 Hours (10 Days)					C	C	C	C
255 Hours (max.)	C	C	C	C	C	C	C	C

C = SWITCH CLOSED WITH OTHERS OPEN

gated through NOR gate U9B to the STOP output. With jumper K in the 1-2 position, the START output is switched ON through inverters U9B and C by Flip-Flop U10A. With jumper K in the 2-3 position, the START output is switched ON each time the STOP is switched OFF. Counter U11 counts the output pulses (16 Hz) at the STOP output. When the count reaches 8, Flip-Flop U10 is reset by a 1 output from U11, Pin 11. Counter U11 is also reset by NOR gate U9A.

These 8 pulses at a 16 Hz rate from the Master Checkback Module are recognized at the remote Checkback Modules as a command to switch to the test mode.

Flip-Flop U21A is set on the second 1 Hz clock period and U12 switches to a 1 on Q2 (Pin 4), the full power alarm light is turned ON for remote #1, and the 1 is applied to Pin 1 of NAND gate U20A. Remote #1 must send back 8 pulses at a 16 Hz rate during this clock period. These input pulses switch AR2. The output of AR2 is connected to bandpass filter AR4-A and transistor switch Q5. As the pulses are received, Q5 causes the alarm lights to flash at a 16 Hz rate.

The 16 Hz pulses are detected by AR4-D and applied to the clock input of counter U16 through inverter AR4-B. Timing circuit AR4-C is switched LOW by the first pulse and allows U16 to count the pulses. If a pulse is delayed or missing, AR4-C will switch positive, resetting counter U16. This prevents random pulses from counting up to the desired number. When counter U16 reaches 8, Pin 9 switches to a 1, setting Flip-Flop U17-B. This starts counter U19 and when it reaches its predetermined count, Pin 1 momentarily switches to a 1 and this switches NAND gate U20-A to 0 and inverter U20-B to 1, resetting Flip-Flop U21A and turning OFF alarm light #1.

If an additional pulse had been received, AR4-D would have reset U17A, which in turn would have reset U18 before an output was produced. If the 8 pulses are not received within the second period of the 1 Hz clock, Flip-Flop U21A is left set and full power alarm light #1 is left ON.

The sequence described above is repeated for remotes 2 and 3 in the 3rd and 4th 1 Hz clock periods. At the start of 1 Hz clock period 5, Q5 (Pin 1) of U12 switches to a 1, setting Flip-Flop U10B. NOR gate U9A switches to 0, allowing the 16 Hz clock to be gated through NOR gate U9B to the STOP output. When U11 counts up to 4, Pin 1 switches to a

1, resetting Flip-Flop U10B. REDUCED POWER was switched ON when U10B was set and the START output was held OFF by U10A. The 4 pulses from the Master command the remotes to switch to reduced power and return 4 pulses in their respective time slots.

At the start of 1 Hz clock period 6, Q6 (Pin 5) of U12 switches to a 1, setting Flip-Flop U25A, turning ON the reduced power alarm light for remote #1, and applying the 1 to Pin 1 of NAND gate U24A. During this clock period, remote #1 must send back 4 pulses at a 16 Hz rate. The four input pulses are detected as explained above for the eight pulses, except counter U16 sets Flip-Flop U17A and counter U18 is started and, when its count is reached, it applies a 1 to Pin 2 of U24A. This causes a 1 to be applied to Pin 4 of U25A, resetting that Flip-Flop and turning OFF reduced power alarm light #1. The circuits for the reduced power alarms are identical to the full power alarm circuits. The sequence described above is repeated for remotes 2 and 3, in the 7th and 8th 1 Hz clock periods. If any of the remotes (1, 2, or 3) do not exist, the appropriate segments of switch SS are closed to prevent an alarm.

During 1 Hz clock period 9, Pin 11 of U12 switches to a 1, resetting Flip-Flop U7B and preventing Flip-Flop U7A from resetting. U7B switches AR3-A OFF, turning the test light OFF and removing the inhibit from AR3-B & D. If any of the alarms are ON at the end of the test, AR3-D (for full power) or AR3-C (for reduced power) are switched OFF. The output of AR3-D or AR3-C is connected to Test Failure counters U27 and U28 respectively through U26A and U26B. The output from U27 or U28 caused by the first (or second) test failure will start timer U30. When U30 counts to the output selected by jumper 'G' its output will reset the alarm lights and restart the Checkback cycle. After a failure of three test cycles U29C or U29D will turn off transistor Q3 or Q4, de-energizing alarm relay K1 or K2 and closing the alarm contacts. If either AR3-C or AR3-D are switched OFF (Jumper L to 2-3), NAND gate U13C switches to a 1, which applies a reset to Flip-Flop U7A & B (Jumper M connected to 1-2), preventing the unit from going into the test mode until the alarms have been cleared. Under normal conditions Flip-Flop U7A is reset at the beginning of the 1 Hz clock period 10.

If counter (M1) is strapped to count good tests (Jumper B to 1-2), NAND gate U13B remains at 0 during period 9 (if no alarms are ON) and the 1 output from Pin 11 of U12 is switched through to the counter. An alarm causes U13B to switch to a 1 during period 9 and this blocks the pulse at U13D. Connecting jumper B to 2-3 permits each failed test to be counted, since each time U13B switches to a 1 the counter is advanced one count. If jumper L is connected to 1-2, the reduced power tests are also included in the count. Jumper M connected to 1-2 latches the checkback in a "no-test" mode until the alarms are reset.

The automatic timing sequence is started by operating CLOCK RESET switch S2. When this switch is operated, a test is started and the test will automatically be repeated in the number of hours programmed into the clock by switch S1.

A test may be manually initiated at any time, without affecting the automatic timing, by operating MANUAL TEST switch S3. When a test is not in progress, the Master Checkback will recognize the 4 pulse at 16 Hz as a command to switch into the test mode. The output of 4 pulse detector U18, Pin 1, is OR connected by diode CR33 into the test start circuit.

A positive voltage applied to Pin 8 of the checkback disables the output, and therefore stops any test in progress and resets all circuits. It also prevents the unit from switching to the test mode.

SPECIAL APPLICATIONS

Although the Checkback system was designed for a maximum of four stations (one Master and three Remotes) situations may arise where it is desirable to test more than four equipments in a line section or over a system of multiple line sections. In the normal configuration the second through fourth test time slots of the Master Checkback are used for receiving Full Power signals of eight pulses from each of three remote checkbacks, and time slots six through eight (6-8) are used to receive

REDUCED POWER signals of four pulses from each of the same three remote checkbacks.

The number of stations tested can be increased beyond three (to four, five or six) by having some (or all) remote checkbacks respond in only one time slot rather than two as shown in Table II.

One Checkback system can be used on two or more adjacent line sections by connecting the interposing stations in a 'repeater' configuration as shown in the diagram below.

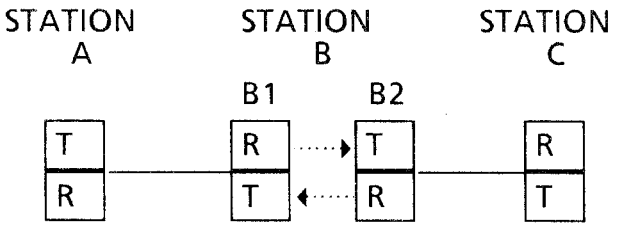
TABLE II

	FULL POWER			REDUCED POWER		
Alarm Indicator	1	2	3	1	2	3
Time Slot	2	3	4	6	7	8
	RESPONDING STATION					
Normal (3 remotes)	#1	#2	#3	#1	#2	#3
4 Remotes	#1	#2	#3†	#1	#2	#4††
5 Remotes	#1	#2†	#3†	#1	#4††	#5††
6 Remotes	#1	#2†	#3†	#4††	#5††	#6††

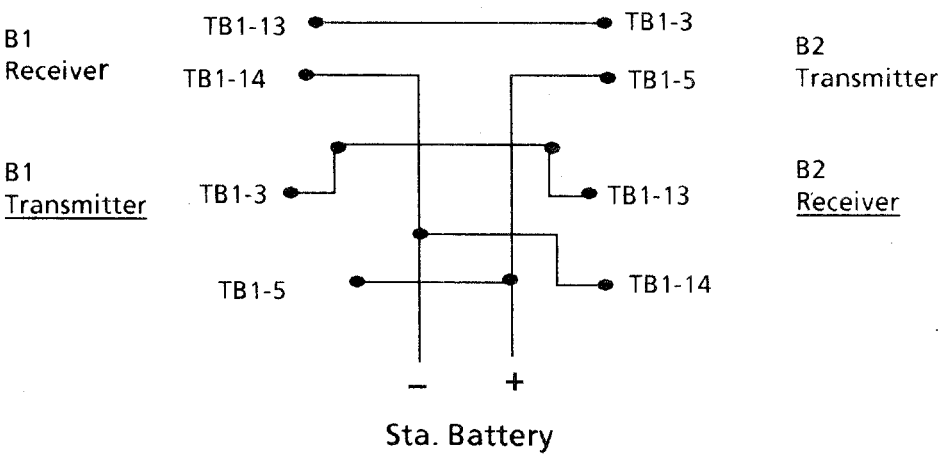
† Remote strapped for FULL POWER response only.

†† Remote strapped for REDUCED POWER response only. See Remote Checkback module description for strapping

In this example the signals from a Master Checkback at station A will be received at station B ,and repeated to station C. Station B1 will respond in its assigned time slot and will repeat the signals of the stations B2 and station C in their assigned time slots. In case of an alarm, the alarm lights at the Master will indicate which remote station (B1, B2, or C), failed to respond.



Connections at Station B:



Sta. Battery

Note that the transmitters must be strapped for STOP priority to assure proper functioning during operation of the protective relays.

NOMINAL OPERATING CHARACTERISTICS

1. Power Requirements:

   +12 VDC, 95 mA
   −12 VDC, 95 mA

2. Outputs:
   Stop, Start and Reduced Power:

   a) OFF: −6 VDC
   b) ON: +6 VDC

3. Inputs:
   a) Checkback Disable:

   (1) OFF: −6 VDC
   (2) ON: +6 VDC

   b) Receive Input:

   (1) OFF: Open Circuit
   (2) ON: Connect to Common

4. Remote Controls:
   Clock Reset, Test and ALarm Reset

   a) ON: 30 - 150V
   b) OFF: 0 VDC

5. Oscillator Frequency (TP1):

   32,768 Hz

6. Pulse Frequency (TP2 - During Test):

   16 Hz

7. Time Slots:

   1 sec.

CHECKBACK MASTER TEST POINT READINGS

TP1	Square wave	32.768 Hz
	Amplitude approx.	15. V pk. to pk.
TP2	Square wave	16 Hz
	Amplitude approx.	15. V pk. to pk.
TP3	Square wave	1 Hz
	Amplitude approx.	15. V pk. to pk.

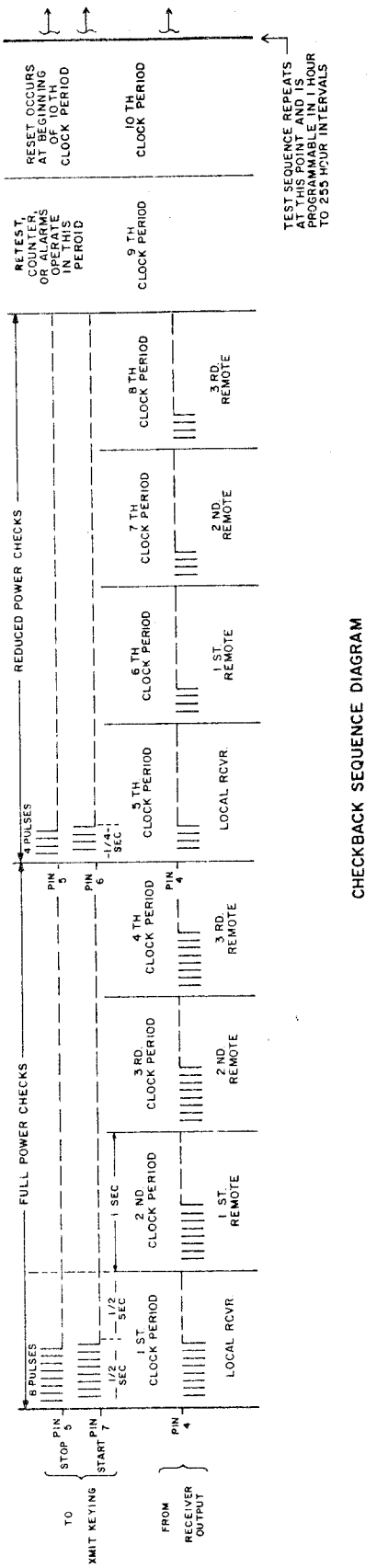


Figure 1 (19D426755-2) Master Checkback Sequence Diagram

ITEM NO.	IDENTIFICATION NUMBER	DESCRIPTION	GROUP NUMBER AND QUANTITY 1	2	3	4	5
AR1	19A134379P001	LIN. OP-AMP RCA CA3130T	1				
AR2	19A116297P002	INT CKT, SC8273G1 BI	1				
AR3	0246A9351P224	OP. AMP. LM224	1				
AR4	19A116297P005	INT CKT LM248	1				
C1	19A116080P101	CAP 0.01 50VDC 10%	1				
C2	19A116080P107	CAP 0.1 50VDC 10%	1				
C3	19A134202P007	CAP 2.2 UF 20V 20% TANT	1				
C4	19A134202P115	CAP 6.8UF 35V 10% TANT	1				
C6	19C300075P68001G	CAP 68KPF 2% 100VDC	1				
C7	19A134202P015	CAP 6.8UF 35V 20% TANT	1				
C8	19A116080P107	CAP 0.1 50VDC 10%	1				
C9	19A116080P107	CAP 0.1 50VDC 10%	1				
C10	19A116080P107	CAP 0.1 50VDC 10%	1				
C11	19A116080P114	CAP .0033 50VDC 10%	1				
C12	0246A9036P222	CAP .0022UF 50V 5% POLY	1				
C13	19A116080P101	CAP 0.01 50VDC 10%	1				
C15	19C300075P68001G	CAP 68KPF 2% 100VDC	1				
C16	19A116080P107	CAP 0.1 50VDC 10%	1				
C17	19A134202P014	CAP 1.UF 35V 20% TANT	1				
C20	0246A9036P103	CAP .01UF 50V 5% POLY	1				
C21	0246A9036P103	CAP .01UF 50V 5% POLY	1				
C22	0246A9036P103	CAP .01UF 50V 5% POLY	1				
C23	0246A9036P103	CAP .01UF 50V 5% POLY	1				
C24	0246A9036P103	CAP .01UF 50V 5% POLY	1				
C25	0246A9036P103	CAP .01UF 50V 5% POLY	1				
C26	0246A9036P103	CAP .01UF 50V 5% POLY	1				
C27	0246A9036P103	CAP .01UF 50V 5% POLY	1				
C28	0246A9036P103	CAP .01UF 50V 5% POLY	1				
C29	0246A9036P103	CAP .01UF 50V 5% POLY	1				
C30	0246A9036P103	CAP .01UF 50V 5% POLY	1				
C31	0246A9036P103	CAP .01UF 50V 5% POLY	1				
C32	0246A9036P103	CAP .01UF 50V 5% POLY	1				
C33	0246A9036P103	CAP .01UF 50V 5% POLY	1				
C34	0246A9036P103	CAP .01UF 50V 5% POLY	1				
C35	0246A9036P103	CAP .01UF 50V 5% POLY	1				
C36	0246A9036P103	CAP .01UF 50V 5% POLY	1				
C37	0246A9036P103	CAP .01UF 50V 5% POLY	1				
C38	0246A9036P103	CAP .01UF 50V 5% POLY	1				
C39	0246A9036P103	CAP .01UF 50V 5% POLY	1				
C40	0246A9036P103	CAP .01UF 50V 5% POLY	1				
C41	0246A9036P103	CAP .01UF 50V 5% POLY	1				
C42	0246A9036P103	CAP .01UF 50V 5% POLY	1				
C43	0246A9036P103	CAP .01UF 50V 5% POLY	1				
C44	0246A9036P103	CAP .01UF 50V 5% POLY	1				
C45	0246A9036P103	CAP .01UF 50V 5% POLY	1				
C46	0246A9036P103	CAP .01UF 50V 5% POLY	1				
C47	0246A9036P103	CAP .01UF 50V 5% POLY	1				
C48	0246A9036P103	CAP .01UF 50V 5% POLY	1				
C49	0246A9036P103	CAP .01UF 50V 5% POLY	1				
C50	0246A9036P103	CAP .01UF 50V 5% POLY	1				
C51	0246A9036P103	CAP .01UF 50V 5% POLY	1				
C84	0246A9032P271	CAP 270 PFD MICA	1				
C85	0246A9032P271	CAP 270 PFD MICA	1				
D1	0246A9401P4148	DIODE JAN 1N4148	1				
D2	0246A9401P4148	DIODE JAN 1N4148	1				
D3	0246A9401P4148	DIODE JAN 1N4148	1				
D4	0246A9401P4148	DIODE JAN 1N4148	1				
D5	0246A9401P4148	DIODE JAN 1N4148	1				
D6	0246A9401P4148	DIODE JAN 1N4148	1				
D7	0246A9401P4148	DIODE JAN 1N4148	1				
D8	0246A9401P4148	DIODE JAN 1N4148	1				
D9	0246A9401P4148	DIODE JAN 1N4148	1				
D10	0246A9958P001	RED LED 12V LEDCO 4100-2	1				
D11	0246A9401P4148	DIODE JAN 1N4148	1				
D12	0246A9401P4148	DIODE JAN 1N4148	1				
D13	0246A9401P4148	DIODE JAN 1N4148	1				
D14	0246A9401P4148	DIODE JAN 1N4148	1				
D15	0246A9401P4148	DIODE JAN 1N4148	1				
D16	0246A9401P4148	DIODE JAN 1N4148	1				
D17	0246A9958P001	RED LED 12V LEDCO 4100-2	1				

Figure 2 (19D436449 G1 [3]) Master Checkback Parts List

ITEM NO.	IDENTIFICATION NUMBER	DESCRIPTION	GROUP NUMBER AND QUANTITY 1	2	3	4	5
D18	0246A9401P4148	DIODE JAN 1N4148	1				
D19	0246A9401P4148	DIODE JAN 1N4148	1				
D20	0246A9958P001	RED LED 12V LEDCO 4100-2	1				
D21	0246A9401P4148	DIODE JAN 1N4148	1				
D22	0246A9401P4148	DIODE JAN 1N4148	1				
D23	0246A9958P001	RED LED 12V LEDCO 4100-2	1				
D24	0246A9401P4148	DIODE JAN 1N4148	1				
D25	0246A9401P4148	DIODE JAN 1N4148	1				
D26	0246A9958P001	RED LED 12V LEDCO 4100-2	1				
D27	0246A9401P4148	DIODE JAN 1N4148	1				
D28	0246A9401P4148	DIODE JAN 1N4148	1				
D29	0246A9958P001	RED LED 12V LEDCO 4100-2	1				
D30	0246A9401P4148	DIODE JAN 1N4148	1				
D31	0246A9401P4148	DIODE JAN 1N4148	1				
D32	0246A9958P001	RED LED 12V LEDCO 4100-2	1				
D33	0246A9401P4148	DIODE JAN 1N4148	1				
D34	0246A9401P4148	DIODE JAN 1N4148	1				
D35	0246A9401P4148	DIODE JAN 1N4148	1				
D36	0246A9401P4148	DIODE JAN 1N4148	1				
D37	0246A9401P4148	DIODE JAN 1N4148	1				
D38	0246A9401P4148	DIODE JAN 1N4148	1				
D39	0246A9401P4148	DIODE JAN 1N4148	1				
D40	0246A9401P4148	DIODE JAN 1N4148	1				
D41	0246A9401P4148	DIODE JAN 1N4148	1				
D42	0246A9401P4148	DIODE JAN 1N4148	1				
D43	0246A9401P4148	DIODE JAN 1N4148	1				
D44	0246A9401P4148	DIODE JAN 1N4148	1				
D45	0246A9401P4148	DIODE JAN 1N4148	1				
D47	0246A9401P4148	DIODE JAN 1N4148	1				
D48	0246A9401P4148	DIODE JAN 1N4148	1				
D50	0246A9401P4148	DIODE JAN 1N4148	1				
D51	0246A9401P4148	DIODE JAN 1N4148	1				
D52	0246A9401P4148	DIODE JAN 1N4148	1				
D53	0246A9401P4148	DIODE JAN 1N4148	1				
D54	0246A9401P4148	DIODE JAN 1N4148	1				
D55	0246A9401P4148	DIODE JAN 1N4148	1				
D56	0246A9401P4148	DIODE JAN 1N4148	1				
D57	0246A9401P4148	DIODE JAN 1N4148	1				
D58	0246A9401P4148	DIODE JAN 1N4148	1				
D59	0246A9401P4148	DIODE JAN 1N4148	1				
D60	0246A9401P4148	DIODE JAN 1N4148	1				
D61	0246A9401P4148	DIODE JAN 1N4148	1				
D62	0246A9401P4148	DIODE JAN 1N4148	1				
D63	0246A9401P4148	DIODE JAN 1N4148	1				
D68	0246A9401P4148	DIODE JAN 1N4148	1				
D69	0246A9401P4148	DIODE JAN 1N4148	1				
D70	0246A9401P4148	DIODE JAN 1N4148	1				
D71	0246A9401P4148	DIODE JAN 1N4148	1				
D72	0246A9401P4148	DIODE JAN 1N4148	1				
D73	0246A9401P4148	DIODE JAN 1N4148	1				
D74	0246A9401P4148	DIODE JAN 1N4148	1				
D76	0246A9401P4148	DIODE JAN 1N4148	1				
D80	0246A9401P4148	DIODE JAN 1N4148	1				
D81	0246A9401P4148	DIODE JAN 1N4148	1				
D82	0246A9401P4148	DIODE JAN 1N4148	1				
D83	0246A9401P4148	DIODE JAN 1N4148	1				
D84	0246A9401P4148	DIODE JAN 1N4148	1				
D85	0246A9401P4148	DIODE JAN 1N4148	1				
D86	0246A9401P4148	DIODE JAN 1N4148	1				
D87	0246A9401P4148	DIODE JAN 1N4148	1				
D88	0246A9401P4148	DIODE JAN 1N4148	1				
D89	0246A9401P4148	DIODE JAN 1N4148	1				
D90	0246A9401P4148	DIODE JAN 1N4148	1				
D91	0246A9401P4148	DIODE JAN 1N4148	1				
K1	19B209439P003	REL MERC. 24V 1 FORM C	1				
K2	19B209439P003	REL MERC. 24V 1 FORM C	1				
K3	0367A0602G001	COIL	1				
K4	0367A0602G001	COIL	1				
K5	0367A0602G001	COIL	1				
M1	19A144612P002	COUNT ELEC 5 DIGIT 24VDC	1				

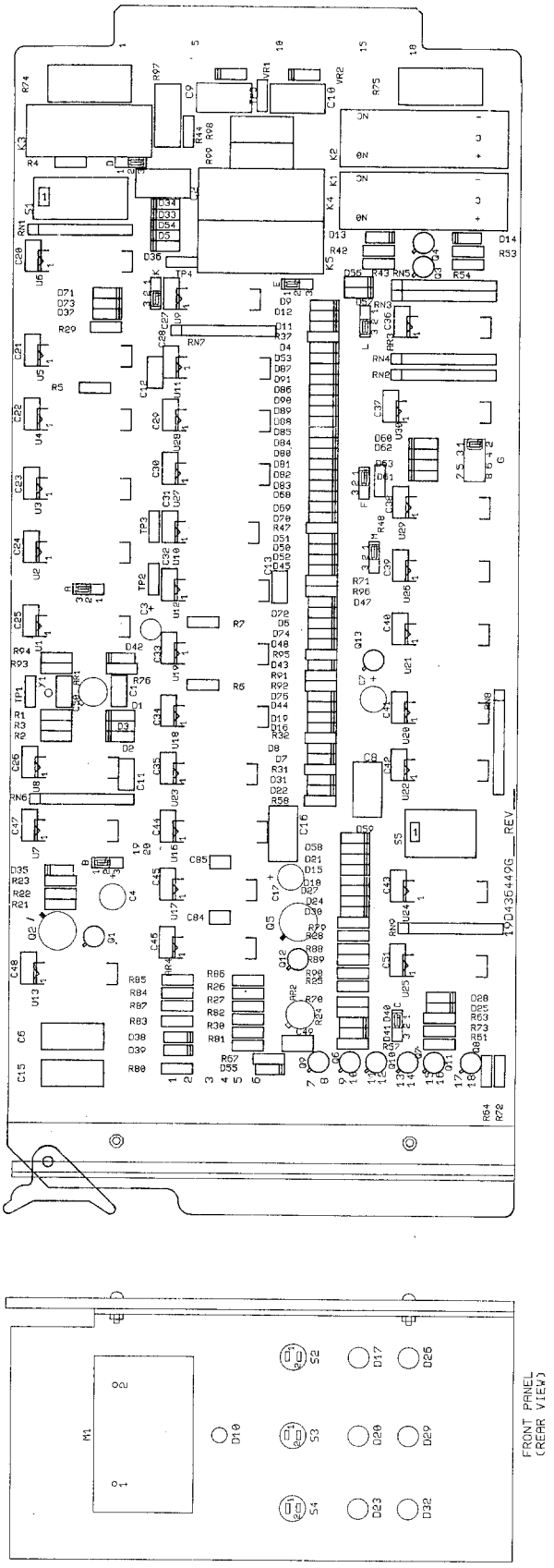
Figure 2 (19D436449 G1 [3]) Master Checkback Parts List

ITEM NO.	IDENTIFICATION NUMBER	DESCRIPTION	GROUP NUMBER AND QUANTITY 1	2	3	4	5
Q1	19A116755P001	NPN TRANS 2N3947	1				
Q2	19A115300P002	TSTR NPN 60V 2N3053	1				
Q3	19A116755P001	NPN TRANS 2N3947	3				
Q4	19A116755P001	NPN TRANS 2N3947	1				
Q5	19A115300P002	TSTR NPN 60V 2N3053	1				
Q6	0246A9214P3251	2N3251 TRANSISTOR BI	1				
Q7	0246A9214P3251	2N3251 TRANSISTOR BI	1				
Q8	0246A9214P3251	2N3251 TRANSISTOR BI	1				
Q9	0246A9214P3251	2N3251 TRANSISTOR BI	1				
Q10	0246A9214P3251	2N3251 TRANSISTOR BI	1				
Q11	0246A9214P3251	2N3251 TRANSISTOR BI	1				
Q12	19A116755P001	NPN TRANS 2N3947	1				
Q13	0246A9214P3251	2N3251 TRANSISTOR BI	1				
R1	0246A9134P3013	RES 301KOHM 1/4W 1% MTL	1				
R2	0246A9134P3013	RES 301KOHM 1/4W 1% MTL	1				
R3	0246A9134P1002	RES 10K OHM 1/4W 1% MTL	1				
R4	0246A9134P1002	RES 10K OHM 1/4W 1% MTL	1				
R5	0246A9134P1003	RES 100K OHM 1/4W 1% MTL	1				
R21	0246A9105P103	RES 10K OHM 1/4W 5% CRN	1				
R22	0246A9105P104	RES 100K OHM 1/4W 5% CRN	1				
R23	0246A9134P10R0	RES 10 OHM 1/4W 1% MTL	1				
R24	0246A9134P5492	RES 54.9K 1/4W 1%	1				
R25	0246A9134P1003	RES 100K OHM 1/4W 1% MTL	1				
R26	0246A9134P4022	RES 40.2KOHM 1/4W 1% MTL	1				
R27	0246A9134P1003	RES 100K OHM 1/4W 1% MTL	1				
R28	0246A9134P5111	RES 5.11KOHM 1/4W 1% MTL	1				
R29	0246A9134P1002	RES 10K OHM 1/4W 1% MTL	1				
R30	0246A9134P1473	RES 147K OHM 1/4W 1% MTL	1				
R31	0246A9134P1002	RES 10K OHM 1/4W 1% MTL	1				
R32	0246A9134P1002	RES 10K OHM 1/4W 1% MTL	1				
R37	0246A9134P1001	RES 1K OHM 1/4W 1% MTL	1				
R42	0246A9105P473	RES 47K OHM 1/4W 5% CRN	1				
R43	0246A9105P103	RES 10K OHM 1/4W 5% CRN	1				
R44	0246A9105P102	RES 1K OHM 1/4W 5% CRN	1				
R47	0246A9134P1003	RES 100K OHM 1/4W 1% MTL	1				
R48	0246A9134P1002	RES 10K OHM 1/4W 1% MTL	1				
R53	0246A9105P473	RES 47K OHM 1/4W 5% CRN	1				
R54	0246A9105P103	RES 10K OHM 1/4W 5% CRN	1				
R57	0246A9134P1001	RES 1K OHM 1/4W 1% MTL	1				
R58	0246A9134P3013	RES 301KOHM 1/4W 1% MTL	1				
R61	0246A9134P1001	RES 1K OHM 1/4W 1% MTL	1				
R63	0246A9134P3013	RES 301KOHM 1/4W 1% MTL	1				
R64	0246A9134P1001	RES 1K OHM 1/4W 1% MTL	1				
R67	0246A9134P1001	RES 1K OHM 1/4W 1% MTL	1				
R70	0246A9134P1001	RES 1K OHM 1/4W 1% MTL	1				
R71	0246A9134P1002	RES 10K OHM 1/4W 1% MTL	1				
R72	0246A9134P1002	RES 10K OHM 1/4W 1% MTL	1				
R73	0246A9134P1001	RES 1K OHM 1/4W 1% MTL	1				
R74	19A116479P2560K	RES 56 OHM 10% 2W FLPRF	1				
R75	19A116479P2560K	RES 56 OHM 10% 2W FLPRF	1				
R76	0246A9134P3013	RES 301KOHM 1/4W 1% MTL	1				
R79	0246A9134P1501	RES 1.5K OHM 1/4W 1% MTL	1				
R80	0246A9134P1001	RES 1K OHM 1/4W 1% MTL	1				
R81	0246A9134P1001	RES 1K OHM 1/4W 1% MTL	1				
R82	0246A9134P1473	RES 147K OHM 1/4W 1% MTL	1				
R83	0246A9134P2943	RES 294K OHM 1/4W 1% MTL	1				
R84	0246A9134P1003	RES 100K OHM 1/4W 1% MTL	1				
R85	0246A9134P1743	RES 174K OHM 1/4W 1% MTL	1				
R86	0246A9134P2370	RES 237 OHM 1/4W 1%	1				
R87	0246A9134P1001	RES 1K OHM 1/4W 1% MTL	1				
R88	0246A9134P1001	RES 1K OHM 1/4W 1% MTL	1				
R89	0246A9134P1002	RES 10K OHM 1/4W 1% MTL	1				
R90	0246A9134P1503	RES 150K OHM 1/4W 1% MTL	1				
R91	0246A9134P1002	RES 10K OHM 1/4W 1% MTL	1				
R92	0246A9134P5112	RES 51.1KOHM 1/4W 1% MTL	1				
R93	0246A9134P5901	RES 5.9K OHM 1/4W 1% MTL	1				
R94	0246A9134P1001	RES 1K OHM 1/4W 1% MTL	1				
R95	0246A9134P1003	RES 100K OHM 1/4W 1% MTL	1				
R96	0246A9134P5112	RES 51.1KOHM 1/4W 1% MTL	1				
R97	0246A9103P203	RES.CARC 5% .1W 20K	1				

Figure 2 (19D436449 G1 [3]) Master Checkback Parts List

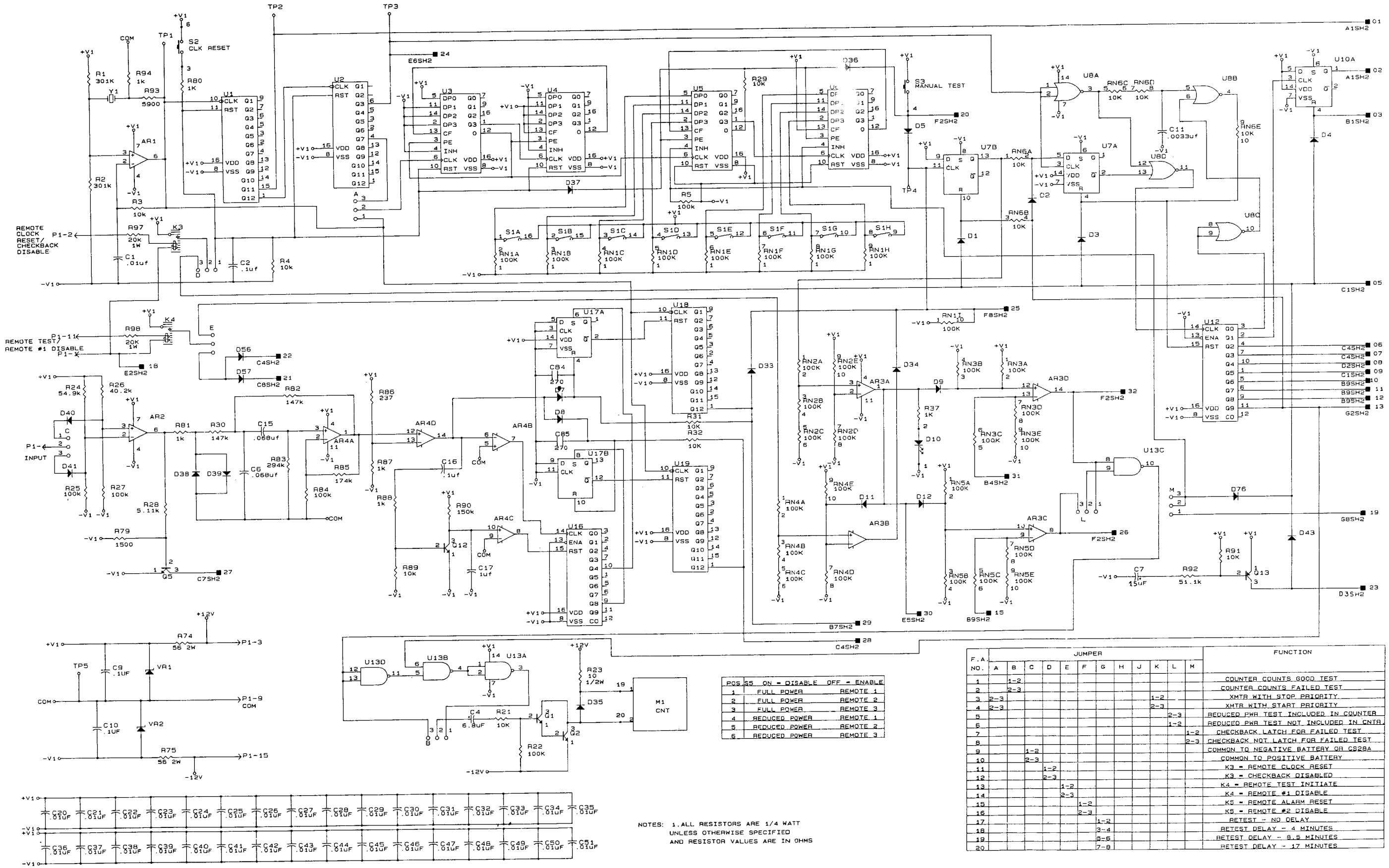
ITEM NO.	IDENTIFICATION NUMBER	DESCRIPTION	GROUP NUMBER AND QUANTITY 1	2	3	4	5
R98	0246A9103P203	RES.CARC 5% ,1W 20K	1				
R99	0246A9103P203	RES.CARC 5% ,1W 20K	1				
RN1	0246A9132P104C	RESNET 10-PIN 9X100K 2%	1				
RN2	0246A9133P104C	RESNET 10-PIN 5X100K 2%	1				
RN3	0246A9133P104C	RESNET 10-PIN 5X100K 2%	1				
RN4	0246A9133P104C	RESNET 10-PIN 5X100K 2%	1				
RN5	0246A9133P104C	RESNET 10-PIN 5X100K 2%	1				
RN6	0246A9133P103C	RESNET 10-PIN 5X10K 2%	1				
RN7	0246A9133P103C	RESNET 10-PIN 5X10K 2%	1				
RN8	0246A9133P103C	RESNET 10-PIN 5X10K 2%	1				
RN9	0246A9133P103C	RESNET 10-PIN 5X10K 2%	1				
S1	0246A9957P003	DIP SWITCH	1				
S2	7481654P006	SW,PUSH,SPNO,RED	1				
S5	0246A9957P002	DIP SWITCH	1				
U1	0246A9502P4040	I.C. 4040 CMOS	1				
U2	0246A9502P4040	I.C. 4040 CMOS	1				
U3	0246A9502P4526	I.C. 4526 CMOS	1				
U4	0246A9502P4526	I.C. 4526 CMOS	1				
U5	0246A9502P4526	I.C. 4526 CMOS	1				
U6	0246A9502P4526	I.C. 4526 CMOS	1				
U7	0246A9502P4013	I.C. 4013 CMOS	1				
U8	0246A9502P4001	I.C. 4001 CMOS	1				
U9	0246A9502P4001	I.C. 4001 CMOS	1				
U10	0246A9502P4013	I.C. 4013 CMOS	1				
U11	0246A9502P4017	I.C. 4017 CMOS	1				
U12	0246A9502P4017	I.C. 4017 CMOS	1				
U13	0246A9502P4011	I.C. 4011 CMOS	1				
U16	0246A9502P4017	I.C. 4017 CMOS	1				
U17	0246A9502P4013	I.C. 4013 CMOS	1				
U18	0246A9502P4040	I.C. 4040 CMOS	1				
U19	0246A9502P4040	I.C. 4040 CMOS	1				
U20	0246A9502P4011	I.C. 4011 CMOS	1				
U21	0246A9502P4013	I.C. 4013 CMOS	1				
U22	0246A9502P4011	I.C. 4011 CMOS	1				
U23	0246A9502P4013	I.C. 4013 CMOS	1				
U24	0246A9502P4011	I.C. 4011 CMOS	1				
U25	0246A9502P4013	I.C. 4013 CMOS	1				
U26	0246A9502P4011	I.C. 4011 CMOS	1				
U27	0246A9502P4017	I.C. 4017 CMOS	1				
U28	0246A9502P4017	I.C. 4017 CMOS	1				
U29	0246A9502P4011	I.C. 4011 CMOS	1				
U30	0246A9502P4040	I.C. 4040 CMOS	1				
VR1	0246A9403P6R2	ZENER 6.2V 5% 400MW	1				
VR2	0246A9403P6R2	ZENER 6.2V 5% 400MW	1				
Y1	19A701383P001	XTAL 32.768 KHZ	1				

Figure 2 (19D436449 G1 [3]) Master Checkback Parts List



* Figure 3 (19D436449 Sh.1 [4]) Master Checkback Outline

* Revised since last issue

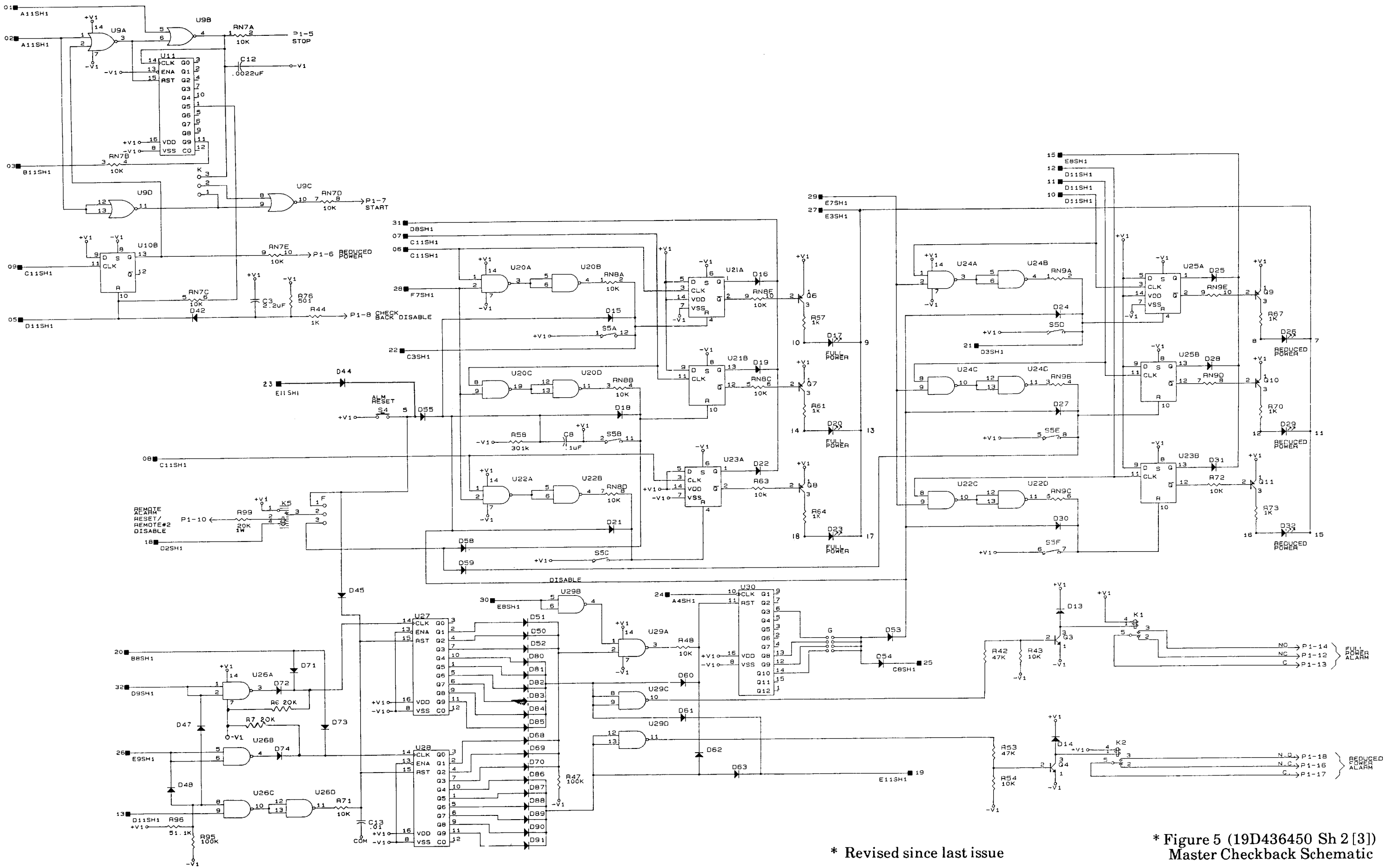


POS	S5 ON = DISABLE	OFF = ENABLE
1	FULL POWER	REMOTE 1
2	FULL POWER	REMOTE 2
3	FULL POWER	REMOTE 3
4	REDUCED POWER	REMOTE 1
5	REDUCED POWER	REMOTE 2
6	REDUCED POWER	REMOTE 3

F.A. NO.	JUMPER A	B	C	D	E	F	G	H	J	K	L	M	FUNCTION
1		1-2											COUNTER COUNTS GOOD TEST
2		2-3											COUNTER COUNTS FAILED TEST
3	2-3									1-2			XMTR WITH STOP PRIORITY
4	2-3									2-3			XMTR WITH START PRIORITY
5												2-3	REDUCED PWR TEST INCLUDED IN COUNTER
6												1-2	REDUCED PWR TEST NOT INCLUDED IN CNTR
7												1-2	CHECKBACK LATCH FOR FAILED TEST
8												2-3	CHECKBACK NOT LATCH FOR FAILED TEST
9		1-2											COMMON TO NEGATIVE BATTERY OR CS28A
10		2-3											COMMON TO POSITIVE BATTERY
11			1-2										K3 = REMOTE CLOCK RESET
12			2-3										K3 = CHECKBACK DISABLED
13				1-2									K4 = REMOTE TEST INITIATE
14				2-3									K4 = REMOTE #1 DISABLE
15					1-2								K5 = REMOTE ALARM RESET
16					2-3								K5 = REMOTE #2 DISABLE
17						1-2							RETEST - NO DELAY
18						3-4							RETEST DELAY - 4 MINUTES
19						5-6							RETEST DELAY - 8.5 MINUTES
20						7-8							RETEST DELAY - 17 MINUTES

* Revised since last issue

* Figure 4 (19D436450 Sh 1 [2])
Master Checkback Schematic



* Revised since last issue

* Figure 5 (19D436450 Sh 2 [3])
Master Checkback Schematic