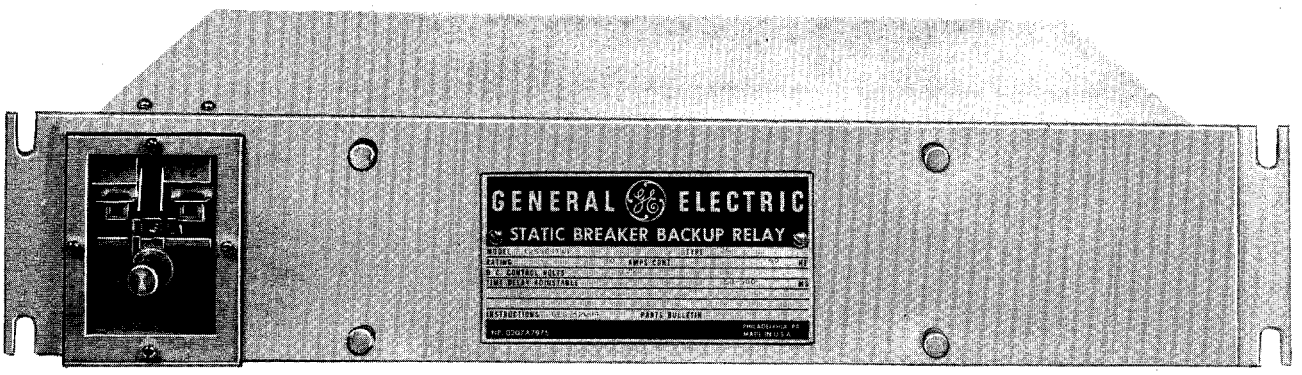
INSTRUCTIONS

GEK-42004

STATIC BREAKER BACKUP RELAY

TYPE SBC41A



POWER SYSTEMS MANAGEMENT DEPARTMENT

GENERAL ELECTRIC

PHILADELPHIA, PA.

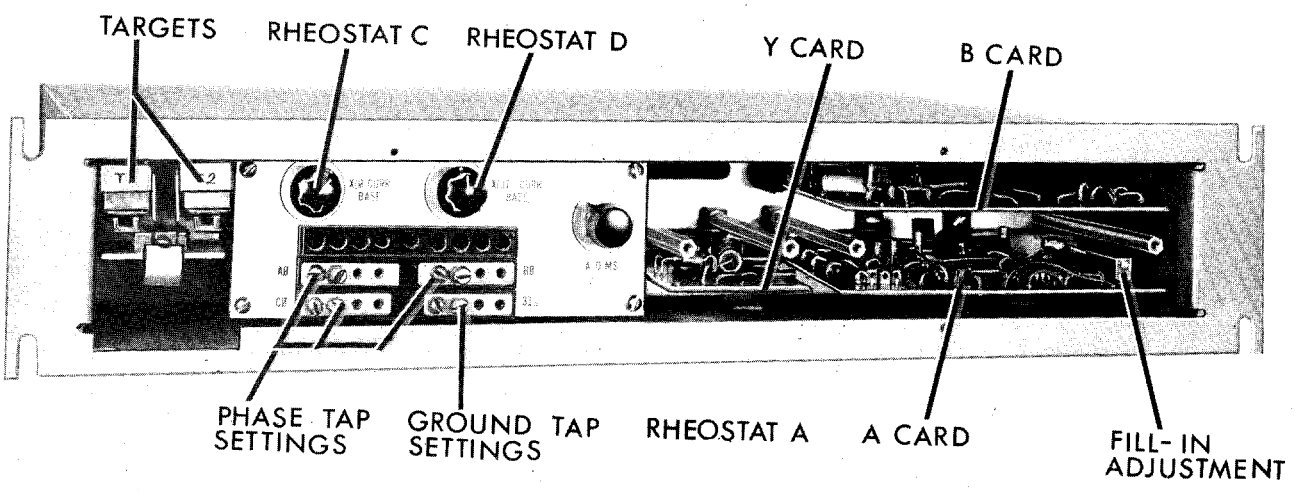


FIG. 1 (8042531) TYPE SBC41A RELAY, FRONT COVER PLATE REMOVED (FRONT VIEW)

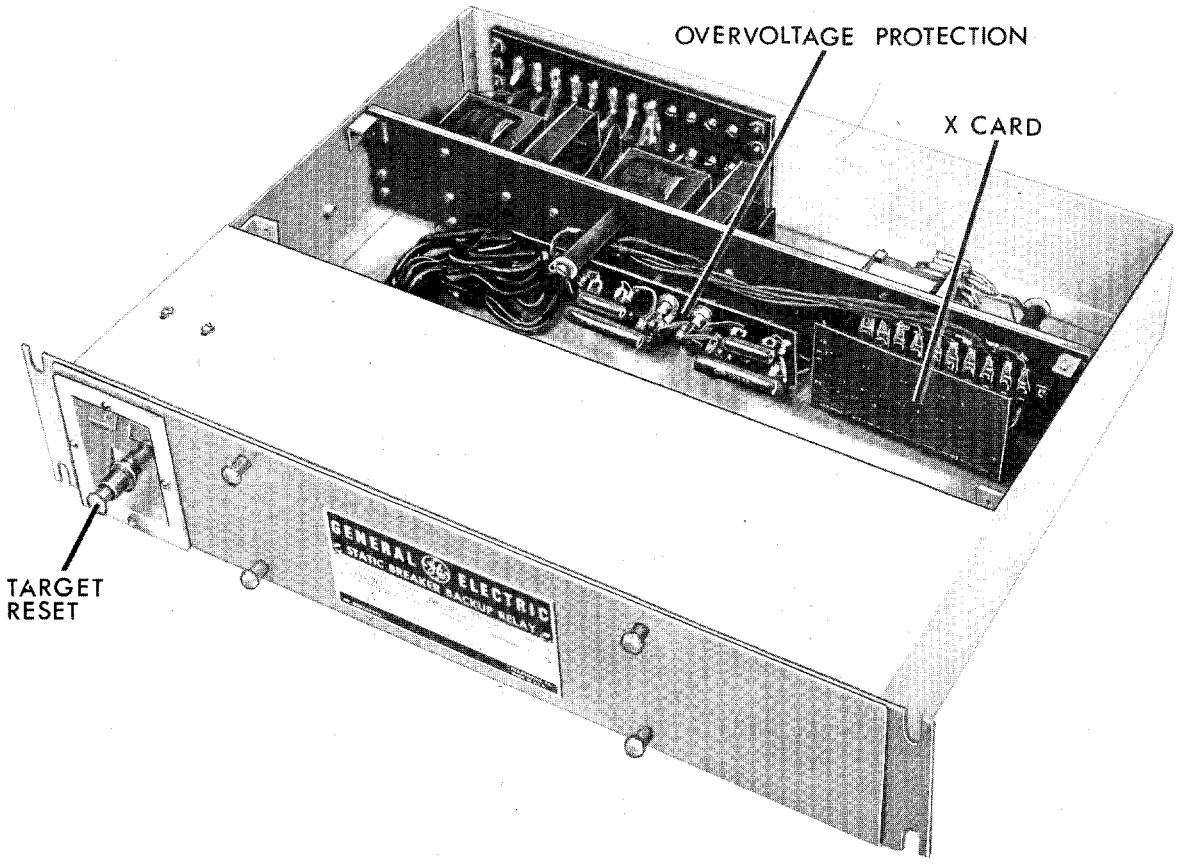


FIG. 2 (8042532) TYPE SBC41A RELAY, TOP COVER PLATE REMOVED (ELEVATED 3/4 VIEW)

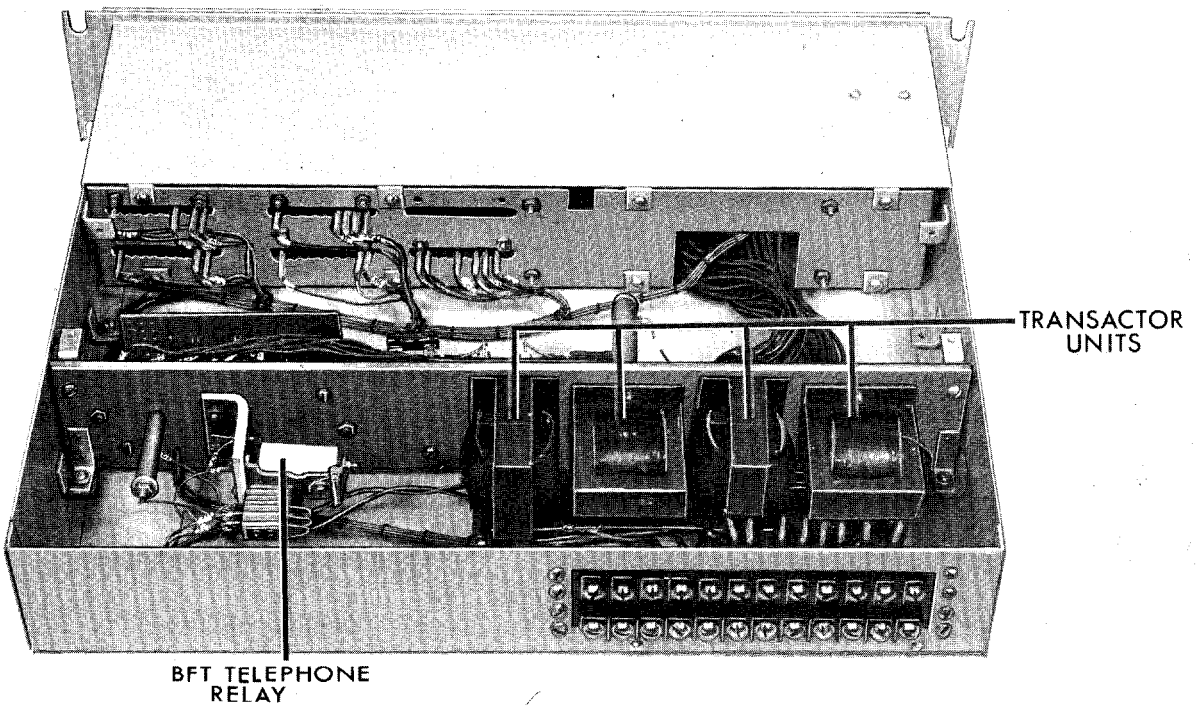


FIG. 3 (8042534) TYPE SBC41A RELAY, TOP COVER PLATE REMOVED (ELEVATED REAR VIEW)

CONTENTS

COVER (8042529) TYPE SBC41A RELAY (FRONT VIEW)

INTRODUCTION

The type SBC41A1 relay is a rack mounted static breaker failure relay designed to provide system backup protection in the event of a circuit breaker failure.

This relay incorporates the major requirements of a breaker failure backup scheme-high Security and Capability for fast closing times. This relay is applicable with any of the several bus/breaker arrangements in general use today; and over a wide range of fault current conditions which may be encountered. One type SBC41A1 relay is required for each breaker in a bus array.

DESCRIPTION

The SBC41A1 relay is mounted in a rack unit. The test facilities are mounted in a separate rack unit and can be connected at the back of the relay with the help of a tap block. The SBC41A1 relay has the following components and features.

1. Input provisions for a contact initiation (BFI, 62X, 62Y) that activates the power supply and the relay.

2. A fast reset current detector with two independently adjustable pickup settings for phase (IA, IB, IC) and ground ((3I0) currents.

3. An adjustable timer to provide time for the primary breaker to operate correctly.

4. Three electrically separate contact output circuits (BFT) with two circuits having electromechanical series targets for tripping the back-up breakers.

5. A regulated power supply.

6. Surge suppression on all AC and DC input circuits.

APPLICATION

The type SBC41 static breaker failure relay is intended for application on a per breaker basis. That is, there is one breaker failure relay associated with each breaker in a bus array. On this basis the current inputs to a particular SBC41 relay must come from CT's that measure the current in the associated breaker. The trip outputs must be routed to initiate the tripping (or transferred tripping) of all breakers necessary to clear the fault upon failure of the breaker associated with the SBC41 relay. This routing will depend upon the bus breaker arrangement. The listing in Table 1 covers the bus arrangements that are in common use today. They are the single bus-single breaker, double bus-double breaker, breaker-and-a-half, and ring bus arrangement; and they are shown in Figures 23,24,25,26 respectively. Each listing in Table 1 indicates the assumed fault location, the breaker which is assumed to have failed, the contact initiation indicates the assumed fault location, the breaker which is assumed to have failed, the contact initiation that activates the SBC41, and which breakers or lockout relays should be tripped by the BFT contacts. For example, in a single-bus-single breaker arrangement (figure 23), if breaker #2 is to be protected, the SBC41 relay receives the currents associated with breaker #2. The contact initiation is from the protective relays of line B. If breaker #2 fails for a fault at F1, the SBC41 relay operates and BFT contact #1 trips the bus lockout relay. For another example consider the ring bus arrangement that is shown in Figure 26. If breaker 1 is to be protected the SBC41 relay receives the currents associated with breaker 1. The contact initiation is from the protective relays of line A for a fault at F1. For a fault at F2 the protective relays of line B provide the contact initiation. Assuming breaker 1 fails for a fault at F1, the SBC41 relay operates and the BFT contacts trip the following; BFT #1 trips breaker 2 and BFT #2 trips breaker 6. BFT #3 trips the lockout relay that transfer trips breakers 7 and 8 and blocks reclosing of 2 and 6.

In the application of the SBC41 relay probably the most important consideration is the setting of the main timer. Figure 5 illustrates all the times involved from the instant the fault occours until the backup circuit breakers operate to clear the fault. This total time must be short enough to enable the system to maintain stability and to limit as much as possible the damage to the faulted equipment. On the other hand, it should be long enough to permit a long enough setting on the breaker failure timer to insure the security of the scheme for normal conditions where the primary circuit breaker clears the fault.

In general, it is a good practice to set the SBC41 timer so that the overall time of operation (including the pick-up time of the current detector and the operating time of the BFT output relay) provides for ample margin without infringing on stability limit in the event of a breaker failure. The IEEE Relay Committee recommends at least 3 cycles of MARGIN.

It is apparent from Figure 5 that for any given total operating time of the SBC41, reducing the dropout time of the current detector will increase the margin. Thus, it is recommended for applications where margins of less than 3 cycles are contemplated that dropout times be reduced by reducing the setting of the fill-in timer of the current detector. The reduction in dropout time must be compatible with the acceptable minimum pick-up of the current detector. (See Figure 6).

The settings of the current detector should be such that they will operate at a level of at least 1.5 times pick-up for any fault for which breaker failure back up is intended to operate. It should be recognized that the function of the current detector is to establish whether or not current is flowing in the associated circuit breaker. In this sense the most sensitive setting is desirable. However, if the settings are such that the current detector is picked up on load, the security of the scheme is reduced since any error in testing etc., that applies dc to the relay could result in any undesired trip out.

Another factor in the selection of a pick-up setting for the current detector is the type of circuit breaker involved. Some circuit breakers insert resistors in the circuit when clearing a fault. This resistor current is maintained for a significant time and may have a substantial magnitude. For such applications the pick-up setting of the current detector should be coordinated with the main timer setting to insure that this resistor current does not result in a false trip. Note that the drop out to pick up ratio of the current detector in all these relays is higher than 95 percent.

Under normal conditions all the SBC41 relays do not have dc applied. Thus, during these periods they are free of all surge problems. DC is applied via BFI or 62X functions only when a fault occurs on a line associated with the breaker being protected.

TABLE I

BUS AND BREAKER ARRANGEMENT	FIG. #	FAULT LOC.	FAILED BREAKER	CURRENT FROM ASSOC. BREAKER	CONTACT INITIATION FROM	BFT CONTACT #1 TRIPS	BFT CONTACT #2 TRIPS	BFT CONTACT #3 TRIPS
Single Bus-Single Bkr.	23	F1	2	2	Line B	Bus Lockout Relay	-	-
Double Bus-Double Bkr.	24	F1 or F2	3	3	Line B or North Bus	North Bus Lock Out Relay	Brkr 4	Lockout relay that transfer trip line B & blocks reclosing of 4
Double Bus-Double Bkr.	24	F1 or F3	4	4	Line B or South Bus	South Bus Lock Out Relay	Brkr 3	Lockout relay that transfer trips line B & blocks reclosing of 3
Breaker and a half	25	F1 or F3	4	4	Line A or North Bus	North Bus Lock Out Relay	Brkr 5	Lockout relay that transfer trips 10 & blocks reclosing of 5
Breaker and a half	25	F1 or F2	5	5	Line A or Line B	Breaker 4	Brkr 6	Lockout Relay that transfer trips brkrs. 10 & 11 & blocks reclosing of 4 & 6.
Breaker and a half	25	F2 or F4	6	6	Line A or Line B	South Bus Lock Out Relay	Brkr 5	Lockout relay that transfer trips 11 & blocks reclosing of 5

(CONTINUED)

TABLE I

BUS AND BREAKER ARRANGEMENT	FIG. #	FAULT LOC.	FAILED BREAKER	CURRENT FROM ASSOC. BREAKER	CONTACT INITIATION FROM	BFT CONTACT #1 TRIPS	BFT CONTACT #2 TRIPS	BFT CONTACT #3 TRIPS
Ring Bus	26	F1 or F2	1	1	Line A or Line B	Breaker 2	Brkr 6	Lockout relay that transfer trips brkrs. 7 & 8 & blocks reclosing of 2 & 6

SBC41A1

This relay model operates in the following manner: When the power supply is activated the level detector produces an output that energizes the A/O timer. If the timer is energized longer than its setting, it indicates that the primary breaker has failed to clear the fault. The pick-up (A) of the timer should be set long enough to give the breaker a chance to trip but short enough to ensure system stability and maximum continuity of service by operating faster than remote second zone relays. Once the A/O timer operates it energizes a transistor switch (TS) that in turn picks up BFT. If the primary breakers had cleared the fault then both the contact initiation (BFI, 62X, 62Y) and the level detector would have dropped out before the timer could have timed out and no back up tripping would take place.

RANGES

I Phase Currents

A. Pickup current is continuously adjustable from 1 to 10 amperes on any phase by means of tap adjustments and a rheostat.

B. Tap Ranges:

1A - 2A)
2A - 4A) See figure 2 for tap selections
4A - 10A)

II Ground Current

A. Pickup current is continuously adjustable from 0.5 to 5 amperes by means of a tap adjustment and a rheostat.

B. Tap Ranges:

0.5A - 1.0A)
1.0A - 2.0A) See figure 2 for tap selections
2.0A - 5.0A)

III Timer

A. A/O timer(50 - 500 msec. See figure 1 for rheostat location

RATINGS

The SBC41A1 current circuits are rated at 10 amps continuously, and have one second thermal rating of 210 amps.

Caution: When Hi-Potting the SBC41A1 remove all external wiring from terminal 10. Do not high pot terminal 10. The reason is that capacitors C1 - C12 are rated for 600 VDC and the Hi-Pot voltage may damage the capacitors.

The breaker failure tripping telephone relay (BFT) is continuously rated at nameplate rated DC supply voltage. Table II lists the ratings of the three electrically seperate BFT contacts.

TABLE

BFT CONTACT RATINGS

RATING	CONTINUOUS CURRENT AMPS	TRIP DUTY AMPS	INTERRUPTION CURRENT (AMPS) INDUCTIVE	NON-INDUCTIVE
125V DC	3	30	0.5	0.75
250V DC	3	30	0.25	0.2
115V 60 HZ	3	30	2.0	4.0
230V 60 HZ	3	30	1.0	2.0

The ratings of the electromechanical targets (T1 and T2) is 1 amp.

SURGE WITHSTAND CAPABILITY

The SBC41A1 relay will withstand the following test voltage waveform without incorrect operation or damage to any component.

The test voltage waveform consists of a high frequency damped oscillation with a frequency of 1.5 megahertz. The source has an internal impedance of 150 ohms. The initial value (zero to peak) is 2500 volts and the damping is such that the envelope of the waveform decays to half the initial value (1250 volts) in 6.0 microseconds. The test voltage is applied between relay surge ground and each of the other relay terminals.

CAPACITANCE CHARGING CAPABILITY

Static relays with contact outputs generally have capacitors placed in parallel with the contacts. The purpose of these capacitors is to protect the static relays from surges which may be coupled to the wires connected on the contact outputs. The BFI contacts associated with static line relays may have these capacitors. If any switches are placed in series with the BFI contacts (DC power switches as an example) the closing of these switches will cause previously uncharged capacitors to charge through the breaker failure relay input circuit. This could result in an incorrect operation in some breaker failure schemes if a seal-in circuit is employed and the current detectors are set below full load current. The SBC41A1 relay however is designed such that the seal-in circuit will not operate if two fully discharged capacitors of equal value are charged into the contact initiation input at stud 17. That is, with minus battery connected to stud 18 and two capacitors connected in series with their center point grounded to relay surge groung and with one end of the capacitors connected to stud 17 and the other end of the capacitors connected through a switch to plus battery, the seal-in of the SBC21 relay will not operate when the switch is closed.

The limiting value of the capacitors for SBC41A1 with a voltage rating of the power supply being 125V is 12UF

BURDENS

The AC burden for each of the current transformer circuits is tabulated in Table III for 5 amperes of 60 Hertz current through each basic current setting range, minimum and maximum respectively.

TABLE III

5 AMP, 60 HERTZ BURDEN

BASIC RANGE	P.U. SETTING (AMPS)	VOLT-AMPS I^2Z (I=5 AMPS)	IMPEDANCE (OHMS)	POWER-FACTOR (LAGGING DEGREES)
Phase (1-2A)	1	0.54	.021	21
Ground (0.5-1A)	0.5	1.12	.045	14
Phase (1-2A)	2.0	0.51	.021	23
Ground (0.5-1A)	1.0	1.1	.044	34
Phase (2-4A)	2.0	0.34	.014	15
Ground (1-2A)	1.0	0.57	.023	19
Phase (2-4A)	4.0	0.33	.014	18
Ground (1-2A)	2.0	0.54	.022	27
Phase (4-10A)	4.0	0.27	.011	19
Ground (2-5A)	2.0	0.38	.016	18
Phase(4-10A)	10.0	0.27	.011	20
Ground (2-5A)	5.0	0.38	.015	26

the overall battery drain at relay terminals #17 and #18 is itemized in TABLE IV under three possible operating conditions.

TABLE IV
BATTERY DRAIN

RATED D.C.	CONDITION	DC DRAIN (AMPS)
125 VDC	DROPPED OUT (NO FAULT) TIMING TRIPPING	0 A 105 ma 167 ma

CHARACTERISTICS

Aside from the logic functions there are four (4) basic units the characteristics of which are important to the application the SBC41A1 relay. These are noted below.

POWER SUPPLY

The SBC41A1 relay covered by this book, contains a regulated power supply. This power supply regulates the voltage to the logic functions so that they perform properly over a range of applied dc voltage from 80 percent to 110 percent of rated voltage.

OUTPUT RELAY (BFT)

The trip output of the SBC41A1 relay consists of a high speed telephone relay with several contacts. The contacts of this telephone relay will close within 1/4 cycle of the instant that the coil circuit is energized from the logic. However, a shorter pulse of energization may also cause the output relay to close its contacts. This is in effect "overtravel". The overtravel of the output relay is less than 2 milliseconds. The dropout time of the output relay is somewhat longer than 2 cycles.

TIMER

The timer in the SBC41A1 relay is extremely accurate and repeatable in performance. The resolution of the setting mechanism is such that this timer may be set as shown on the calibration plate. At any given temperature and setting the timer will repeat its timing operation to within $\pm 2\%$ of its setting. Over the entire range of applied dc voltage from 80 to 110 percent of rating or temperature from -20 to +60 degrees centigrade, the timer will hold its setting to within ± 5 percent of setting.

The timer in the SBC41A1 relay has a very quick reset. If the input to the timer is removed for a time in the order of 0.2 milliseconds or longer it will reset completely. Thus, in order for the timer to time out it requires a continuous unbroken input for the complete timing cycle.

CURRENT DETECTOR

The current detector in SBC41A1 relay is comprised of magnetic input circuits for each phase current and $3I_0$, pickup setting potentiometers, one level sensing circuit, and a fill-in timer. See Figure 7. The level sensing circuit produces an output when the instantaneous magnitude of the input exceeds its fixed pick up sensitivity. The output will go away as soon as the instantaneous magnitude ofthe input gets below its fixed drop out level which is greater than 95 percent of the pickup level. The fill-in timer will produce an output as soon as a signal appears at its input. This output will persist until the input from the level sensing circuit goes away and the adjustable timer delay dropout setting on the fill-in timer expires.

As will be noted from figure 7 the input to the level sensing circuit is provided with four transactor circuits. The voltage outputs from each transactor is proportional to the respective current inputs. The outputs of the transactors are individually rectified and the phase circuits are separated from the ground ($3I_0$) circuit. A portion of each of the two circuits is supplied to the level sensing circuit via potentiometers. Since the sensitivity of the level sensing circuit is fixed by design, the pick up settings for phase and ground currents are made independently by means of the two potentiometers in conjunction with the current tap selection. Note, that since the output of all three phase bridge rectifier circuits are in parallel, the level dector responds to the highest of the three phase currents.

For a phase-to-phase or phase-to-ground fault or single-phase test simulation, the voltage applied to the input of the level sensing circuit will be a full wave rectified signal. This signal starts at zero magnitude, builds up to a maximum on a sine wave curve. and then drops off on a sine wave curve to zero

magnitude. This is repeated as long as the current input conditions exist. It is obvious that the output of the level sensing circuit cannot be continuous under these conditions since it will, regardless of the magnitude of the input, dropout twice each cycle every time the rectified input approaches and passes through zero. It is for this reason that the fill-in timer is employed to "ride over" these gaps in output from the level sensing circuit. The amount of fill in time required will depend on the magnitude of the input to the level sensing circuit. The range of pick-up adjustment as given under the section on RATINGS is based on the assumption that the fill-in timer will be set for (8.7 milliseconds) something longer than a half cycle drop out so that a continuous output from this timer will be obtained when the peak value of the input signal to the level sensing circuit is just equal to the sensitivity of that circuit. This is the normal factory setting of the fill-in timer and it results in a "drop out" time of the current detector that is about 10 milliseconds. (See figure 8). The dropout time is somewhat longer than the fill-in time because of the stored energy in the magnetic circuits after the current disappears.

As was noted above, the main timer required continuous input for the duration of its settings in order to time out. Thus, a continuous output is required from the fill-in timer. If faster overall drop out time of the current detector is required, it is necessary to reduce the fill-in timer setting. With this reduced fill-in timer setting and no other change, a higher input current will be required into the current detector circuits in order to produce a continuous output from the fill-in timer. (See figure 9). It is important to note that pick up of the current detector is defined as the RMS sine wave current applied at the input of the relay that produces a continuous output from this detector for the given fill-in timer setting. It should be recognized that in making the pick up setting only single phase current inputs should be used. Three phase current inputs tend to fill in the gaps so that the input to the level sensing circuit never goes to zero (See figure 10).

In summation, the normal factory setting on the fill-in timer is set for approximately 9 milliseconds. With this setting the drop out time of the current detector will be about 10 milliseconds. The range of pick up adjustment will be as given under the section on RATINGS. If faster drop out times are desired, the fill-in timer must be set for a shorter time and this in effect raises the pickup of the relay. This relationship is illustrated in Figure 9. Pick-up current is defined as the RMS sine wave current required to produce a continuous output from the current detector.

Since the application of the SBC41A1 relay, no dc voltage is applied until after the associated line relays operate, (see figure 4) there will be some slight operating delay in the pickup of the current detector. Figure 11 indicates the maximum and minimum operating times as a function of current as a multiple pick-up setting. The variation in time is a result of the instant in the current cycle at which the dc is applied. Note that these curves apply for single-phase fault or single phase test currents. For 3-phase faults or 3-phase test currents the minimum time curve will apply regardless of the incident angle of the current at the instant the dc is applied.

SETTINGS

The following settings must be made in the SBC41A1 relay covered by this book. The settings should be made in the order in which they are listed below.

1. Current Detector fill-in timer setting
2. Main Time Delay setting
3. Phase Current pick up setting
4. Ground current pick up setting
5. Link Position settings

The section under APPLICATION itemized the considerations involved in the selection of settings for items 1 - 4 above.

There are reasons for the order listed above in which the settings should be made. These reasons and other considerations are noted below.

It is important that the fill-in timer setting be made first because, as explained in the section under CHARACTERISTICS, the pick-up range of the current detector will vary depending on this setting. The section under "ACCEPTANCE TEST" describes exactly how this setting should be made or checked.

The next setting to be made is the time delay of the main timer. Since in the field the SBC41A1 relay does not normally have dc voltage applied, the current detectors are not operating regardless of magnitude of current until BFI or 62X contacts close to apply dc. This means that before the timer can start timing it is necessary for the fault detectors to pick-up. For this reason it is necessary to set the main timer so that the over all time from the instant the dc voltage is applied to the relay until any output is obtained from the BFT contacts is equal to the desired time delay. This test must be performed with current into the relay prior to applying the dc.

The magnitude of this current is an important consideration in this setting. Since the current detector cannot pick up until the instantaneous magnitude of the input current exceeds its sensitivity, there can be some variation in timing on a statistical basis depending on what instant in the current cycle the dc voltage is applied. In order to limit this variation it is recommended that the input current to the relay be selected in the range of 5 to 10 times the pick up setting. Thus, for setting this timer it is suggested that single phase current be fed into the ground circuit with the ground pickup setting on the minimum possible setting. This input current should then be selected to be about 5 to 10 times the RMS value required to get a continuous output from the current detector. This arrangement will limit the statistical variation to some fraction of a millisecond. The circuit and the instructions to make these settings are given in the section under "ACCEPTANCE TEST."

It should be noted that with the above settings the relay will, for severe faults operate in the set time. For low current faults it may get a few milliseconds slower which is in the direction to provide slightly more margin for these faults where stability and damage considerations are considerably less onerous.

After setting the main time delay the pick up settings on phase and ground currents should be made as indicated in the section under "ACCEPTANCE TEST." The considerations related to the actual settings to select have been discussed in the section under APPLICATION.

OPERATING PRINCIPLES

INTRODUCTION

The operating sequence of logic signals for the SBC41A1 can be followed with the aid of the internal connections diagram as shown in figure 12.

The SBC41A1 contain fuctional elements as described below.

a) +10.2V, -10.2V DC zener regulated power supply with RF surge suppression:

(Printed Circuit Card identified as "Y")

b) A.C. circuit surge suppression

(C1 through C8)

c) Three (3) range primary tapped transactors and tap blocks for $Phase_A$, $Phase_B$, $Phase_C$, 3Io current circuits:

(TRA, TRB, TRC, TRD ___ TB1, TB2, TB3, TB4)

d) Quad full wave bridge for full wave rectification of ØA, ØB, ØC, and 3Io transactor outputs

(Printed Circuit Card identified as "X")

e) Relay mounted components necessary for vernier transactor voltage control, over voltage protection and signal "OR":

(R1, R3, P1; R2, R4, P2; Z1; Z2; D1, D2)

f) Level detector circuitry necessary to detect AC level and convert ("FILL-IN" to DC logic levels:

Printed Circuit Card identified as "A")

g) Breaker failure timer with continuous adjustment from 50 to 500 Msec. with reed relay drive.

(Printed Circuit Card identified as "B" and externally mounted rheostat P3, A/O)

h) Breaker failure tripping relay (BFT) ____ type J telephone relay with surge suppression (D3) and current limit (R5). Having three (3) normally open contacts and two (2) electromechanical targets (T1, T2).

PRINTED CIRCUIT CARDS

The following sections describe the operation of the printed circuit cards. Table V shows the printed circuit card internal included in SBC41A1 model.

TABLE V

"A" Card	Fig. 13
"B" Card	Fig. 14
"X" Card	Fig. 15
"Y" Card	Fig. 16

"A" CARD (Level Detector with Adjustable "FILL-IN")

The power supply voltages are connected to the following pins:

+10.2VDC	Pin #10	(Red test point)
Ref.	Pins #1 and #20	(Black test point)
-10.2VDC	Pin #11	

The input information is supplied to Pin #2 of "A" Card. The output information (logic level) is obtained at Pin #12.

The MC1709L operational amplifier's invert input (4) is biased at approximately +2.4 volts DC, by R1 and ZD1. While the input at TP2 is below this level, TP3 has a negative voltage level present. As TP2 (Non-invert input) signal becomes more positive than the 2.4 VDC, the Op-Amp swings positive (TP3) and drives Q1 on.

In a quiescent dropped out state then, TP3 is a negative signal; Q1 is off, Q2 is off, the unijunction oscillator P1, C3 and Q3 is oscillating; Q5 is off; Q6 is on and the signal at TP4 is "0". When TP3 comes high, Q1 goes on, the unijunction oscillator stops oscillating and the capacitor C3 is fully discharged, Q2 comes on, Q4 stays non conducting, Q5 comes on Q6 goes off, and the output at Tp4 comes high.

Now as the Tp3 signal goes negative again, Q1 goes off, Q2 remains conducting by virtue of the previously conducting Q5 and feed back loop D3, D4, and R14. The C3 capacitor begins to charge with the (R10+P1) X (C) time constant, and the output signal remains ON.

When the C3 capacitor voltage reaches the firing level of the unijunction, a pulse is generated thus turning on the SCR Q4, which turns off Q5, resets the feed back circuit, drives Q6 on and yields a "0" output voltage. In effect, the circuitry after the Op-Amp provides the adjustable "Fill-In" time (time delay dropout) described elsewhere in this text.

In practice, the RC time constant is factory set such that the time delay on the card (P1 adjustment) is slightly greater than 1/2 cycle on a 60 Hertz basis (i.e. approximately 8.7 milliseconds).

Since the A/O timer resetsin less than 1/4 milliseconds, this "Fill-In" time plug energy decay time in the magnetics both contribute to the total dropout time shown in Figure 20.

"B" CARD (Adjustable/O timer (s) and Reed Driver)

The card has its reed relay (RD) output at Pins #12, and #14; +10.2VDC @ Pin #10 (Red test point); Ref. @ Pins #1 and #20 (Black test point); and -10.2VDC @ Pin #11.

The 0165B4687 G1 consists of an A/O timer with input at Pin #2 and its timer rheostat (external) across Pins #3 and #4.

A/O TIMER

In the quiescent off state (not timing) Q1 is off, Q2 is on, C3 is fully discharged, Q3 is off, Q4 is off, Q5 is off, and the reed relay remains de-energized, therefore, the contact between Pins #12 and #14

stays open.

In the timing state, Q1 is turned on by the presence of an input signal. Q2 is off and C3 is charging thru R7 and the external rheostat. At pickup, C3 is charged to approximately 6.5 volts and Q3 is on providing base current to Q4 on. With Q4 on, Q5 turns on which in turn provides current for the reed relay and the contact between Pins #12 and #14 closes. This contact output will remain closed until Q1 switches off, Q2 turns on and C3 discharges. When C3 discharges Q3 turns off, Q4 turns off, Q5 turns off, and the reed relay is de-energized.

The timing range for the A/O timer is from 50 to 500 milliseconds and is adjusted by a 0.75 meg ohm non-linear rheostat external of the printed circuit card.

"X" CARD (Quad. Full Wave Bridge)

0165B4796 (FIG. 15) ALSO G1

This card functions as a full wave bridge for the three phase and residual transactor secondary circuits.

The inputs and outputs are noted below:

PHASE	INPUT	OUTPUT
AØ	#1, #2	PIN #9
BØ	#3, #4	PIN #9
CØ	#5, #6	PIN #9
3Io	#7, #8	PIN #10

Reference is Pin #11

Note that the three (3) phase outputs are logically "ORed" on this board @ output Pin #9. In short, this means that the phase voltage of greatest magnitude in time will prevail @ the output Pin #9.

"Y" CARD (Zener Regulated Power Supply)

GE ASSEMBLY	FIGURE
0183B2302	16

This card functions as a single rated zener regulated +10.2 volt DC, -10.2 volt DC power supply. The ohmic value of RØ (External to Card) for 125 VDC is 1000 ohms.

Note that for input connections, (+) rated DC and (-) DC, are connected to pins #10 and #6 respectively.

DY1 is a rectifier which prohibits momentary negative voltage excursions on the DC bus from drawing the +10.2 or -10.2 volt buses out of regulation.

Zener diodes ZY1 and ZY2 are the 10.2volt 5% regulators and ZY3 and ZY4 are the -10.2 volt 5% regulators. The cathode of ZY1 (TP2 is a red test point supplies +10.2 volts to the relay circuits. The anode of ZY2, common with the cathode of ZY3 (TP1 is a black test point) provides relay circuit reference. The anode of ZY4 (TP3 is a green test point) supplies -10.2 volts to the relay circuits. Capacitor CY5 is the regulated DC ripple filter.

Resistor R6 insures power supply load balance during the transient energization of the power supply.

II. Current Detectors

A. General Description

The three phase elements (AØ, BØ, CØ... the outputs of which are combined in logical "OR") and the residual element ($3I_0$) are independently adjustable from the front of the relay in continuous increments as follows:

PHASE	RESIDUAL
1-2A	0.5-1A

(CONTINUED)

PHASE	RESIDUAL
2-4A	1-2A
4-10A	2-5A

The four (4) links at the bottom of the relay provide for the above listed discrete ranges of adjustment, while the two (2) lower rheostats provide for the continuous adjustment within a range. The four tap blocks are identified as AØ, BØ, CØ, and $3I_0$ respectively; and range selection for the three position tap blocks increases from left to right. The seven (7) lines scribed on the nameplate associated with each rheostat indicates an approximate current detector pickup level calibration (factory) in multiples of the base pickup as follows reading clockwise: 1.0, 1.2, 1.4, 1.6, 1.8, 2.0, 2.5 X (base pickup)

Note that these pickup calibration marks apply to the factory convention of setting the current detector with 8.7 millisecond "fill-in" time.

The following two examples demonstrate the current detector setting calculation using the calibration marks. The assumption is, of course, that the current detector has an undisturbed factory calibration.

1. The AØ tap block screw is in the middle position (range 2-4A). The phase rheostat knob is pointing at the 4th mark from the left (1.6X range base). Since the relay is in the range 2-4A the range base equals 2A. Multiplying the range base by the calibration mark multiple, we have: Pickup: 1.6 X 2 = 3.2A. so, approximately 3.2A RMS through the AØ current circuit is the level of current necessary to pickup up the current detector. Similarly, the above applies for B and C phase current.

2. The residual ($3I_0$) tap block screw is in the right position (range 2-5A). The $3I_0$ rheostat knob is pointing at the second calibration mark from the left (1.2X base range). Since the relay is in the range 2-5A, the $3I_0$ range base equals 2A. Multiplying the range base by the calibration mark multiple, we have: Pickup: 1.2 X 2 = 2.4A. So, approximately 2.4A RMS through the $3I_0$ current circuit level of residual current necessary to pick up the current detector.

ACCEPTANCE TESTS

Immediately upon receipt of the relay an INSPECTION AND ACCEPTANCE TEST should be made to insure that no damage has been sustained in shipment and that the relay calibrations have not been disturbed. If the examination or test indicates that readjustment is necessary, refer to the section on SERVICING.

CAUTION: WHEN HI-POTTING THE SBC41 REMOVE ALL EXTERNAL WIRING FROM TERMINAL 10. DO NOT HIGH POT TERMINAL 10. THE REASON IS THAT CAPACITORS C1-C12 ARE RATED FOR 600 VDC AND THE HI-POT VOLTAGE MAY DAMAGE THE CAPACITORS.

These tests may be performed as part of the installation or acceptance tests at the discretion of the user. Since most operating companies use different procedures for acceptance and installation tests, the following section includes all applicable tests that may be performed on these relays.

Setting or checking all SBC relays consist of the following tests and these tests must be performed in the following order.

A. FILL IN TIMER SETTING

The fill-in timer is essentially an adjustable dropout timer which is factory set to 8.7 milliseconds. Other fill-in times less than 8.7 milliseconds are obtainable, but lowering the fill-in raises the pick up level as shown on the graph of Figure 6. As an example, if the fill-in time of 5 milliseconds is required and set, then the 5 millisecond fill-in pickup level is approximately 1.24 times the 8.7 millisecond setting. (See Figure 6 and the CHARACTERISTICS section for other parameters).

The timer and its associated adjustment potentiometer are located on the "A" card (left card see Figure 2). Set up the test circuit shown on Figure 17 and perform the following instructions:

1. Apply rated D.C. to relay terminals 17(+) and 18 (-).

2. Insure that the relay circuit currents are zero by removing the lower connection block.

3. Make the oscilloscope and contact circuits described on Figure 17 being certain to observe the caution that the scope power cord is ungrounded. The reason for this latter caution is the relay signal reference is at a different potential than the system ground.

Opening the normally open contact in the circuit removes signal from the timer input and thereby allows for fill-in timer measurement.

Place the scope in an external triggering mode with negative slope and note that upon opening the depressed normally open contact, a positive signal goes to about "0" volts in about 8.5 - 9.0 milliseconds.

If the measuremnt is less than or greater than this range, correctly set the time to precisely 8.7 milliseconds by adjusting the potentiometer located in the lower corner of the "A" card.

B. CURRENT DETECTOR PICKUP TEST

Having checked or adjusted the fill-in time setting per section A, set up the test current circuit of Figure 18.

Connect an oscilloscope such that the vertical input is connected to TP4 of the "A" card and reference is connected to TP1 of the "A" card. The oscilloscope power cord should be ungrounded.

The following test is for a fill-in time setting of 8.7 milliseconds:

1. Set all current tap blocks as follows:

AØ	1-2A
BØ	1-2A
CØ	1-2A
$3I_0$	0.5-1

2. Set both current rheostat pointers to the 1X range base (first calibration line going clockwise).

3. Apply current to the AØ terminals per Figure 18 until the oscilloscope indicates a continuous DC output. The input current shall be approximately one (1) ampere.

4. Repeat three (3) above for phase B and C.

5. Apply current to the $3I_0$ terminals per Figure 45 until the oscilloscope indicates a continuous DC output. The input current shall be approximately 0.5 amps.

6. Using the procedure above, check the other taps and multiples of current settings.

To test the current detector pickup for fill-in times less than 8.7 milliseconds use the above procedure except that the pickup currents will be higher and have approximate values per figure 6. Also, see CHARACTERISTICS section for other parameters.

C. CURRENT DETECTOR PICK UP SETTING

1. Use the procedure of the previous section (B) except set the current rheostats to the desired current pickup and secure the rheostats.

D. TRIPPING TIMERS

The rheostat on the front of the relay associated with the trip timer is identified as the A/O. The seven (7) calibration marks which are scribed represent 50, 75, 100, 200, 300, 400, 500 (milliseconds)

The "A" signifys a continuously adjustable pickup time delay in the range of 50 to 500 milliseconds. The "O" signifies that the timer resets "instantaneously" (in reality, in less than 200 microseconds).

Set up the AC, DC and oscilloscope connections shown in Figure 19. Apply the current to the ground circuit on the .5 tap at X1 base pickup. Observe the following two cautions:

1. The system side circuits of the BFT contacts must be removed before the test connections are made (use of an XLA test plug is recommended).

2. The Oscilloscope must not be grounded...use a 3 to 2 prong power cord adapter. The reason for this latter caution is that relay reference is near (-) DC potential and ground potential is generally about 1/2 DC potential.

To check or set the timer, use the following procedure:

Set the test current into the relay at 5X pickup. Upon closing the BFI contact of Figure 19, the scope trace is initiated. Note that since rated DC voltage is triggering the scope, the trigger feature should be operated in the attenuated mode. After the timer under test (A/O) has timed out and the BFT relay has operated, the BFT contacts close and the scope trace goes to "O" volts. The time from trace initiation until the signal goes to zero is the breaker failure tripping time.

For the SBC41A1 relay timer settings follow the subsequent instruction.

Note that the A/O timer rheostat is identified as such and clockwise rotation of each increases the tripping time.

1. SBC41A1 (A/O) Initiate timing of the relay as explained above by closing the BFI contact. Set the length of tripping time by adjusting the A/O rheostat. Lock the rheostat position and check several times that the tripping time is consistent.

E. LOGIC FUNCTIONS, SETTINGS AND TESTS

Having set the current detectors and the A/O timer, perform the following tests using the Fig. 18 test circuit for the ØA configuration. Let the test current be 1.5X current detector pickup.

INSTALLATION PROCEDURE

I. INTRODUCTION

The location should be clean and dry, free from dust and excessive vibration, and well lighted to facilitate inspection and testing.

The relay should be mounted on a vertical surface. The outline and panel diagram is shown in Fig. 20.

The internal connection diagram for the relay is shown in Fig. 12. The wiring diagram is given in Fig. 4.

One of the mounting studs or screws should be permanently connected to surge ground by a conductor not less than No. 12 B & S gage copper wire or its equivalent. (See Fig. 12).

The relay may be tested without removing it trom the panel by using a 12XLA13A test plug. This plug makes connections only with the relay and does not distrub any shorting bars in the case. Of course, the 12XLA12A test plug may also be used. Although this test plug allows greater testing flexibility, it also requires C.T. shorting jumpers and the exercise of greater care since connections are made to both the relay and the external circuitry. Additional information on the XLA test plugs may be obtained from GEI-25372.

All alternating current operated devices are affected by frequency. Since non-sinusoidal waveforms can be analyzed as a fundamental plus harmonics of the fundamental frequency, it follows that alternating current devices (relays) will be affected by the applied waveform. Therefore, in order to properly test alternating current relays it is essential to use a sine wave of current.

CAUTION: WHEN HI-POTTING THE SBC41 REMOVE ALL EXTERNAL WIRING FROM TERMINAL 10. DO NOT HIGH POT TERMINAL 10. THE REASON IS THAT CAPACITORS C1-C12 ARE RATED FOR 600 VDC AND THE HI-POT VOLTAGE MAY DAMAGE THE CAPACITORS.

Since most operating companies use different procedures for installation tests, the section under ACCEPTANCE contains all necessary test which may be performed as part of the installation procedure at the discretion of the user.

The minimum suggested test are as follows:

II. TIMER TEST

Test per timing test as explained in section titled ACCEPTANCE.

III. CURRENT DETECTOR PICKUP SETTING

Set up the test current circuit of Figure 18.

Place an oscilloscope on the A card TP4 as an indication of current detector pickup. Note that a "0" volt signal denotes dropout and a positive DC signal represents current detector pickup.

As a quick check on each of the relay calibration marks, perform the following:

Place all current tap block screws in the middle position.

AØ	2-4A
BØ	2-4A
CØ	2-4A
$3I_0$	1-2A

Place both current rheostat pointers to the first calibration line (i.e. 1X range base).

Apply test current to each of the four current circuits per Figure 18 and adjust the current level until the "A" card TP4 indicates that the current detector has just picked up. The current levels should be as follows for the four circuits: 1.9-2.1A RMS phase circuits---0.95-1.05A RMS residual circuit.

Having selected the phase and residual current detector settings to be used on the system (1-10A for phase and 0.5-5A for residual) set the tap plugs to the appropriate range selection: as an example a 6A phase setting should use the third tap block range (4-10A). Set up the AØ current circuit of Figure 18, and set the RMS value of current to the desired current detector pickup level exactly. Slowly adjust the phase rheostat til the current detector just picks up. Check that the current detector pickup level on the remaining two phases is +5% of the original setting. Lock the phase rheostat and be sure that the current detector setting has not drifted in the interim. Arrange the $3I_0$ current circuit of Fig. 18 and calibrate the residual rheostat til the current detector just picks up. Lock the residual rheostat, and check that the operate level has not changed.

PERIODIC CHECKS AND ROUTINE MAINTENANCE

In view of the vital role of protective relays in the operation of a power system it is important that a periodic test program be followed. It is recognized that the interval between periodic checks will vary depending upon environment, type of relay and the user's experience with periodic testing. Until the user has accumulated enough experience to select the test interval best suited to his individual requirements it is suggested that the points listed under INSTALLATION PROCEDURE be checked at an interval of from one to two years.

CONTACT CLEANING

For cleaning relay contacts, a flexible burnishing tool should be used. This consists of a flexible strip of metal with an etched-roughened surface resembling in effect a superfine file. The polishing action is so delicate that no scratches are left, yet it will clean off any corrosion throughly and rapidly. Its flexibility insures the cleaning of the actual points of contact. Do not use knives, files, abrasive paper or cloth of any kind to clean relay contacts.

SERVICING

Should servicing of the relay become necessary, follow the test procedures as explained in the section titled ACCEPTANCE TEST, for calibration and test of the relay. Telephone relay contact cleaning is located in the section titled PERIODIC CHECKS AND ROUTINE MAINTENANCE. Also, see section on RENEWAL PARTS for servicing printed circuit cards.

RECEIVING, HANDLING AND STORAGE

These relays, when not included as a part of a control panel, will be shipped in cartons designed to protect them against damage. Immediately upon receipt of a relay, examine it for any damage sustained in transit. If injury or damage resulting from rough handling is evident, file a damage claim at once with the transportation company and promptly notify the nearest General Electric Aparatus Sales Office.

Reasonable care should be exercised in unpacking the relay in order that none of the parts are injured or the adjustments disturbed.

If the relays are not to be installed immediately, they should be stored in their original cartons in a place that is free from moisture, dust and metallic chips. Foreign matter collected on the outside of the case may find its way indide when the cover is removed and cause trouble in the operation of the relay.

RENEWAL PARTS

It is recommended that sufficient quantities of renewal parts be carried in stock to enable the prompt replacement of any that are worn, broken, or damaged.

Should a printed circuit card become inoperative, it is recommended that this card be replaced with a spare. In most instances, the user will be anxious to return the equipment to service as soon as possible and the insertion of a spare card represents the most expeditious means of accomplishing this. The faulty card can then be returned to the factory for repair or replacement.

Although it is not generally recommended, it is possible with the proper equipment and trained personnel to repair cards in the field. This means that a trouble-shooting program must isolate the specific

component on the card which has failed. By referring to the internal connection diagram for the card, it is possible to trace through the card circuit by signal checking and, hence determine which component has failed. This, however, may be time consuming and if the card is being checked in place in its unit, as is recommended, will extend the outage time of the equipment.

CAUTION: GREAT CARE MUST BE TAKEN IN REPLACING COMPONENT ON THE CARDS. SPECIAL SOLDERING EQUIPMENT SUITABLE FOR USE ON THE DELICATE SOLID-STATE COMPONENTS MUST BE USED AND, EVEN THEN, CARE MUST BE TAKEN NOT TO CAUSE THERMAL DAMAGE TO THE COMPONENTS, AND NOT TO DAMAGE OR BRIDGE OVER THE PRINTED CIRCUIT BUSSES THE REPAIRED AREA MUST BE RECOVERED WITH A SUITABLE HIGH-DI-ELECTRIC PLASTIC COATING TO PREVENT POSSIBLE BREAKDOWNS ACROSS THE PRINTED CIRCUIT BUSSES DUE TO MOISTURE OR DUST.

ADDITIONAL CAUTION: DUAL IN LINE INTEGRATED CIRCUITS ARE ESPECIALLY DIFFICULT TO REMOVE AND REPLACE WITHOUT SPECIALIZED EQUIPMENT. FURTHERMORE, MANY OF THESE COMPONENTS ARE USED ON PRINTED CIRCUIT CARDS WHICH HAVE BUS RUNS ON BOTH SIDES. THESE ADDITIONAL COMPLICATIONS REQUIRE VERY SPECIAL SOLDERING EQUIPMENT AND REMOVAL TOOLS AS WELL AS ADDITIONAL SKILLS AND TRAINING WHICH MUST BE CONSIDERED BEFORE FIELD REPAIRS ARE ATTEMPTED.

When ordering renewal parts, address the nearest Sales Office of the General Electric Company, specify quantity required, name of the part wanted, and the complete model number of the relay for which the part is required.

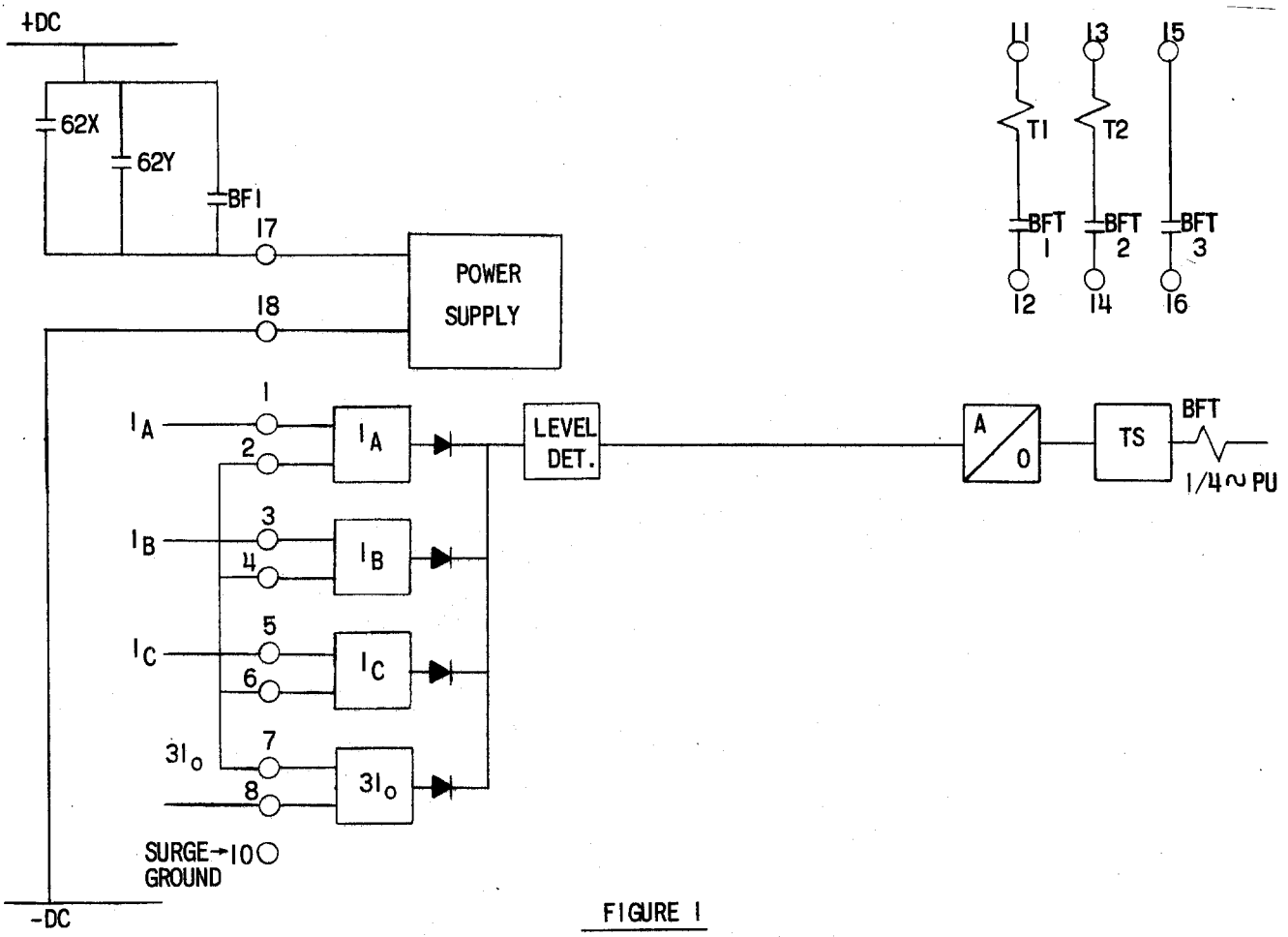


FIGURE 1

NOTE: CONNECT STUD 10 (SURGE GROUND) TO GROUND BUS ON PANEL

FIG. 4 (0227A7121-1) EXTERNAL CONNECTION DIAGRAM FOR THE SBC41A RELAY

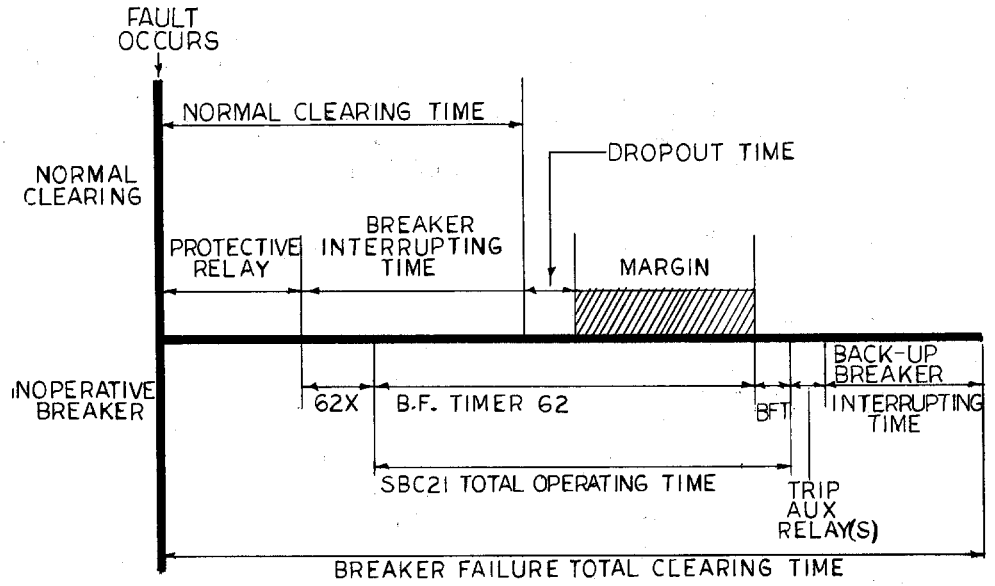


FIG. 5 (0227A7128-1) BREAKER FAILURE TIME CHART FOR THE SBC41A RELAY

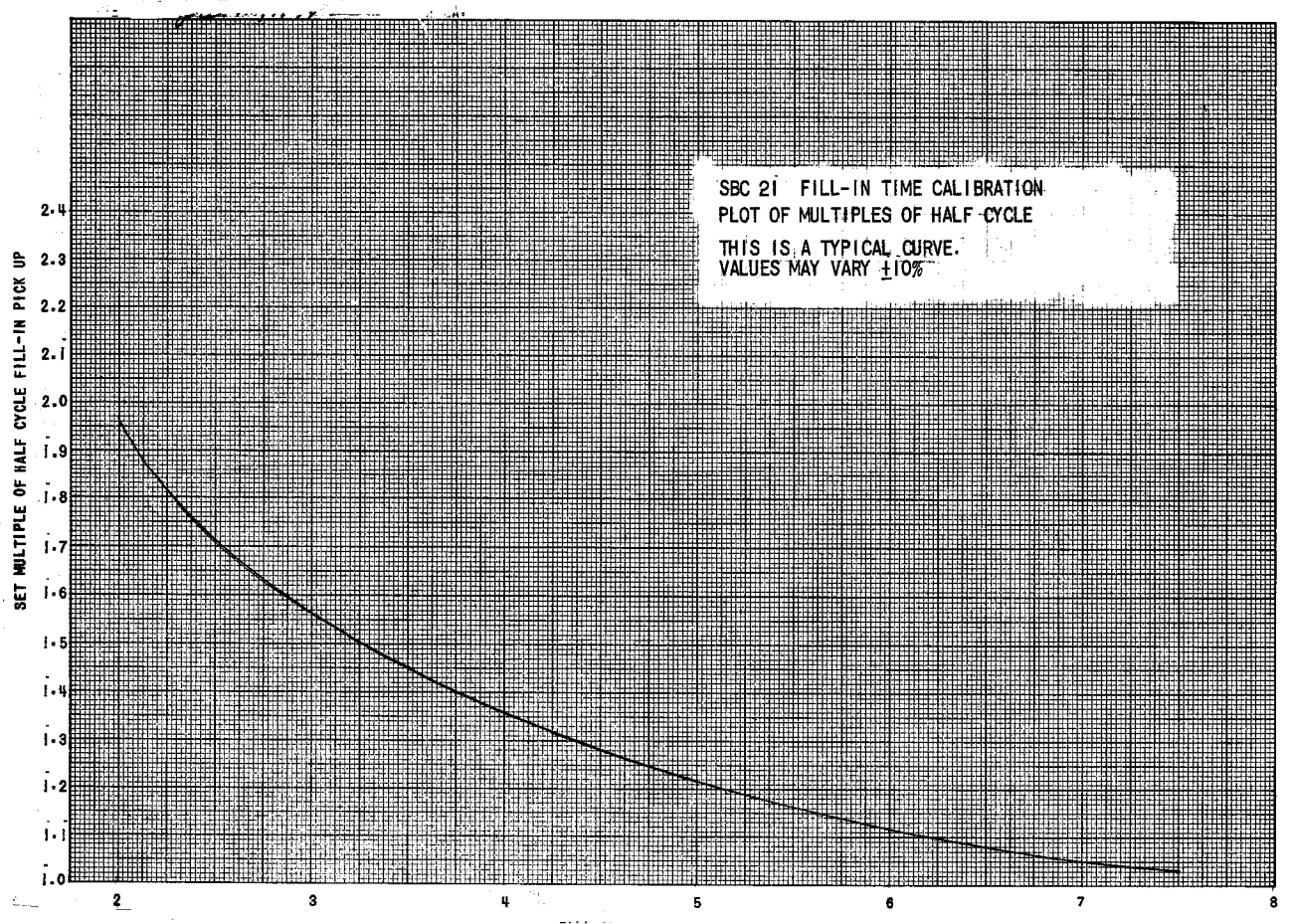


FIG. 6 (0246A2206-0 SH. 1) FILL-IN TIME CALIBRATION GRAPH FOR THE SBC41A RELAY

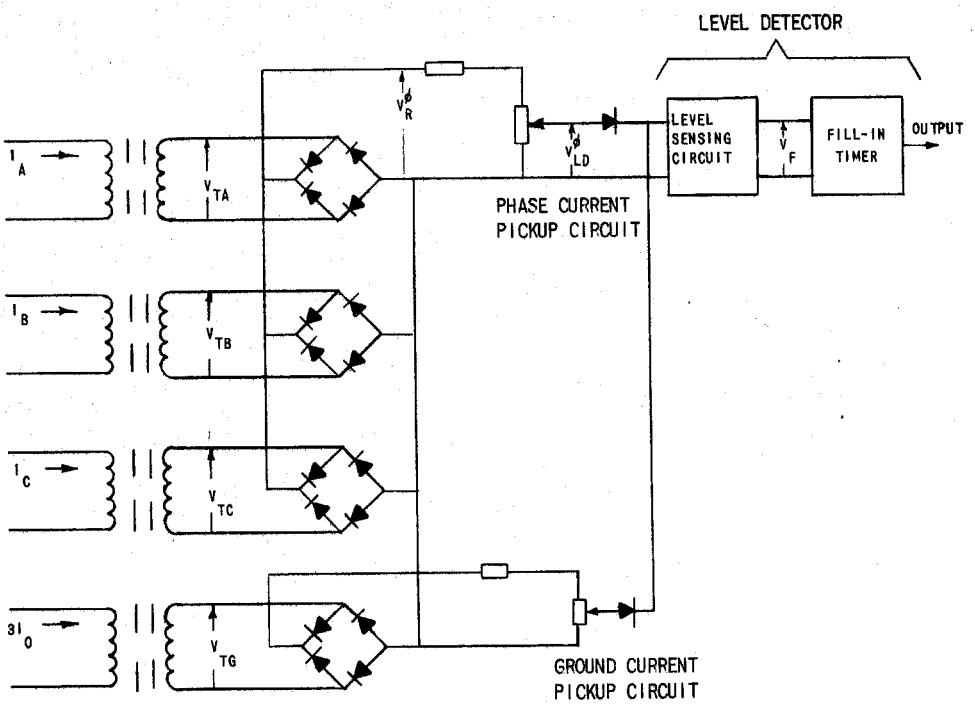


FIG. 7 (0246A2272-0) CURRENT DETECTOR CIRCUIT ILLUSTRATION FOR THE SBC41A RELAY

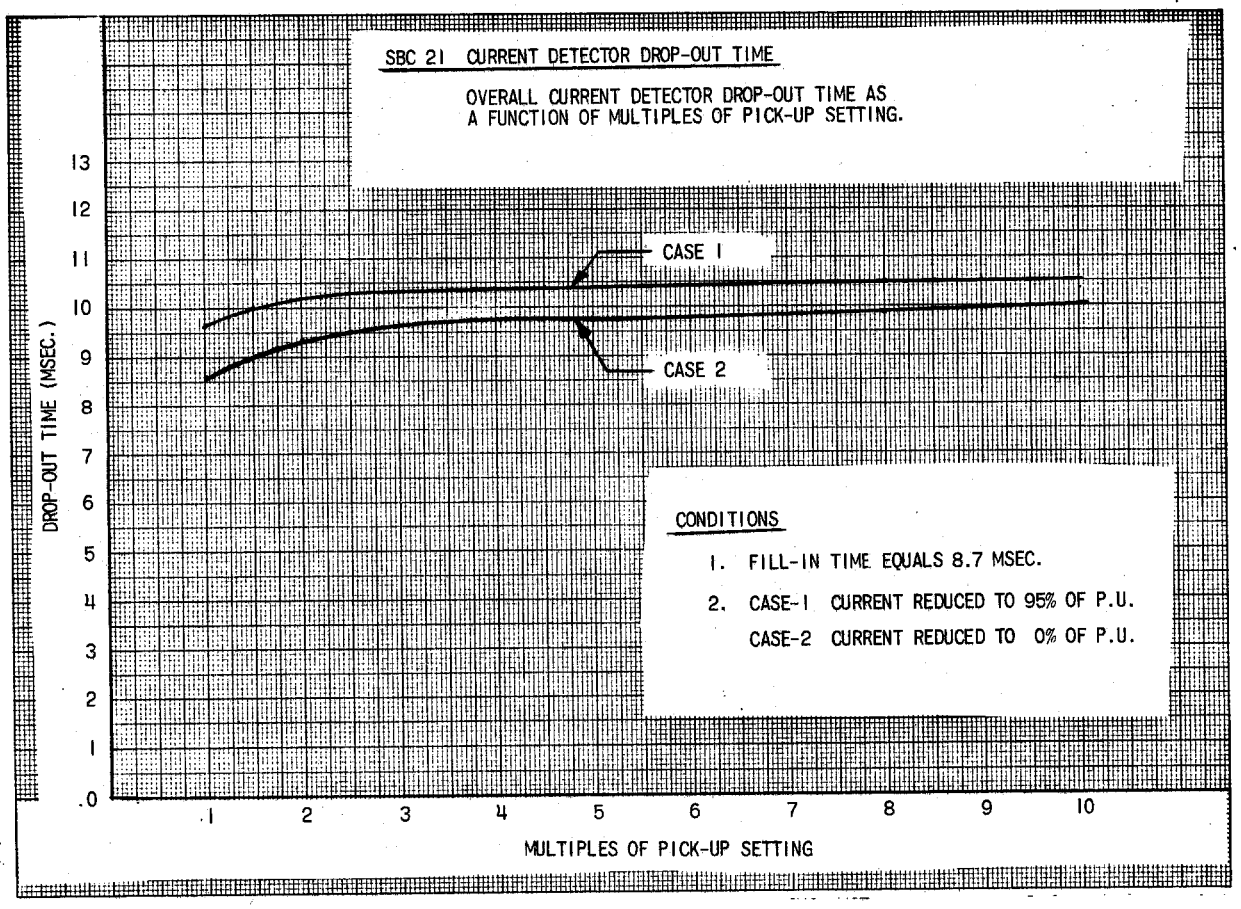


FIG. 8 (0246A2206-0 SH. 4) CURRENT DETECTOR DROP-OUT TIME GRAPH FOR THE SBC41A RELAY

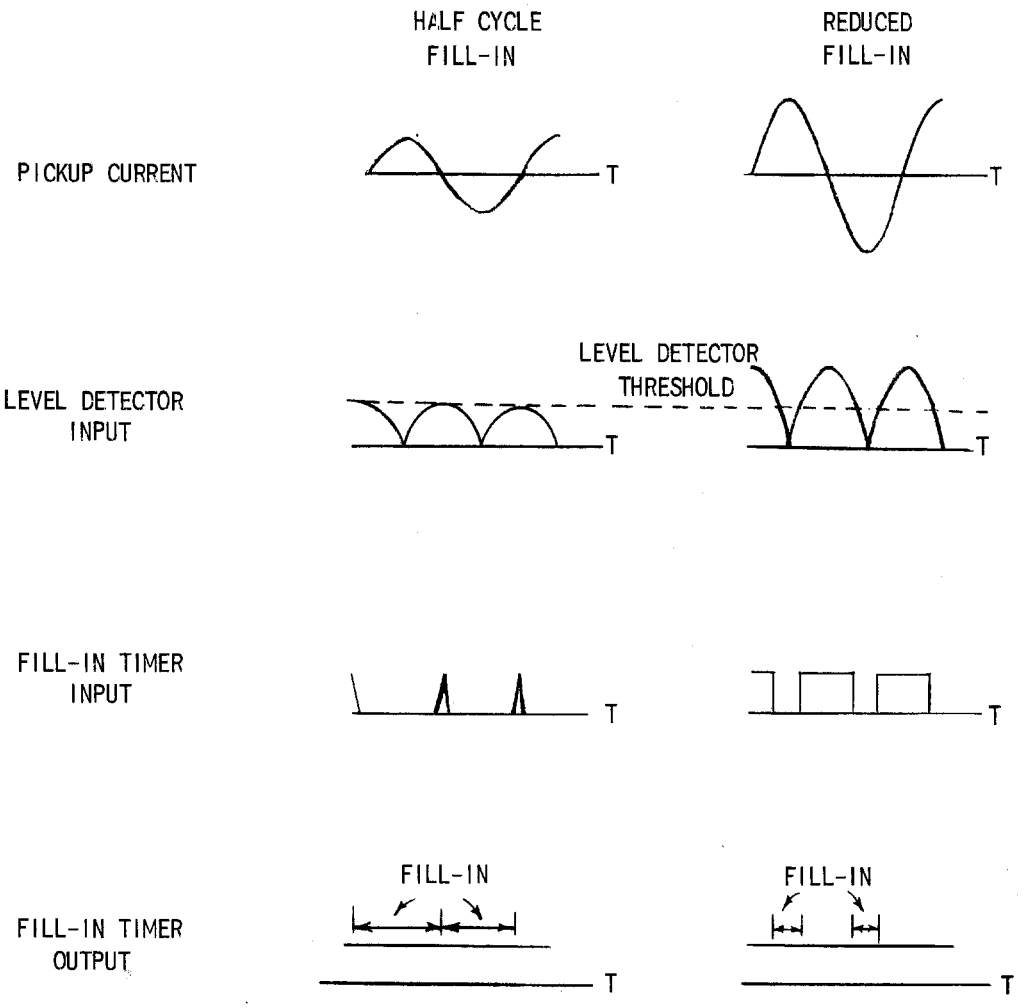


FIG. 9 (0246A2273-0) CURRENT DETECTOR PICKUP CURRENT FOR REDUCED FILL-IN TIMES FOR THE SBC41A RELAY

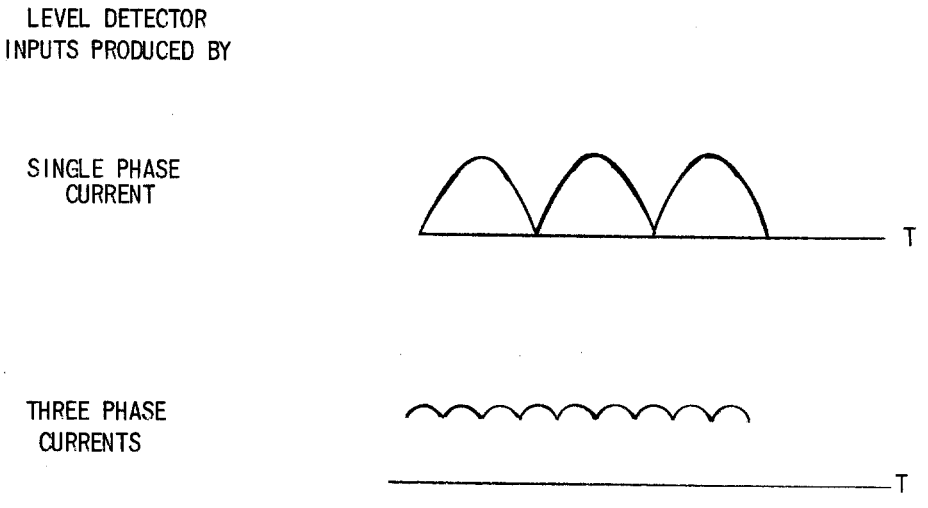


FIG. 10 (0246A2274-0) CURRENT DETECTOR LEVEL DETECTOR INPUTS PRODUCED BY SINGLE PHASE AND THREE PHASE CURRENTS FOR THE SBC41A RELAY

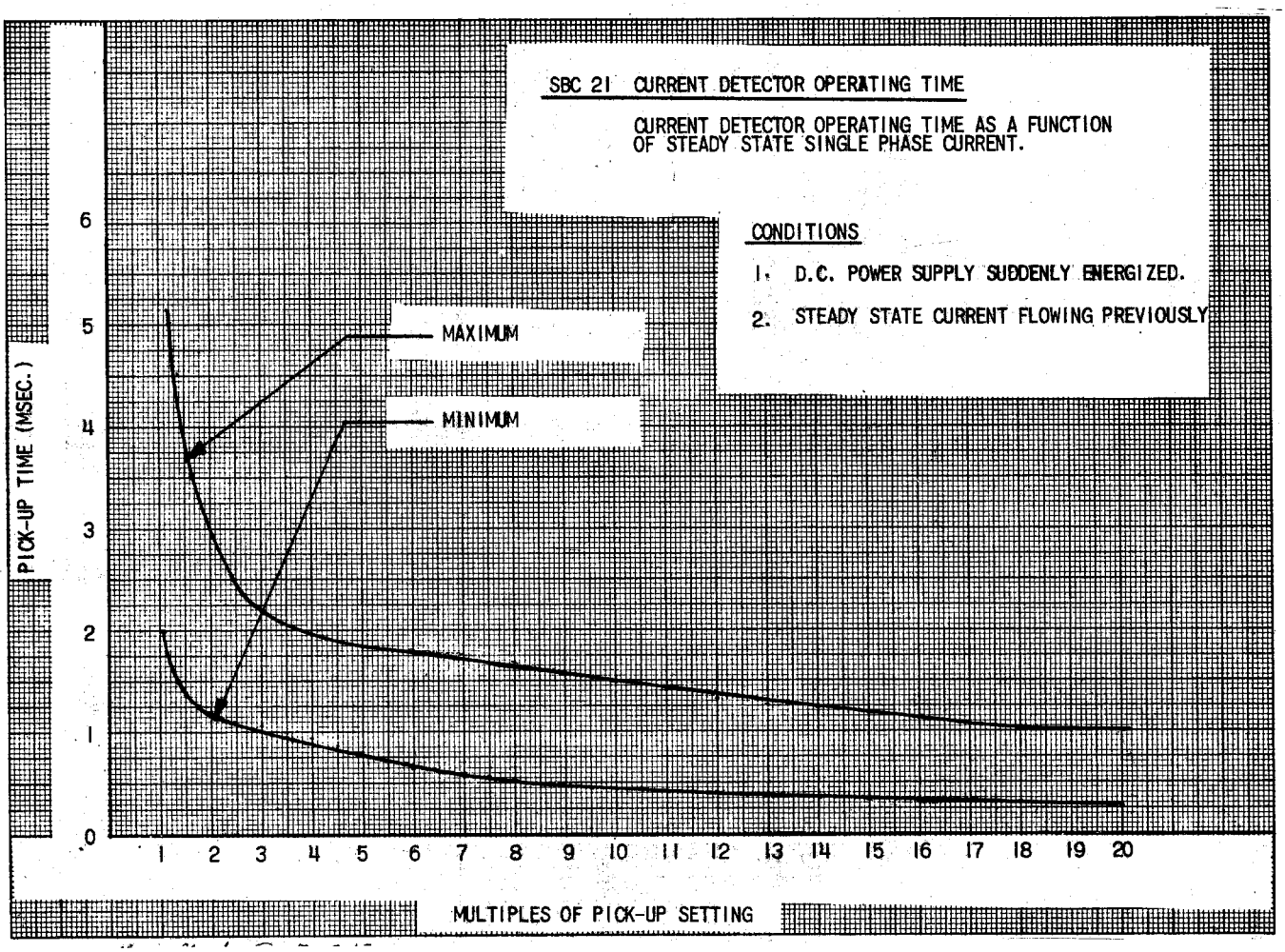


FIG. 11 (0246A2206-0 SH. 3) CURRENT DETECTOR OPERATING TIME FOR THE SBC41A RELAY

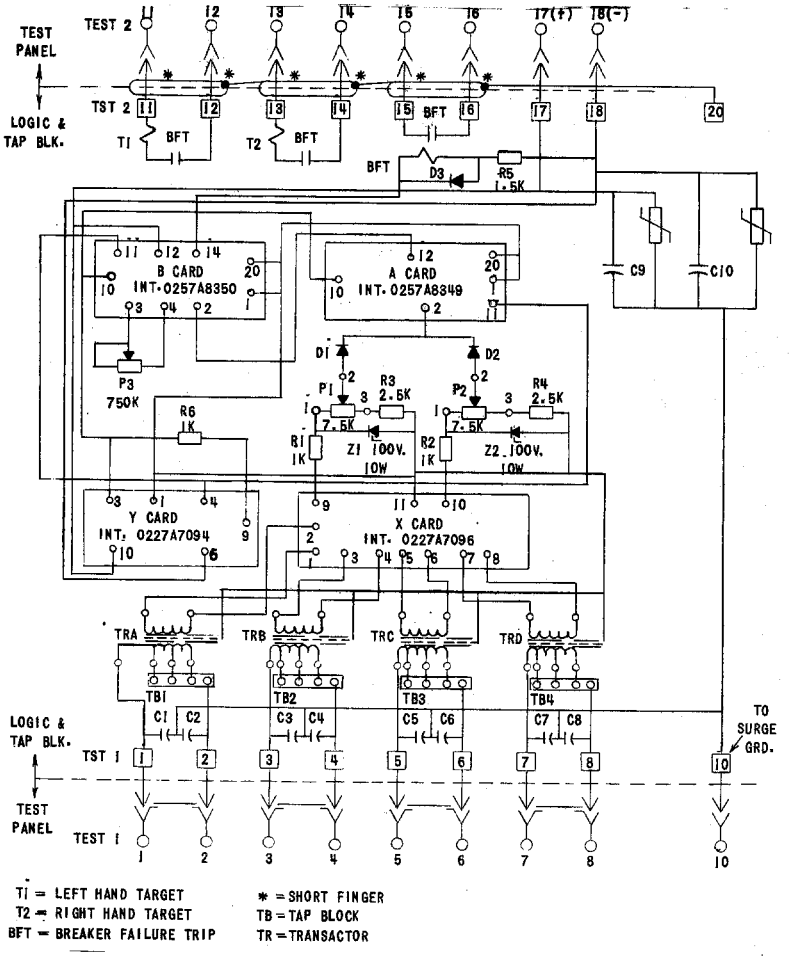


FIG. 12 (0257A5047-2 SH. 1) INTERNAL CONNECTIONS FRONT VIEW

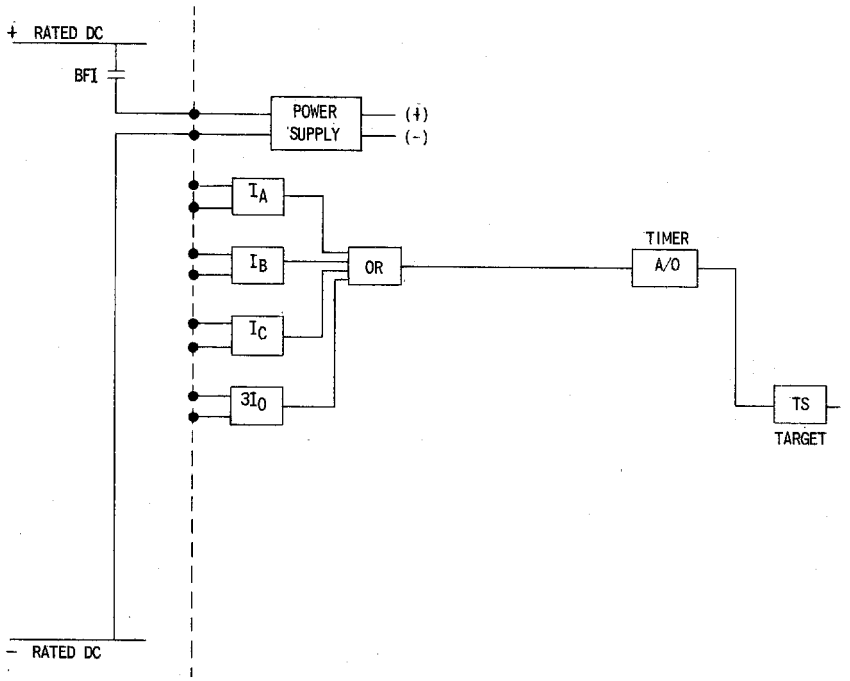


FIG. 12A (0257A5047-0 SH. 2) OVERALL LOGIC DIAGRAM FOR SBC41A

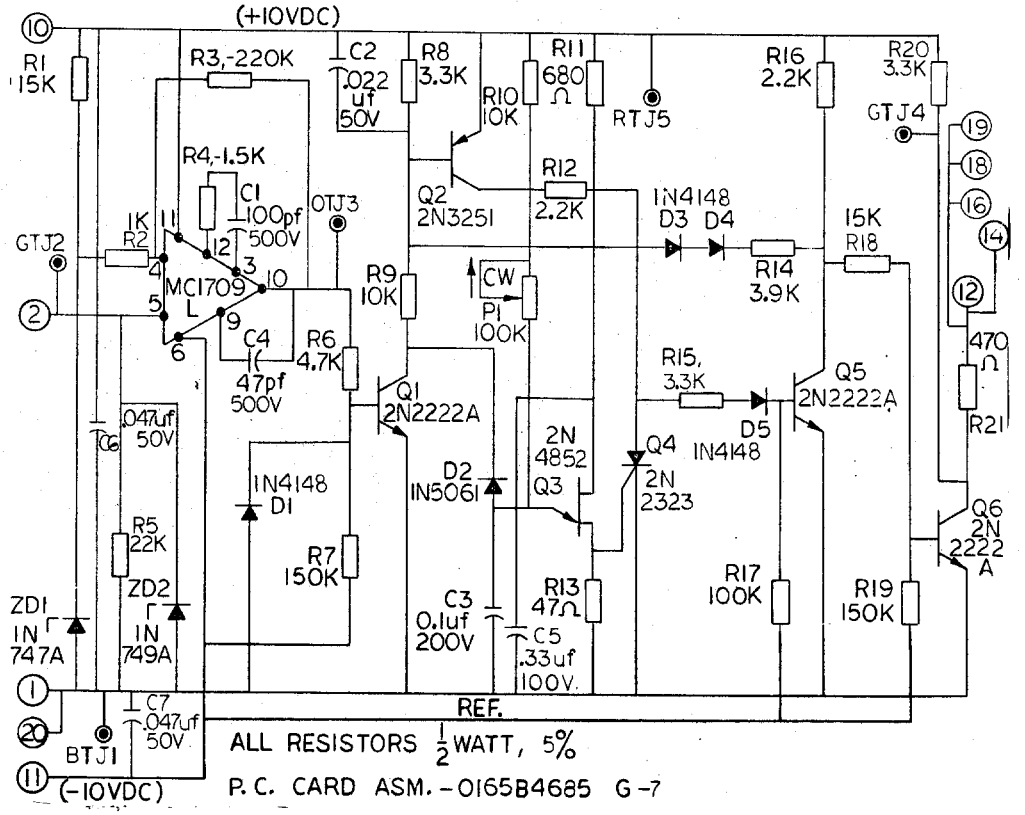


FIG. 13 (0257A8349-0) LEVEL DETECTOR WITH ADJUSTABLE MILLISECOND FILL-IN TIME FOR THE SBC41A RELAY ("A" CARD)

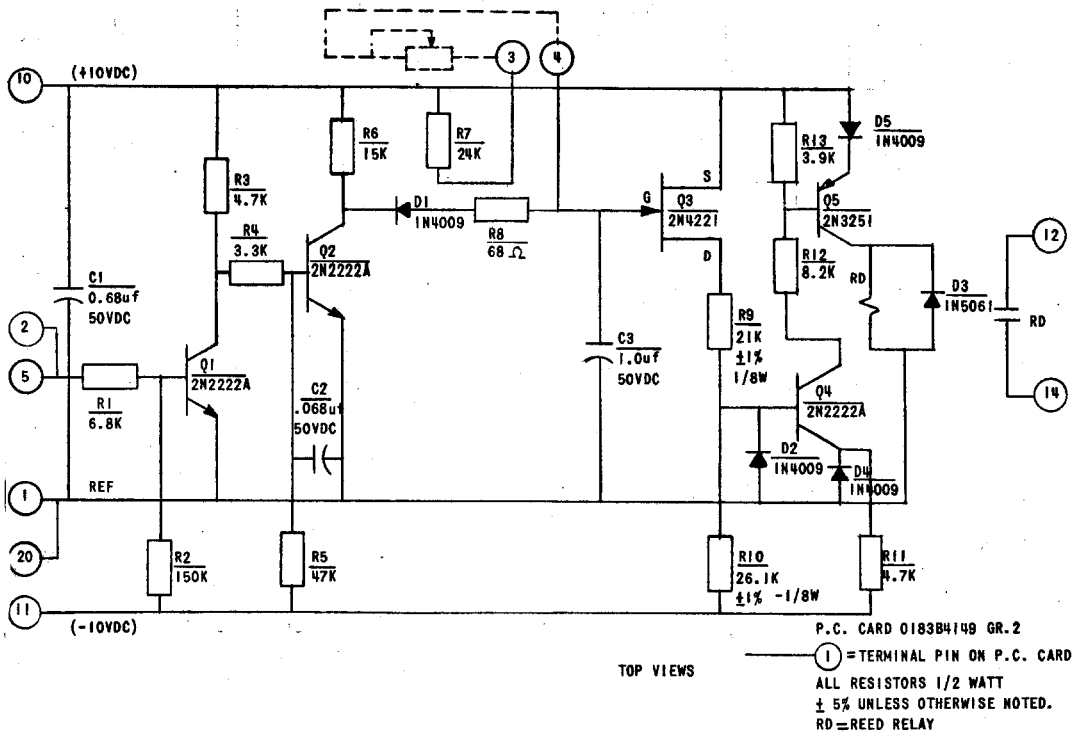


FIG. 14 (0257A8350-0) A/O TIMER AND REED DRIVER FOR THE SBC41A RELAY ("B" CARD)

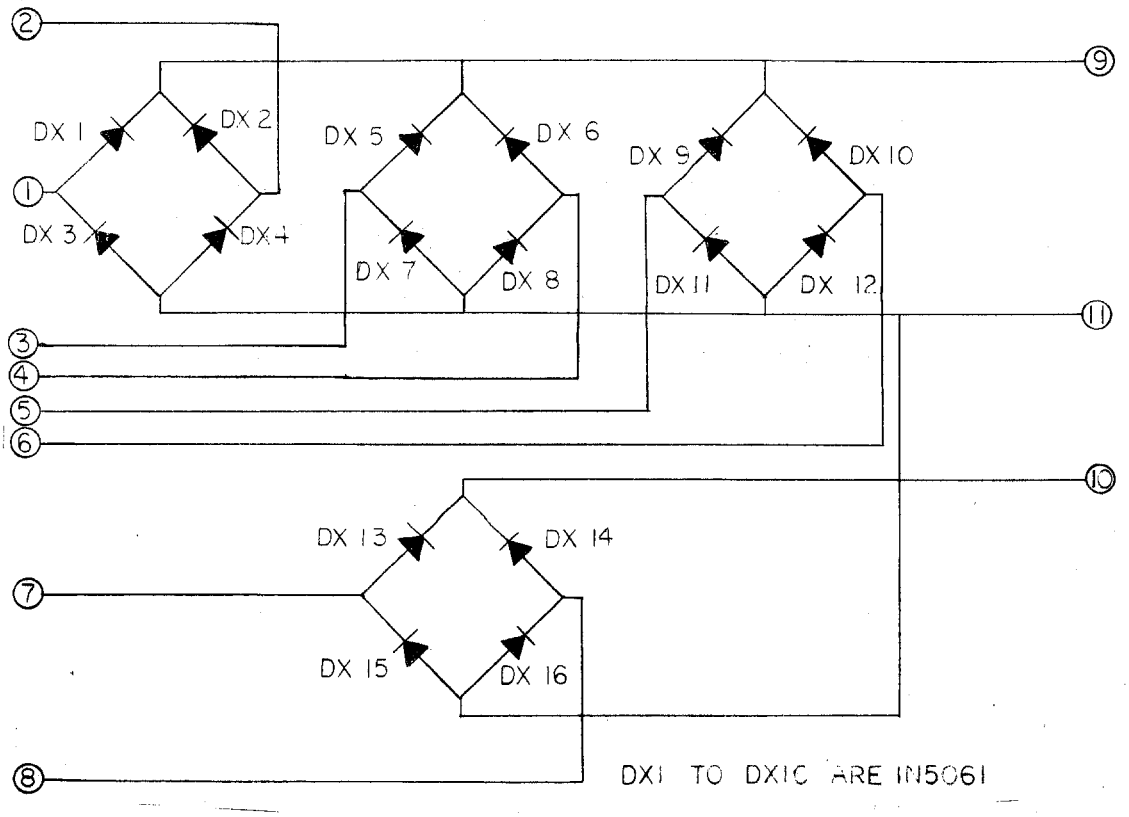


FIG. 15 (0227A7096-0) FULL WAVE BRIDGES FOR THE SBC41A RELAY ("X" CARD)

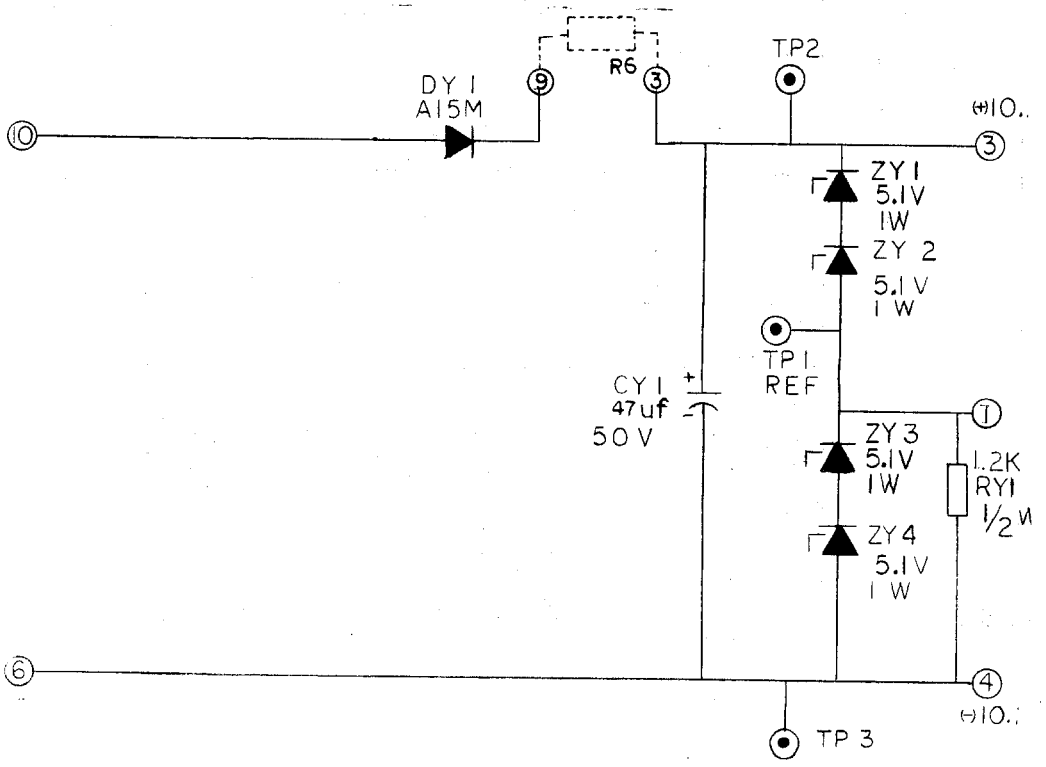
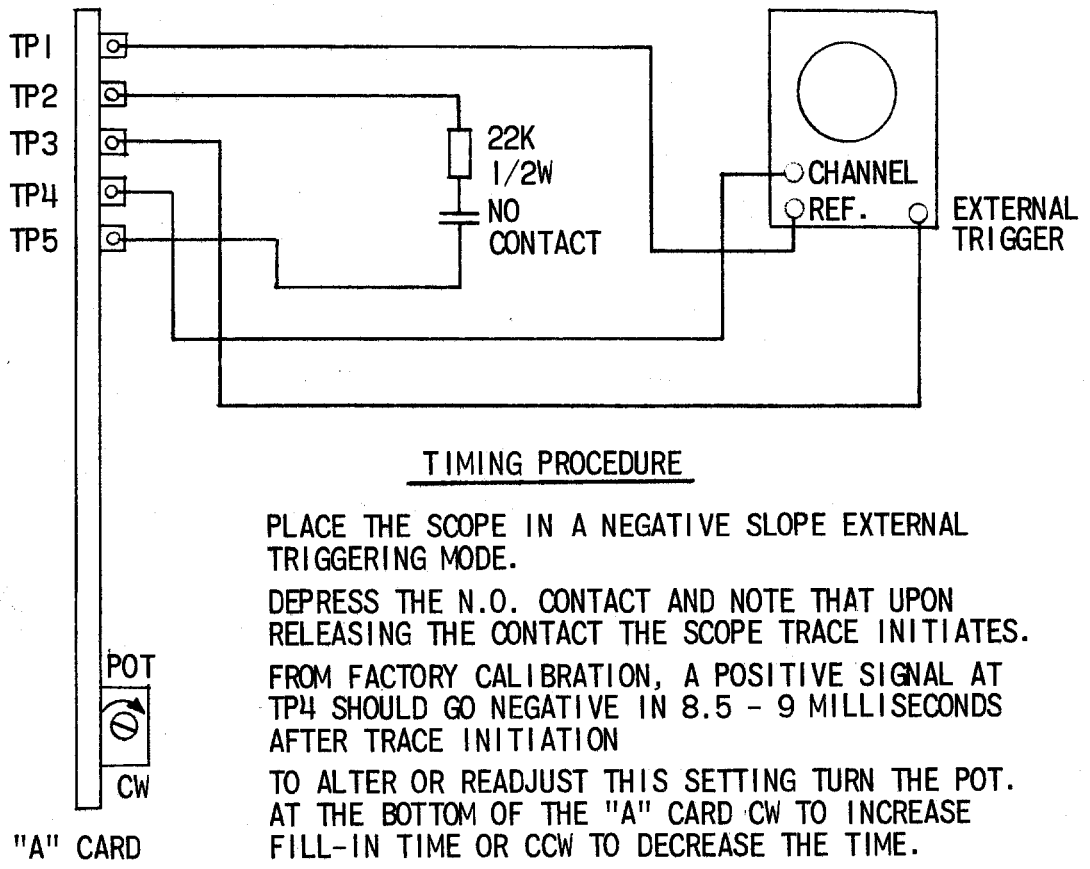


FIG. 16 (0227A7094-6) POWER SUPPLY FOR THE SBC41A RELAY ("Y" CARD)

INSTRUCTIONS:

1. APPLY RATED DC TO RELAY TERMINALS 17 (+) AND 18 (-).
2. CHECK THAT THE CT CURRENTS INTO THE RELAY CIRCUITS EQUAL ZERO. (PULL LOWER CONNECTION PLUG).
3. SET UP OSCILLOSCOPE AND CONTACT CIRCUITS AS SHOWN BELOW.
4. BE SURE THAT THE OSCILLOSCOPE POWER CHORD IS UNGROUNDED.



TIMING PROCEDURE

PLACE THE SCOPE IN A NEGATIVE SLOPE EXTERNAL TRIGGERING MODE.

DEPRESS THE N.O. CONTACT AND NOTE THAT UPON RELEASING THE CONTACT THE SCOPE TRACE INITIATES.

FROM FACTORY CALIBRATION, A POSITIVE SIGNAL AT TP4 SHOULD GO NEGATIVE IN 8.5 - 9 MILLISECONDS AFTER TRACE INITIATION

TO ALTER OR READJUST THIS SETTING TURN THE POT. AT THE BOTTOM OF THE "A" CARD CW TO INCREASE FILL-IN TIME OR CCW TO DECREASE THE TIME.

FIG. 17 (0246A2203-0) FILL-IN TIME SETTING TEST CIRCUIT FOR THE SBC41A RELAY

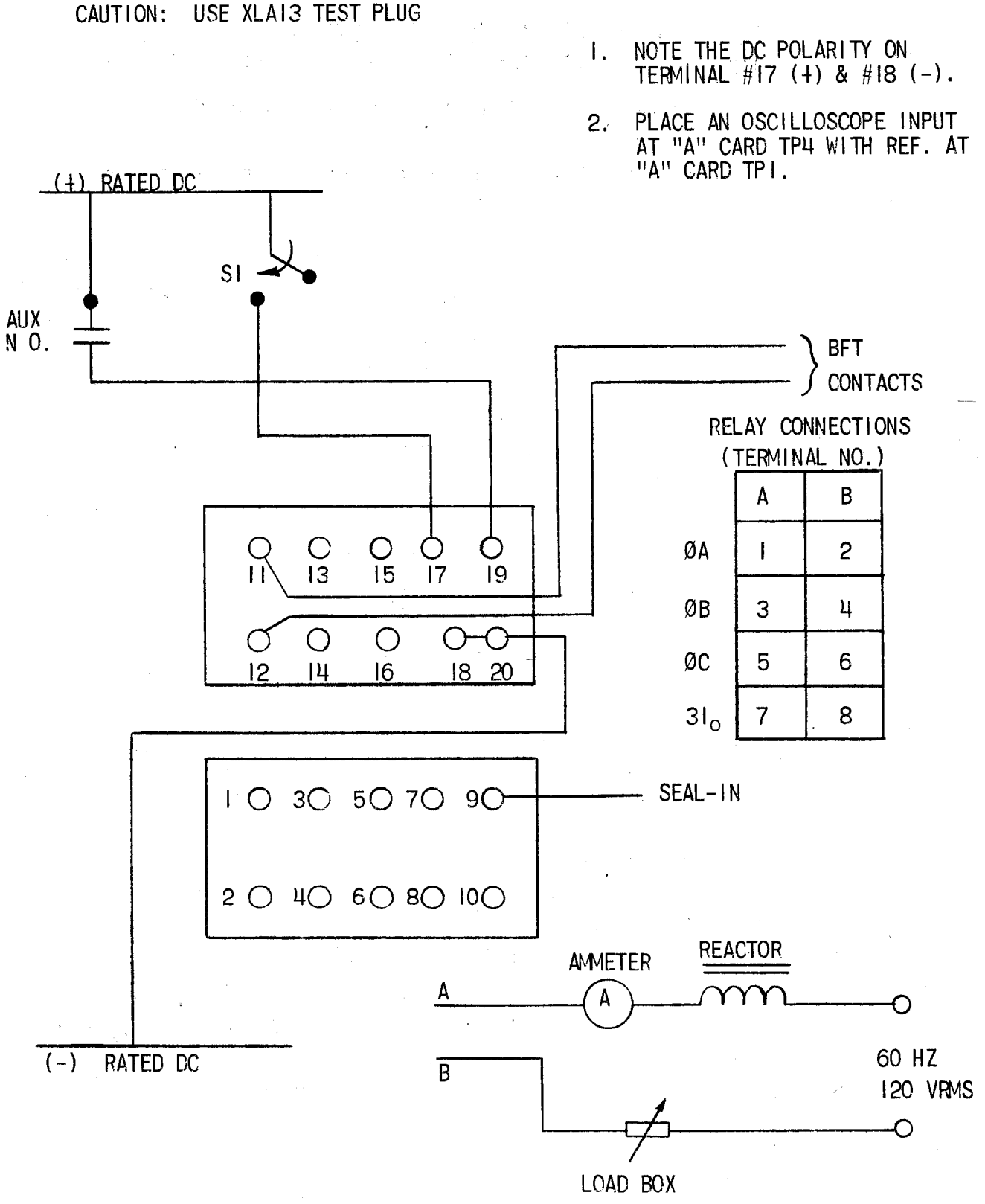


FIG. 18 (0246A2204-1) CURRENT DETECTOR TEST CIRCUIT FOR THE SBC41A RELAY

CAUTION : SYSTEM CIRCUITS AT CONTACT TERMINALS #11 AND #12 MUST BE REMOVED FOR TEST (USE AN XLA13 TEST PLUG)

a. SET AMMETER CURRENT (A) TO 5 TIMES THE PICK-UP CURRENT LEVEL.

b. INITIATE TIMING SEQUENCE BY CLOSING THE BFI CONTACT.

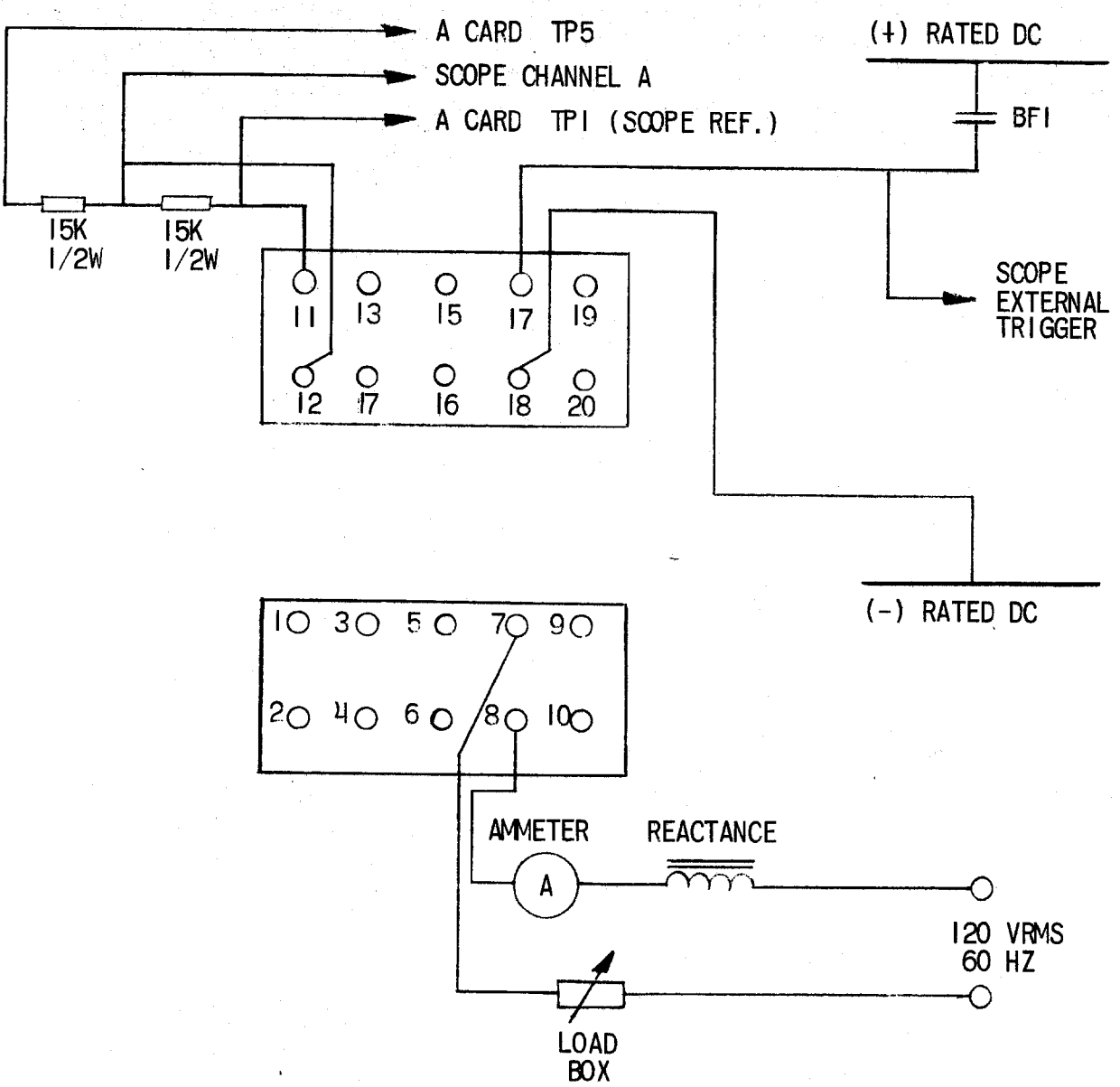


FIG. 19 (0246A2202-1) OVERALL TIMING TEST CIRCUIT FOR THE SBC41A RELAY

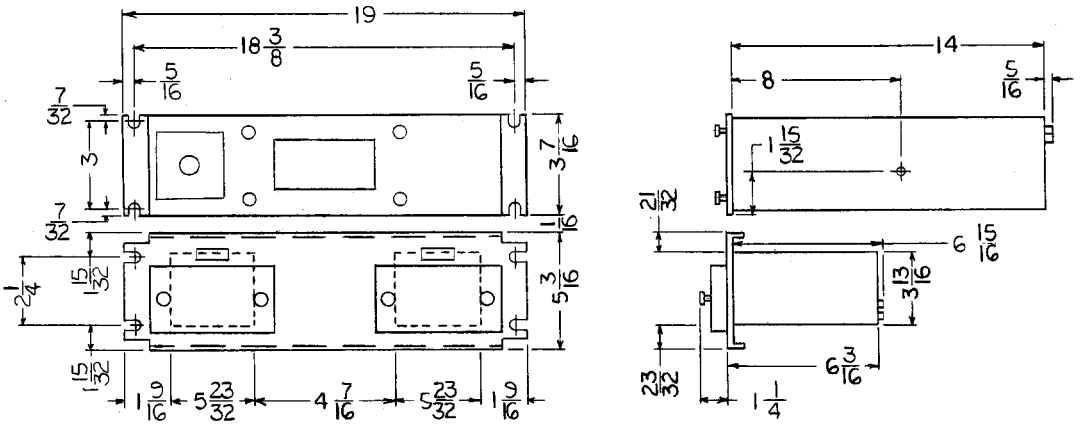
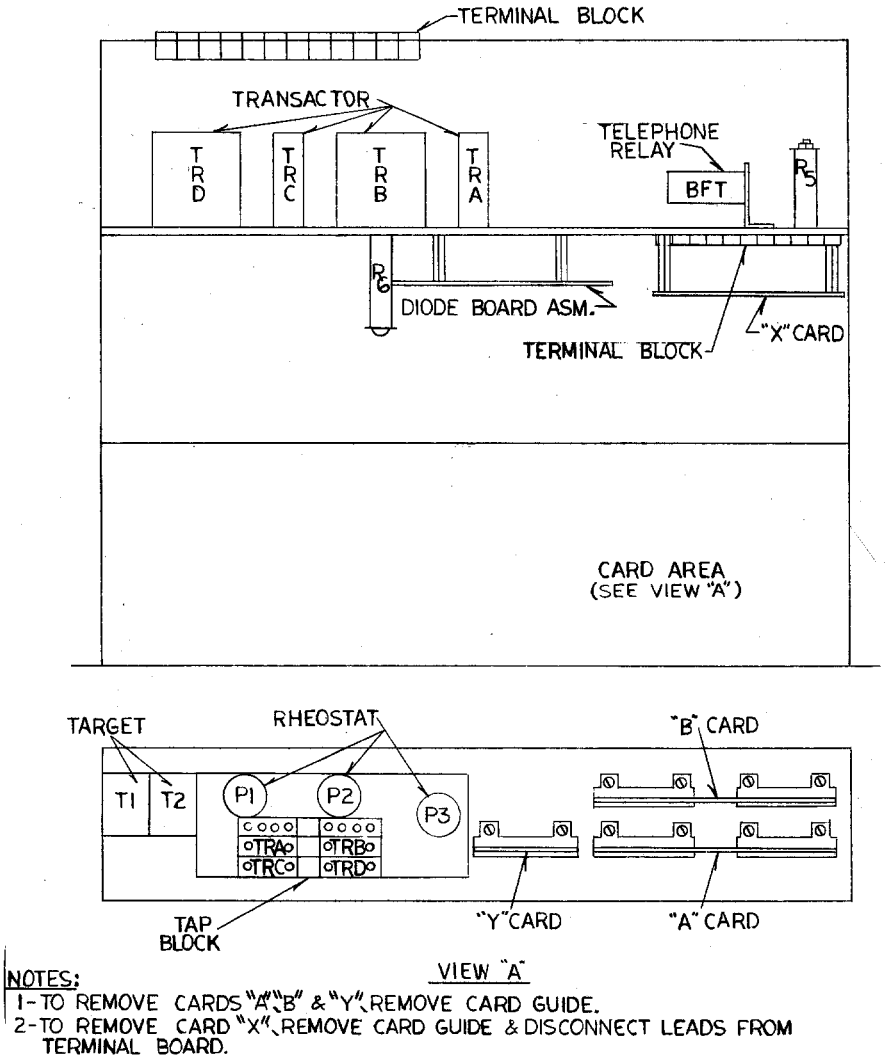
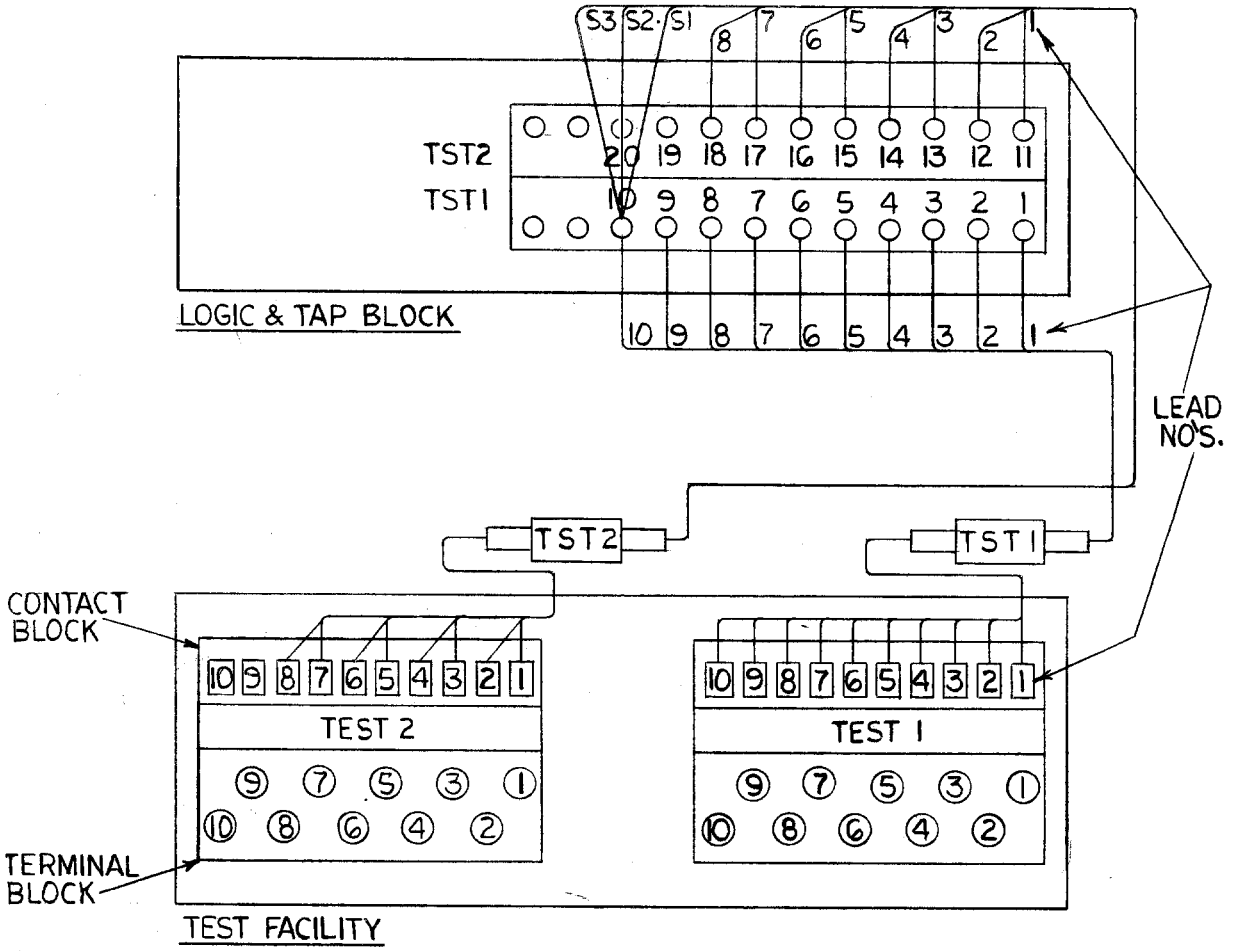


FIG. 20 (0257A5723-0) OUTLINE AND MOUNTING DIMENSIONS LOGIC AND TAP BLOCK WITH TEST PANEL



NOTES:
1-TO REMOVE CARDS "A","B" & "Y", REMOVE CARD GUIDE.
2-TO REMOVE CARD "X", REMOVE CARD GUIDE & DISCONNECT LEADS FROM TERMINAL BOARD.

FIG. 21 (0257A5721-4) COMPONENT LOCATION DIAGRAM LOGIC AND TAP BLOCK



BACK VIEW

FIG. 22 (0257A5056-2) CONNECTION OF LOGIC AND TAP BLOCK WITH TEST PANEL

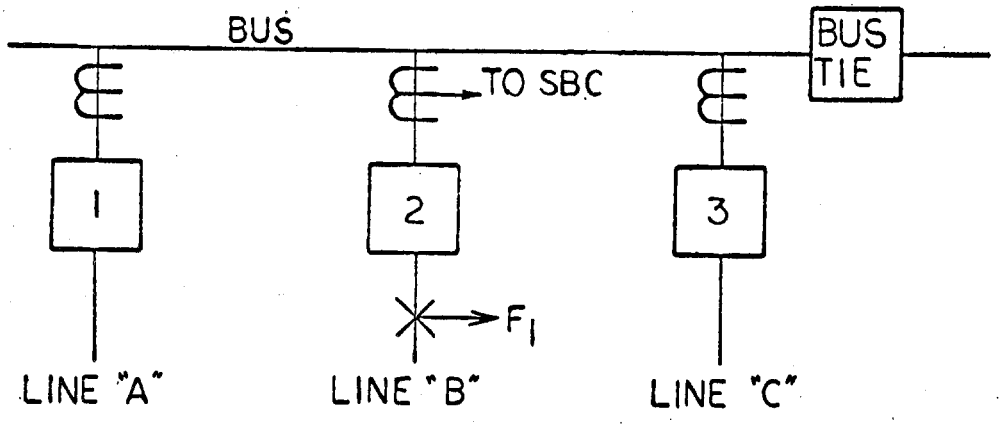


FIG. 23 (0246A2279-1) RELAY APPLICATION SINGLE BUS, SINGLE BREAKER

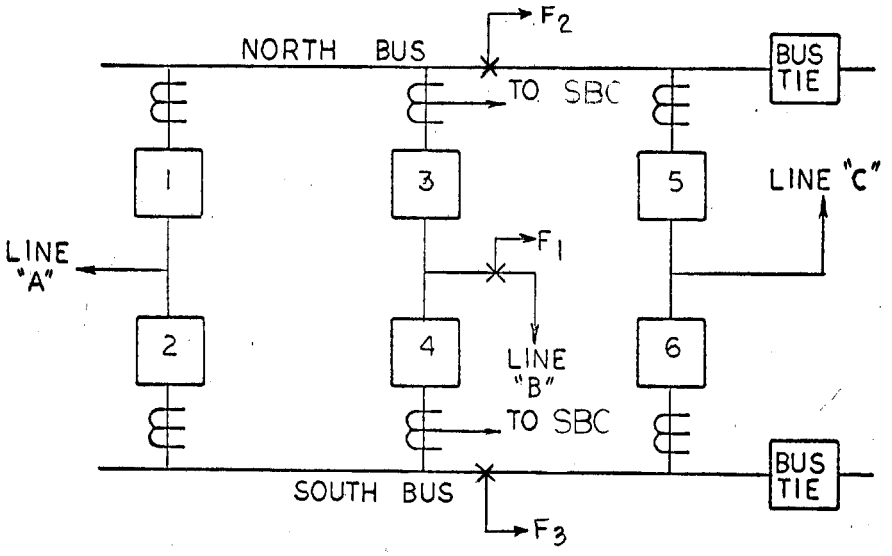


FIG. 24 (0246A2277-2) RELAY APPLICATION DOUBLE BUS, DOUBLE BREAKER

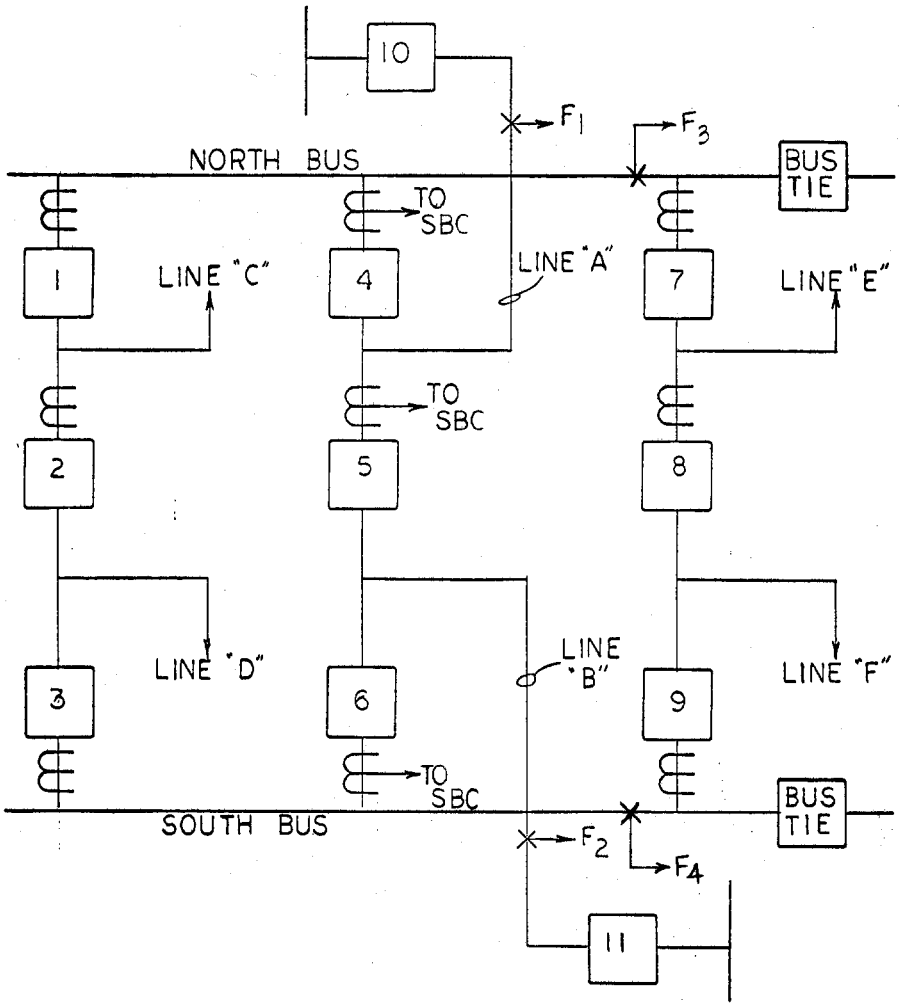


FIG. 25 (0246A2280-2) RELAY APPLICATION BREAKER-AND-A-HALF

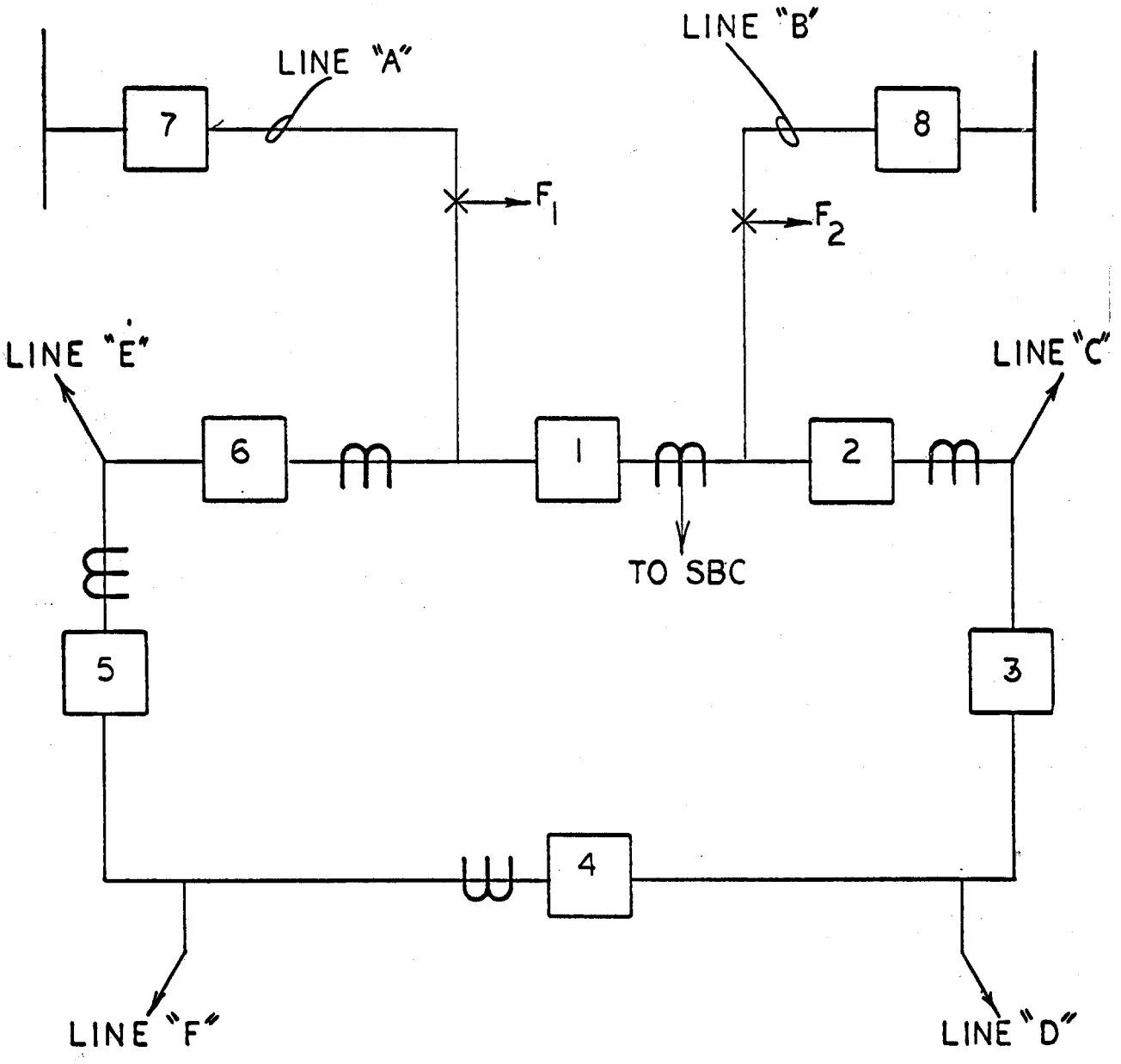


FIG. 26 (0246A2278-1) RELAY APPLICATION RING BUS

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