**INSTRUCTIONS** GEK-45461

# STATIC FEEDER POTENTIAL RELAY

## TYPE SFV71A

GENERAL ELECTRIC

CONTENTS

# STATIC FEEDER POTENTIAL RELAY TYPE SFV71A

## DESCRIPTION

The type SFV71A relay is a static voltage detector relay that was designed specifically to detect voltage level variations on a three phase feeder circuit employing shunt capacitors. The relay utilizes symmetrical components, derived from system quantities, to operate associated level detectors and logic circuitry to determine whether the capacitors should be placed in or removed from service. A type SSA power supply and an equipment test panel are also required to form a complete terminal of equipment.

The relay is packaged in a four-rack unit case (one rack unit = 1.75 inches) suitable for mounting in a standard 19 inch rack. The internal connections for the relay are shown in Figure 2 and the component location diagram is shown in Figure 3. Detailed information on the printed circuit cards can be found in GEK-34158. The relay outline and mounting dimensions are shown in Figure 1.

The following functions are included in the SFV71A relay:

### LEVEL DETECTORS

$V_{1-1}$ High set positive sequence voltage level detector
$V_{1-2}$ Low set positive sequence voltage level detector
$V_{1-3}$ High set positive sequence voltage level detector
$V_2$ Low set negative sequence voltage level detector
$V_0$ Low set zero sequence voltage level detector

### OUTPUT FUNCTIONS

T1 Telephone relay, 4 normally open contacts
T2 Telephone relay, 2 normally open contacts
R1 Reed relay, 2 normally open contacts

### CONTACT CONVERTERS

Two Contact Converters, CC1 and CC2, are provided to convert the operation of normally open external contacts into input signals compatible with the relay logic.

## APPLICATION

The SFV71A relay is designed specifically for application in those circuits employing shunt capacitors. The relay uses positive, negative and zero sequence voltage components with associated level detectors to determine if the shunt capacitors should be placed in or removed from service.

Basically, the relay will permit the capacitors to be placed in service as the result of a voltage dip caused by the loss of a line or loss of a generator, etc. On the other hand, the logic is so arranged that it will prevent insertion of the capacitors during fault conditions. A level detector is also provided to initiate removal of the capacitors when the system voltage rises above a preset level. The contact converters enabled the user to initiate insertion or block insertion of the capacitors via externally operated contacts.

For a complete description of the scheme in which the relay is employed, refer to the overall logic diagram and description supplied with each terminal of equipment.

## RATINGS

The Type SFV71A relay is designed for use in an environment where the ambient temperature around the relay case is between -20°C and +65°C.

The Type SFV71A relay requires a ±15 volt d-c power source which can be obtained from a Type SSA power supply.

The positive and negative sequence potential circuits of the Type SFV71A relay are rated at 208 volt a-c or 120 volt a-c; see the unit nameplate.

The zero sequence potential circuit may be rated at 69 volt a-c or 120 volt a-c for continuous duty. Refer to the unit nameplate for the specific rating. The corresponding one second ratings are 360 volt a-c and 208 volt a-c, respectively.

The contacts of the telephone type relays that are used for the T1 and T2 functions, will make and carry three amperes continuously and will interrupt up to 180 volt amperes resistive (60 volt amperes inductive).

The contacts of the reed relay that is used for R1 is rated at 100 volt amperes. It will make and carry three amperes continuous current.

Each converter in this relay has a link for selecting the proper voltage for the coil circuit of the contact converter. The three possible voltages are 48 volt d-c, 125 volt d-c and 250 volt d-c.

## BURDENS

The Type SFV71A relay presents a maximum burden to the Type SSA power supply of:

300 milliamperes from the +15 volt d-c supply

270 milliamperes from the -15 volt d-c supply

Each contact converter, when energized, will draw approximately 10 milliamperes from the station battery, regardless of the top setting.

The a-c potential burden (ø-ø) is as follows:

| | POSITIVE SEQUENCE CIRCUIT | NEGATIVE SEQUENCE CIRCUIT | ZERO SEQUENCE CIRCUIT |
|---|---|---|---|
| R | 20000 | 20000 | 17487 |
| X | 46700 | 46700 | 6431 |
| Z | 50802 | 50802 | 18632 |

## RANGES

The ranges given in this section are typical for the Type SFV71A relay. Refer to the unit nameplate for the ranges of a particular relay.

$V_{1-1}$ 90-105 percent of rated phase-to-phase voltage

$V_{1-2}$ 70- 90 percent of rated phase-to-phase voltage

$V_{1-3}$ 95-115 percent of rated phase-to-phase voltage

$V_2$ 2-20 percent of rated phase-to-phase voltage

$V_0$ 2-2 percent of rated phase-to-neutral voltage

## OPERATING PRINCIPLES

### INTRODUCTION

The SFV71A relay uses signals derived from positive, negative and zero sequence components to operate various level detectors in the unit.

POSITIVE SEQUENCE VOLTAGE NETWORK

The positive sequence voltage network is shown on the internal connection diagram of Figure 2. The positive sequence voltage network consists of three phase-to-phase voltage transformers (TA, TB, TC) and an active (uses operational amplifiers) sequence network which is contained on the F154 printed circuit card in position AG. The voltage at test point TP19 is given by the relationship:

$$V_{TP2} = 0.017 \times V_{A-P}$$

$V_{A-P}$ is the positive sequence component of the input voltage.

NEGATIVE SEQUENCE VOLTAGE NETWORK

The negative sequence voltage network is shown on the internal connection diagram of Figure 2. The negative sequence voltage network consists of three phase-to-phase voltage transformers (TD, TE, TF) and an active (uses operational amplifiers) sequence network which is contained at the F155 printed circuit card in position J. The voltage at test point TP13 is given by the relationship:

$$V_{TP13} = 0.017 \times V_{A-N}$$

$V_{A-N}$ is the negative sequence component of the input voltage.

Potentiometers P1 and P2 are used to cancel small errors due to the potential source which supplies the relay.

ZERO SEQUENCE VOLTAGE NETWORK

Zero sequence voltage is applied to the input of a level detector which is contained in the D117 printed circuit card in position H. An output from this level detector is produced whenever the value of the zero sequence voltage is greater than its preset pickup level.

CONTACT CONVERTERS

The purpose of this function is to convert a contact operation into a signal that is compatible with the logic circuit of the SFV71A; this permits manual control of the unit from a remote position. These contact converters are labeled CC1 and CC2 on the overall logic drawing; they are labeled RR1 and RR2 on the internal connections drawing for the SFV71A, Figure 2.

## CALCULATIONS OF SETTINGS

See the overall logic diagram and description supplied with each scheme for the proposed settings to be made on the various functions included in this relay.

## RECEIVING HANDLING AND STORAGE

These relays will normally be supplied as a part of a static relay equipment, mounted in a rack or cabinet with other static relays and test equipment. Immediately upon receipt of a static relay equipment, it should be unpacked and examined for any damage sustained in transit. If injury or damage resulting from rough handling is evident, file a damage claim at once with the transportation company and promptly notify the nearest General Electric Sales Office.

Reasonable care should be exercised in unpacking the equipment. If the equipment is not to be installed immediately, it should be stored indoors in a location that is free from moisture, dust, and metallic chips, and severe atmospheric contaminants.

Just prior to final installation the shipping support bolt should be removed from each side of all relay units to facilitate possible future unit removal for maintenance. These shipping support bolts are approximately eight inches back from the relay unit front panel. Static relay equipment, when supplied in swing rack cabinets, should be securely anchored to the floor or to the shipping pallet to prevent the equipment from tipping over when the swing rack is opened.

## INSTALLATION TESTS

CAUTION

THE LOGIC SYSTEM SIDE OF THE D-C POWER SUPPLY USED WITH MOD III STATIC RELAY EQUIPMENT IS ISOLATED FROM GROUND. IT IS A DESIGN CHARACTERISTIC OF MOST ELECTRONIC INSTRUMENTS THAT ONE OF THE SIGNAL INPUT TERMINALS IS CONNECTED TO THE INSTRUMENT CHASSIS. IF THE INSTRUMENT USED TO TEST THE RELAY EQUIPMENT IS ISOLATED FROM

GROUND, ITS CHASSIS MAY HAVE AN ELECTRICAL POTENTIAL WITH RESPECT TO GROUND. THE USE OF A CONNECTION TO THE EQUIPMENT, SUCH AS A TEST LEAD INADVERTENTLY DROPPING AGAINST THE RELAY CASE, MAY CAUSE DAMAGE TO THE LOGIC CIRCUITRY.

NO EXTERNAL TEST EQUIPMENT SHOULD BE LEFT CONNECTED TO THE STATIC RELAYS WHEN THEY ARE IN PROTECTIVE SERVICE, SINCE TEST EQUIPMENT GROUND REDUCES THE EFFECTIVENESS OF THE ISOLATION PROVIDED.

## CONSTRUCTION

The SFV71A relay is packaged in an enclosed metal case with a hinged front cover and removable top cover. The case is suitable for mounting in a standard 19 inch rack. The outline and mounting dimensions and the physical location of the components are shown in Figures 1 and 3 respectively.

The potential is brought into the SFV71A through twelve-point terminals strips located on the rear of the relay case. The a-c potential connections are made on the FA terminal strip and the d-c input connections for the contact converter are made on the FD terminal strip.

Connection to the R1, T1 and T2 contacts is made through twelve-point terminal strips located on the rear of the relay case. The R1 and T2 contact connections are made on the FB terminal strip; the T1 contact connections are made on the FC terminal strip.

The SFV71A relay contains printed circuit cards identified by a code number such as: F154, D117, L102 where F designates filter, D designates level detector and L designates logic. The printed circuit cards plug in from the front of the unit. The sockets are identified by letter designations or addresses (J, K, L, etc.) which appear on the guide strips in front of each socket, on the connection diagram and on the printed circuit card itself. The test points (TP1, TP2, etc.), shown on the internal connections diagram, are connected to instrument test jacks on a test card in position T or AT. The jacks are numbered from top to bottom with TP1 to TP10 on the AT card and TP11 to TP20 on the T card. TP1 is connected to relay reference, TP2 is connected to -15 volt d-c and TP10 to +15 volt d-c. Output signals are measured with respect to relay reference. Logic signals are approximately +15 volt d-c for the ON or "logic one" condition, and less than 1 volt d-c for the OFF or "logic zero" condition. Filter card outputs are analog signals with a range of -15 volt to +15 volt.

The internal connections and information on design and testing of the printed circuit cards may be found in the Printed Circuit Card Instruction Book, GEK-34158.

Relay signals can be monitored with an oscilloscope, a portable high impedance voltmeter or the equipment test panel meter. When time-delay cards are to be adjusted or checked, an oscilloscope which can display two traces simultaneously and which has a calibrated horizontal sweep should be used.

## REQUIRED TESTS AND ADJUSTMENTS

The SFV71A relay is usually supplied from the factory mounted and wired as part of a complete static relay equipment. The necessary tests and adjustments are listed below. All steps should be performed per the procedures under Detailed Testing Instructions to insure that no shipping damage has occurred. The steps should be performed in the order shown.

1) Negative sequence voltage network balance setting
2) Negative sequence network calibration
3) Positive sequence network calibration
4) Zero sequence calibration
5) Timer adjustment

## Detailed Testing Instructions

### 1) Negative Sequence Voltage Network Balance Check

The purpose of this test is to adjust the trimmer potentiometers P1 and P2. Because these potentiometers are intended to correct small errors due to the potential source, it is necessary to set these pots with the unit connected to the system. For preliminary tests before installation, these potentiometers may be left at the factor setting.

With the connections of Figure 4 observe the waveform at TP13 with the oscilloscope. This voltage should be less than 0.2 volt peak-to-peak and consist primarily of a third harmonic. Potentiometers P1 and P2 should be alternately adjusted to obtain the lowest possible signal magnitude at TP13.

2) Negative Sequence Network Calibration

Using the negative sequence connections of Figure 5, apply rated (ø-ø) potential. Use a voltmeter and check for 1.7 to 2.3 volt rms at TP13.

$V_2$ Pickup Level Adjustment - Adjust the potential source to the voltage level that is equal to the desired pickup level for the negative sequence level detector (V2). Observe the output at test point TP15 with an oscilloscope. Adjust the potentiometer on the printed circuit card in position "K" to the position that causes the output at TP15 to just step to 15 volt d-c, turning the potentiometer clockwise increases the pickup setting of the card.

3) Positive Sequence Network Calibration

Using the positive sequence connections of Figure 6, apply the rated (ø-ø) potential. Use a voltmeter and check for 1.7 to 2.3 volt (rms) at TP19.

$V_{1-2}$ Pickup Level Adjustment - Adjust the potential source to the voltage level that is equal to the desired pickup level for the low level positive sequence level detector ($V_{1-2}$). Observe the output at test point TP12 with an oscilloscope. Adjust the potentiometer on the printed circuit card in position "AH" to the position that causes the output at TP12 to just step to 15 volt d-c.

$V_{1-1}$ Pickup Level Adjustment - Adjust the potential source to the voltage level that is equal to the desired pickup level for the positive sequence level detector ($V_{1-1}$). Observe the output at test point TP6 with an oscilloscope. Adjust the potentiometer on the printed circuit card in position "AJ" to the position that causes the output at TP6 to just step to 15 volt d-c.

$V_{1-3}$ Pickup Level Adjustment - Adjust the potential source to the voltage level that is equal to the desired pickup level for the high level positive sequence level detector ($V_{1-3}$). Observe the output at test point TP4 with an oscilloscope. Adjust the potentiometer on the printed circuit card in position "AK" to the position that causes the output at TP4 to just step to 15 volt d-c.

4) Zero Sequence Calibration

Make the zero sequence connections of Figure 7. Adjust the potential source to the voltage level that is equal to the desired pickup level for the zero sequence level detector ($V_0$). Observe the output at test point TP16 with an oscilloscope. Adjust the potentiometer on the printed circuit card in position "H" to the position that causes the output at TP14 to just step to 15 volt d-c.

5) Timer Adjustments

In order to adjust the time-delay cards, an oscilloscope that has a calibrated horizontal sweep is needed. The oscilloscope should be able to display two traces simultaneously or it should have provisions for external triggering.

When adjusting a timer card it is necessary to remove the card which supplies the input to the timer. The timer test circuit should be connected to the test point at the card input and the vertical input to the oscilloscope should be connected to the test point at the card output. The oscilloscope trigger or second vertical input should also be connected to the test point at the input to the card.

The timer test circuit is shown in Figure 8. Opening the normally closed contact causes the output to step up to +5 volts d-c after the pickup delay of the timer. To increase the pickup time, turn the potentiometer on the timer card clockwise; to decrease the time, turn it counterclockwise. Closing the contact causes the timer output to drop out. Check the internal connections, Figure 2, for the locations of the printed cards and test points.

OVERALL EQUIPMENT TEST

After the SFV71A relay has been calibrated, a series of operating checks is advisable.

The elementary, overall logic, and logic description for the specific job will be useful. The test can be performed by applying a-c potential to the relay, varying the magnitude of this potential and checking that the proper output is obtained as each level detector operates.

## PERIODIC CHECKS AND ROUTINE MAINTENANCE

### PERIODIC TESTS

All the functions included in the SFV71A relay may be checked at periodic intervals using the procedures described in Installation Tests.

The following checks should be made during periodic tests:

a) Negative sequence pickup level check ($V_2$)

b) Positive sequence pickup level checks ($V_{1-1}$, $V_{1-2}$ and $V_{1-3}$)

c) Zero sequence pickup level check ($V_0$)

### TROUBLE SHOOTING

Any trouble shooting of the equipment can be done by signal tracing; by using the logic diagram and the various test points, it should be possible to quickly isolate the trouble.

A test adapter card is supplied with each static relay equipment to supplement the prewired test points on the test cards. Use of the adapter card is described in the card instruction book GEK-34158.

A dual-trace oscilloscope is a valuable aid to detailed trouble shooting, since it can be used to determine phase shift, operate and reset times as well as input and output levels. A portable dual-trace oscilloscope with a calibrated sweep and trigger facility is recommended.

### SPARE PARTS

To minimize possible outage time, it is recommended that a complete maintenance program should include the stocking of at least one spare card of each type. It is possible to replace damaged or defective components on the printed circuit cards, but great care should be taken in soldering so as not to damage or bridge-over the printed circuit busses, or overheat the semi-conductor components. The repaired area should be recovered with a suitable high-dielectric plastic coating to prevent possible breakdowns across the printed busses due to moisture and dust. The wiring diagrams for the cards in the SFV71A relay are included in the card book GEK-34158; the card types are shown on the component location diagram (Figure 3).

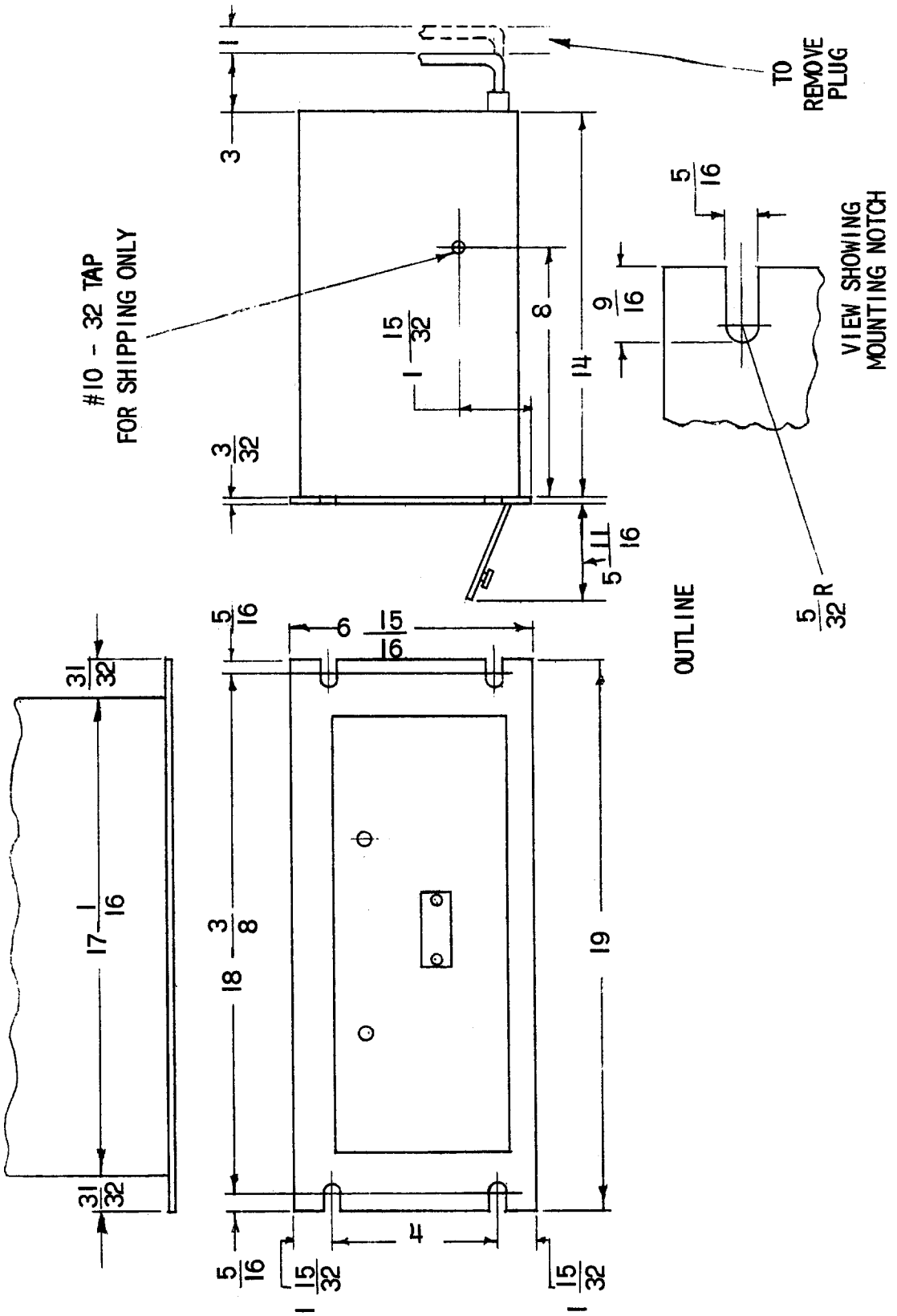



Fig. 1 (0227A2037-0) OUTLINE AND MOUNTING DIMENSIONS FOR THE TYPE SFV71A RELAY

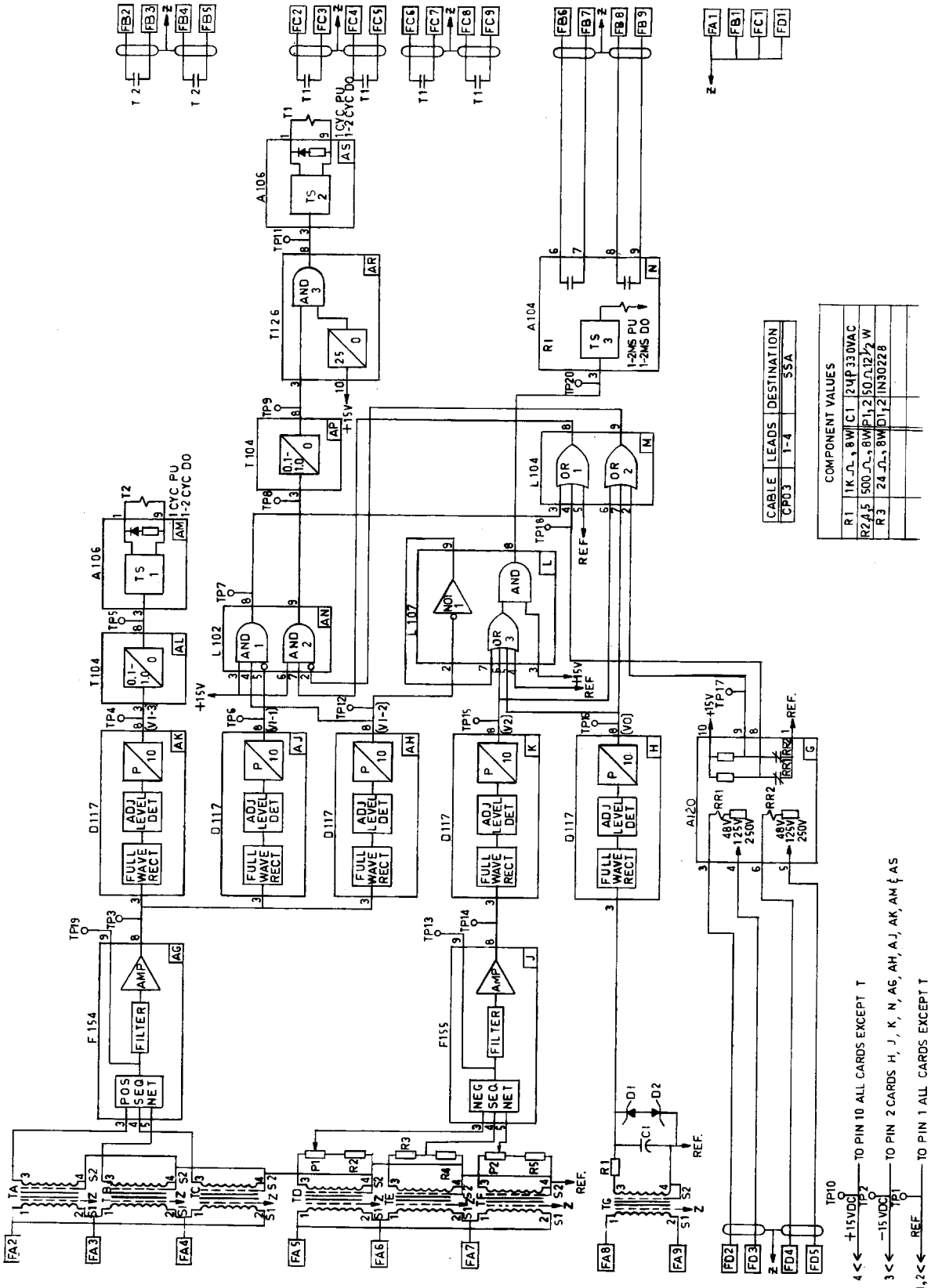
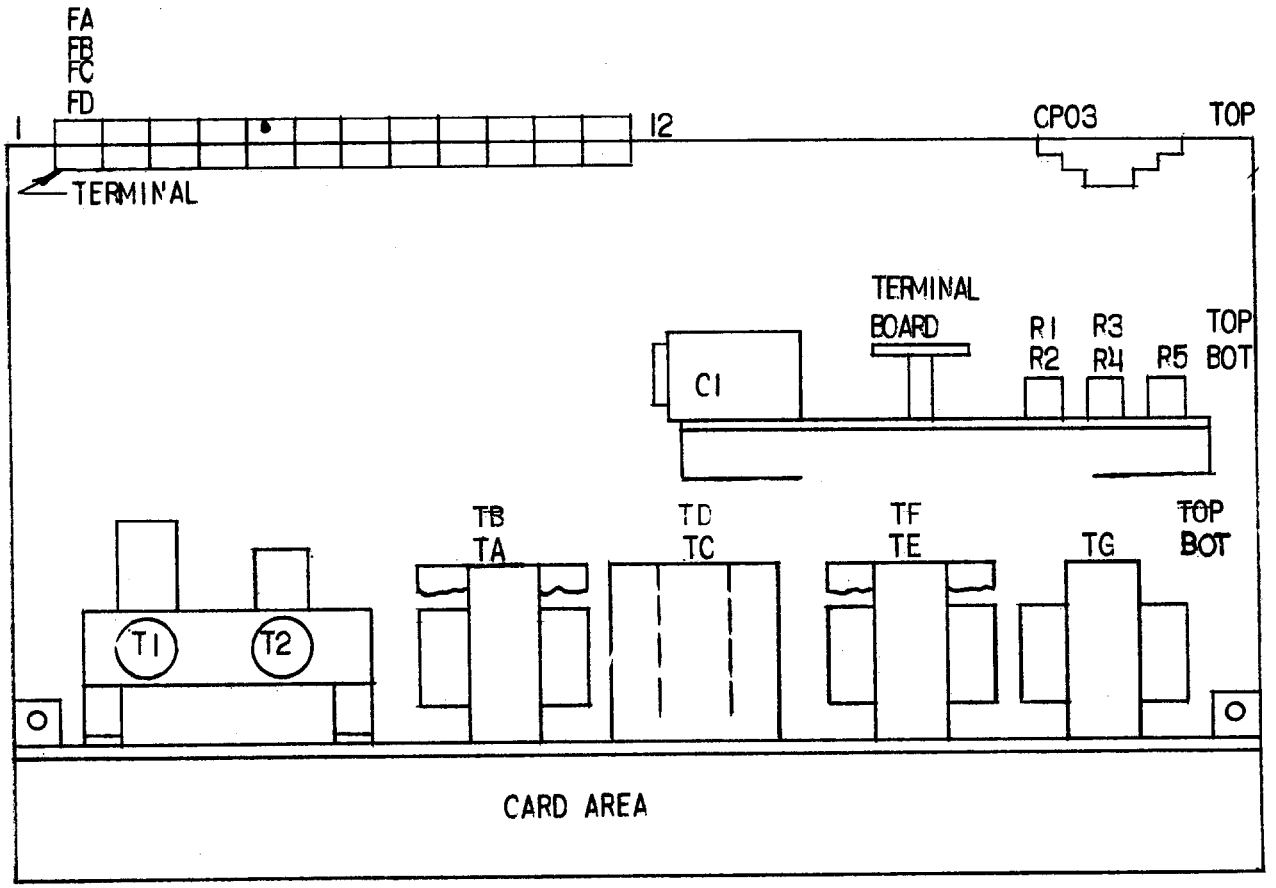
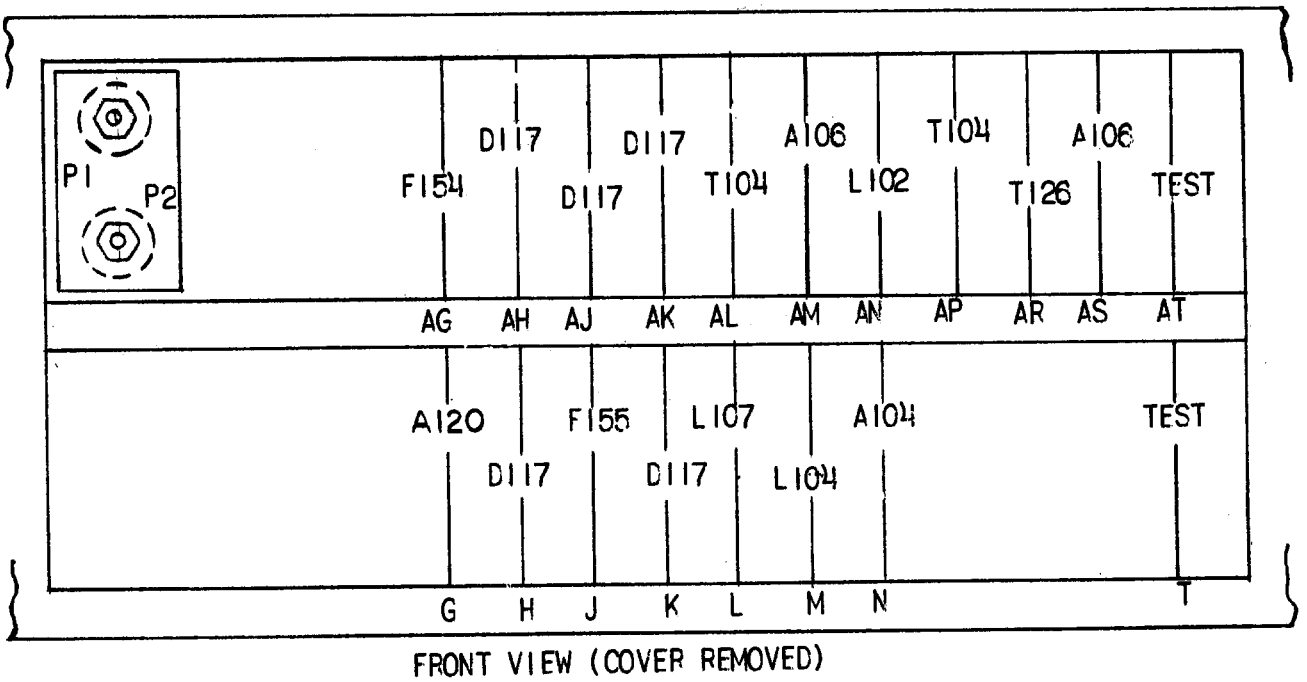



Fig. 2 (0171C7818-1) INTERNAL CONNECTIONS DIAGRAM FOR THE TYPE SFV71A RELAY

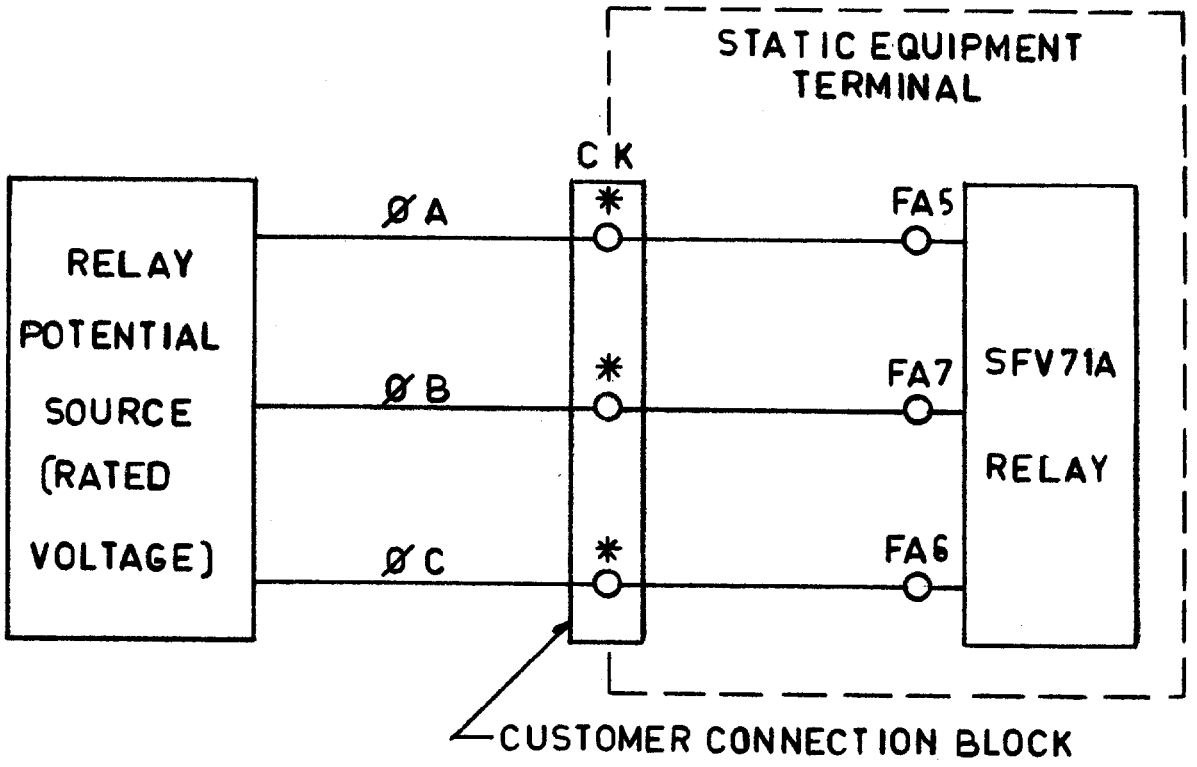



PLAN VIEW (COVER REMOVED)



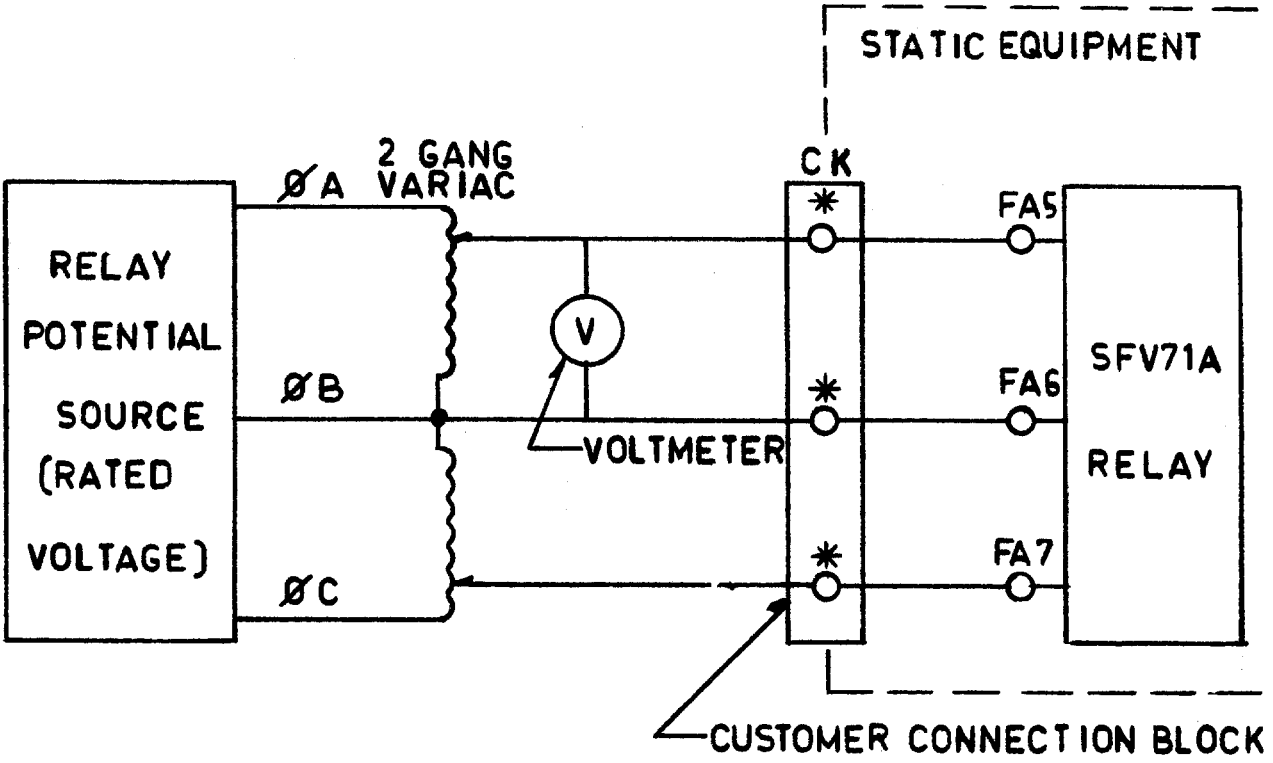

FRONT VIEW (COVER REMOVED)

Fig. 3 (0257A8727-0) COMPONENT LOCATION DIAGRAM FOR THE TYPE SFV71A RELAY



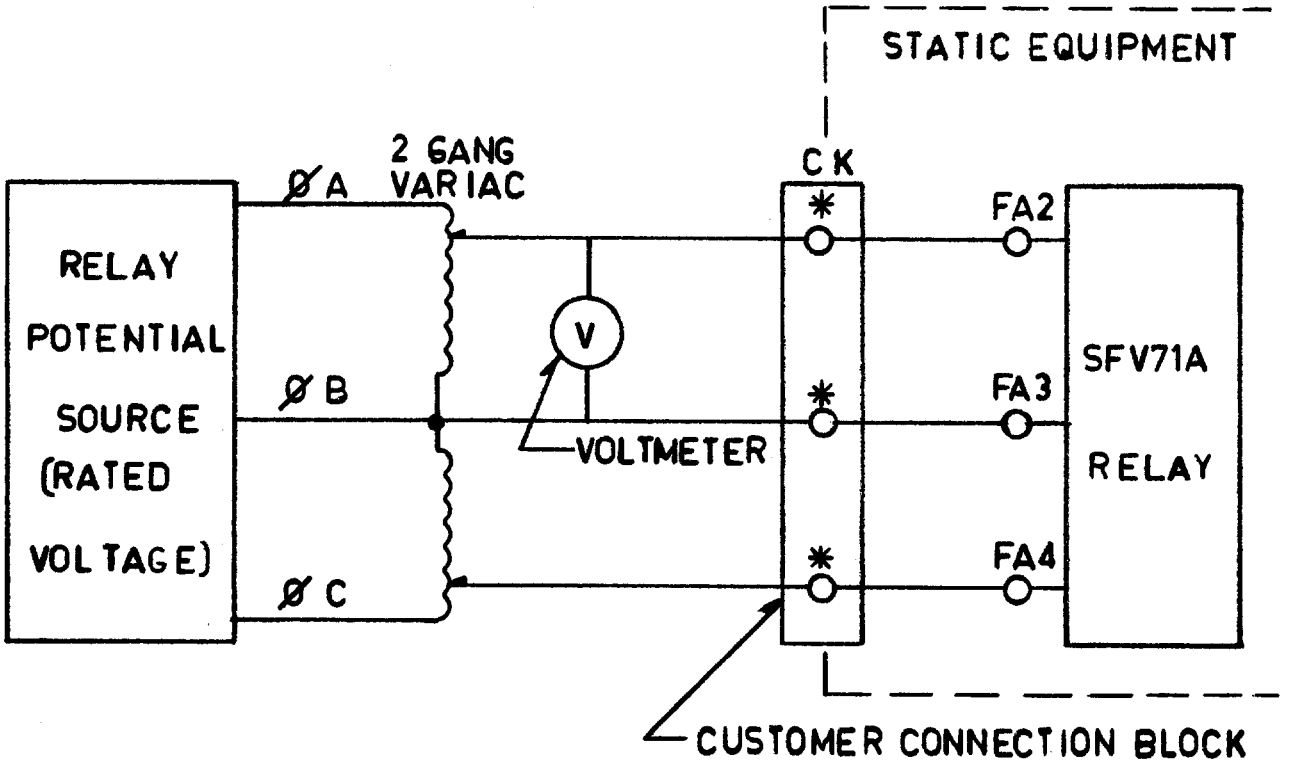

* SEE ELEMENTARY FOR TERMINAL NUMBERS ON CK BLOCK

Fig. 4 (0257A9627-0) TEST CIRCUIT FOR NEGATIVE SEQUENCE VOLTAGE NETWORK BALANCE CHECK



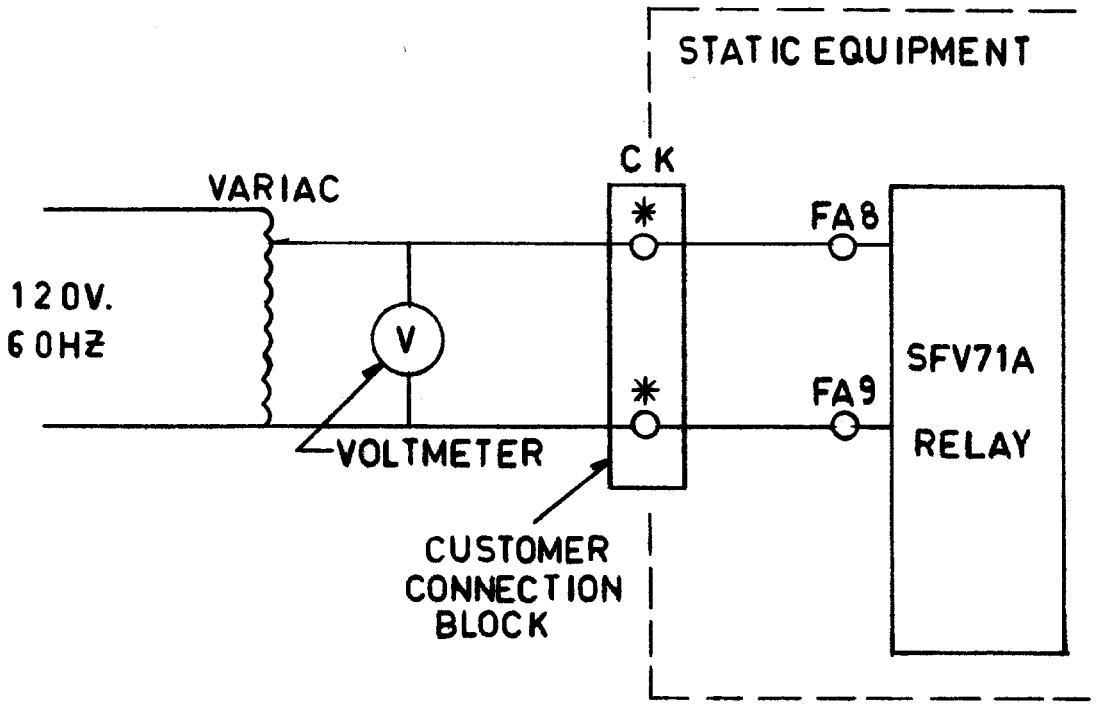

* SEE ELEMENTARY FOR TERMINAL NUMBERS ON CK BLOCK

Fig. 5 (0257A9628-0) NEGATIVE SEQUENCE VOLTAGE NETWORK TEST CIRCUIT



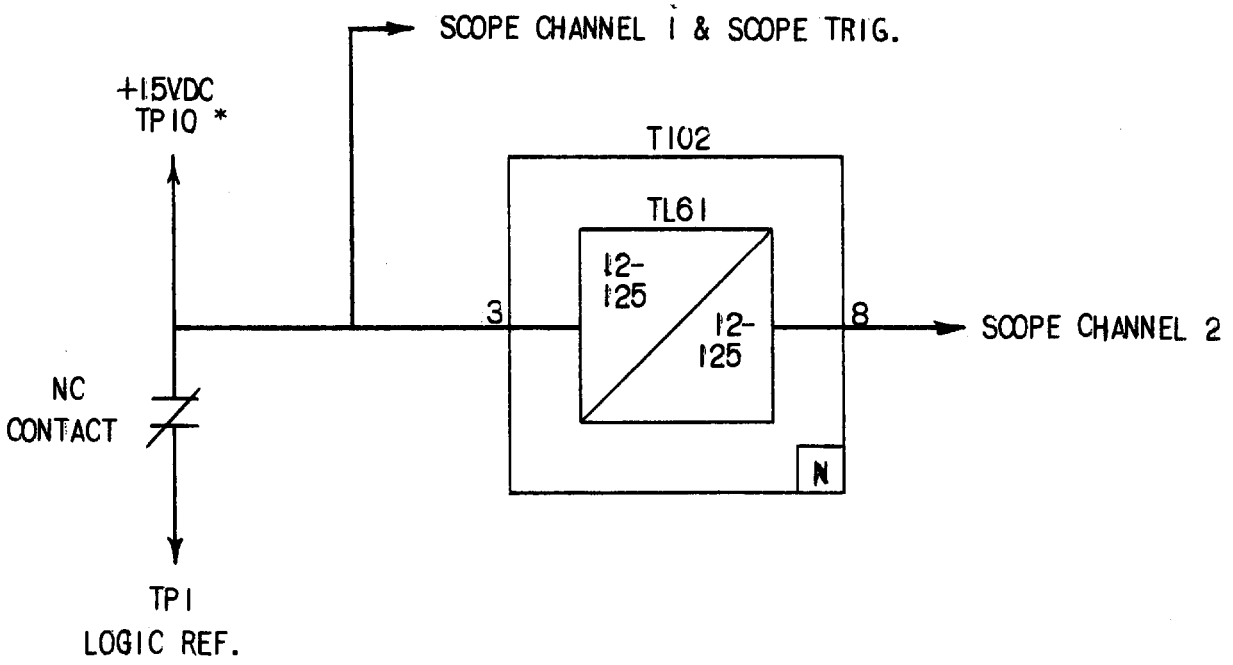

* SEE ELEMENTARY FOR TERMINAL NUMBERS ON CK BLOCK

Fig. 6 (0257A9629-0) POSITIVE SEQUENCE VOLTAGE NETWORK TEST CIRCUIT




* SEE ELEMENTARY FOR TERMINAL NUMBERS ON CK BLOCK

Fig. 7 (0257A9630-0) TEST CIRCUIT FOR THE ZERO SEQUENCE VOLTAGE LEVEL DETECTOR




* THE 15VDC SIGNAL AT PIN 10 HAS A CURRENT LIMITING RESISTOR MOUNTED ON THE TEST CARD.

Fig. 8 (0246A7987-0) LOGIC TIMER TEST CIRCUIT