INSTRUCTIONS

GEK- 34083

AUXILIARY LOGIC UNIT

TYPE SLA52A

POWER SYSTEMS MANAGEMENT DEPARTMENT

GENERAL ELECTRIC

CONTENTS

DESCRIPTION

The Type SLA52A relay is an auxiliary unit. The Type SLA52A relay is not intended to be used by itself, but rather as part of a complement of equipment that forms a protective relaying scheme. For a complete description of the overall scheme in which this relay is employed, refer to the overall logic diagram and its associated logic description that is supplied with each terminal of equipment.

The Type SLA52A relay is packaged in a four rack unit (1 R.U. = 1 3/4") enclosed metal case suitable for mounting on a 19 inch rack. The outline and mounting dimensions are shown in Figure 1. The internal connections for the SLA52A relay are shown in Figure 2. The component and card locations are shown in Figure 3.

APPLICATION

The Type SLA52A relay was originally designed to operate in conjunction with Type SLYP, Type SLYN, Type SLC, Type SLLP, Type SLAT and Type SSA relays in a directional comparison scheme for series compensated lines. The SLA52A design incorporates circuit flexibility to permit various logic options. Refer to the overall logic diagram and associated option chart for a particular equipment to determine which logic options are utilized. If unconnected matrix option points are shown on the associated overall logic diagram it is the users responsibility to select the desired utilization. The logic description that accompanies the overall logic diagram will generally discuss the merits of those options indicated on the overall logic diagram.

RATINGS

The Type SLA52A relay is designed for use in an environment where the air temperature outside the relay case does not exceed $65^{o}C$.

The Type SLA52A relay requires a ±15 VDC power source which can be obtained from a Type SSA power supply.

Each contact converter in this relay has a link for selecting the proper voltage for the coil circuit of the contact converter. The three possible voltages are 48 VDC, 125 VDC and 250 VDC.

BURDENS

The SLA52A relay presents a burden of 350 ma to the +15 VDC supply of the Type SSA power supply.

Each contact converter, when energized, will draw approximately 10 ma. from the station battery, regardless of tap setting.

OPERATING PRINCIPLES

A. LOGIC CIRCUIT

The functions of the Type SLA52A relay involve basic logic (AND, OR, AND NOT) where the presence or absence of signals, rather than their magnitude, controls the operation. Signals are measured with respect to a reference bus accessible at TP1. In general, a signal below 1 VDC represents an OFF or LOGIC ZERO condition; an ON or LOGIC ONE condition is represented by a signal of approximately +15 VDC.

The symbols used on the internal connection diagram (Figure 2) are explained by the legend shown in Figure 4.

The matrix block options shown in the internal connections of the SLA52A relay are provided at the factory. The connections are shown on the associated overall logic and are listed on the associated option chart. A sample option chart for the Type SLA52A relay is shown in Figure 5.

B. CONTACT CONVERTERS

The purpose of this function is to convert a contact operation into a signal that is compatible with the logic circuit of the Type SLA52A relay. These contact converters are labeled CC1, CC2, and CC3. These contact converters have a non-adjustable 4 millisecond pickup delay.

CC1

Contact Converter 1 is energized by a contact associated with the external reclose circuitry and provides the solid state logic with a logic 1 when reclosure is initiated. The output of CC1 energizes TL5 which provides an inhibit signal to M_1B. This inhibit signal prevents M_1B operation following breaker main pole closure.

CC2

Contact Converter 1 is energized by a contact associated with the external reclose circuitry and provides the solid state logic with a logic 1 when reclosure is initiated. The output of CC1 energizes TL5 which provides an inhibit signal to M_1B. This inhibit signal prevents M_1B operation following breaker main pole closure.

CC2

Contact Converter 2, when energized, keys the transmitter.

CC3

CC3 supplies one input to AND15 and is energized by a channel failure indication contact. A combination of reclose attempt indication, fault detector output and a channel failure will produce an AND15 direct trip output.

C. DATA MONITORING POINTS

The Type SLA52A relay has provisions to provide 36 data monitoring outputs. These data monitoring (DLA) points are selected on the matrix blocks and are listed on the option chart (Figure E). A data logging amplifier (DLA) unit is used to translate these logic signals into usable outputs.

D. CHANNEL INTERFACE

The logic of the Type SLA52A relay includes an isolation interface (Figure 6) between the relays in the scheme and the associated channel. The circuitry of the isolation interface provides a signal path but maintains metallic isolation. This feature makes it possible to maintain isolation between the DC supply used for the relays and that employed by the channel.

When pins 9 and 10 are both connected to relay reference, a metallically separate positive logic signal appears at pin 11 with respect to 12. The output from the isolation interface is a 5 VDC, 20 ma. signal.

CALCULATION OF SETTINGS

This section covers those timers in the SLA52A that require field adjustment.

TL2 (10-30/100-300)

The TL2 timer maintains the MB blocking function output even though the MB measuring unit may reset for a sustained external three phase fault. This is explained in the logic description associated with a particular logic diagram. It is recommended that the pickup time be set at 30 milliseconds to allow reliable tripping for an internal three phase fault. The TL2 reset time must be set at least as long as the breaker failure total clearing time minus the reset time of the MB characteristic timer.

TL3 (1-8/10-80) AND TL10 (1-8/0) BLOCKING MODE

Together these two timers form the trip integrating function. The combined pickup delay of these two timers is given by:

Integrator P.U. = Blocking Unit P.U. - Tripping Unit P.U. + Margin + Channel Time

The maximum difference between blocking and tripping unit pickup is 2 ms. The recommended margin is 2 ms. The equation to determine the total integrator time is then:

Integrator P.U. = 4 + Channel Time (ms.)

It is recommended that the total trip integrator pickup delay never be set for less than 7 ms. It is further recommended that the TL3 timer pickup be set for 3 ms. and that the TL10 timer pickup be set for the remainder of the trip integrator pickup delay. The TL3 reset delay should be set at 10 ms.

TL3 (1-8/10-80): UNBLOCKING MODE

The TL10 timer is deleted when the unblocking mode is used. The TL3 pickup delay should be set for 5 ms. - channel time or 3 ms. whichever is greater. The reset delay should be set for 10 ms.

TL6 AND TL7 (10-80/0)

These two timers permit time delay to be introduced into the various direct trip logic circuits. Refer to the logic description associated with a particular logic diagram for a discussion of the direct trip functions and the corresponding time delays.

TL1 (10-80/10-80)

This timer is associated with the M_1OB out of step blocking function. Refer to the logic description and the SLYP instruction book for a discussion on how to determine the pickup delay setting of the TL1 timer. The reset delay should be set for 40 ms.

TL11 (10-80/10-80): UNBLOCKING MODE

This timer is present only when the unblocking mode is used. The pickup delay time should be set for 4 ms. + channel time + trip integrator pickup delay or 10 ms., whichever is greater. The reset delay should be set for 50 ms.

CONSTRUCTION

The SLA52A relay is packaged in an enclosed metal case with hinged front covers and removable top cover. The outline and mounting dimensions of the case and the physical location of the components are shown in Figures 1 and 3 respectively.

The SLA52A relay contains printed circuit cards identified by a code number such as A111, T102, L104 where A designates auxiliary function, T designates time delay function, and L designates logic function. The printed circuit cards plug in from the front of the unit. The sockets are marked with letter designations or "addresses" (D, E, F, etc.) which appear on the guide strips in front of each socket, on the component location drawing, on the internal connection diagram and on the printed circuit card. The test points (TP1, TP2, etc.) shown on the internal connection diagram are connected to instrument jacks on a test card in position T or AT with TP1 at the top of the AT card. *TP10 is tied to +15 VDC through a 1.5K resistor. This resistor limits the current when TP10 is used to supply a logic signal to a card.

The links shown on the internal connection diagram are used to select certain logic options. The links are located on the printed circuit cards.

Other logic options are selected by means of taper tip jumpers and matrix blocks. These matrix blocks are located in the rear of the unit as shown in Figure C. The green (G), black (B), and violet (V) matrix blocks have 20 individual matrix points. The red (R) block has 20 points which are grouped in pairs. The yellow (Y) block has 20 points which are grouped in 10 common points; 1 to 10 are tied to +15 VDC, 11 to 20 are tied to reference. A tool for inserting and removing the taper tip jumpers is supplied with each relay.

RECEIVING, HANDLING AND STORAGE

These relays will normally be supplied as a part of a static relay equipment, mounted in a rack or cabinet with other static relays and test equipment. Immediately upon receipt of a static relay equipment, it should be unpacked and examined for any damage sustained in transit. If injury or damage resulting from rough handling is evident, file a damage claim at once with the transportation company and promptly notify the nearest General Electric Sales Office.

Reasonable care should be exercised in unpacking the equipment. If the equipment is not to be installed immediately, it should be stored indoors in a location that is free from moisture, dust, metallic chips, and severe atmospheric contaminants.

Just prior to final installation the shipping support bolt should be removed from each side of all relay units, to facilitate possible future unit removal for maintenance. These shipping support bolts are approximately 8 inches back from the relay front panel. Static relay equioment, when supplied in swing rack cabinets, should be securely anchored to the floor or to the shipping pallet to prevent the equipment from tipping over when the swing rack is opened.

TEST INSTRUCTIONS

CAUTION

If the SLA52A relay that is to be tested is installed in an equipment which has already been connected to the power system, disconnect the outputs in the associated Type SLAT relay from the system.

A. GENERAL

The SLA52A relay is supplied from the factory either mounted in a static relay equipment or as a separate unit associated with measuring relays, a Type SSA power supply, and some form of channel equipment. All relay units for a given terminal of static relaying equipment are tested together at the factory, and each unit will have the same summary number stamped on its nameplate.

In general, when a time range is indicated on the internal connections diagram, the timer has been factory set at a mid-range value. Timers should be set for the operating on reset times indicated on the associated overall logic diagram. Where a time range is indicated on the overall logic diagram, the timer should be set for the value recommended for that function in the descriptive writeup accompanying the overall logic diagram. Where a setting depends upon conditions encountered on a specific application, this is so stated and the factors influencing the choice of setting are described. The procedure for checking and setting the timers is described in a later section.

B. OPERATIONAL CHECKS

Operation of the SLA52A unit can be checked by observing the signals at the twenty test points (TP1 to TP20) in the SLA52A, by observing the operation of the associated channel equipment, or by observing the cutput functions in the associated Type SLAT tripping relay. The test points are located on two test cards in positions T and AT, and are numbered 1 to 20 from top to bottom. TP1 is the reference bus for the logic circuit; TP10 is at +15 VDC. The remaining points are located at various strategic points throughout the logic as shown on the internal connection diagram (Figure 2). Test point voltages can be monitored with a portable high impedance voltmeter, the voltmeter on the test panel of the associated equipment, or an oscilloscope.

C. TEST CARD ADAPTER

The test card adapter provides a convenient means of gaining access to any pin of a particular card. Detailed information on the use of the test adapter card is included in the card instruction book GEK-34158.

D. TIMER ADJUSTMENTS AND TESTS

When the time delay cards are to be adjusted or checked, an oscilloscope that can display two traces simultaneously and that has a calibrated horizontal sweep should be used.

In order to test the time cards it is necessary to remove the card previous to the timer (see Table I) and to place the timer card in a card adapter. The card adapter allows access to the input and output of the timer is they are not brought out on test points. The timer test circuit is shown in Figure 7. Opening the N.C. contact causes the output to step up to +15 VDC after the pickup delay of the timer. To increase the pickup time turn the upper potentiometer on the timer card clockwise; to decrease the time turn it counter-clockwise. Closing the contact causes the timer output to drop out after the reset time delay setting of card. If the timer card is provided with a variable reset delay, it can be adjusted by the lower potentiometer on the timer card (CW increases reset time).

TABLE I

TIME UNDER TEST	POSITION	REMOVE CARD IN POSITION
TL1	AG	AF
TL2	AE	AD
TL3	K	AK
TL5	AC	A*
TL6	P	AN
TL7	M	L
TL10	J	H
TL11	AJ	AP
TL12	Non - Adjustable	

* Also remove S card in associated SLYP, connect Pin 4 of TL5 to Ref.

E. OVERALL EQUIPMENT TESTS

After the SLA52A relay and the associated static relay units have been individually calibrated and tested for the desired settings, a series of overall operating circuit checks is advisable.

The elementary, overall logic, and logic description for the specific job will be useful for determining the overall operation of the scheme.

Overall equipment tests can be performed by applying AC current and voltages to the measuring units as specified in the instruction book for the measuring units and checking that proper outputs are obtained from the associated SLAT when the measuring units operate.

MAINTENANCE

A. PERIODIC TESTS

It should be sufficient to check the outputs produced at test points in the SLA52A when periodic calibration tests are made on the associated measuring units, for example the phase and ground relays in line relaying scheme. No separate periodic tests on the SLA52A itself should be required.

B. TROUBLE SHOOTING

In any trouble shooting of equipment, it should first be established which unit is functioning incorrectly. The overall logic diagram supplied with the equipment shows the combined logic of the complete equipment and the various test points in each unit. By signal tracing, using the overall logic diagram and the various test points, it should be possible to quickly isolate the trouble.

A test adapter card is supplied with each static relay equipment to supplement the prewired test points on the test cards. Use of the adapter card is described in the card instruction book GEK-34158.

A dual-trace oscilloscope is a valuable aid to detailed trouble shooting, since it can be used to determine phase shift, operate and reset times as well as input and output levels. A portable dual-trace oscilloscope with a calibrated sweep and trigger facility is recommended.

C. SPARE PARTS

To minimize possible outage time, it is recommended that a complete maintenance program should include the stocking of at least one spare card of each type. It is possible to replace damaged or defective components on the printed circuit cards, but great care should be taken in soldering so as not to damage or bridge-over the printed circuit busses, or overheat the semi-conductor components. The repaired area should be recovered with a suitable high-dielectric plastic coating to prevent possible breakdowns across the printed busses due to moisture and dust. The wiring diagrams for the cards in the SLA52A relay are included in the card book GEK-34158.

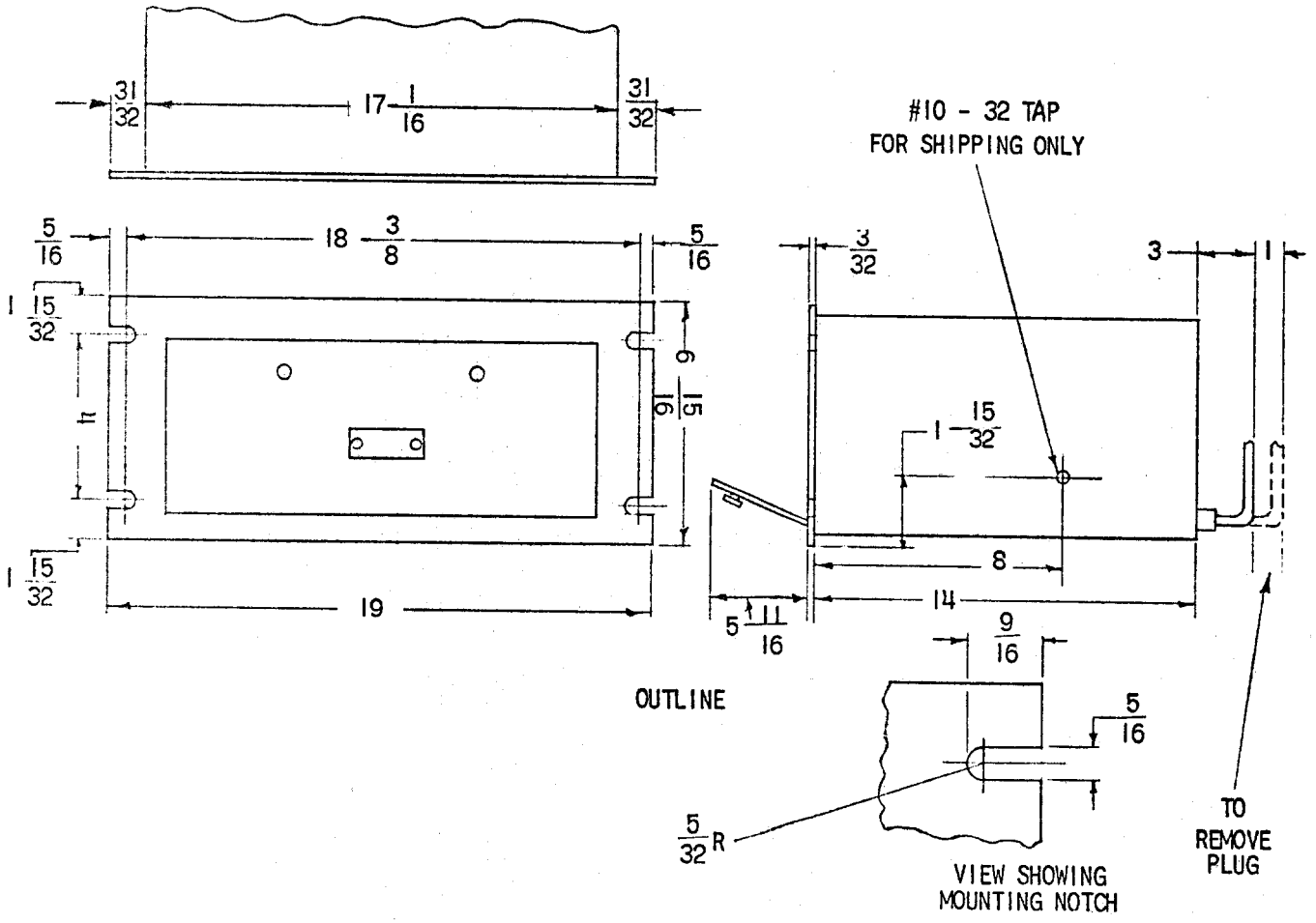


FIG. 1 (0227A2037-0) Outline And Mounting Dimensions For The Type SLA52A Relay

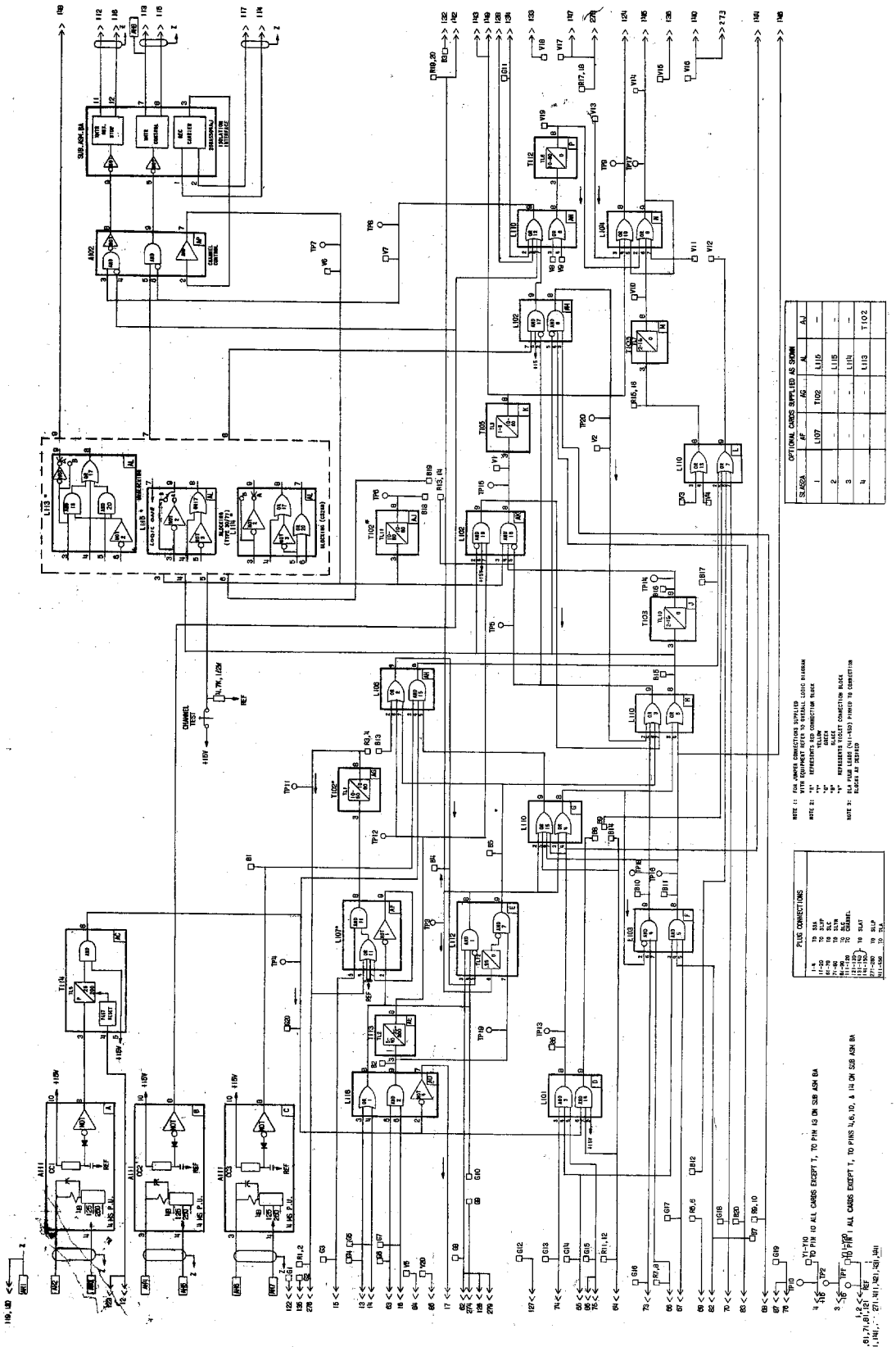
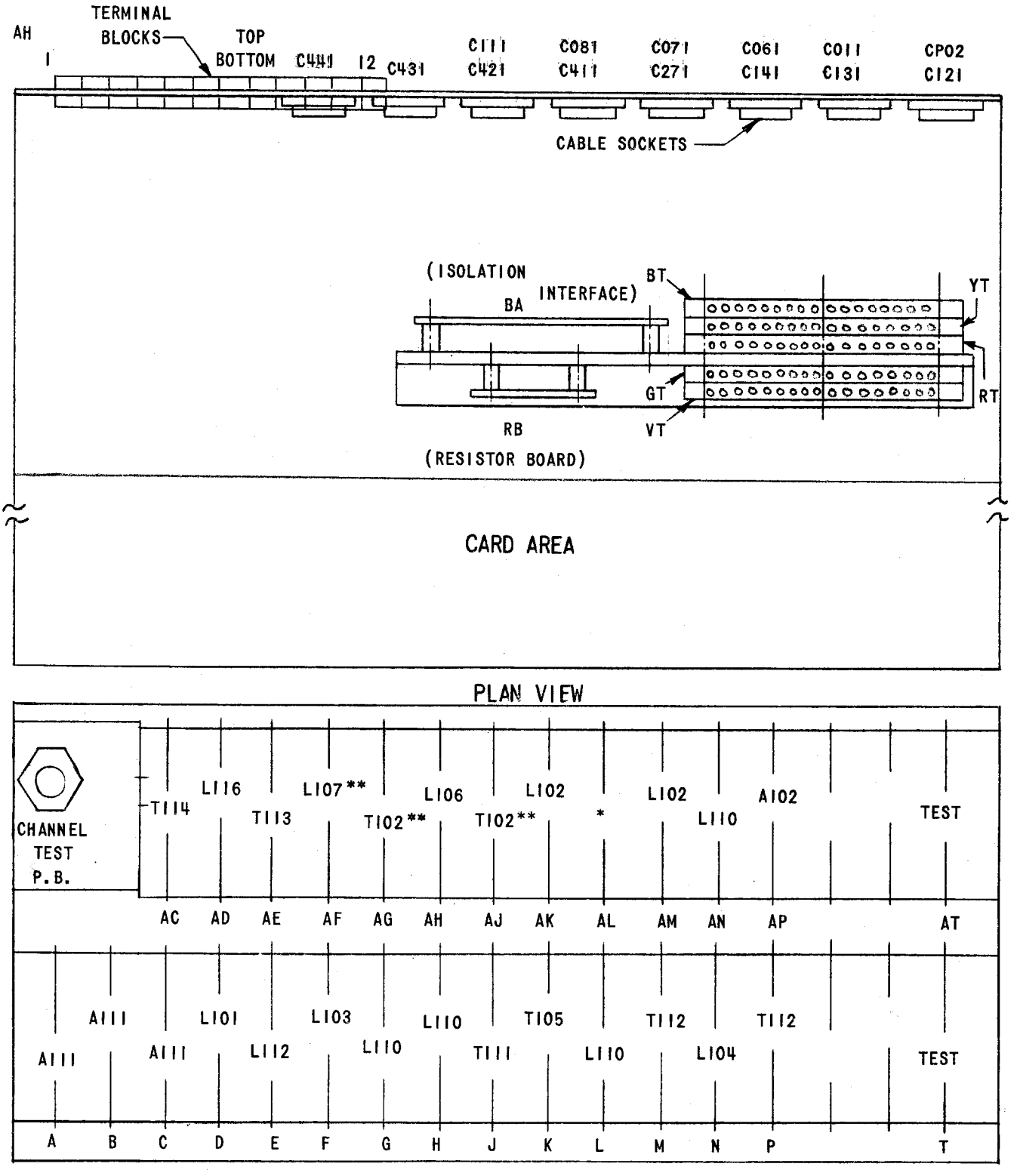


FIG. 2 (0121D9450-5) Internal Connections For The Type SLA52A Relay



*- SEE INTERNAL FOR CARD IDENTIFICATION. (0121D9450) **- OPTIONAL CARDS

FIG. 3 (0246A3565-1) Component Locations For The Type SLA52A Relay

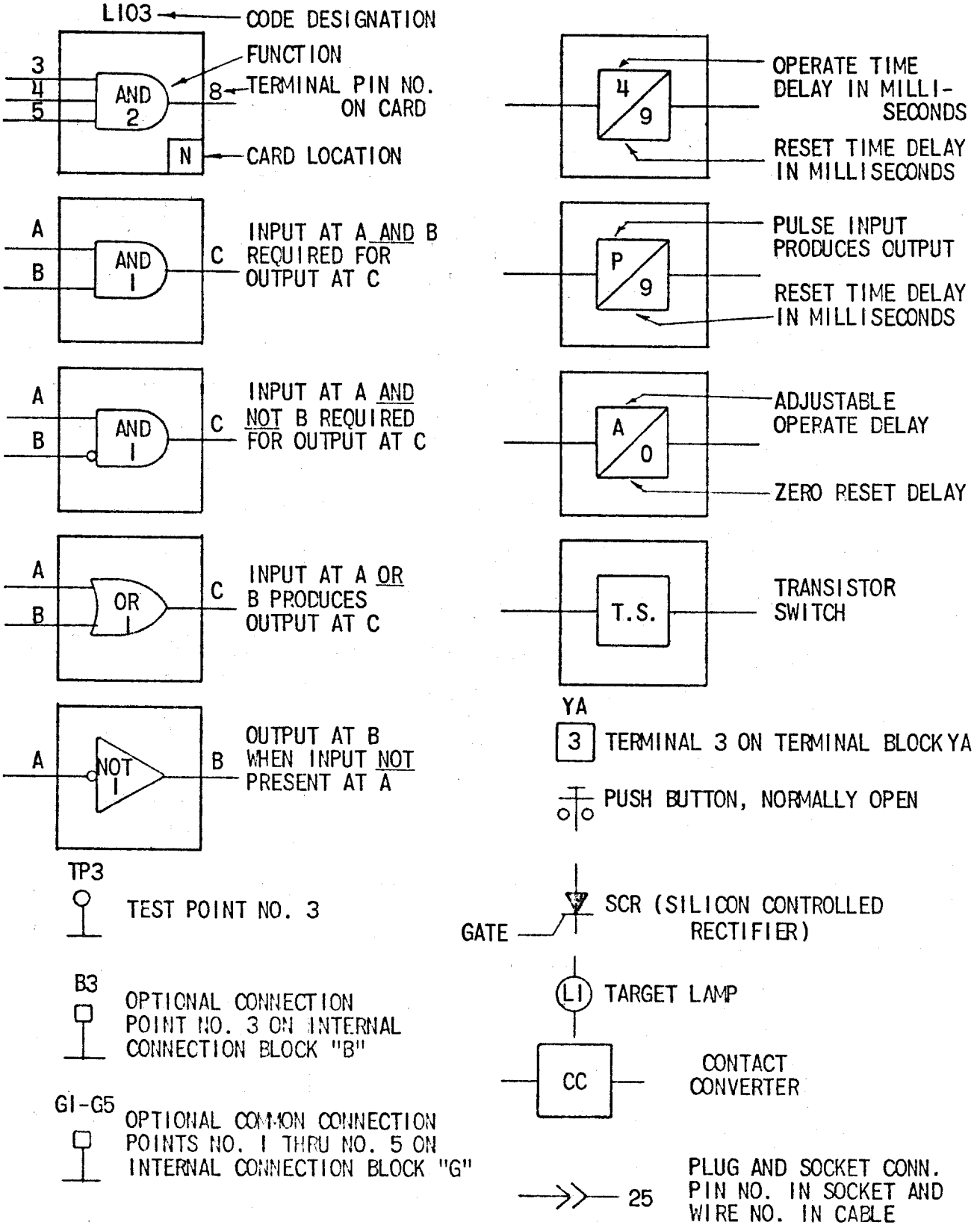


FIG. 4 (0227A2047-0) Logic And Internal Connection Diagram Legend

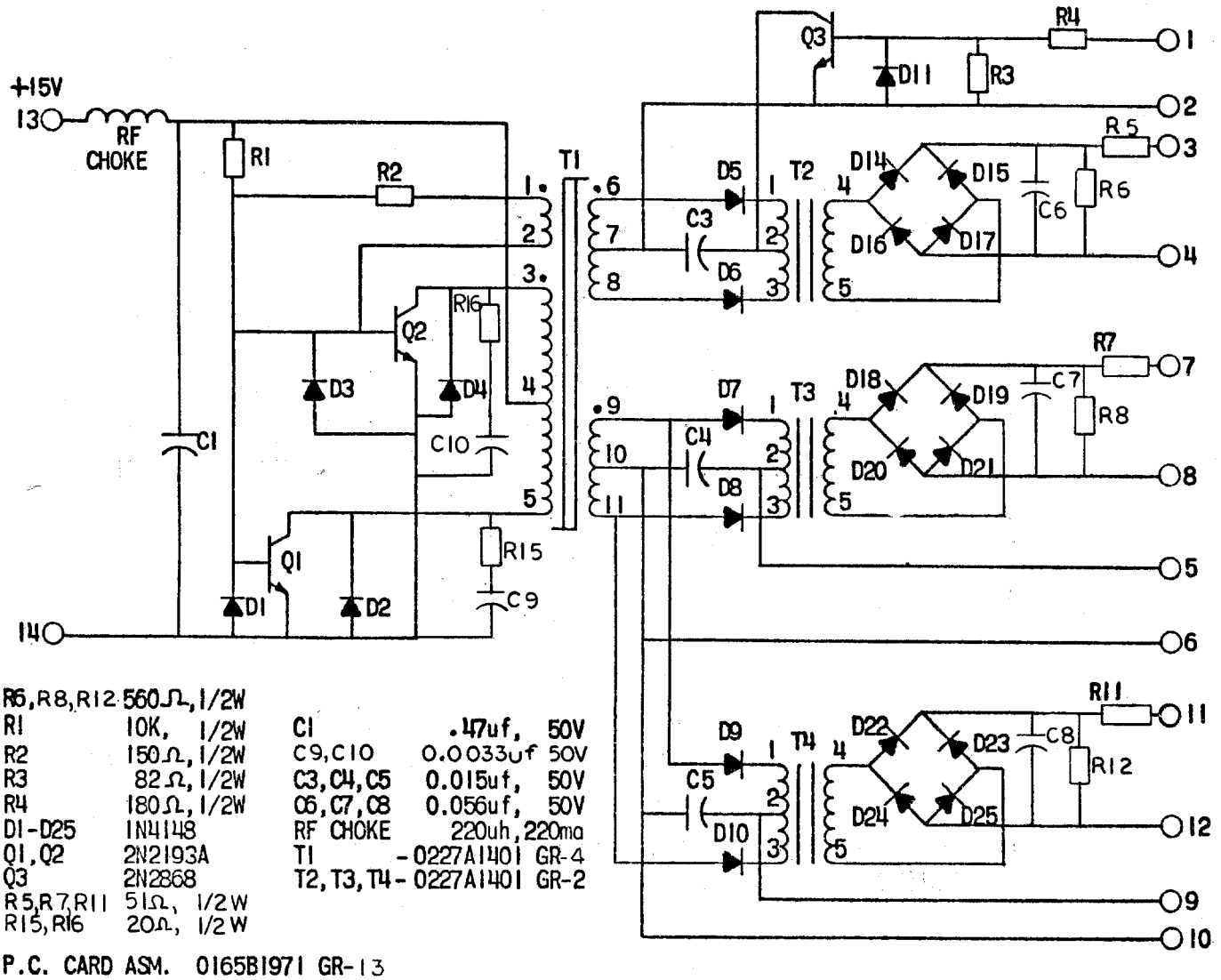
THE FOLLOWING CONNECTIONS ARE TO BE MADE TO THE TERMINAL BLOCKS IN THE REAR OF THE SLA LOGIC UNIT. (2)

FROM	TO
V1	436
V2	430
V3	V12
V4	Y12
V6	437
V7	438
V8	Y13
V9	Y14
V11	Y11
V13	R17
V18	Y15
G1	Y17
G2	Y18
G4	412
G5	413
G7	442
G9	Y16
G11	440
G12	433
G13	415
G14	416
G16	443
G17	417

FROM	TO
G18	418
G20	420
R3	424
R4	B13
R5	419
V5	B12
R8	B20
R10	444
R12	414
R13	435
R16	432
R18	439
R19	B3
R20	425
B2	423
B4	422
B6	426
B8	B9
B10	427
B11	428

FROM	TO
B15	429
B17	434

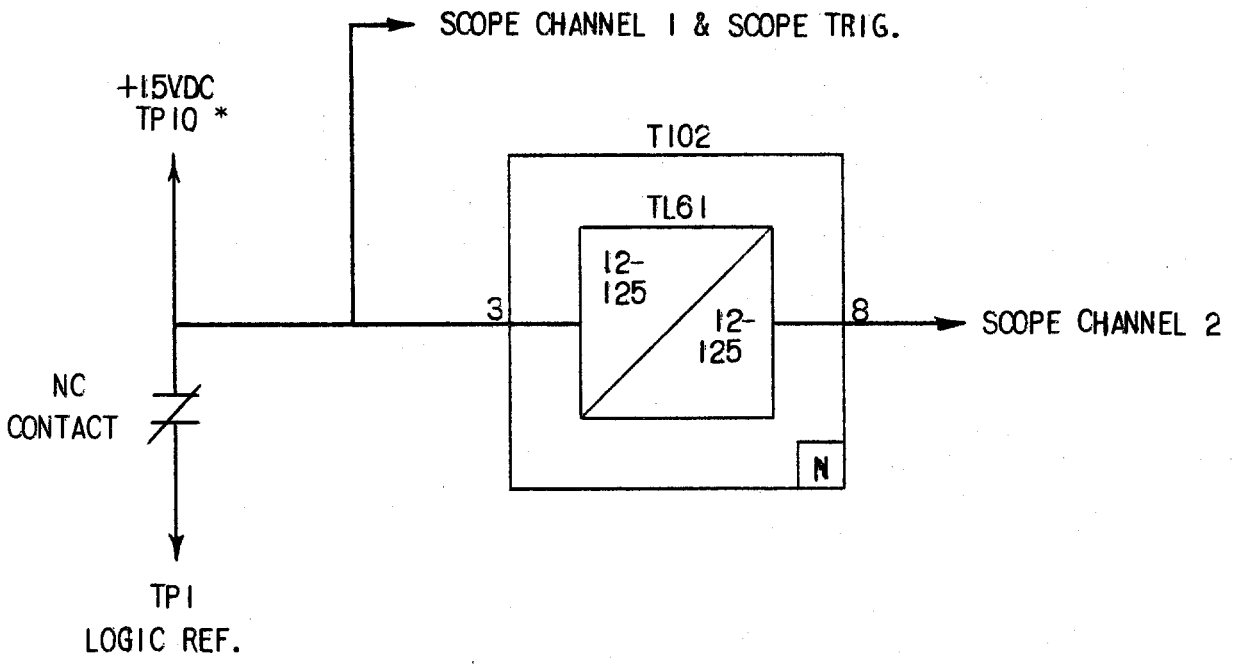
FIG. 5 (0227A2050-2 SH. 2) Sample Option Chart For The Type SLA52A Relay



R6,R8,R12	560Ω, 1/2W	C1	.47uf, 50V
R1	10K, 1/2W	C9,C10	0.0033uf 50V
R2	150Ω, 1/2W	C3,C4,C5	0.015uf, 50V
R3	82Ω, 1/2W	C6,C7,C8	0.056uf, 50V
R4	180Ω, 1/2W	RF CHOKE	220uh, 220ma
D1-D25	1N4148	T1	-0227A1401 GR-4
Q1,Q2	2N2193A	T2,T3,T4	-0227A1401 GR-2
Q3	2N2868		
R5,R7,R11	51Ω, 1/2W		
R15,R16	20Ω, 1/2W		

P.C. CARD ASM. 0165B1971 GR-13

FIG. 6 (0208A5504-AJ-0) Isolation Interface Circuit



* THE 15VDC SIGNAL AT PIN 10 HAS A CURRENT LIMITING RESISTOR MOUNTED ON THE TEST CARD.

FIG. 7 (0246A7987-0) Logic Timer Test Circuit