



# INSTRUCTIONS

GEK-41961

TYPE SLA51D

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**POWER SYSTEMS MANAGEMENT DEPARTMENT**

**GENERAL  ELECTRIC**

**PHILADELPHIA, PA.**

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DESCRIPTION

The SLA51D is an auxiliary logic relay designed to be used in directional comparison ON-OFF carrier schemes. The relay contains the necessary logic to interpret output signals from associated measuring functions and translate them to an appropriate auxiliary output and tripping relay. In addition to the SLA51D relay, appropriate ground and phase relays plus a power supply and auxiliary tripping relay are required to complete a particular relaying scheme.

The type SLA51D relay is packaged in a four rack unit enclosed metal case. The relay is suitable for mounting in a 19 inch rack and mounting and outline dimensions are shown in Figure 1. Internal connections for the SLA51D relay are shown in Figure 3, and the component and card locations are shown in Figure 2.

APPLICATION

The SLA51D relay is designed to operate in conjunction with appropriate phase and ground relays in a directional comparison ON-OFF carrier blocking scheme. A circuit is included to permit carrier tripping at AND7 for a loss of DC in the associated CS26B.

Protection features required in a relaying scheme often vary from scheme to scheme and it is sometimes desirable to provide certain features initially with the scheme or to provide features so that they may be added at a later date in the field. To this end, the SLA51D design has incorporated circuit flexibility to permit implementation of certain optional features. Printed circuit cards L108 and T102, shown dotted in Figure 3, are used whenever out-of-step detection is required. Matrix blocks "R", "Y", "G" and "B", each with a number of points, are provided in all SLA51D relays to permit various logic arrangements to be made simply by connecting jumper leads between appropriate points. For example, a jumper between G6 and B5, shown dotted in Figure 3, will allow the out-of-step detection option to block all pilot tripping by applying the NOT input to AND7. On the other hand, jumpering between G6 and B6 will block reclosing by applying the NOT input to the appropriate AND function in the associated SLAT tripping relay. These examples can best be understood by referring to the overall logic diagram and instruction books supplies with a particular relaying scheme.

Various points in the logic can be monitored by providing jumpers from any of the available matrix points to plugs located on the rear of the SLA51D relay. This option is further described in paragraph "C", "Data Monitoring Points", under the section headed OPERATING PRINCIPLES.

For the specific options and the logic arrangement supplies with a particular scheme, refer to the logic diagram and logic descriptive writeup supplies with that scheme. If it is desired to make logic changes at a later date, the diagrams and instruction books supplied with a particular scheme should be studied to determine the means for implementing the changes. If, after study of the diagrams, further assistance is required, contact the nearest General Electric District Sales Office.

There are no measuring functions to be set in the SLA51D relay, but there is included certain timers that must be set in accordance with the demands of the particular system to be protected. Refer to the section under SETTINGS for a description of these timers and for suggestions to be used in making the settings.

RATINGS

The Type SLA51D relay is designed for use in an environment where the air temperature outside the relay case does not exceed  $-20^{\circ}\text{C}$  or  $+65^{\circ}\text{C}$ .

The Type SLA51D relay requires  $\pm 15$  VDC power source which can be obtained from a Type SSA power supply.

Each contact converter in this relay has a link for selecting the proper voltage for the coil circuit of the contact converter. The three possible voltages are 48 VDC, 125 VDC and 250 VDC.

***These instructions do not purport to cover all details or variations in equipment nor to provide for every possible contingency to be met in connection with installation, operation or maintenance. Should further information be desired or should particular problems arise which are not covered sufficiently for the purchaser's purposes, the matter should be referred to the General Electric Company.***

BURDENS

The SLA51D relay presents a burden of 270 ma to the +15 VDC supply of the Type SSA power supply.

Each contact converter, when energized, will draw approximately 10 ma. from the station battery, regardless of tap setting.

OPERATING PRINCIPLESLOGIC CIRCUIT

The functions of the Type SLA51D relay involve basic logic (AND, OR, and NOT) where the presence or absence of signals, rather than their magnitude, controls the operation. Signals are measured with respect to a reference bus accessible at TP1. In general, a signal below 1 VDC represents an OFF or LOGIC ZERO condition; an ON or LOGIC ONE condition is represented by a signal of approximately +15 VDC.

The symbols used on the internal connection diagram (Figure 3) are explained by the legend shown in Figure 4.

The matrix block options shown in the internal connections of the SLA51D relay are provided at the factory. The connections are shown on the associated overall logic and are listed on the associated option chart. A sample option chart for the Type SLA51D relay is shown in Figure 9.

CONTACT CONVERTERS

The purpose of this function is to convert a contact operation into a signal that is compatible with the logic circuit of the Type SLA51D relay. Those contact converters are labeled CC1 and CC2. These contact converters have a non-adjustable 4 millisecond pickup delay.

CC1

Contact converter 1 is energized by an external contact to stop carrier transmission.

CC2

Contact converter 2, when energized, prevents relay carrier tripping and relay control of carrier but permits auxiliary control of carrier.

DATA MONITORING POINTS

Type SLA51D relay has provisions to provide data monitoring outputs. The data monitoring (DLA) points are selected on the matrix blocks and are listed on the option chart. Any matrix block points which are not used for logic connections may be monitored. Key points in the logic have more than one matrix point to allow both logic and monitoring connections. A data logging amplifier (DLA) relay is used to translate these logic signals into usable outputs.

CHANNEL INTERFACE

The logic of the Type SLA51D relay includes an isolation interface (Figure 5) between the relays in the scheme and the associated channel. The circuitry of the isolation interface provides a signal path but maintains metallic isolation. This feature makes it possible to maintain isolation between the DC supply used for the relays and that employed by the channel.

When pins 9 and 10 are both connected to relay reference, a metallically separate positive logic signal appears at pin 11 with respect to 12. The output from the isolation interface is a 5 VDC, 20 ma. signal.

An additional interface unit is used to provide DC supervision in conjunction with the received carrier signal; this interface unit is shown in Figure 6.

CONSTRUCTION

The SLA51D relay is packaged in an enclosed metal case with hinged front covers and removable top cover. The outline and mounting dimensions of the case and the physical location of the components are shown in Figures 1 and 2 respectively.

The SLA51D relay contains printed circuit cards identified by a code number such as A111, T102, L104 where A designates auxiliary function, T designates time delay function, and L designates logic function. The printed circuit cards plug in from the front of the unit. The sockets are marked with letter designations or "addresses" (D, E, F, etc.) which appear on the guide strips in front of each socket, on the component location drawing, on the internal connection diagram and on the printed circuit card. The test points (TP1, TP2, etc.) shown on the internal connection diagram are connected to instrument jacks on a test card in position T or AT with TP1 at the top of the AT card. \*TP10 is tied to +15 VDC through a 1.5K resistor. This resistor limits the current when TP10 is used to supply a logic signal to a card.

Other logic options are selected by means of taper tip jumpers and matrix blocks. These matrix blocks are located in the rear of the unit as shown in Figure 2. The green (G) matrix block has ten points in two 5 point common groups. The black (B) matrix block has 20 individual matrix points. The red (R) block has 20 points which are grouped in pairs. The yellow (Y) block has 20 points which are grouped in 10 common points; 1 to 10 are tied to +15 VDC, 11 to 20 are tied to reference. A tool for inserting and removing the taper tip jumpers is supplied with each relay.

RECEIVING, HANDLING AND STORAGE

These relays will normally be supplied as a part of a static relay equipment, mounted in a rack or cabinet with other static relays and test equipment. Immediately upon receipt of a static relay equipment, it should be unpacked and examined for any damage sustained in transit. If injury or damage resulting from rough handling is evident, file a damage claim at once with the transportation company and promptly notify the nearest General Electric Sales Office.

Reasonable care should be exercised in unpacking the equipment. If the equipment is not to be installed immediately, it should be stored indoors in a location that is free from moisture, dust, metallic chips, and severe atmospheric contaminants.

Just prior to final installation the shipping support bolt should be removed from each side of all relay units, to facilitate possible future unit removal for maintenance. These shipping support bolts are approximately 8 inches back from the relay front panel. Static relay equipment, when supplied in swing rack cabinets, should be securely anchored to the floor or to the shipping pallet to prevent the equipment from tipping over when the swing rack is opened.

INSTALLATION TESTSCAUTION

THE LOGIC SYSTEM SIDE OF THE DC POWER SUPPLY USED WITH MOD III STATIC RELAY EQUIPMENT IS ISOLATED FROM GROUND. IT IS A DESIGN CHARACTERISTIC OF MOST ELECTRONIC INSTRUMENTS THAT ONE OF THE SIGNAL INPUT TERMINALS IS CONNECTED TO INSTRUMENT CHASSIS. IF THE INSTRUMENT USED TO TEST THE RELAY EQUIPMENT IS ISOLATED FROM GROUND, ITS CHASSIS MAY HAVE AN ELECTRICAL POTENTIAL WITH RESPECT TO GROUND. THE USE OF A TEST INSTRUMENT WITH A GROUNDED CHASSIS WILL NOT AFFECT THE TESTING OF THE EQUIPMENT. HOWEVER, A SECOND GROUND CONNECTION TO THE EQUIPMENT, SUCH AS A TEST LEAD INADVERTENTLY DROPPING AGAINST THE RELAY CASE, MAY CAUSE DAMAGE TO THE LOGIC CIRCUITRY. NO EXTERNAL TEST EQUIPMENT SHOULD BE LEFT CONNECTED TO THE STATIC RELAYS WHEN THEY ARE IN PROTECTIVE SERVICE, SINCE TEST EQUIPMENT GROUNDING REDUCES THE EFFECTIVENESS OF THE ISOLATION PROVIDED.

GENERAL

If the SLA51D relay that is to be tested is installed in an equipment which has already been connected to the power system, disconnect the outputs in the associated Type SLAT relay from the system.

The SLA51D relay is supplied from the factory either mounted in a static relay equipment or as a separate unit associated with measuring relays, a Type SSA power supply, and some form of channel equipment. All relay units for a given terminal of static relaying equipment are tested together at the factory, and each unit will have the same summary number stamped on its nameplate.

In general, when a time range is indicated on the internal connection diagram, the timer has been factory set at a mid-range value. Timers should be set for the operating or reset times indicated on the associated overall logic diagram. Where a time range is indicated on the overall logic diagram, the timer should be set for the value recommended for that function in the descriptive writeup accompanying the overall logic diagram. Where a setting depends upon conditions encountered on a specific application, this is so stated and the factors influencing the choice of setting are described. The procedure for checking and setting the timers is described in a later section.

OPERATIONAL CHECKS

Operation of the SLA51D unit can be checked by observing the signals at the twenty test points (TP1 to TP20) in the SLA51D, by observing the operation of the associated channel equipment, or by observing the output functions in the associated Type SLAT tripping relay. The test points are located on two test cards in positions T and AT, and are numbered 1 to 20 from top to bottom. TP1 is the reference bus for the logic circuit; TP10 is at +15 VDC. The remaining points are located at various strategic points throughout the logic as shown on the internal connection diagram (Figure 3). Test point voltages can be monitored with a portable high impedance voltmeter, the voltmeter on the test panel of the associated equipment, or an oscilloscope.

TEST CARD ADAPTER

The test card adapter provides a convenient means of gaining access to any pin of a particular card. Detailed information on the use of the test adapter card is included in the card instruction book GEK-34158.

TIMER ADJUSTMENTS AND TESTS

When the time delay cards are to be adjusted or checked, an oscilloscope that can display two traces simultaneously and that has a calibrated horizontal sweep should be used.

In order to test the time cards it is necessary to remove the card previous to the timer (see Table I) and to place the timer card in a card adapter. The card adapter allows access to the input and output of the timer if they are not brought out on test points. The timer test circuit is shown in Figure 7. Opening the N.C. contact causes the output to step up to +15 VDC after the pickup delay of the timer. To increase the pickup time turn the upper potentiometer on the timer card clockwise; to decrease the time turn it counter-clockwise. Closing the contact causes the timer output to drop out after the reset time delay setting of card. If the timer card is provided with a variable reset delay, it can be adjusted by the lower potentiometer on the timer card (CW increases reset time).

TABLE I

TIME UNDER TEST	POSITION	REMOVE CARD IN POSITION
TL /40	E	C
TL 4/0	F	D
TL 25/35	M	L
TL 3/50	S	R

CONTACT CONVERTER TESTS

Operation of the contact converters can be checked by placing the contact converter card in a card adapter, after checking the voltage tap selected agrees with the station battery voltage. Connect the station DC through a switch to the appropriate pair of terminals of the terminal strip, AH, mounted on the rear of the relay. The terminal numbers and polarity of connections for each of the contact converters are shown in the internal connection diagram, Figure 3. Output of the contact converter card may be monitored between pin 8 and pin 1 (reference) on the card adapter with either a scope or meter. Closure of the switch in the test source will provide a +15 volt DC signal at pin 8 of the card adapter.

ISOLATION INTERFACE TESTS

Operation of the three functions (received carrier, transmitter control, and transmitter auxiliary stop) of the isolation interface can be checked without direct connections to the subassembly. External test connections are made to the pins of the C111 socket mounted in the rear of the unit, see Figure 2.

Logic circuit test connections are made at the socket pins of the channel control card in position "AM".

Received carrier operation test connections are shown in Figure 8A. For this test do not remove channel control card in position "AM". Closure of the N.O. contact will simulate a received carrier signal and scope display will go from a logic "0" to a logic "1".

For the transmitter control and transmitter auxiliary stop checks remove the channel control card "AM" from its socket and replace it with a test card adapter and test card to gain access to the "AM" socket pins. Transmitter control test connections are shown in Figure 8B. The test contact in the open position simulates a logic "1" condition which holds off the transmitter control output of the isolation interface. Closure of the N.O. contact generates a logic "0" condition initiating a transmitter control output producing, a 5-6 volt DC signal across the output loading resistor. The transmitter auxiliary stop function can be tested in a similar manner using the test connections of Figure 8C and the output again will provide a 5-6 volt DC signal across the output loading resistor.

Carrier DC control test connections are shown in Figure 8D. Closure of the N.O. contact will simulate the presence of a DC control signal. The output is noted at pin 7 of the A102 card in position AG. This output will go from a logic "0" to a logic "1".

### OVERALL EQUIPMENT TESTS

After the SLA51D relay and the associated static relay units have been individually calibrated and tested for the desired settings, a series of overall operating circuit checks is advisable.

The elementary, overall logic, and logic description for the specific job will be useful for determining the overall operation of the scheme.

Overall equipment tests can be performed by applying AC current and voltages to the measuring units as specified in the instruction book for the measuring units and checking that proper outputs are obtained from the associated SLAT when the measuring units operate.

### MAINTENANCE

#### PERIODIC TESTS

It should be sufficient to check the outputs produced at test points in the SLA51D when periodic calibration tests are made on the associated measuring units, for example, the phase and ground relays in line relaying scheme. No separate periodic tests on the SLA51D should be required.

#### TROUBLE SHOOTING

In any trouble shooting of equipment, it should first be established which unit is functioning incorrectly. The overall logic diagram supplied with the equipment shows the combined logic of the complete equipment and the various test points in each unit. By signal tracing, using the overall logic diagram and the various test points, it should be possible to quickly isolate the trouble.

A test adapter card is supplied with each static relay equipment to supplement the prewired test points on the test cards. Use of the adapter card is described in the card instruction book GEK-34158.

A dual-trace oscilloscope is a valuable aid to detailed trouble shooting, since it can be used to determine phase shift, operate and reset times as well as input and output levels. A portable dual-trace oscilloscope with a calibrated sweep and trigger facility is recommended.

#### SPARE PARTS

To minimize possible outage time, it is recommended that a complete maintenance program should include the stocking of at least one spare card of each type. It is possible to replace damaged or defective components on the printed circuit cards, but great care should be taken in soldering so as not to damage or bridge-over the printed circuit busses, or overheat the semi-conductor components. The repaired area should be recovered with a suitable high-dielectric plastic coating to prevent possible breakdowns across the printed buses due to moisture and dust. The wiring diagrams for the cards in the SLA51 relay are included in the card book GEK-34158.

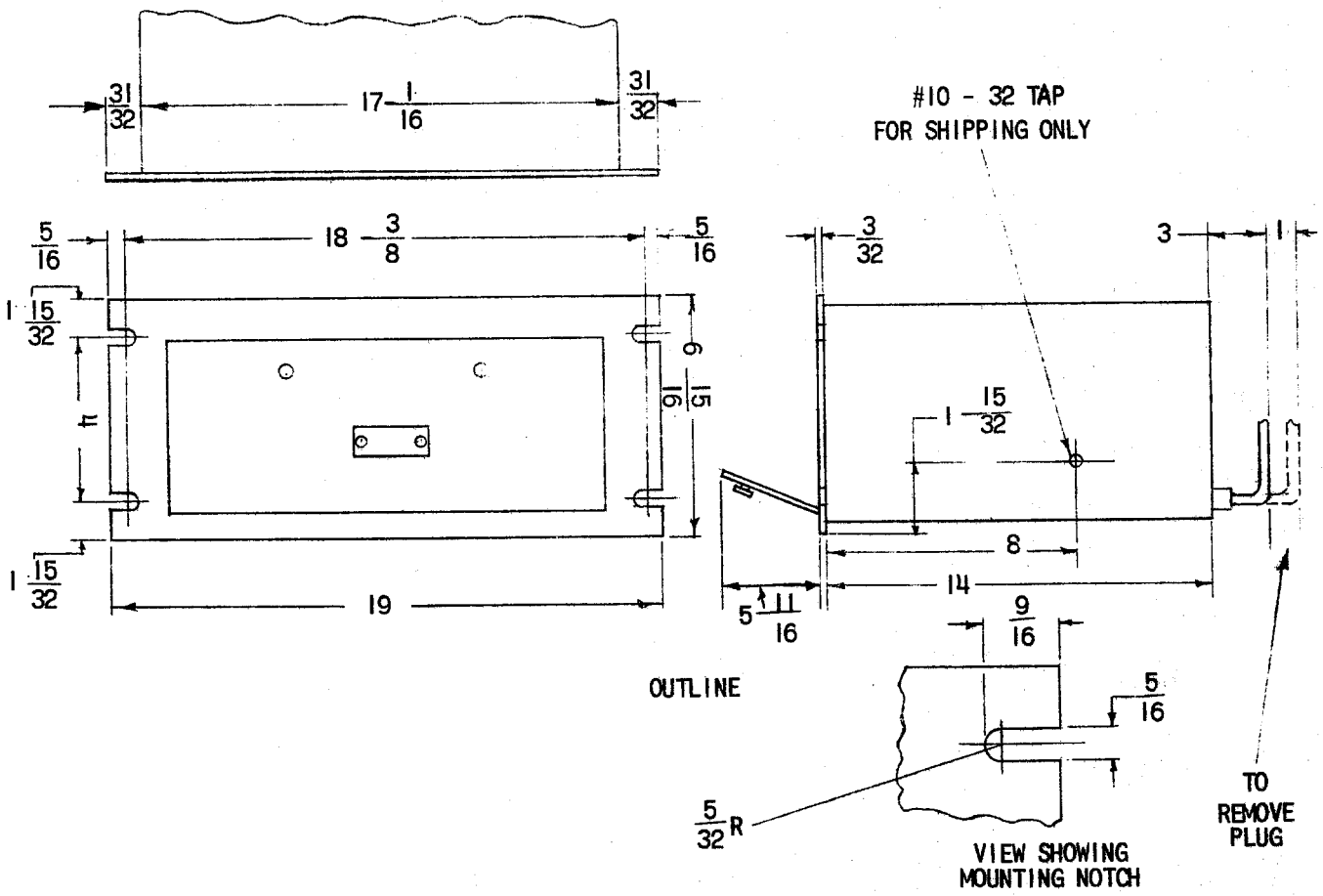


FIG. 1 (0227A2037-0) OUTLINE AND MOUNTING DIMENSIONS FOR THE TYPE SLA51D RELAY



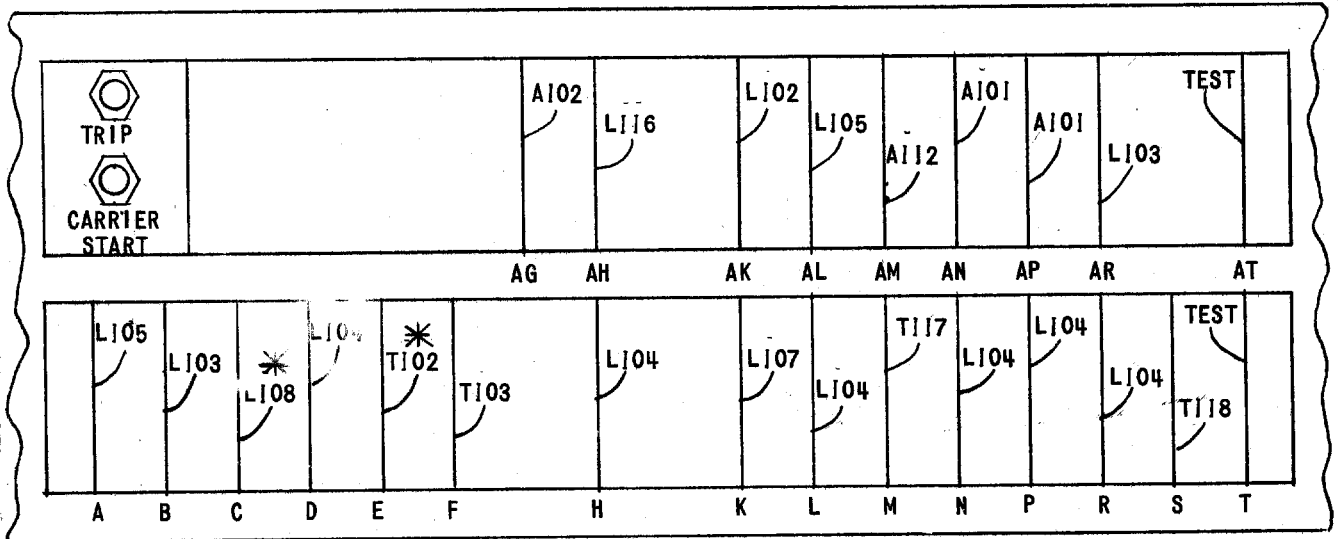
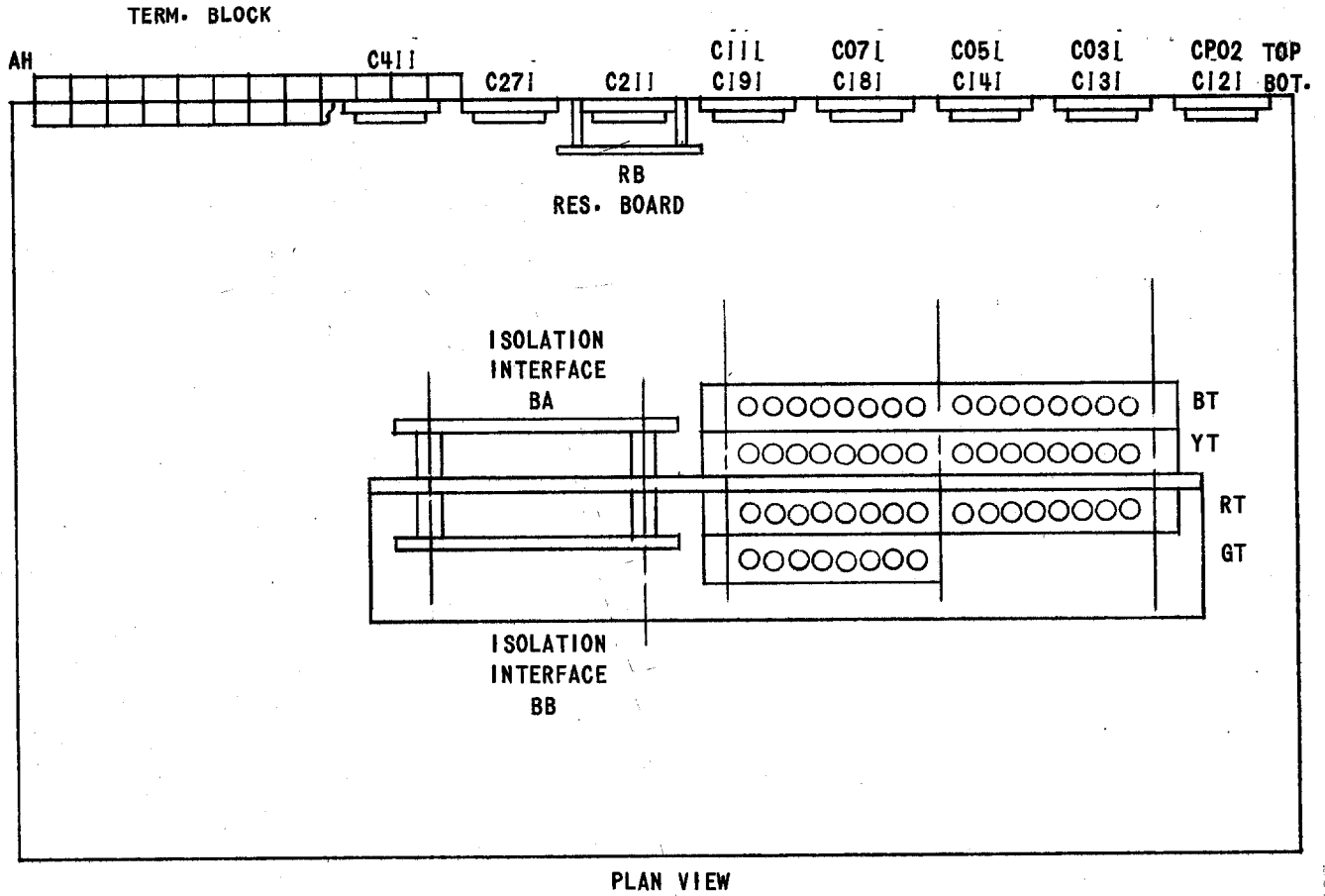


FIG. 2 (0227A2184-0) COMPONENT LOCATION DIAGRAM FOR THE TYPE SLA51D RELAY

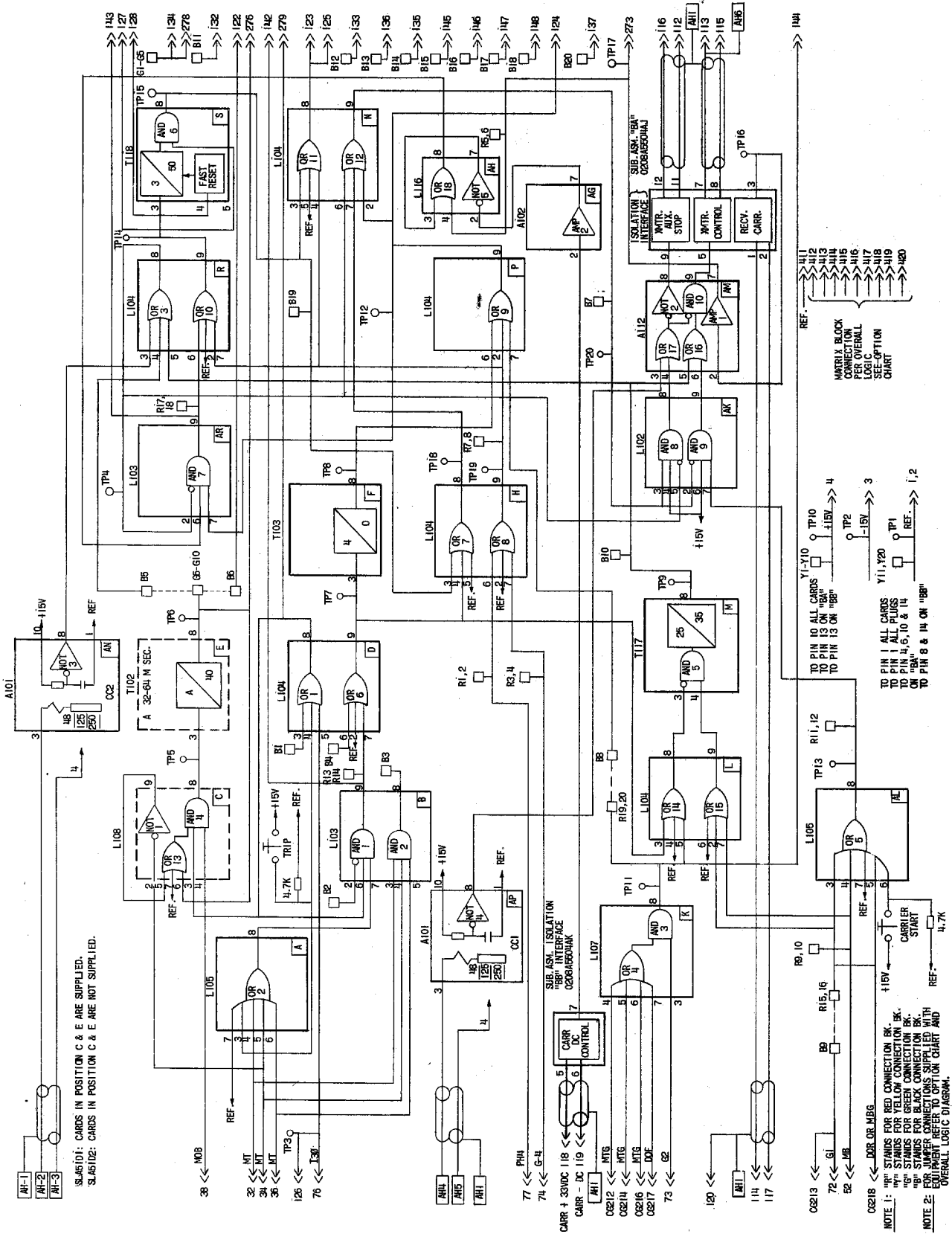


FIG. 3 (0149C7371-0) INTERNAL CONNECTIONS FOR THE TYPE SLA51D RELAY

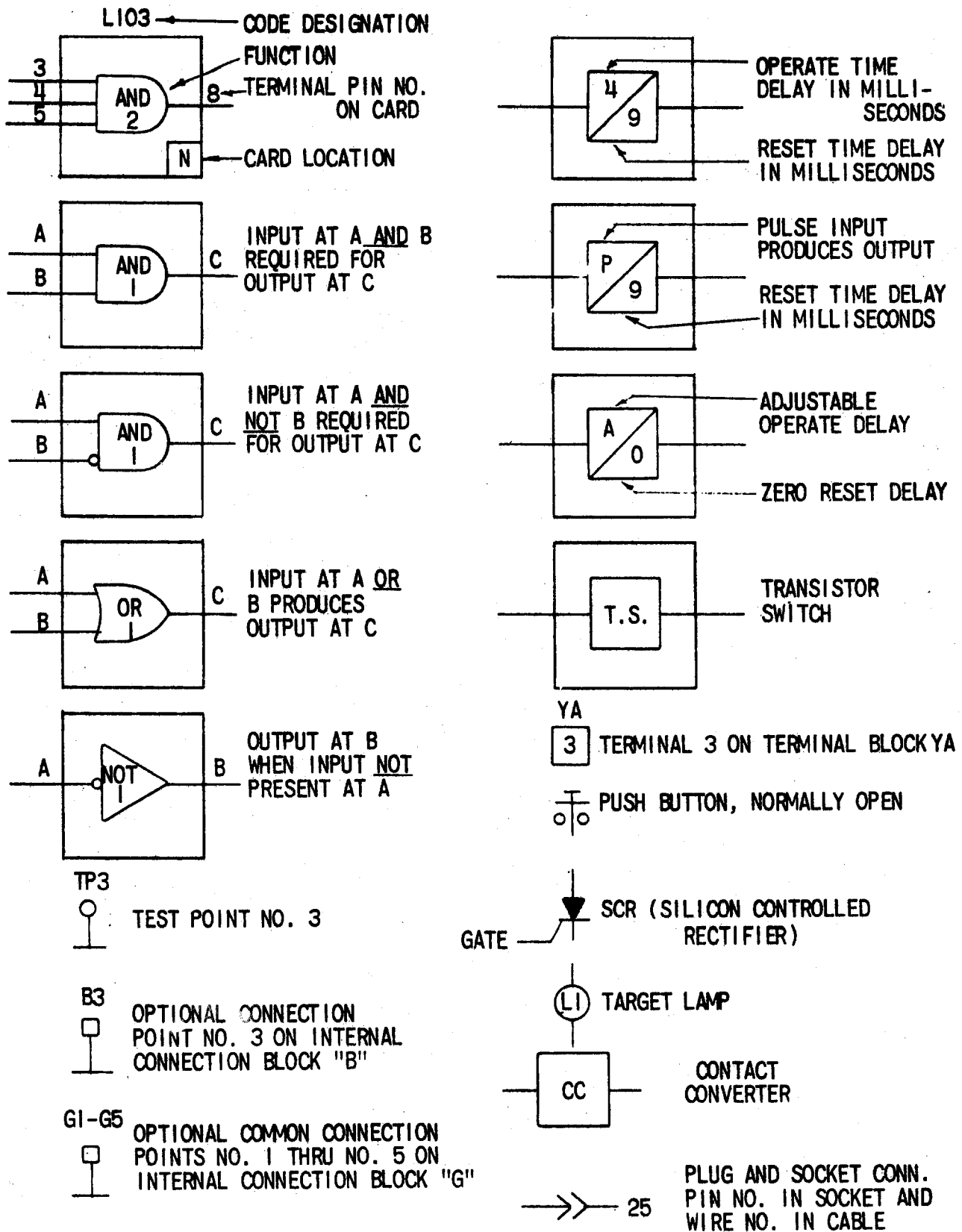
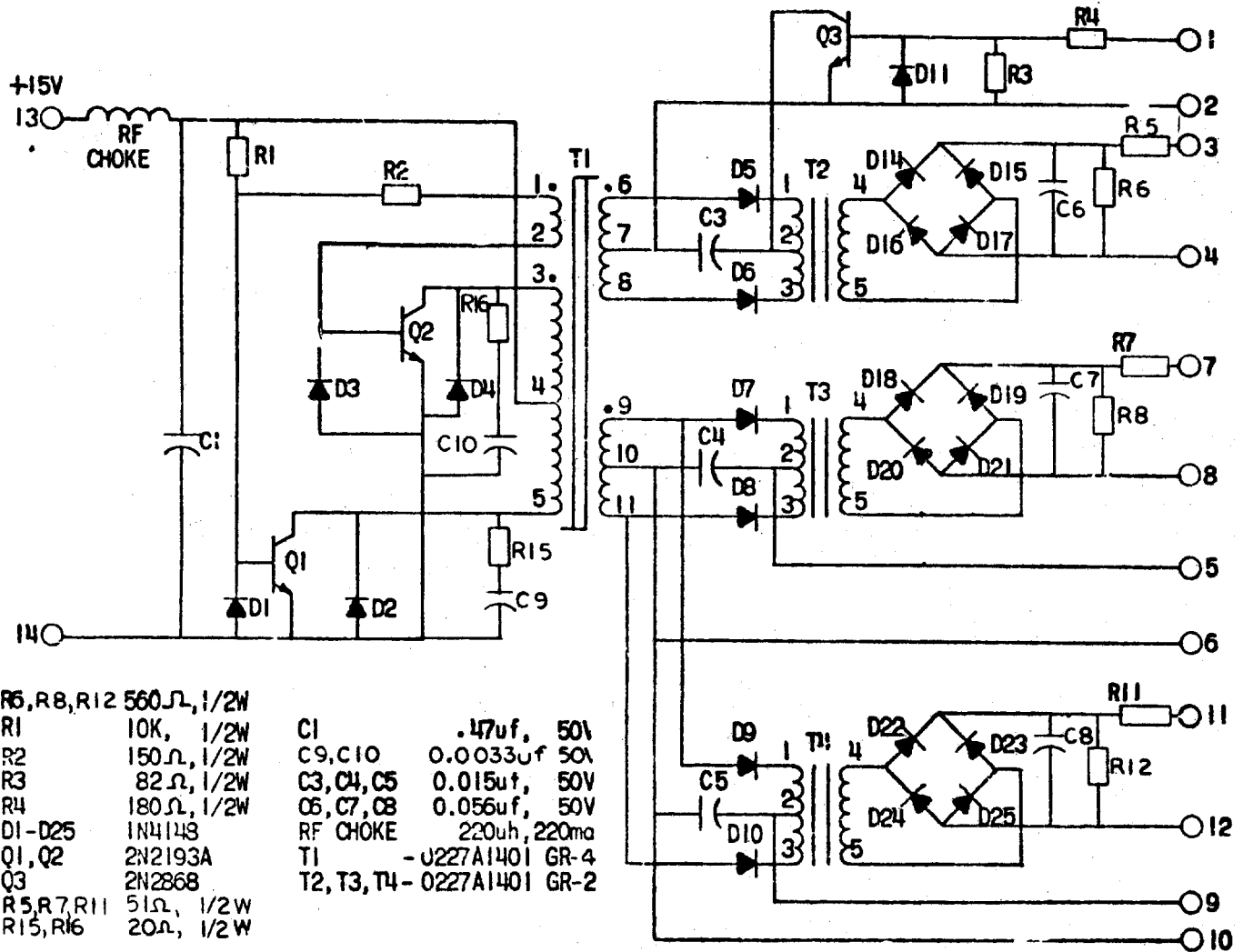


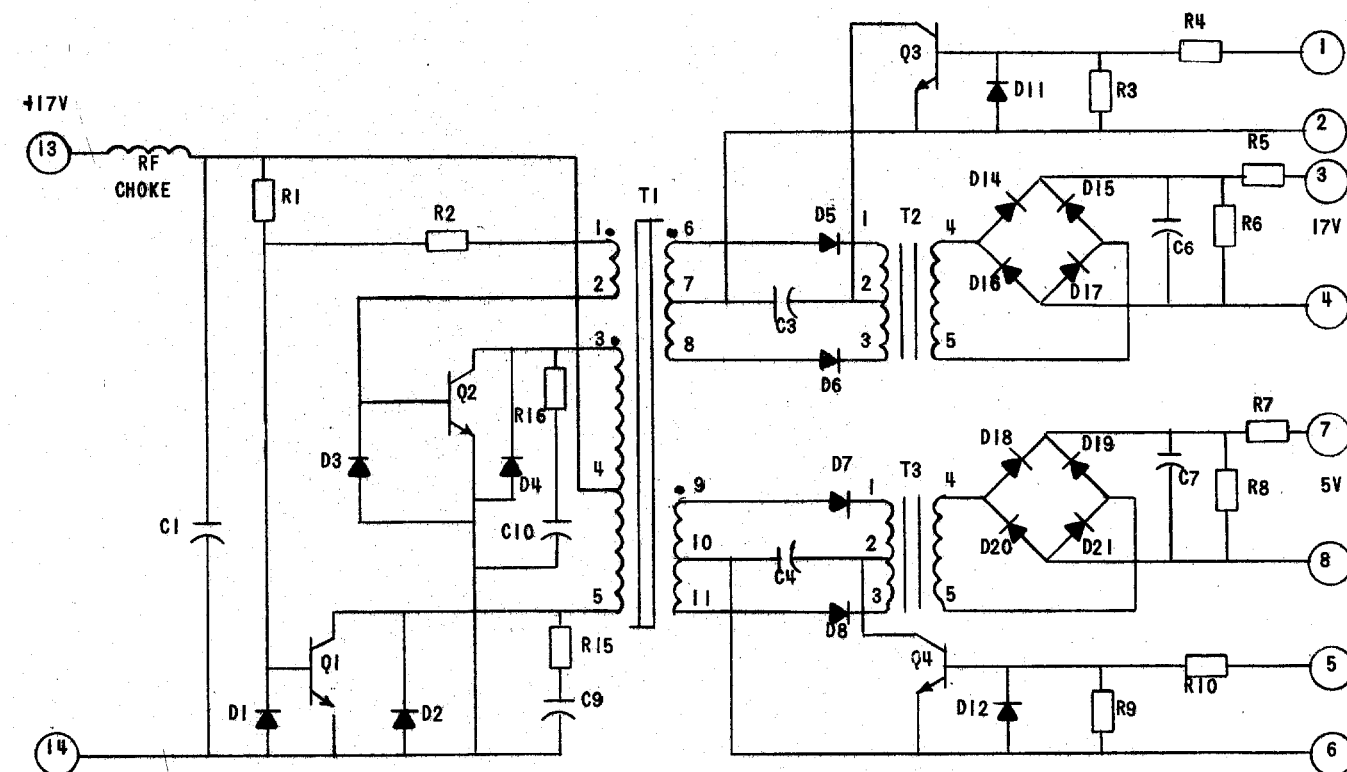
FIG. 4 (0257A2047-0) LOGIC AND INTERNAL CONNECTIONS DIAGRAM LEGEND



- |             |            |            |                 |
|-------------|------------|------------|-----------------|
| R6, R8, R12 | 560Ω, 1/2W | C1         | .47uf, 50V      |
| R1          | 10K, 1/2W  | C9, C10    | 0.0033uf, 50V   |
| R2          | 150Ω, 1/2W | C3, C4, C5 | 0.015uf, 50V    |
| R3          | 82Ω, 1/2W  | C6, C7, C8 | 0.056uf, 50V    |
| R4          | 180Ω, 1/2W | RF CHOKE   | 220uh, 220ma    |
| D1-D25      | 1N4148     | T1         | -J227A1401 GR-4 |
| Q1, Q2      | 2N2193A    | T2, T3, T4 | -0227A1401 GR-2 |
| Q3          | 2N2868     |            |                 |
| R5, R7, R11 | 51Ω, 1/2W  |            |                 |
| R15, R16    | 20Ω, 1/2W  |            |                 |

P.C. CARD ASM. 0165B1971 GR-13

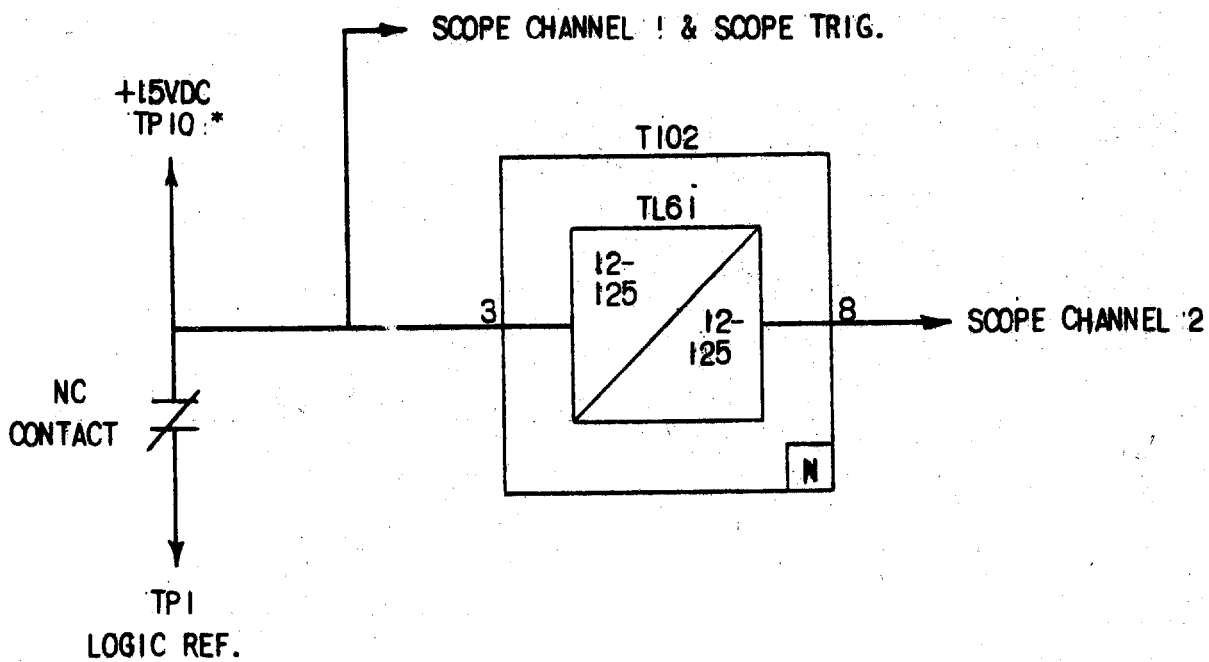
FIG. 5 (0208A5504AJ-1) INTERNAL CONNECTIONS FOR THE ISOLATION INTERFACE



R1	10K	L/2W	D1 TO 21	1N4148
R2	150 Ω	L/2W	Q1, 2	2N2193A
R3	82 Ω	1/2W	Q3, 4	2N2868
R4	180 Ω	1/2W	C1	.47uf 50V
R5	3.3K	1/2W	C3, 4	0.015uf 50V
R6	6.8K	1/2W	C6, 7	0.056uf 50V
R7	51 Ω	1/2W	C9, 10	0.0033uf 50V
R8, 9	560 Ω	1/2W	T1	0227A1401 G-4
R10	5100 Ω	1/2W	T2	" G-3
R15, 16	20 Ω	1/2W	T3	" G-2
RF CHOKE	220uh, 220ma			

P.C. CARD ASM.  
0165B1971 G-14

FIG. 6 (Q208A5504AK-2) INTERNAL CONNECTIONS FOR THE DC CONTROL ISOLATION INTERFACE



\* THE 15VDC SIGNAL AT PIN 10 HAS A CURRENT LIMITING RESISTOR MOUNTED ON THE TEST CARD.

FIG. 7 (0246A7987-0) LOGIC TIMER TEST CIRCUIT

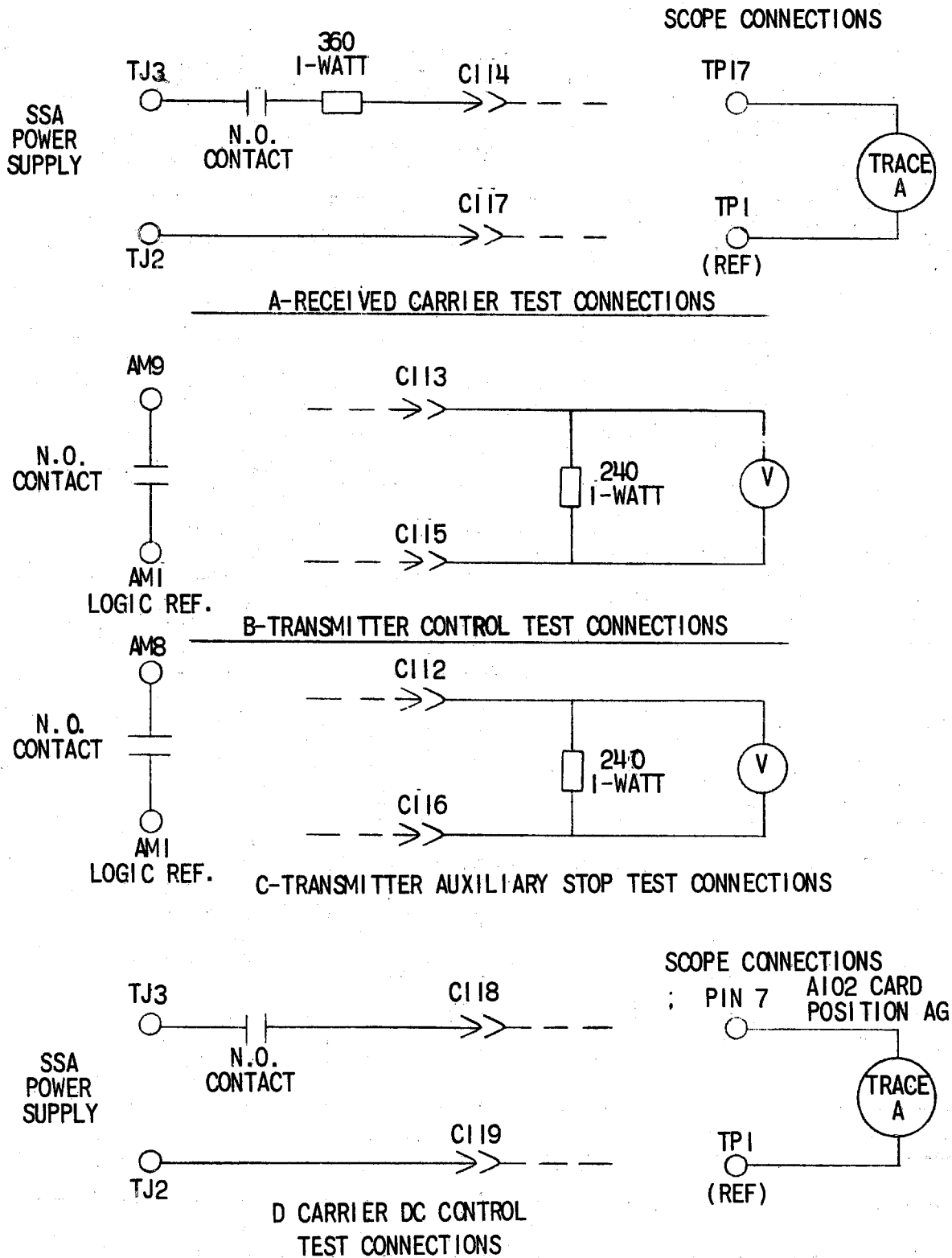


FIG. 8 (0246A6245-0) ISOLATION INTERFACE TEST CIRCUIT

THE FOLLOWING CONNECTIONS ARE TO BE MADE TO THE  
MATRIX BLOCKS INSIDE OF THE SLA LOGIC UNIT.

24

FROM	TO	FROM	TO	FROM	TO
B1	Y13				
B2	G6				
B4	Y14				
B5	Y12				
B6	Y11				
B7	B11				
B8	R19				
B9	R15				
B15	R1				
B16	R3				
B20	R5				

FIG. 9 (0227A2050-0 SH.24)SAMPLE OPTION CHART FOR THE TYPE SLA51D RELAY