INSTRUCTIONS

GEK-45327A

STATIC AUXILIARY

LOGIC RELAY

TYPE SLA52D

GENERAL ELECTRIC

CONTENTS

STATIC AUXILIARY (11385)
LOGIC RELAY (11385)
TYPE SLA52D (11385)

DESCRIPTION

Type SLA52D auxiliary logic relay is not intended to be used by itself, but rather as part of a complement of equipment that forms a relay protective relaying scheme. The inputs of this relay are obtained from the equipment measuring relays and the outputs of this unit are supplied to the associated tripping relay, channel equipment and data logging amplifiers. Input and output connections are provided by ten conductor shielded cables and specific sockets mounted on the rear of this relay. For a description of the overall scheme in which this relay is employed, refer to the overall logic diagram and its associated logic description that is supplied with each terminal of equipment.

The internal connection diagram for the SLA52D relay is shown in Figure 1. This relay is packaged in a four rack unit (1 R. U. = 1 3/4") enclosed metal case suitable for mounting on a 19-inch rack, the outline and mounting dimensions are shown in Figure 3.

APPLICATION

Type SLA52D relay was originally designed to operate in conjunction with the following relay types: SLYP, SLYN, SLC and SLAT in a directional comparision scheme for series compensated lines. The SLA52D design in corporates circuit flexibility to permit various logic options. Refer to the overall logic diagram, internal connection diagram and associated option chart for a particular equipment to determine which logic options are utilized. If any unconnected matrix option points are shown on the associated overall logic diagram it is the user's responsibility to select the desired utilization. The logic description that accompanies the overall logic diagram will generally discuss the merits of those options indicated on the overall logic diagram.

RATINGS

SLA52D relay is designed for use in an environment where the air temperature outside the relay case does not exceed 65 degrees C.

This relay requires a ±15 volt DC power source which can be obtained from a Type SSA (form 50 and higher) power supply.

Each contact converter in this relay has a link for selecting the proper voltage for the included coil circuit. The three possible voltages are 48, 125, and 250 VDC.

OPERATING PRINCIPLES

Logic Circuits

Functions of this relay involve basic logic (and, or, and not) and timers where the presence of absence of signals, rather than their magnitude, controls the operation. All signals are measured with respect to relay reference bus accessible at the preselected test point (TPI) and pin 1 of all logic cards except network cards (type N). In general, a signal below 1 VDC represents an OFF or LOGIC ZERO condition; an ON or LOGIC ONE condition is represented by a signal of approximately +15 VDC.

The symbols used on the internal connection diagram, Figure 1, are explained by the legend shown in Figure 4.

Matrix block connections shown in the internal connection diagram are prewired at the factory per the associated option chart. These connections are shown on the associated overall logic diagram. A sample option chart is shown in Figure 5.

Some of the matrix block connections may be customer options, which will be shown as options on the overall logic and must be selected by the user before the relay is placed in service.

CONTACT CONVERTERS

This function converts an external contact operation through a relay isolator into a signal that is compatible with the logic circuit of the SLA52D relay. The included contact converters are identified as CC1, CC2, and CC3.

A. CONTACT CONVERTER CC1

This converter is energized by a contact associated with the external reclose circuitry and provides a logic 1 when reclosure is initiated. Output of CC1 energizes TL5 which provides an inhibit signal to MB operation following breaker main pole closure.

B. CONTACT CONVERTER CC2

Contact converter CC2 is energized by an external contact and provides an output to key the transmitter through OR12.

C. CONTACT CONVERTER CC3

This converter provides on input to AND15 and is energized by an external channel failure indication contact. A combination of reclose attempt, fault detector output and a channel failure will produce an AND15 direct trip output.

DATA MONITORING POINTS

Type SLA52D relay has provisions to provide 30 data monitoring outputs. The data monitoring (DLA) points are selected on the matrix blocks and are listed on the option chart. Any matrix block points which are not used for logic connections may be monitored. Key points in the logic have more than one matrix point to allow both logic and monitoring connections. A data logging amplifier (DLA) relay is used to translate these logic signals into usable outputs.

CHANNEL INTERFACE

The Type SLA52D relay includes an isolation interface, Figure 6, between the relays in the scheme and the associated channel. Circuitry of the isolation interface provides a signal path but maintains metallic isolation. This feature makes it possible to maintain isolation between the DC supply used for the relays and that employed by the channel.

When pins 9 and 10 are both connected to the relay reference, a metallically separate positive logic signal appears at pin 11 with respect to pin 12. The output from the isolation interface is a 5 VDC, 20 ma signal.

CALCULATION OF SETTINGS

This section covers those timers in the SLA52D that require field adjustment.

TL2 (10-30/100-300)

The TL2 timer is intended to maintain co-ordination between MB and MT on external capacitive faults where breaker failure occurs. Refer to the logic description for specific recommendations.

TL3 (1-8/10-80) and TL10 (1-8/0)

These timers provide the co-ordinating time delay between the tripping units at one end and the blocking units at the other. Both timers are used in a blocking scheme, while only TL3 is used in an unblocking or permissive trip scheme. Refer to the logic description for specific recommendations.

TL5 (P/25-200)

The TL5 timer is used in the line pickup scheme to provide a permissive signal for 3 or 4 cycles after the line is closed on a fault (assuming V1, does not pickup). A typical setting is 200 MS dropout.

TL1 (10-80/10-80)

The TL1 timer is part of the out of step blocking circuitry and its setting is dependant on the MOB setting and system conditions, as described in the logic description.

TL6 AND TL7 (10-80/10)

These two timers, when used, permit time delay to be added in the circuitry for special situations, which will be discussed in the logic description.

TL11 (10-80/10-80)

This timer is used in a signal repeat circuit when the unblocking mode is used. A typical pickup and reset setting is 50 MS.

CONSTRUCTION

The SLA52D relay is packaged in an enclosed metal case with hinged front covers and removable top cover. The outline and mounting dimensions of the case and the physical location of the components are shown in Figures 2 and 3 respectively.

The SLA52D relay contains printed circuit cards identified by a code number such as A111, T102, L104 where A designates auxiliary function, T designates time delay function, and L designates logic function. The printed circuit cards plug in from the front of the unit. The sockets are marked with letter designations or "addresses" (D, E, F, etc.) which appear on the guide strips in front of each socket, on the component location drawing, on the internal connection diagram and on the printed circuit card. The test points (TP1, TP2, etc.) shown in the internal connection diagram are connected to instrument jacks on a test card in position T or AT with TP1 at the top of the AT card. TP10 is tied to +15 VDC through a 2.2KΩ resistor. This resistor limits the current when TP10 is used to supply a logic signal to a card.

The links shown on the internal connection diagram are used to select certain logic options. The links are located on the printed circuit cards.

Other logic options are selected by means of taper tip jumpers and matrix blocks. These matrix blocks are located in the rear of the unit as shown in Figure 3. The green (G), black (B), white (W), orange (O) and violet (V) matrix blocks have 20 individual matrix points. The red (R) block has 20 points which are grouped in pairs. The yellow (Y) block has 20 points which are grouped in 10 common points; 1 to 10 are tied to +15 VDC, 11 to 20 are tied to reference. Tools for inserting and removing the taper tip jumpers are supplied with each relay.

RECEIVING, HANDLING and STORAGE

These relays will normally be supplied as a part of a static relay equipment, mounted in a rack or cabinet with other static relays and test equipment. Immediately upon receipt of a static relay equipment, it should be unpacked and examined for any damage sustained in transit. If injury or damage resulting from rough handling is evident, file a damage claim at once with the transportation company and promptly notify the nearest General Electric Sales Office.

Reasonable care should be exercised in unpacking the equipment. If the equipment is not to be installed immediately, it should be stored indoors in a location that is free from moisture, dust, metallic chips, and severe atmospheric contaminants.

Just prior to final installation the shipping support bolt should be removed from each side of all relay units, to facilitate possible future unit removal for maintenance. These shipping support bolts are approximately 8 inches back from the relay front panel. Static relay equipment, when supplied in swing rack cabinets, should be securely anchored to the floor or to the shipping pallet to prevent the equipment from tipping over when the swing rack is opened.

INSTALLATION TESTS

CAUTION

THE LOGIC SYSTEM SIDE OF THE DC POWER SUPPLY USED WITH MOD III STATIC RELAY EQUIPMENT IS ISOLATED FROM GROUND. IT IS A DESIGN CHARACTERISTIC OF MOST ELECTRONIC INSTRUMENTS THAT ONE OF THE SIGNAL INPUT TERMINALS IS CONNECTED TO INSTRUMENT CHASSIS. IF THE INSTRUMENT USED TO TEST THE RELAY EQUIPMENT IS ISOLATED FROM GROUND, ITS CHASSIS MAY HAVE AN ELECTRICAL POTENTIAL WITH RESPECT TO GROUND. THE USE OF A TEST INSTRUMENT WITH A GROUNDED CHASSIS WILL NOT AFFECT THE TESTING OF THE EQUIPMENT. A SECOND GROUND CONNECTION TO THE EQUIPMENT, SUCH AS A TEST LEAD INADVERTENTLY DROPPING AGAINST THE RELAY CASE, MAY CAUSE DAMAGE TO THE LOGIC CIRCUITRY. NO EXTERNAL TEST EQUIPMENT SHOULD BE LEFT CONNECTED TO THE STATIC RELAYS WHEN THEY ARE IN PROTECTIVE SERVICE, SINCE TEST EQUIPMENT GROUNDING REDUCES THE EFFECTIVENESS OF THE ISOLATION PROVIDED.

GENERAL

If the SLA52D relay that is to be tested is installed in an equipment which has already been connected to the power system, disconnect the outputs in the associated Type SLAT relay from the system.

The SLA52D relay is supplied from the factory either mounted in a static relay equipment or as a separate unit associated with measuring relays, a Type SSA power supply, and some form of channel equipment. All relay units for a given terminal of static relaying equipment are tested together at the factory, and each unit will have the same summary number stamped on its nameplate.

In general, when a time range is indicated on the internal connections diagram, the timer has been factory set at a mid-range value. Timers should be set for the operating and reset times indicated on the associated overall logic diagram. Where a time range is indicated on the overall logic diagram, the timer should be set for the value recommended for that function in the descriptive writeup accompanying the overall logic diagram. Where a setting depends upon conditions encountered on a specific application, this is so stated and the factors influencing the choice of setting are described. The procedure for checking and setting the timers is described in a later section.

OPERATIONAL CHECKS

Operation of the SLA52D unit can be checked by observing the signals at the twenty test points (TP1 to TP20) in the SLA52D, by observing the operation of the associated channel equipment, or by observing the output functions in the associated Type SLAT tripping relay. The test points are located on two test cards in positions T and AT, and are numbered 1 to 20 from top to bottom. TP1 is the reference bus for the logic circuit; TP10 is at +15 VDC. The remaining points are located at various strategic points throughout the logic as shown on the internal connection diagram (Figure 1). Test point voltages can be monitored with a portable high impedance voltmeter, the voltmeter on the test panel of the associated equipment, or an oscilloscope.

TEST CARD ADAPTER

The test card adapter provides a convenient means of gaining access to any pin of a particular card. Detailed information on the use of the test adapter card is included in the card instruction book GEK-34158.

TIMER ADJUSTMENTS AND TESTS

When the time delay cards are to be adjusted or checked, an oscilloscope that can display two traces simultaneously and that has a calibrated horizontal sweep should be used.

In order to test the time cards it is necessary to remove the card previous to the timer (see Table I) and to place the timer card in a card adapter. The card adapter allows access to the input and output of the timer if they are not brought out on test points. The timer test circuit is shown in Figure 7. Opening the N. C. contact causes the output to step up to +15 VDC after the pickup delay of the timer. To increase the pickup time turn the upper potentiometer on the timer card clockwise; to decrease the time turn it counter-clockwise. Closing the contact causes the timer output to drop out after the reset time delay setting of card. If the timer card is provided with a variable reset delay, it can be adjusted by the lower potentiometer on the timer card (CW increases reset time).

TABLE I

TIME UNDER TEST	POSITION**	REMOVE CARD IN POSITION
TL1	AG**	AF
TL2	AE	AD
TL3	K	AK
TL5	AC	A*
TL6	P**	AN
TL7	M**	L
TL10	J**	H
TL11	AJ*	AP
TL12	NON- ADJUSTABLE	

*Also remove S card in associated SLYP, connect Pin 4 of TL5 to Ref.

**NOTE- All cards listed are not supplied see option card chart on internal connection diagram, Figure 1.

CONTACT CONVERTER TESTS

Operation of the contact converters can be checked by placing the contact converter card in a card adapter, after checking the voltage tap selected agrees with the station battery voltage. Connect the station DC through a switch to the appropriate pair of terminals of the terminal strip, AH, mounted on the rear of the relay. The terminal numbers and polarity of connections for each of the three contact converters are shown in the internal connection diagram, Figure 1. Output of the contact converter card may be monitored between pin 8 and pin 1 (reference) on the card adapter with either a scope or meter. Closure of the switch in the test source will provide a +15 volt DC signal at pin 8 of the card adapter.

ISOLATION INTERFACE TESTS

Operation of the three functions (received carrier, transmitter control, and transmitter auxiliary stop) of the isolation interface can be checked without direct connections to the subassembly. External test connections are made to the pins of the C111 socket mounted on the rear of the unit, see Figure 3. Logic circuit test connections are made at the socket pins of the channel control card in position "AP".

Received carrier operation test connections are shown in Figure 8A. For this test do not remove channel control card in position "AP". Closure of the N. O. contact will simulate a received carrier signal and scope display will go from a logic "0" to a logic "1".

For the transmitter control and transmitter auxiliary stop checks remove the channel control card "AP" from its socket and replace it with a test card adapter and test card to gain access to the "AP" socket pins. Transmitter control test connections are shown in Figure 8B. The test contact in the open position simulates a logic "1" condition which holds off the transmitter control output of the isolation interface. Closure of the N. O. contact generates a logic "0" condition initiating a transmitter control output producing, a 5-6 volt DC signal across the output loading resistor. The transmitter auxiliary stop function can be tested in a similar manner using the test connections of Figure 8C and the output again will provide a 5-6 volt DC signal across the output loading resistor.

OVERALL EQUIPMENT TESTS

After the SLA52D relay and the associated static relay units have been individually calibrated and tested for the desired settings, a series of overall operating circuit checks is advisable.

The elementary, overall logic, and logic description for the specific job will be useful

for determining the overall operation of the scheme.

Overall equipment tests can be performed by applying AC current and voltages to the measuring units as specified in the instruction book for the measuring units and checking that proper outputs are obtained from the associated SLAT when the measuring units operate.

MAINTENANCE

PERIODIC TESTS

It should be sufficient to check the outputs produced at test points in the SLA52D when periodic calibration tests are made on the associated measuring units, for example the phase and ground relays in line relaying scheme. No separate periodic tests on the SLA52D itself should be required.

TROUBLE SHOOTING

In any trouble shooting of equipment, it should first be established which unit is functioning incorrectly. The overall logic diagram supplied with the equipment shows the combined logic of the complete equipment and various test points in each unit. By signal tracing, using the overall logic diagram and the various test points, it should be possible to quickly isolate the trouble.

A test adapter card is supplied with each static relay equipment to supplement the prewired test points on the test cards. Use of the adapter card is described in the card instruction book GEK-34158.

A dual-trace oscilloscope is a valuable aid to detailed trouble shooting, since it can be used to determine phase shift, operate and reset times as well as input and output levels. A portable dual-trace oscilloscope with a calibrated sweep and trigger facility is recommended.

SPARE PARTS

To minimize possible outage time, it is recommended that a complete maintenance program should include the stocking of at least one spare card of each type. It is possible to replace damaged or defective components on the printed circuit cards, but great care should be taken in soldering so as not to damage or bridge-over the printed circuit busses, or overheat the semi-conductor components. The repaired area should be recovered with a suitable high-dielectric plastic coating to prevent possible breakdowns across the printed busses due to moisture and dust. The wiring diagrams for the cards in the SLA52D relay are included in the card book GEK-34158.

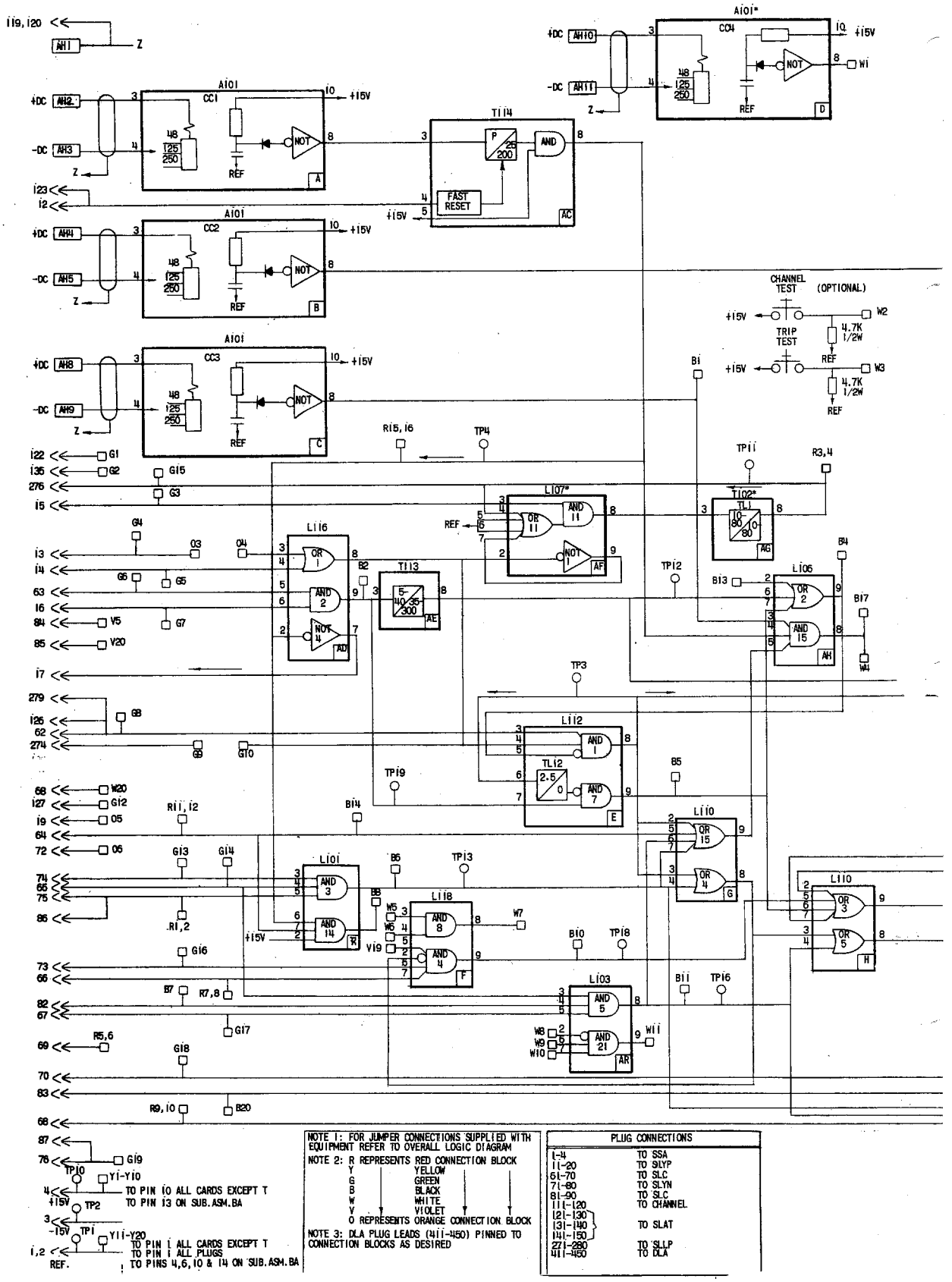
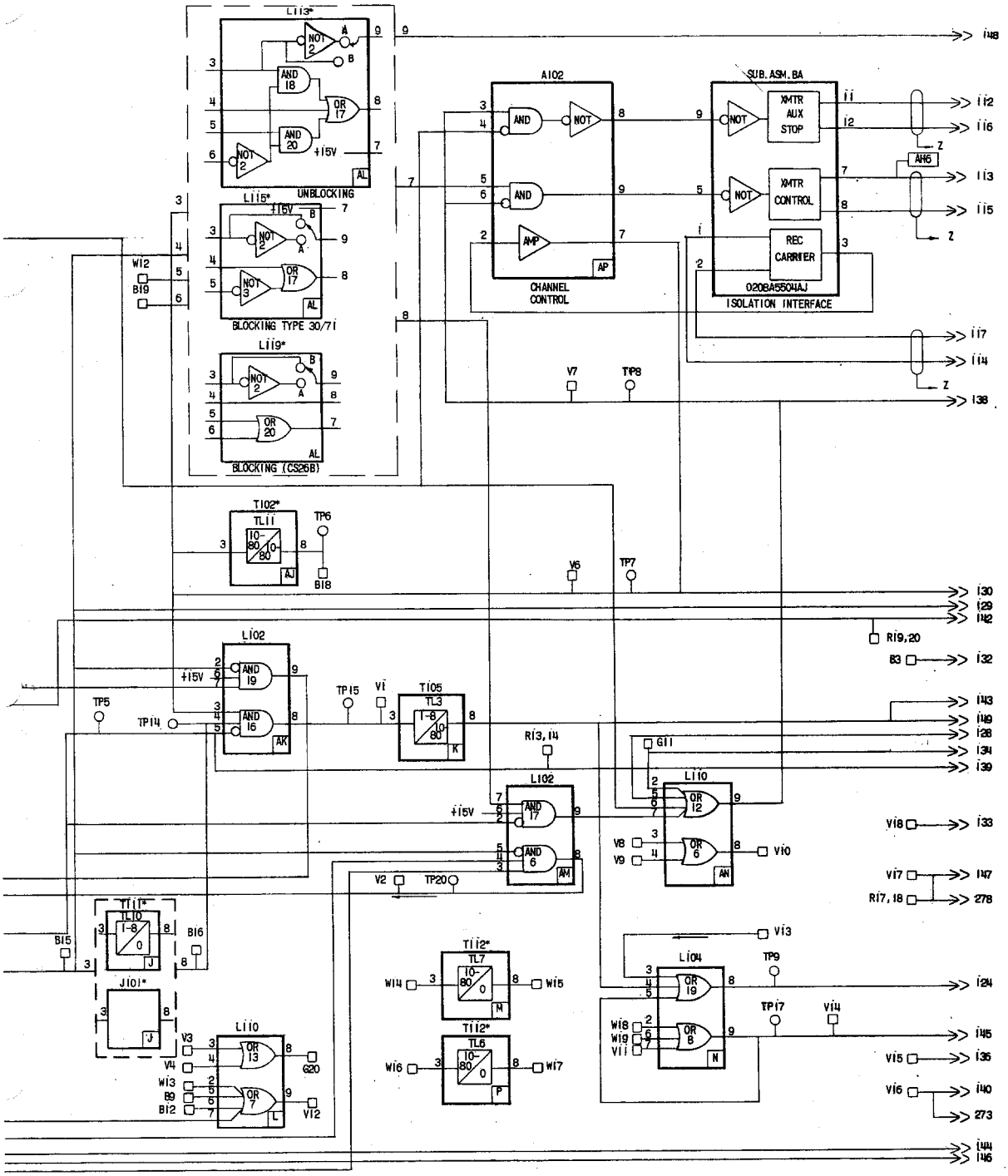


FIG. 1 (0121D9496-0) INTERNAL



* OPTIONAL CARDS - SUPPLIED AS SHOWN BELOW											
CARD LOCATION	D	M	P	AF	AG	AJ	J		AL		
MODEL / CARD CODE	A101	T112	T112	L107	T102	T102	J101	T111	L113	L115	L119
SLA52D1				X	X			X		X	

N DIAGRAM FOR TYPE SLA52D RELAY

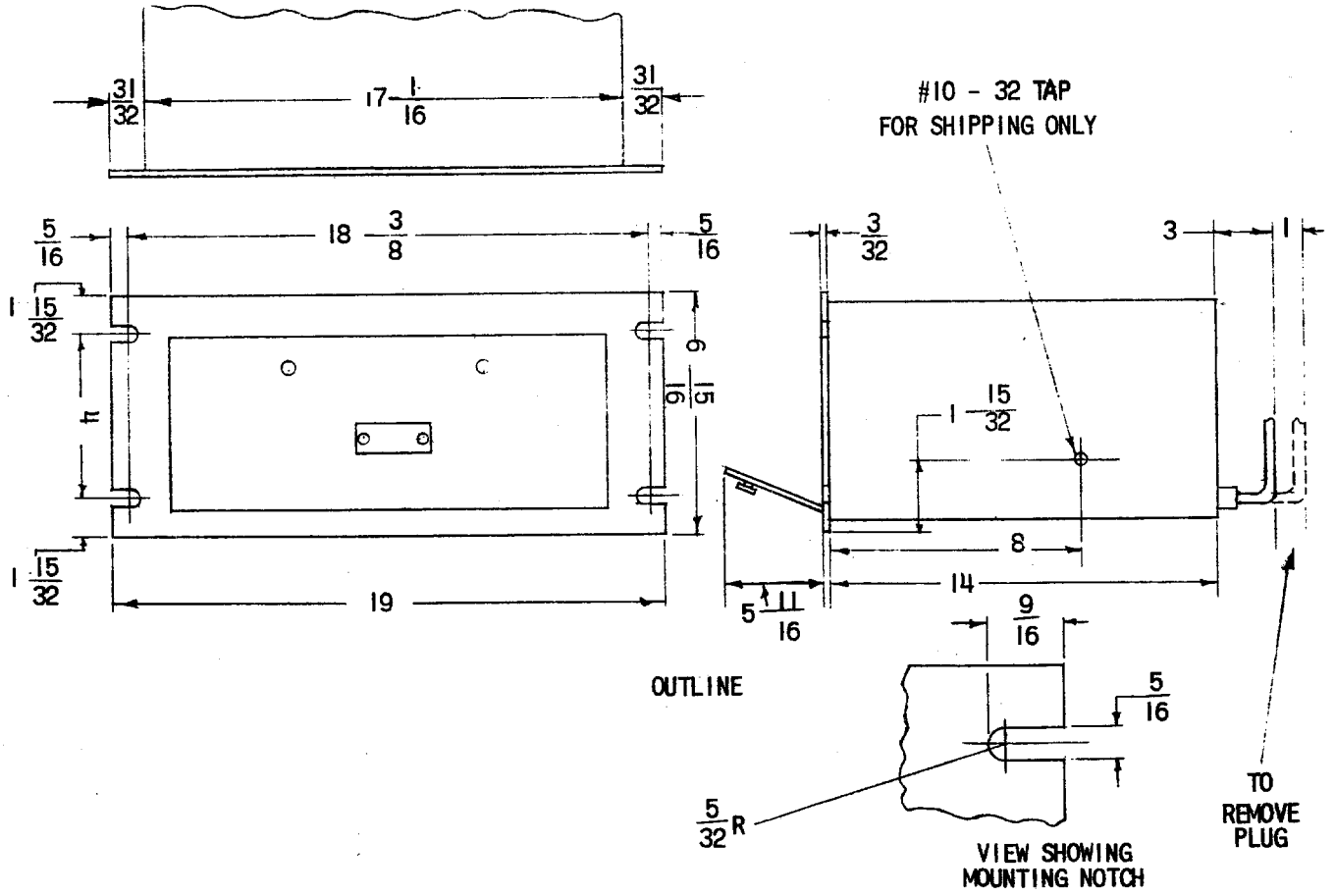


FIG. 2 (0227A2037-0) OUTLINE AND MOUNTING DIMENSIONS FOR THE TYPE SLA52D RELAY

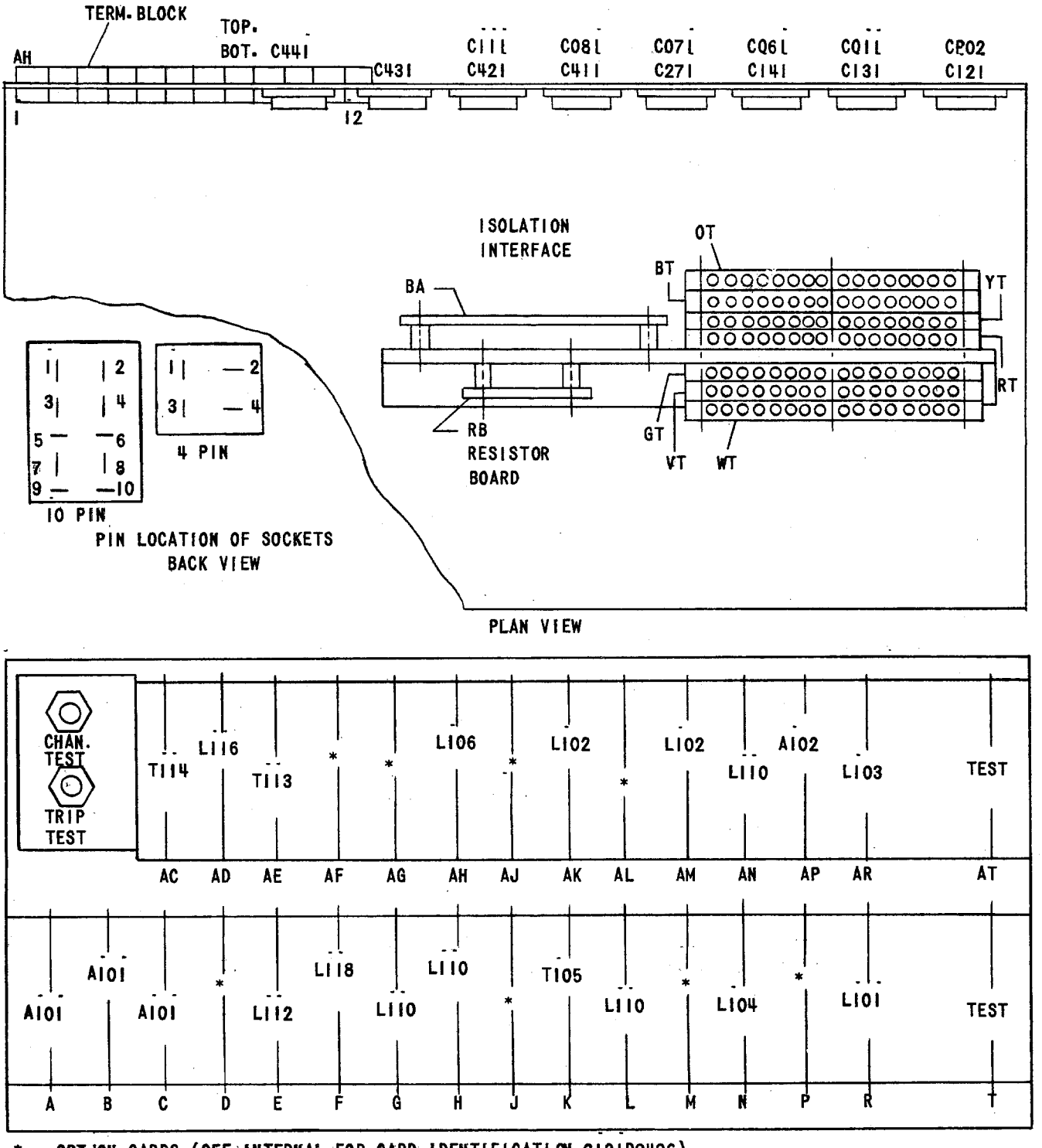


FIG. 3 (0257A5745-0) COMPONENT AND CARD LOCATIONS FOR TYPE SLA52D RELAY

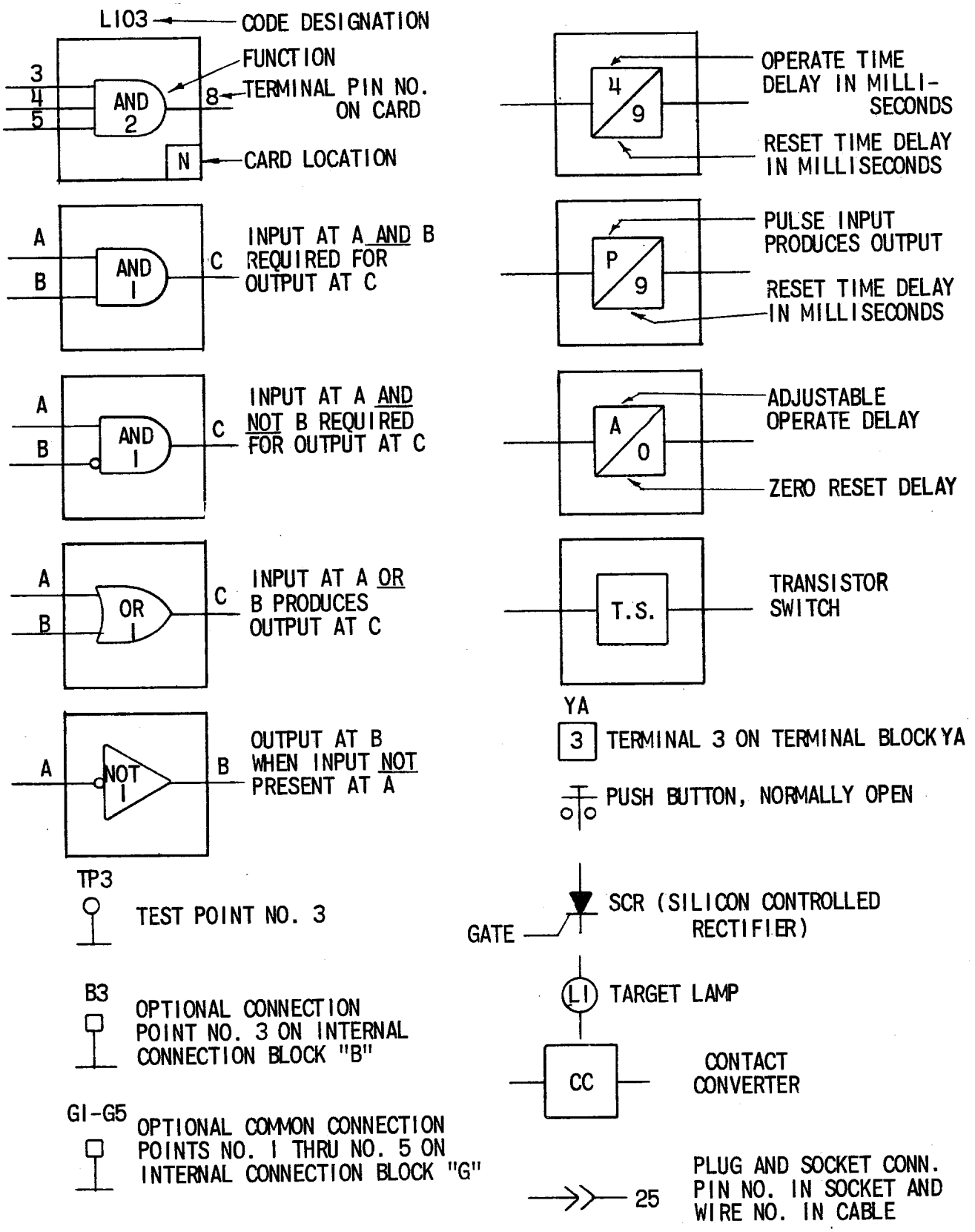


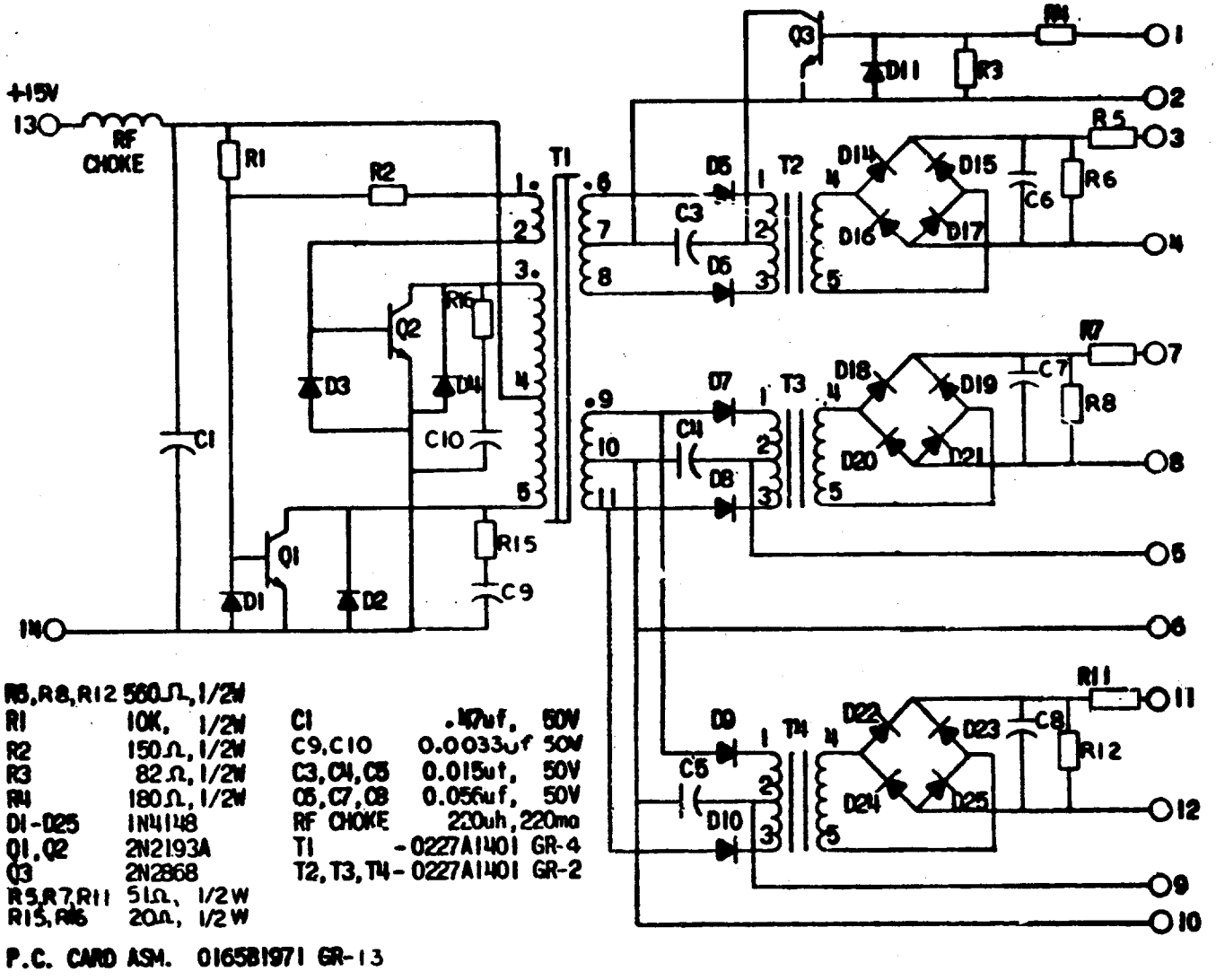
FIG. 4 (0227A2047-0) LOGIC AND INTERNAL CONNECTION DIAGRAM LEGEND

(5)= LOGIC FUNCTION CARD PIN NUMBER

OPTION BLOCK JUMPERS		LOGIC FUNCTION	
FROM	TO	FROM	TO
W2	W12	CHANNEL TEST P.B.	NOT3 (5)
W3	W19	TRIP TEST P.B.	OR8 (6)
W4	V8	AND15(8)	OR6 (3)
Y16	W8	REF	AND21(2)
G4	W9	PL13	AND21(6)
G8	W10	PL62	AND21(7)
W11	V9	AND21(9)	OR6 (4)
W13	Y17	OR7 (2)	REF
V12	W18	OR7 (9)	OR8(2)
V10	V3	OR6 (8)	OR13 (3)
06	V4	PL72	OR13 (4)
G20	V11	OR13 (8)	OR8 (7)
Y3	V19	+15 VOLT	AND4 (5)
G1	G15	PL122	TL1 (8)
Y18	G2	REF	PL135
G19	R7	PL76, PL87	AND4 (7)
V15	B13	REF	OR2 (2)
R5	B12	PL69	OR7 (6)
R19	B3	PL142	PL132
Y19	05	REF	PL19
Y20	04	REF	OR1 (3)
B14	B9	PL64	OR7 (5)

OPTION BLOCK JUMPERS		LOGIC FUNCTION	
FROM	TO	FROM	TO
V13	Y12	OR19	REF

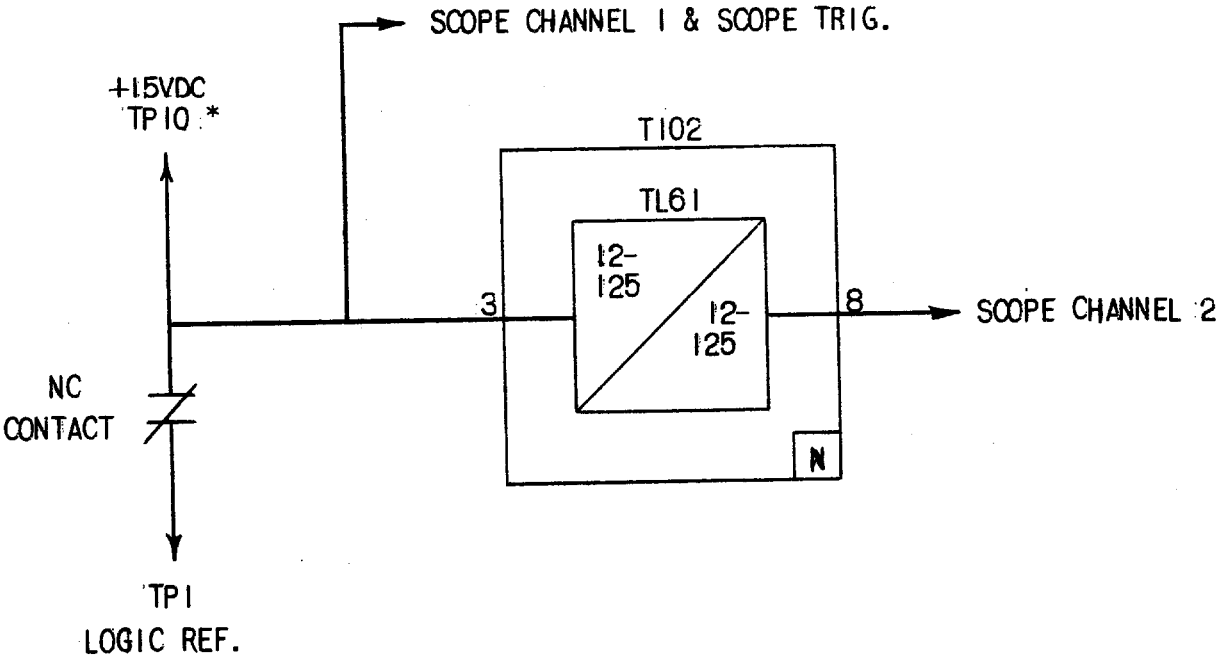
FIG. 5 (0227A2050-0) sh. 33 SAMPLE OPTION CHART



R5,R8,R12	560Ω, 1/2W		
R1	10K, 1/2W	C1	.47uf, 50V
R2	150Ω, 1/2W	C9,C10	0.0033uf 50V
R3	82Ω, 1/2W	C3,C4,C5	0.015uf, 50V
R4	180Ω, 1/2W	C6,C7,C8	0.056uf, 50V
D1-D25	1N4148	RF CHOKE	220uh, 220ma
Q1,Q2	2N2193A	T1	-0227A1401 GR-4
Q3	2N2868	T2,T3,T4	-0227A1401 GR-2
R5,R7,R11	51Ω, 1/2W		
R15,R16	20Ω, 1/2W		

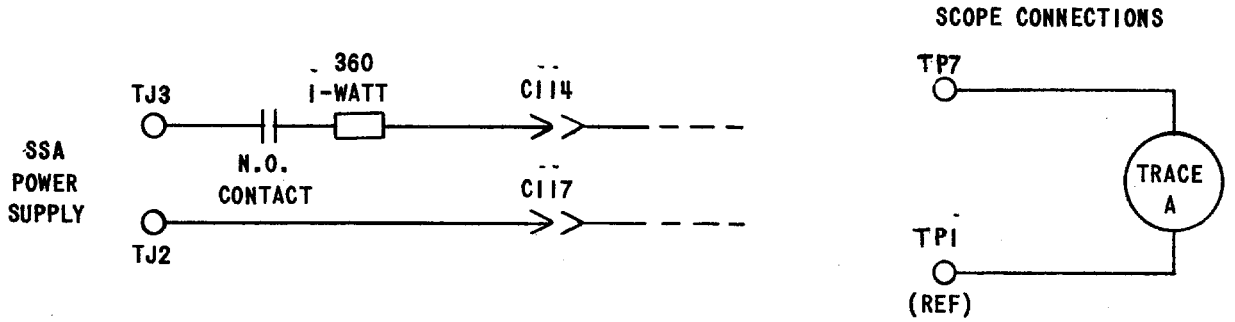
P.C. CARD ASM. 0165B1971 GR-13

FIG. 6 (0208A5504AJ-1) ISOLATION INTERFACE CIRCUIT

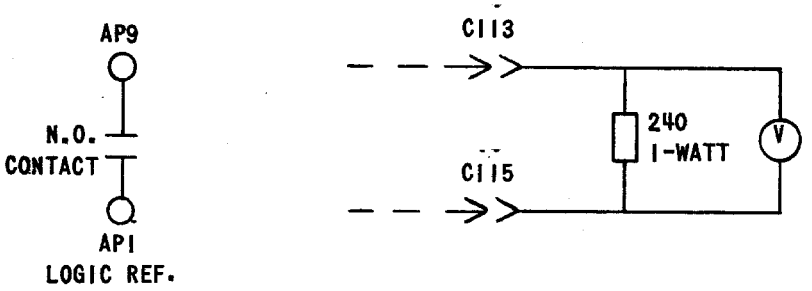


* THE 15VDC SIGNAL AT PIN 10 HAS A CURRENT LIMITING RESISTOR MOUNTED ON THE TEST CARD.

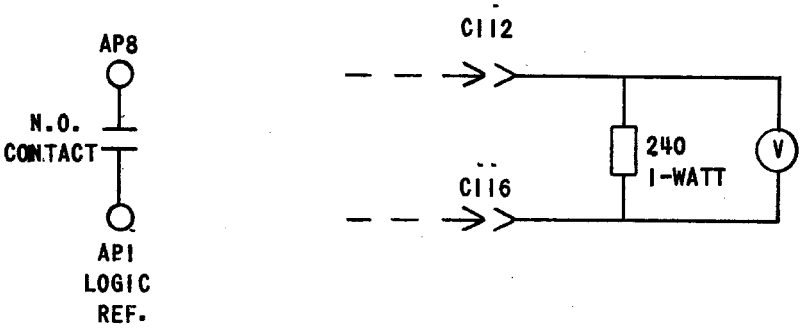
FIG. 7 (0246A7987-0) LOGIC TIMER TEST CIRCUIT



A-RECEIVED CARRIER TEST CONNECTIONS



B-TRANSMITTER CONTROL TEST CONNECTIONS



C-TRANSMITTER AUXILIARY STOP TEST CONNECTIONS

FIG. 8 (0257A6212-0) ISOLATION INTERFACE TEST CONNECTIONS

Meter and Control
Business Department

5/90-200

General Electric Company
205 Great Valley Parkway
Malvern, PA 19355