INSTRUCTIONS

GEK-45445

STATIC AUXILIARY

LOGIC RELAY

TYPE SLA52F

POWER SYSTEMS MANAGEMENT DEPARTMENT

GENERAL ELECTRIC

PHILADELPHIA, PA.

CONTENTS

DESCRIPTION

The SLA52F relay is an auxiliary logic unit used in conjunction with fault detecting relays such as the SLYP and SLCN, and an output relay, SLAT, to form a directional comparison relaying scheme for series compensated lines or uncompensated lines. The SLA52F is designed for use with carrier equipment in blocking schemes.

The SLA52F has the flexibility of design to permit adding a number of options in the field such as direct trip units, "line pickup" circuitry, etc. This design flexibility is achieved by the use of option matrix points and prewired sockets for optional card additions.

Refer to the logic description for a description of the type of scheme provided, the initial optional features selected, and application considerations to determine the timer settings, as well as the fault detector settings in the SLYP and SLCN.

RATINGS

The SLA52F relay is designed for use in an environment where the air temperature outside the relay case is between -20°C and +65°C.

The Type SLA52F relay requires a +15 VDC power source which can be obtained from a Type SSA power supply.

Each contact converter in this relay has a link for selecting the proper voltage for the coil circuit of the contact converter. The three possible voltages are 48 VDC, 125 VDC and 250 VDC.

BURDENS

The SLA52F relay presents a burden of 300 ma to the +15 VDC supply of the Type SSA power supply.

Each contact converter, when energized, will draw approximately 10 ma from the station battery, regardless of tap setting.

OPERATING PRINCIPLES

A. LOGIC CIRCUIT

The functions of the Type SLA52F relay involve basic logic (AND, OR, AND NOT) where the presence or absence of signals, rather than their magnitude, controls the operation. Signals are measured with respect to a reference bus accessible at TP1. In general, a signal below 1 VDC represents an OFF or LOGIC ZERO condition; and ON or LOGIC ONE condition is represented by a signal of approximately +15 VDC.

The symbols used on the internal connection diagram (Figure 1) are explained by the legend shown in Figure 2.

The matrix block connections shown in the internal connections of the SLA52F relay are prewired at the factory. The connections are shown on the associated overall logic and are listed on the associated option chart. A sample option chart for the TYPE SLA52F relay is shown in Figure 3.

Some of the matrix block connections may be customer options. In this instance, they will be shown as options on the overall logic and must be selected by the user before the unit is placed in service.

B. CONTACT CONVERTERS

The purpose of this function is to convert a contact operation into a signal that is compatible with the logic circuit of the TYPE SLA52F relay. These contact converters are labeled CC1, CC2, and CC3.

CC1, CC2, CC3

These converters are incorporated into the relay thru matrix point connections. This type of incorporation provides many specialized circuit arrangements to suit individual customer's present and future needs.

C. CHANNEL INTERFACE

The logic of the Type SLA52F relay includes an isolation interface (Figure 4) between the relays in the scheme and associated carrier. The circuitry of the isolation interface provides a signal path but maintains isolation. This feature makes it possible to maintain isolation between the DC supply used for the relays and that employed by the channel.

When pins 9 and 10 are both connected to relay reference, a metallically separate positive logic signal appears at pin 11 with respect to 12. The output from the isolation interface is a 5 VDC, 20 ma signal.

CALCULATION OF SETTINGS

Refer to the logic description for application considerations in determining the timer settings requiring field adjustment.

CONSTRUCTION

The SLA52F relay is packaged in an enclosed metal case with hinged front covers and removable top cover. The outline and mounting dimensions of the case and the physical location of the components are shown in Figures 5 and 6 respectively.

The SLA52F relay contains printed circuit cards indentified by a code number such as A111, T102, L104 where A designates auxiliary function, T designates time-delay function, and L designates logic function. The printed circuit cards plug in from the front of the unit. The sockets are marked with letter designations or "addresses" (D,E,F, etc.) which appear on the guide strips in front of each socket, on the component location drawing, on the internal connection diagram and on the printed circuit card. The test points (TP1, TP2, etc.) shown in the internal connection diagram are connected to instrument jacks on a test card in position T or AT with TP1 at the top of the AT card. TP10 is tied to +15 VDC through a 1.5KΩ resistor. This resistor limits the current when TP10 is used to supply a logic signal to a card.

The links shown on the internal connection diagram are used to select certain logic options. The links are located on the printed circuit cards.

Other logic options are selected by means of taper tip jumpers and matrix blocks. These matrix blocks are located in the rear of the unit as shown in Figure 6. The green (G), black (B), white (W), brown (BR), red (R), orange (O), and violet (V) matrix blocks have 20 individual matrix points. The yellow (Y) block has 20 points which are grouped in 10 common points; 1 to 10 are tied to +15 VDC, 11 to 20 are tied to reference. Tools for inserting and removing the taper tip jumpers are supplied with each relay.

RECEIVING HANDLING AND STORAGE

These relays will normally be supplied as a part of a static relay equipment, mounted in a rack or cabinet with other static relays and test equipment. Immediately upon receipt of a static relay equipment, it should be unpacked and examined for any damage sustained in transit. If injury or damage resulting from rough handling is evident, file a damage claim at once with the transportation company and promply notify the nearest GENERAL ELECTRIC SALES OFFICE.

Reasonable care should be exercised in unpacking the equipment. If the equipment is not to be installed immediately, it should be stored indoors in a location that is free from moisture, dust, metallic chips, and severe atmospheric contaminants.

Just prior to final installation the shipping support bolt should be removed from each side of all relay units to facilitate possible future unit removal for maintenance. These shipping support bolts are approximately 8 inches back from the relay front panel. Static relay equipment, when supplied in swing rack cabinets, should be securely anchored to the floor or to the shipping pallet to prevent the equipment from tipping over when the swing rack is opened.

INSTALLATION TESTS

If the SLA52F relay that is to be tested is installed in an equipment which has already been connected to the power system, disconnect the outputs in the associated Type SLAT relay from the system.

CAUTION

THE LOGIC SYSTEM SIDE OF THE DC POWER SUPPLY USED WITH MOD III STATIC RELAY EQUIPMENT IS ISOLATED FROM GROUND. IT IS A DESIGN CHARACTERISTIC OF MOST ELECTRONIC INSTRUMENTS THAT ONE OF THE SIGNAL INPUT TERMINALS IS CONNECTED TO INSTRUMENT CHASSIS. IF THE INSTRUMENT USED TO TEST THE RELAY EQUIPMENT IS ISOLATED FROM GROUND, ITS CHASSIS MAY HAVE AN ELECTRICAL POTENTIAL WITH RESPECT TO GROUND. THE USE OF A TEST INSTRUMENT WITH A GROUNDED CHASSIS WILL NOT AFFECT THE TESTING OF THE EQUIPMENT. A SECOND GROUND CONNECTION TO THE EQUIPMENT, SUCH AS A TEST LEAD INADVERTENTLY DROPPING AGAINST THE RELAY CASE, MAY CAUSE DAMAGE TO THE LOGIC CIRCUITRY. NO EXTERNAL TEST EQUIPMENT SHOULD BE LEFT CONNECTED TO THE STATIC RELAYS WHEN THEY ARE IN PROTECTIVE SERVICE, SINCE TEST EQUIPMENT GROUNDING REDUCES THE EFFECTIVENESS OF THE ISOLATION PROVIDED.

A. GENERAL

The SLA52F relay is supplied from the factory either mounted in a static relay equipment or as a separate unit associated with measuring relays, a Type SSA power supply, and some form of carrier equipment. All relay units for a given terminal of static relaying equipment are tested together at the factory, and each unit will have the same summary number stamped on its nameplate.

Timers should be set for the operating and reset times indicated on the associated overall logic diagram. Where a time range is indicated on the overall logic diagram, the timer should be set for the value recommended for that function in the descriptive write-up accompanying the overall logic diagram. Where a setting depends upon conditions encountered on a specific application, this is so stated and the factors influencing the choice of setting are described. The procedure for checking and setting the timers is described in a later section.

B. OPERATIONAL CHECKS

Operation of the SLA52F unit can be checked by observing the signals at the twenty test points (TP1 to TP20) in the SLA52F, by observing the operation of the associated carrier equipment, or by observing the output functions in the associated Type SLAT tripping relay. The test points are located on two test cards in positions T and AT, and are numbered 1 to 20 from top to bottom. TP1 is the reference bus for the logic circuit; TP2 is at -15 VDC and TP10 is at +15 VDC. The remaining points are located at various strategic points throughout the logic as shown on the internal connection diagram (Figure 2). Test point voltages can be monitored with a portable high-impedance voltmeter, the voltmeter on the test panel of the associated equipment, or an oscilloscope.

C. TEST CARD ADAPTER

The test card adapter provides a convenient means of gaining access to any pin of a particular card. Detailed information on the use of the test adapter card is included in the card instruction book GEK-34158

D. TIMER ADJUSTMENTS AND TESTS

When the time-delay cards are to be adjusted or checked, an oscilloscope that can display two traces simultaneously and that has a calibrated horizontal sweep should be used.

In order to test the time cards it is necessary to remove the card which supplies the input to the timer (see Table 1 for normal use) and to place the timer card in a card adapter. The card adapter allows access to the input and output of the timer if they are not brought out on test points. The timer test circuit is shown in Figure 7. Opening the N.C. contact causes the output to step up to +15 VDC after the pickup delay of the timer. To increase the pickup time turn the upper potentiometer on the timer card clockwise; to decrease the time turn it counterclockwise. Closing the contact causes the timer output to drop out after the reset time-delay setting of card. If the timer card is provided with a variable reset delay, it can be adjusted by the lower potentiometer on the time card (CW increases reset time).

TABLE 1

TIMER UNDER TEST	POSITION**	REMOVE CARD IN POSITION
TL1	AB**	A*
TL2	AH**	***
TL3	K**	E
TL4	N**	L
TL5	AJ**	***
TL6	AR	R

* Also remove AS card and, connect pin 4 of TL1 to REF.
** NOTE: All cards listed are not supplied, see option card chart on internal conn. diag. Fig. 1.
*** Refer to option chart or overall logic to decide what card in the SLA52F supplies the input to these timers. Remove these cards to prevent damage to them.

E. CONTACT CONVERTER TESTS

Operation of the contact converters can be checked by placing the contact converter card in a card adapter, after checking the voltage tap selected agrees with the station battery voltage. Connect the station DC through a switch to the appropriate pair of terminals of the terminal strip, AH, mounted on the rear of the relay. The terminal numbers and polarity of connections for each of the three contact converters are shown in the internal connection diagram , Figure 1. Output of the contact converter card may be monitored between pin 8 or 9 and pin 1 (reference) on the card adapter with either a scope or meter. Closure of the switch in the test source will provide a +15 volt DC signal at pin 8 or 9 of the card adapter.

F. ISOLATION INTERFACE TESTS

Operation of the three functions (received carrier, transmitter control, and transmitter auxiliary stop) of the isolation interface can be checked without direct connections to the subassembly. External test connections are made to the pins of the C111 socket mounted on the rear of the unit, see Figure 6. Logic circuit test connections are made at the socket pins of the channel control card in position "AN".

Received carrier operation test connections are shown in Figure 8A. For this test do not remove channel control card in position "AN". Closure of the N.O. contact will simulate a received carrier signal and scope display will go from a logic "0" to a logic "1".

For the transmitter control and transmitter auxiliary stop checks remove the carrier control card "AN" from its socket and replace it with a test card adapter and test card to gain access to the "AN" socket pins. Transmitter control test connections are shown in Figure 8B. The test contact in the open position simulates a logic "1" condition which holds off the transmitter control output of the isolation interface. Closure of the N.O. contact generates a logic "0" condition initiating a transmitter control output producing a 5-6 volt DC signal across the output loading resistor. The transmitter auxiliary stop function can be tested in a similar manner using the test connections of Figure 8C and the output again will provide a 5-6 volt DC signal across the output loading resistor.

G. OVERALL EQUIPMENT TESTS

After the SLA52F relay and the associated static relay units have been individually calibrated and tested for the desired settings, a series of overall operating circuit checks is advisable.

The elementary, overall logic, and logic description for the specific job will be useful for determining the overall operation of the scheme.

Overall equipment tests can be performed by applying AC current and voltages to the measuring units as specified in the instruction boook for the measuring units and checking that proper outputs are obtained from the associated SLAT when the measuring units operate.

MAINTENANCE

A. PERIODIC TESTS

It should be sufficient to check the outputs produced at test points in the SLA52F when periodic calibration tests are made on the associated measuring units, for example the phase and ground relays in line-relaying scheme. No separate periodic tests on the SLA52F itself should be required.

B. TROUBLE SHOOTING

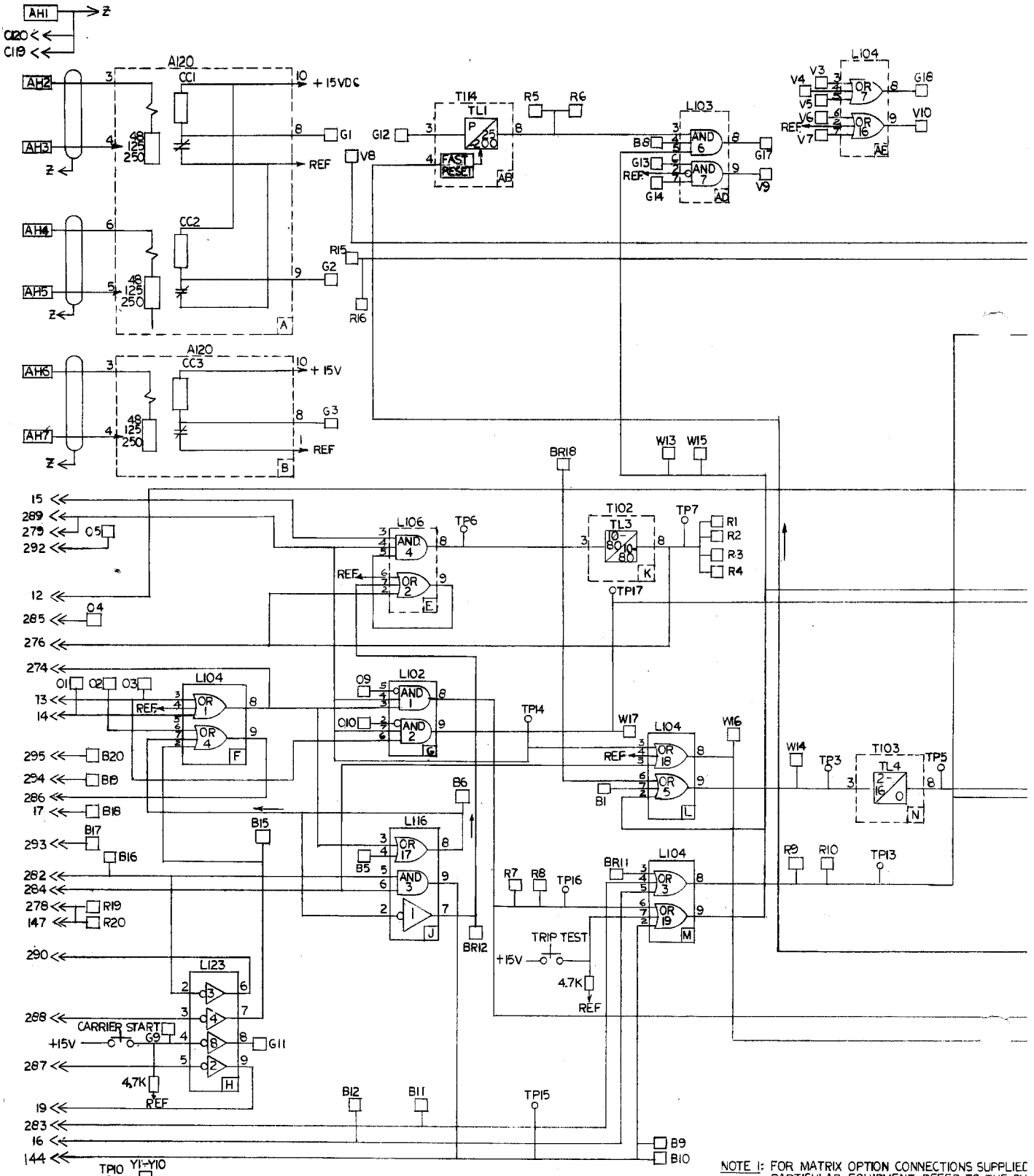
In any trouble shooting of equipment, it should first be established which unit is functioning incorrectly. The overall logic diagram supplied with the equipment shows the combined logic of the complete equipment and the various test points in each unit. By signal tracing, using the overall logic diagram and the various test points, it should be possible to quickly isolate the trouble.

A test adapter card is supplied with each static relay equipment to supplement the prewired test points on the test cards. Use of the adapter card is described in the card instruction book GEK-34158.

A dual-trace oscilloscope is a valuable aid to detailed trouble shooting, since it can be used to determine phase shift, operate and reset times as well as input and output levels. A portable dual-trace oscilloscope with a calibrated sweep and trigger facility is recommended.

C. SPARE PARTS

To minimize possible outage time, it is recommended that a complete maintenance program should include the stocking of at least one spare card of each type. It is possible to replace damaged or defective components on the printed circuit cards, but great care should be taken in soldering so as not to damage or bridge-over the printed circuit busses, or overheat the semi-conductor components. The repaired area should be recovered with a suitable high-dielectric plastic coating to prevent possible breakdowns across the printed busses due to moisture and dust. The wiring diagrams for the cards in the SLA52F relay are included in the card book GEK-34158.

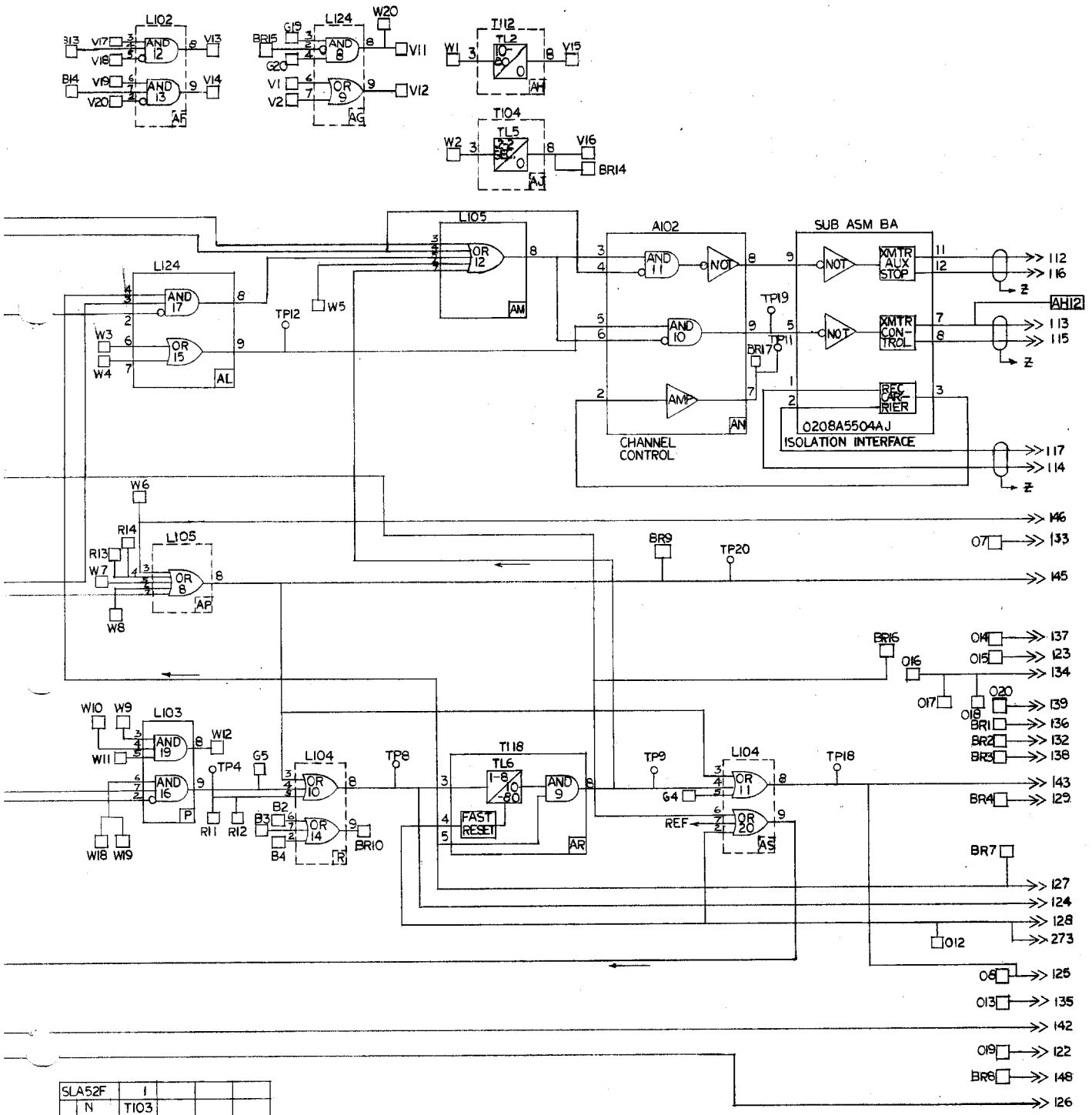


NOTE 1: FOR MATRIX OPTION CONNECTIONS SUPPLIED
PARTICULAR EQUIPMENT, REFER TO THE OV
LOGIC DIAGRAM

NOTE 2:

"R"	REPRENTS	RED
"Y"	"	YELLOW
"O"	"	ORANGE
"G"	"	GREEN
"V"	"	VIOLET
"W"	"	WHITE
"B"	"	BLACK
"BR"	"	BROWN

FIG. 1 (0136D1424-1



SLA52F	1			
OPTIONAL CARDS	N	T103			
	R	L104			
	AB				
	AD				
	AE				
	AF				
	AG	L124			
	AH				
	AJ	T104			
	AP	L105			
	AS	L104			
	A	A120			
	B				
	E				
	K				

SLA52F INTERNAL CONNECTIONS

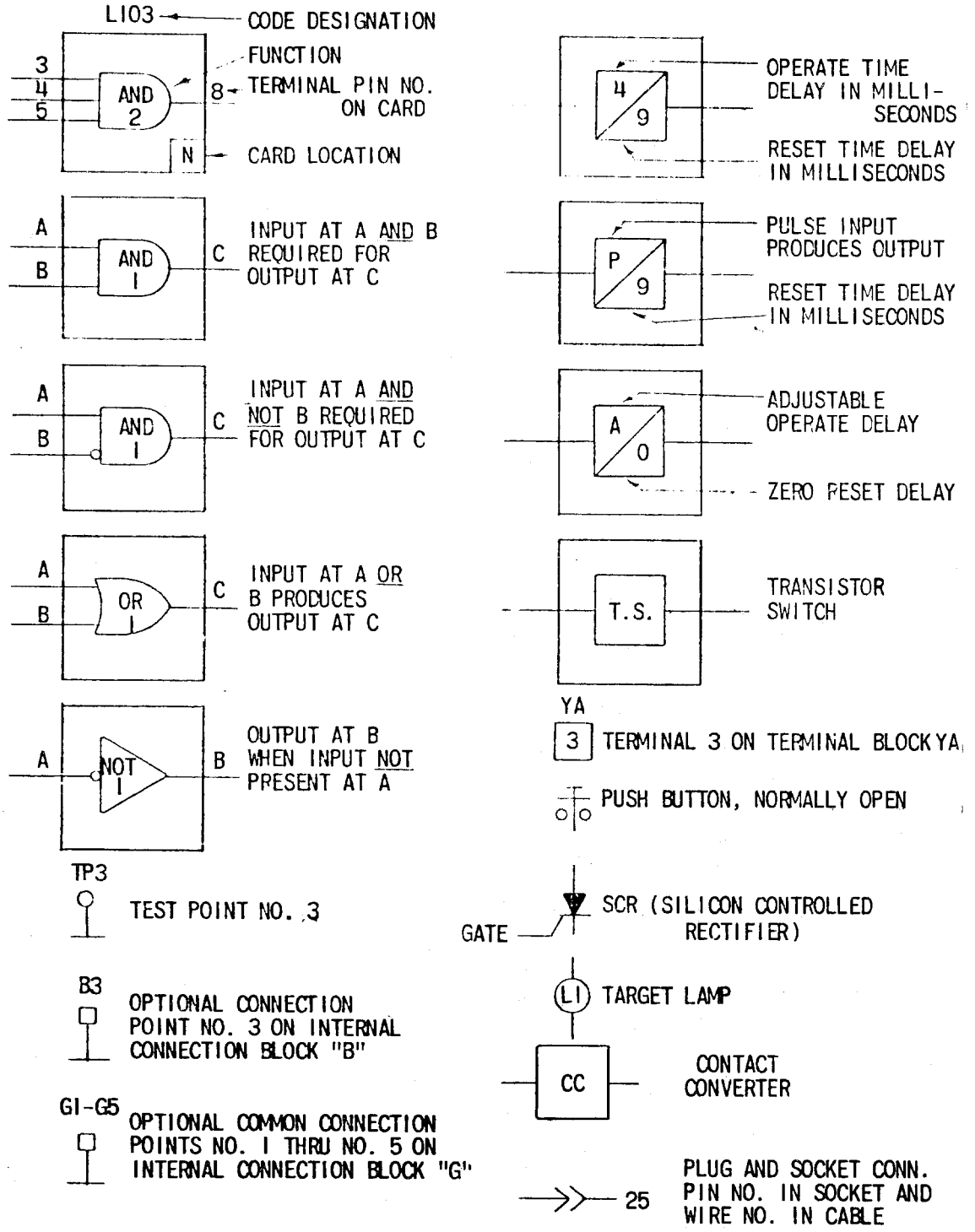


FIG. 2 (227A2047-0) LOGIC AND INTERNAL DIAGRAM LEGEND

PL= CABLE PLUG

(5)=LOGIC FUNCTION CARD PIN NUMBER

(76)

MATRIX BLOCK JUMPERS		LOGIC FUNCTION	
FROM	TO	FROM	TO
O15	Y1	PL123	+15VDC
O4	W6	PL285	OR8 (3)
B12	O10	PL16	AND2(2)
O13	Y11	PL135	REF
R13	Y12	OR8 (4)	REF
W7	R14	OR8 (5)	OR8 (4)
W8	V11	OR8 (6)	AND8(6)
B5	Y14	OR17 (4)	REF
O2	Y15	OR4 (6)	REF
G2	R15	CC2 (9)	OR12 (3)
BR11	R16	OR3 (3)	OR12 (3)
O9	Y16	AND 1 (5)	REF
BR12	B18	NOT 1 (7)	PL17
R9	W3	OR3 (8)	OR15(6)
G9	W4	NOT 8(4)	OR15(7)
W13	W2	OR19 (9)	TL5 (3)
B1	Y17	OR5 (7)	REF

MATRIX BLOCK JUMPERS		LOGIC FUNCTION	
FROM	TO	FROM	TO
BR18	Y18	OR5 (6)	REF
G1	V8	CC1 (8)	OR12(3)
W5	Y19	OR12 (6)	REF
BR17	W18	AMP (7)	AND16
G5	BR8	AND16 (9)	PL148
V16	R11	TL5 (8)	OR10(5)
R12	O19	OR10 (5)	PL122
G4	Y20	OR11 (5)	REF
B19	G20	PL294	AND8(4)
B16	G19	PL282	AND8(3)
R10	BR15	OR3 (8)	AND8(2)
R20	BR14	PL147	TL5 (8)

FIG. 3 (0227A2050-0 SH. 76) SAMPLE OPTION CHART FOR THE TYPE SLA52F RELAY

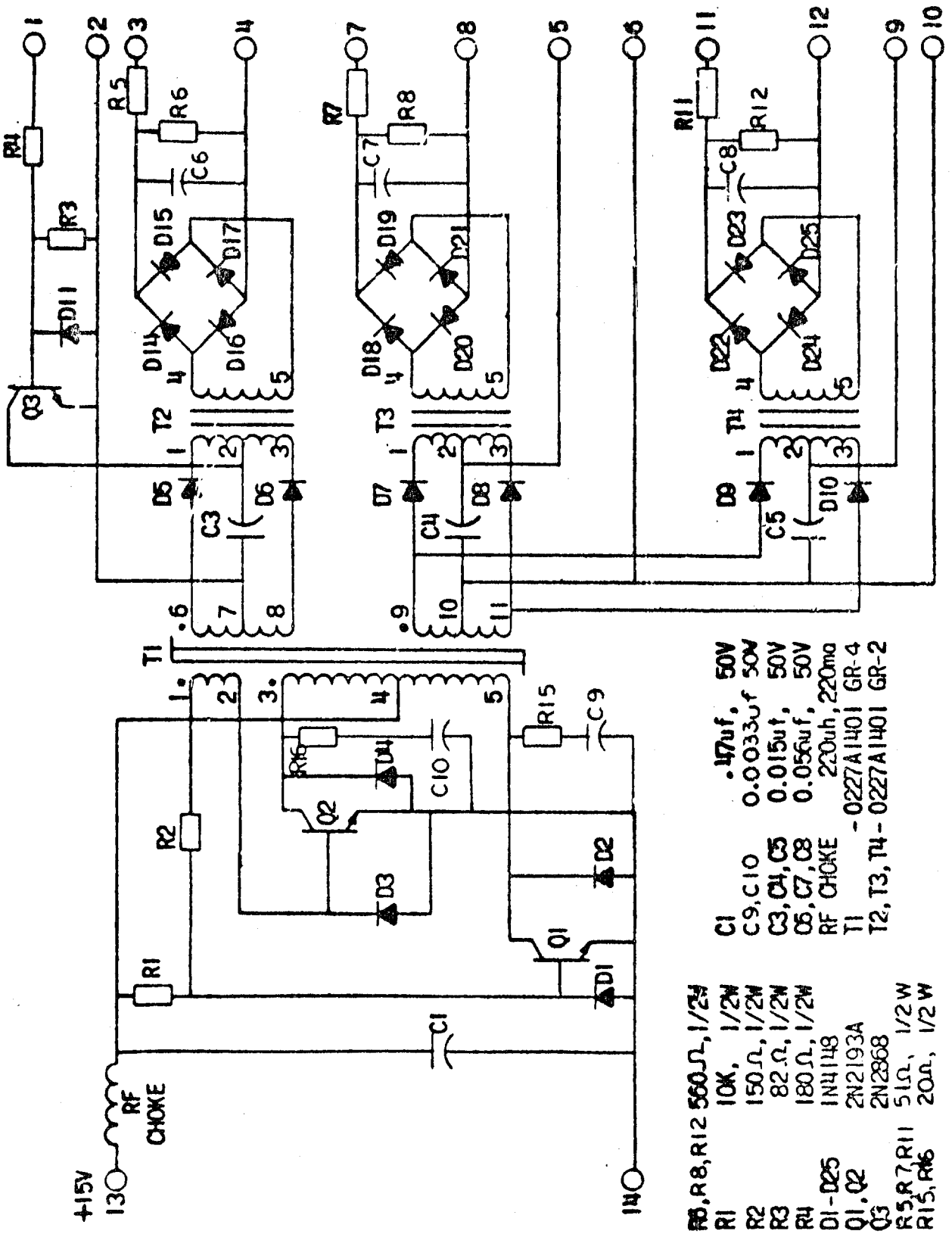


FIG. 4 (0208A5504AJ-1) ISOLATION INTERFACE FOR CS26B

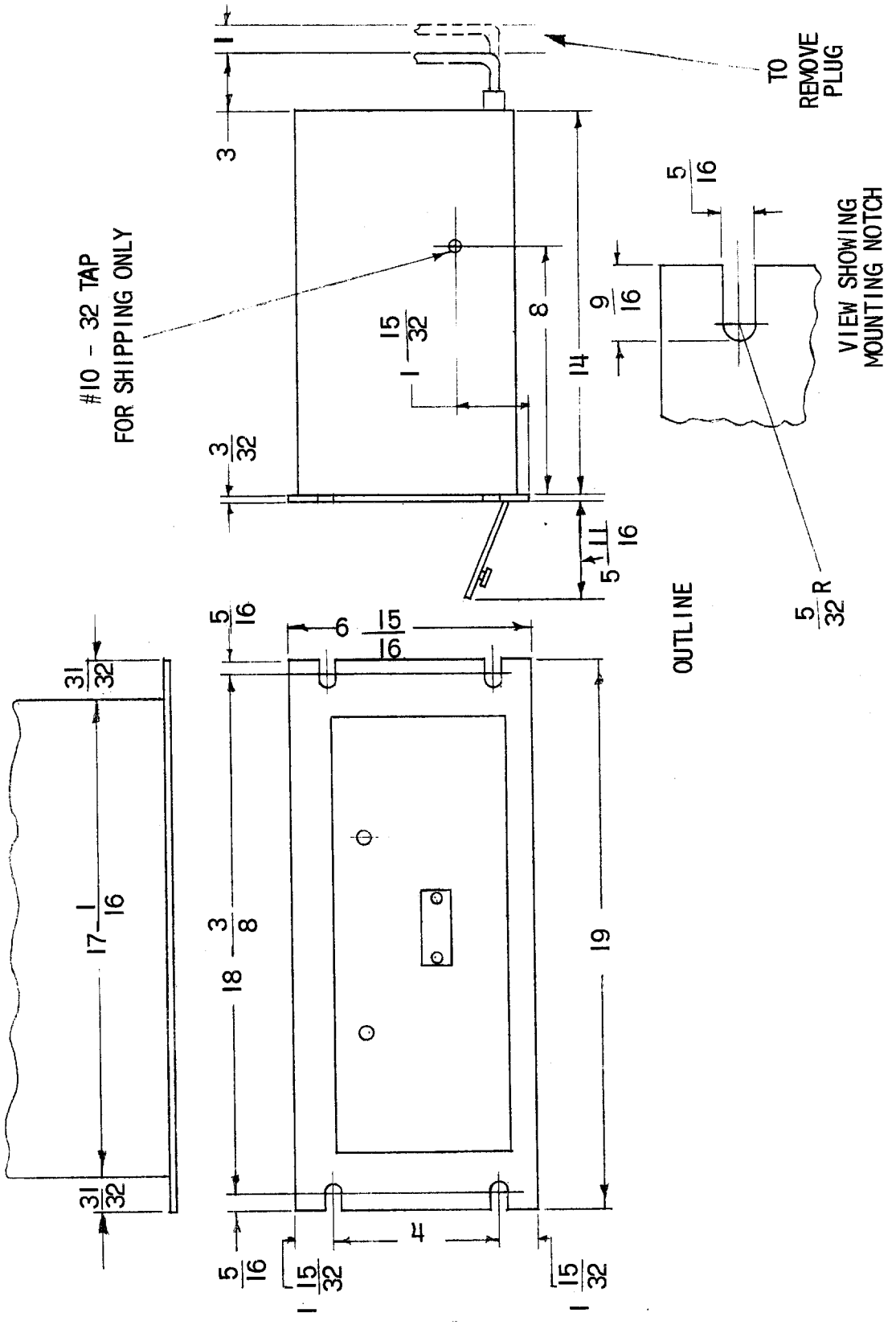
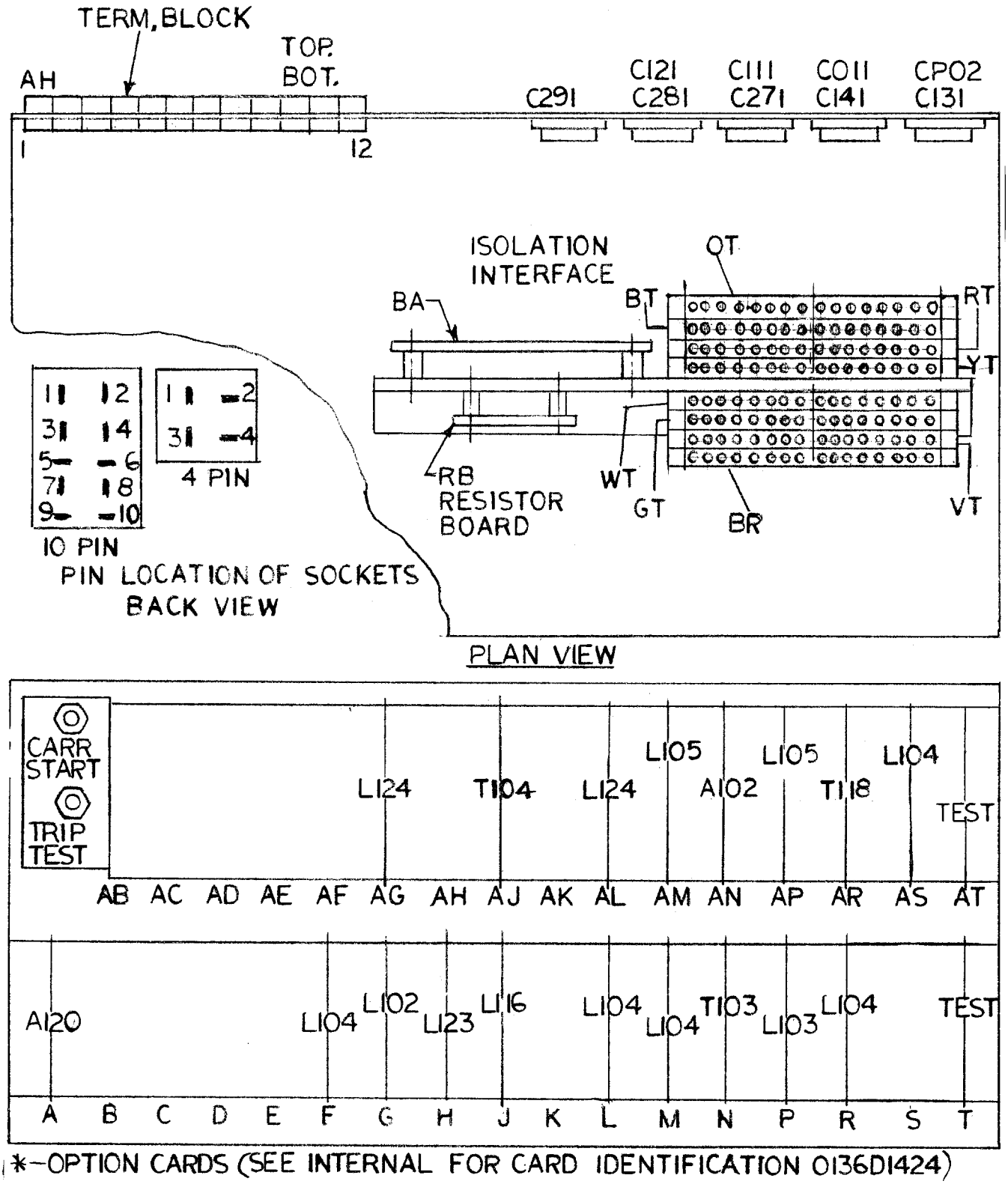
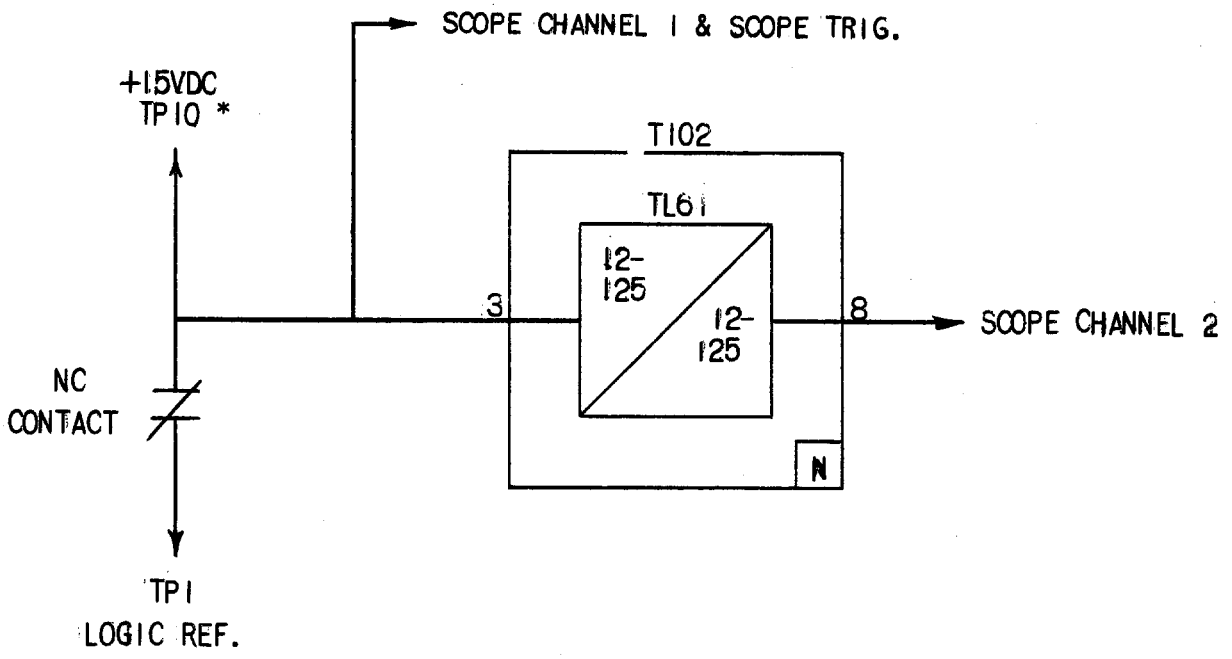


FIG. 5 (0227A2037-0) OUTLINE AND MOUNTING DIMENSIONS



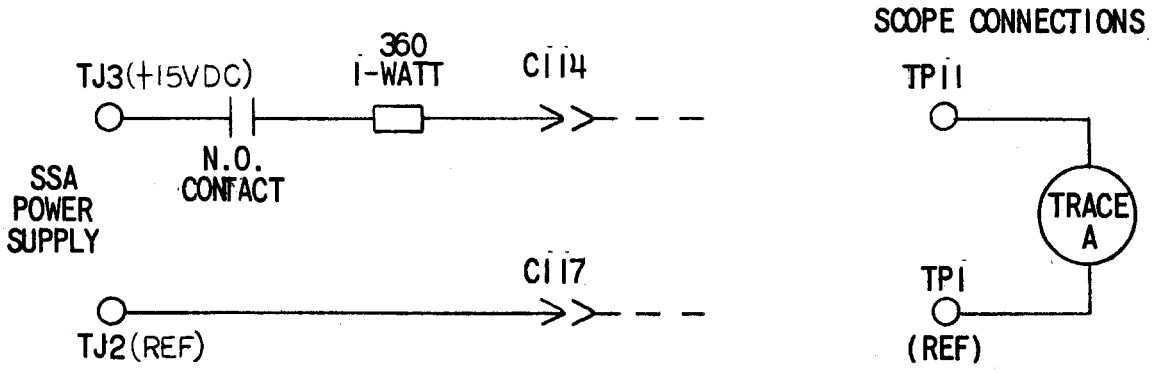
*-OPTION CARDS (SEE INTERNAL FOR CARD IDENTIFICATION 0136D1424)

FIG. 6 (0257A8701-0) COMPONENT LOCATION DIAGRAM

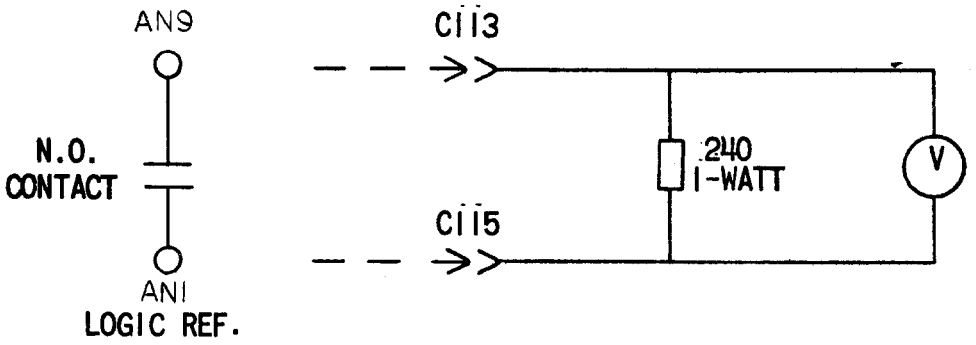


* THE 15VDC SIGNAL AT PIN 10 HAS A CURRENT LIMITING RESISTOR MOUNTED ON THE TEST CARD.

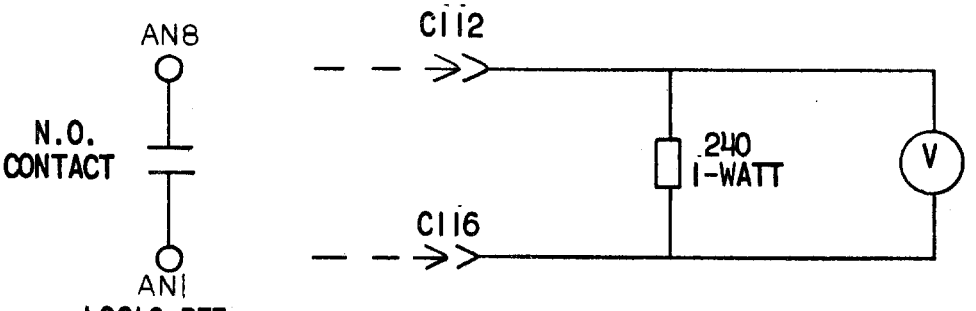
FIG. 7 (0246A7987-0) LOGIC TIMER TEST CIRCUIT



A-RECEIVED CARRIER TEST CONNECTIONS



B-TRANSMITTER CONTROL TEST CONNECTIONS



C-TRANSMITTER AUXILIARY STOP TEST CONNECTIONS

FIG. 8 (0257A8778-0) ISOLATION INTERFACE TEST CIRCUIT