INSTRUCTIONS

GEK-49775A
Supersedes GEK-49775A

STATIC AUXILIARY LOGIC RELAY

TYPE SLA51J

GENERAL ELECTRIC

CONTENTS

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DESCRIPTION

The SLA51J relay is an auxiliary logic relay designed to be used in phase comparison frequency shift carrier schemes. The relay contains the necessary logic to interpret output signals from associated measuring functions and translate them to an appropriate auxiliary output and tripping relay. In addition to the SLA51J relay, appropriate measuring relays plus a power supply and auxiliary tripping relay are required to complete a particular relaying scheme.

The type SLA51J relay is packaged in a four rack unit enclosed metal case. The relay is suitable for mounting in a 19 inch rack and the mounting and outline dimensions are shown in Figure 1. Internal connections for the SLA51J relay are shown in Figure 2, and the component and card locations are shown in Figure 3.

APPLICATION

The SLA51J relay is designed to operate in conjunction with appropriate SLD relays and a frequency shift channel in a phase comparison scheme. Circuits are also included for SLY first and second zone phase distance back-up protection.

Protection features required often vary from scheme to scheme and it is sometimes desirable to provide certain features initially with the scheme or to provide features so that they may be added at a later date in the field. To this end, the SLA51J design has incorporated circuit flexibility to permit implementation of certain optional features. Printed circuit card T119 shown dotted in Figure 2, is used with three terminal lines where a second receiver is used. Matrix block "B" with a number of points, is provided in SLA51J relays to permit various logic arrangements to be made simply by connecting jumper leads between appropriate points. For example, a jumper between B14 and B15, shown dotted in Figure 2, will allow the out-of-step detection option to block first zone tripping by applying the NOT input to AND 1. On the other hand, jumpering between B16 and B17 will block reclosing by applying the NOT input to the appropriate AND function in the associated SLAT tripping relay. These examples can best be understood by referring to the overall logic diagram and instruction books supplied with a particular relaying scheme. A logic option chart drawing is also supplied with each equipment to show the specific optional jumpers supplied initially.

Various points in the logic can be monitored by providing jumpers from any of the available matrix points to plugs located on the rear of the SLA51J relay. The plugs may be provided initially with the equipment or added at a later date. This option is further described in paragraph "C", DATA MONITORING POINTS, under the section headed OPERATING PRINCIPLES.

For the specific options and the logic arrangement supplied with a particular scheme, refer to the logic diagram and logic descriptive write-up supplied with that scheme. If it is desired to make logic changes at a later date, the diagrams and instruction books supplied with a particular scheme should be studied to determine the means for implementing the changes. If, after study of the diagrams, further assistance is required, contact the nearest General Electric District Sales Office.

There are no measuring functions to be set in the SLA51J relay, but there are included certain timers that must be set in accordance with the demands of the particular system to be protected. Refer to the section under SETTINGS for a description of these timers and for suggestions to be used in making the settings.

RATINGS

The Type SLA51J relay is designed for use in an environment where the air temperature outside the relay case does not exceed -20°C or +65°C.

The type SLA51J relay requires ±15 VDC power source which can be obtained from a Type SSA power supply.

The contact converter in this relay has a link for selecting the proper voltage for the coil circuit. The three possible voltages are 48 VDC, 125 VDC and 250 VDC.

BURDENS

The SLA51J relay presents a burden of 225 milliamperes to the +15 VDC supply of the Type SSA power supply.

Each contact converter, when energized, will draw approximately 10 milliamperes from the station battery, regardless of tap setting.

OPERATING PRINCIPLES

A. LOGIC CIRCUIT

The functions of the Type SLA51J relay involve basic logic (AND, OR, AND NOT) where the presence or absence of signals, rather than their magnitude, controls the operation. Signals are measured with respect to a reference bus accessible at TP1. In general, a signal below one VDC represents an OFF or LOGIC ZERO condition; an ON or LOGIC ONE condition is represented by a signal of approximately +15 VDC.

The symbols used on the internal connection diagram (Figure 2) are explained by the legend shown in Figure 4.

The matrix block options shown in the internal connections of the SLA51J relay are provided at the factory. The connections are shown on the associated overall logic and are listed on the associated option chart. A sample option chart for the Type SLA51J relay is shown in Figure 5.

B. CONTACT CONVERTER

The purpose of this function is to convert a contact operation into a signal that is compatible with the logic circuit of the Type SLA51J relay. This contact converter is labeled CC1. This contact converter has a non-adjustable four millisecond pickup delay, and is energized by an external contact to block operation comparer circuit.

C. DATA MONITORING POINTS

Optional data monitoring points can be brought out from the matrix block to plugs mounted in available knockouts at the rear of the SLA51J relay. Each plug contains nine monitoring points and reference. When ordered, the selected monitoring points on the matrix block are listed on the option chart which represents the factory wiring configuration for the relay options. Changes in selection of monitored points may be easily made, but this must be done inside the relay. If monitoring points are not ordered, they may be provided at a later date by adding the cable plug(s) and associated wiring as required. An additional data logging amplifier is required to monitor these points.

D. CHANNEL INTERFACE

The logic of the Type SLA51J relay includes an isolation interface (Figure 6) between the relays in the scheme and the associated channel. The circuitry of the isolation interface provides a signal path but maintains metallic isolation. This feature makes it possible to maintain isolation between the d-c supply used for the relays and that employed by the channel.

When a LOGIC ONE condition exists at pin one, a metallically separate positive logic signal appears at pin 3 with respect to 4. The output from the isolation interface is a 5 VDC, 20 milliamperes signal.

SETTINGS

The SLA51J contains six timers. One of the timers (TL3) is factory set and does not generally need field adjustment. Timer TL6 is also factory set, but it may require field adjustment.

Timer TL6 is part of the comparer-integrator scheme. The normal three millisecond pickup setting is intended to provide coordination between receiver input and the MT input to the comparer AND7. The pickup setting allows for the transmitter-receiver operating time plus the signal propagation time. A safety margin of at least one (1) millisecond should be added when setting the pickup of this timer. For longer transmitter-receiver operating times, such as with narrow band carrier, a longer pickup time should be considered. Long transmission lines (longer signal propagation time) may also require that the pickup setting be increased. It should be remembered that tripping will be delayed in accordance with the pickup setting

of this timer. The purpose of the reset delay of this timer is to hold the channel in the trip condition some time after tripping and so ensure that the remote relay will have ample time to operate.

The other four timers require field adjustment.

The B/16 timer in the SLY and timer TL4 in the SLA51J are part of the out-of-step detection scheme. The B/16 timer forms a "tomato" (outer) characteristic; thus the distance a swing must travel before the mho (inner) characteristic is encountered is determined by the pickup setting of this timer. Timer TL4 is used to measure the time of travel between the outer and inner characteristic. An out-of-step condition will be detected when both timers are adjusted properly. The setting of both timers should be based on the results of system swing studies.

Timer TL2 is the Zone 2 backup timer. The range of the pickup is 100 milliseconds to 2000 milliseconds. The timer setting must be such that coordination with the corresponding remote Zone 1 protection is obtained.

Timers TL5 and TL1 are the symmetry and phase-delay timers. The settings of both of these timers are affected by service conditions; therefore, these timers require field adjustment. The symmetry adjustment should be set first.

SYMMETRY ADJUSTMENT

Timer TL5 is included to compensate for any asymmetry that may exist in the pickup and drop-out of the channel equipment. The purpose of this setting is to assure that the near end comparer receives equal on-and-off half cycles when the transmitter at the remote end is keyed for equal on-and-off half cycles. See the section titled SYMMETRY AND PHASE-DELAY TIMER ADJUSTMENTS for instructions for making this setting in the field.

PHASE-DELAY ADJUSTMENT

Timer TL1 is intended to delay the local input to the comparer by the same amount of time that it takes for the remote signal to arrive. This time is equal to the channel delay in the communication equipment plus the propagation time of the signal. This setting should be made after the symmetry adjustment setting discussed above.

For instructions relating to the method of adjustment, see the TIMER ADJUSTMENT AND TESTS section of this book.

CONSTRUCTION

The SLA51J relay is packaged in an enclosed metal case with hinged front covers and removable top cover. The outline and mounting dimensions of the case and the physical location of the components are shown in Figures 1 and 3 respectively.

The SLA51J relay contains printed circuit cards identified by a code number such as A111, T102, L104 where A designates auxiliary function, T designates time-delay function, and L designates logic function. The printed circuit cards plug in from the front of the unit. The sockets are marked with letter designations or "addresses" (D, E, F, etc.) which appear on the guide strips in front of each socket, on the component location drawing, on the internal connection diagram and on the printed circuit card. The test points (TP1, TP2, etc.) shown on the internal connection diagram are connected to instrument jacks on a test card in position T or AT with TP1 at the top of the AT card. TP10 is tied to +15 VDC through a 1.5K resistor. This resistor limits the current when TP10 is used to supply a logic signal to a card.

Other logic options are selected by means of taper tip jumpers and matrix blocks. These matrix blocks are located in the rear of the unit as shown in Figure 3. The green (G) matrix block has ten points in two five-point common groups. The black (B) matrix block has 20 individual matrix points. The red (R) block has 20 points which are grouped in pairs. The yellow (Y) block has 20 points which are grouped in 10 common points; 1 to 10 are tied to +15 VDC, 11 to 20 are tied to reference. A tool for inserting and removing the taper tip jumpers is supplied with each relay.

RECEIVING, HANDLING AND STORAGE

These relays will normally be supplied as a part of a static relay equipment, mounted in a rack or cabinet with other static relays and test equipment. Immediately upon receipt of a static relay equipment, it should be unpacked and examined for any damage sustained in transit. If injury or damage resulting from rough handling is evident, file a damage claim at once with the transportation company and promptly notify the nearest General Electric Sales Office.

Reasonable care should be exercised in unpacking the equipment. If the equipment is not to be installed immediately, it should be stored indoors in a location that is free from moisture, dust, metallic chips, and severe atmospheric contaminants.

Just prior to final installation the shipping support bolt should be removed from each side of all relay units, to facilitate possible future unit removal for maintenance. These shipping support bolts are approximately eight inches back from the relay front panel. Static relay equipment, when supplied in swing rack cabinets, should be securely anchored to the floor or to the shipping pallet to prevent the equipment tipping over when the swing rack is opened.

TEST INSTRUCTIONS

CAUTION:

THE LOGIC SYSTEM SIDE OF THE DC POWER SUPPLY USED WITH MOD III STATIC RELAY EQUIPMENT IS ISOLATED FROM GROUND. IT IS A DESIGN CHARACTERISTIC OF MOST ELECTRONIC INSTRUMENTS THAT ONE OF THE SIGNAL INPUT TERMINALS IS CONNECTED TO THE INSTRUMENT CHASSIS. IF THE INSTRUMENT USED TO TEST THE RELAY EQUIPMENT IS ISOLATED FROM GROUND, ITS CHASSIS MAY HAVE AN ELECTRICAL POTENTIAL WITH RESPECT TO GROUND. THE USE OF A TEST INSTRUMENT WITH A GROUNDED CHASSIS WILL NOT AFFECT THE TESTING OF THE EQUIPMENT. HOWEVER, A SECOND GROUND CONNECTION TO THE EQUIPMENT, SUCH AS A TEST LEAD INADVERTENTLY DROPPING AGAINST THE RELAY CASE, MAY CAUSE DAMAGE TO THE LOGIC CIRCUITRY. NO EXTERNAL TEST EQUIPMENT SHOULD BE LEFT CONNECTED TO THE STATIC RELAYS WHEN THEY ARE IN PROTECTIVE SERVICE, SINCE TEST EQUIPMENT GROUNDING REDUCES THE EFFECTIVENESS OF THE ISOLATION PROVIDED.

A. GENERAL

If the SLA51J relay that is to be tested is installed in an equipment which has already been connected to the power system, disconnect the outputs in the associated Type SLAT relay from the system.

The SLA51J relay is supplied from the factory either mounted in a static relay equipment or as a separate unit associated with measuring relays, a Type SSA power supply, and some form of channel equipment. All relay units for a given terminal of static relaying equipment are tested together at the factory, and each unit will have the same summary number stamped on its nameplate.

In general, when a time range is indicated on the internal connection diagram, the timer has been factory set at a mid-range value. Timers should be set for the operating or reset times indicated on the associated overall logic diagram. Where a time range is indicated on the overall logic diagram, the timer should be set for the value recommended for that function in the descriptive write-up accompanying the overall logic diagram. Where a setting depends upon conditions encountered on a specific application, this is so stated and the factors influencing the choice of setting are described. The procedure for checking and setting the timers is described in a later section.

B. OPERATIONAL CHECKS

Operation of the SLA51J unit can be checked by observing the signals at the twenty test points (TP1 to TP20) in the SLA51J, by observing the operation of the associated channel equipment, or by observing the output functions in the associated Type SLAT tripping relay. The test points are located on two test cards in positions T and AT, and are numbered 1 to 20 from top to bottom. TP1 is the reference bus for the logic circuit; TP10 is at +15 VDC. The remaining points are located at various strategic points throughout the logic as shown on the internal connection diagram (Figure 2). Test point voltages can be monitored with a portable high impedance voltmeter, the voltmeter on the test panel of the associated equipment, or an oscilloscope.

C. TEST CARD ADAPTER

The test card adapter provides a convenient means of gaining access to any pin of a particular card. Detailed information on the use of the test adapter card is included in the card instruction book GEK-34158.

D. TIMER ADJUSTMENTS AND TESTS

When the time-delay cards are to be adjusted or checked, an oscilloscope that can display two traces simultaneously and that has a calibrated horizontal sweep should be used.

In order to test the time cards it is necessary to remove the card previous to the timer (see Table I) and to place the timer card in a card adapter. The card adapter allows access to the input and output of the timer if they are not brought out on test points. The timer test circuit is shown in Figure 7. Opening the normally closed contact causes the output to step up to +15 VDC after the pickup delay of the timer. To increase the pickup time turn the upper potentiometer on the timer card clockwise; to decrease the time turn

it counter-clockwise. Closing the contact causes the timer output to drop out after the reset time-delay setting of card. If the timer card is provided with a variable reset delay, it can be adjusted by the lower potentiometer on the timer card (clockwise increases reset time).

TABLE I

TIME UNDER TEST	POSITION	REMOVE CARD IN POSITION
TL2 0.1-2/0	M	H
TL4 32-64/40	K	J
TL3 35/40	AL	AJ
TL6 3/35	AK	AJ

E. SYMMETRY AND PHASE-DELAY TIMER ADJUSTMENTS

The symmetry timer (TL5, "AR" position) and phase-delay timer (TL1, "AH" position) final settings must be made in the field after the transmitters, receivers and coupling equipment have been tuned and adjusted for proper sensitivity per the channel instructions. Operation of the squaring amplifier and fault detectors, FDL and IM, are required for accomplishment of the final symmetry and phase-delay adjustments; refer to the measuring unit instruction book for the recommended procedure.

The symmetry adjustment must be accomplished prior to phase-delay adjustments as described in the measuring unit instructions. The transient blocking timer (TL3, "AL" position) should be removed to prevent continuous channel keying when the logic trip bus is energized. Clockwise adjustment of P1 and P2 on TL5, "AR" position card, increases the pickup delay or drop-out delay respectively. Conversely, counterclockwise adjustment reduces the respective operate times. The minimum delay on pickup which allows equal half cycle block and trip output as measured at TP4 is the recommended final setting.

After the symmetry adjustment has been accomplished, the phase-delay adjustment is made to obtain the proper alignment of the local signal with the received signal; refer to the measuring unit instructions. Clockwise adjustment of P1 or P2 on TL1, "AH" position card, increases the pickup or drop-out delay respectively. The final setting is the alignment of the trip attempt signal monitored at TP8 compared to the trip or block signal monitored at TP12 which is dependent upon internal or external fault simulation during the adjustment.

F. CONTACT CONVERTER TESTS

Operation of the contact converter can be checked by placing the contact converter card in a card adapter, after checking the voltage tap selected agrees with the station battery voltage. Connect the station direct current through a switch to the appropriate pair of terminals of the terminal strip, AH, mounted on the rear of the relay. The terminal numbers and polarity of connections of the contact converter is shown in the internal connection diagram, Figure 2. Output of the contact converter card may be monitored between Pin 8 and Pin 1 (reference) on the card adapter with either a scope or meter. Closure of the switch in the test source will provide a +15 volt d-c signal at Pin 8 of the card adapter.

G. ISOLATION INTERFACE TESTS

Operation of the three functions (Receive #1, Receive #2 and Transmitter) of the isolation interface can be checked without direct connections to the subassembly. External test connections are made to the pins of the C111 socket mounted on the rear of the unit, see Figure 3. Logic circuit test connections are made at test points through test card positions "T" and "AT".

Receive #1 operation test connections are shown in Figure 8A. Closure of the normally open contact will simulate a trip signal being received by receiver #1 and scope display will go from a logic "0" to a logic "1". Receive #2 is tested in a similar manner using the connections shown in Figure 8B.

For the Transmitter test, remove card in position "AG" and make the connections shown in Figure 8C. The test contact in the open position simulates a logic "1" condition which causes a transmitter keying output to be produced, a 5-6 volt d-c signal across the output loading resistor. Closure of the normally open contact simulates a logic "0" condition which produces no transmitter keying output.

H. OVERALL EQUIPMENT TESTS

After the SLA51J relay and the associated static relay units have been individually calibrated and tested for the desired settings, a series of overall operating circuit checks is advisable.

The elementary, overall logic, and logic description for the specific job will be useful for determining the overall operation of the scheme.

Overall equipment tests can be performed by applying alternating current and voltages to the measuring units as specified in the instruction book for the measuring units and checking that proper outputs are obtained from the associated SLAT when the measuring units operate.

MAINTENANCE

A. PERIODIC TESTS

It should be sufficient to check the outputs produced at test points in the SLA51J when periodic calibration tests are made on the associated measuring units, for example, the phase and ground relays in line relaying scheme. No separate periodic tests on the SLA51J itself should be required.

B. TROUBLESHOOTING

In any troubleshooting of equipment, it should first be established which unit is functioning incorrectly. The overall logic diagram supplied with the equipment shows the combined logic of the complete equipment and the various test points in each unit. By signal tracing, using the overall logic diagram and the various test points, it should be possible to quickly isolate the trouble.

A test adapter card is supplied with each static relay equipment to supplement the prewired test points on the test cards. Use of the adapter card is described in the card instruction book GEK-34158.

A dual-trace oscilloscope is a valuable aid to detailed troubleshooting, since it can be used to determine phase shift, operate and reset times as well as input and output levels. A portable dual-trace oscilloscope with a calibrated sweep and trigger facility is recommended.

C. SPARE PARTS

To minimize possible outage time, it is recommended that a complete maintenance program should include the stocking of at least one spare card of each type. It is possible to replace damaged or defective components on the printed circuit cards, but great care should be taken in soldering so as not to damage or bridge-over the printed circuit buses, or overheat the semi-conductor components. The repaired area should be recovered with a suitable high-dielectric plastic coating to prevent possible breakdowns across the printed buses due to moisture and dust. The wiring diagrams for the cards in the SLA51J relay are included in the card book GEK-34158.

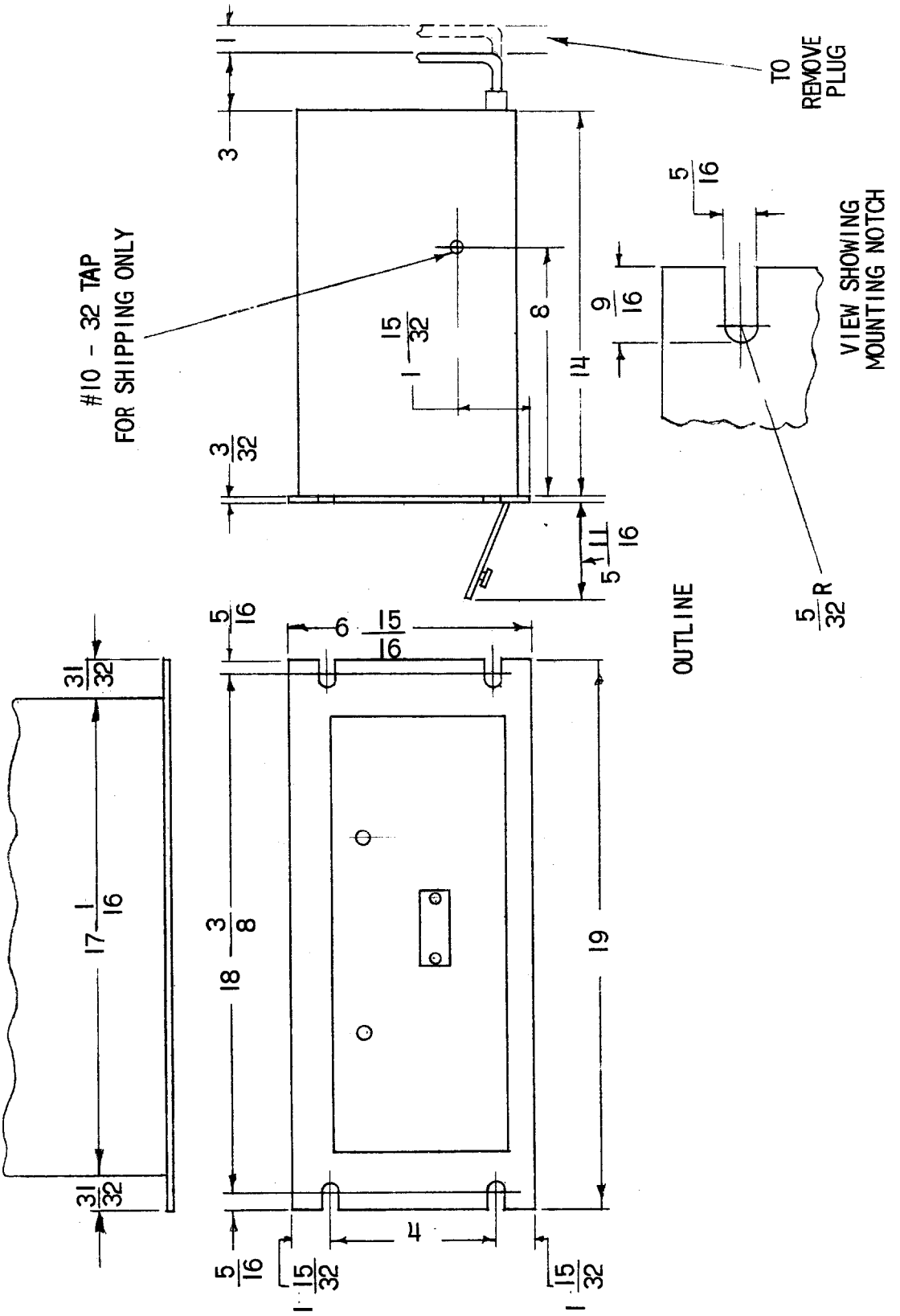


Fig. 1 (0227A2037-1) OUTLINE AND MOUNTING DIMENSIONS FOR THE TYPE SLA51J RELAY

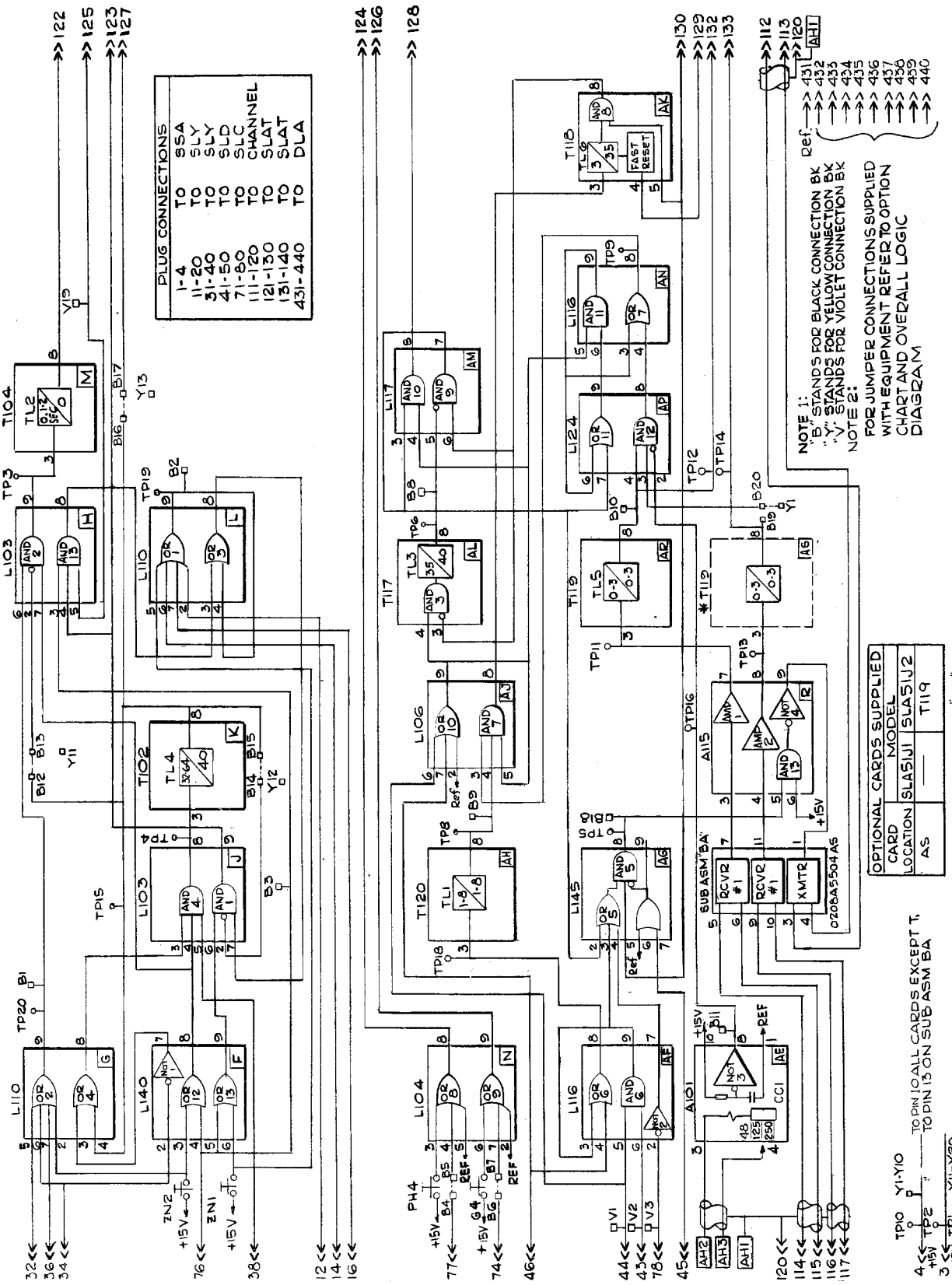


Fig. 2 (0171C7872-6) INTERNAL CONNECTIONS FOR THE TYPE SLA51J RELAY

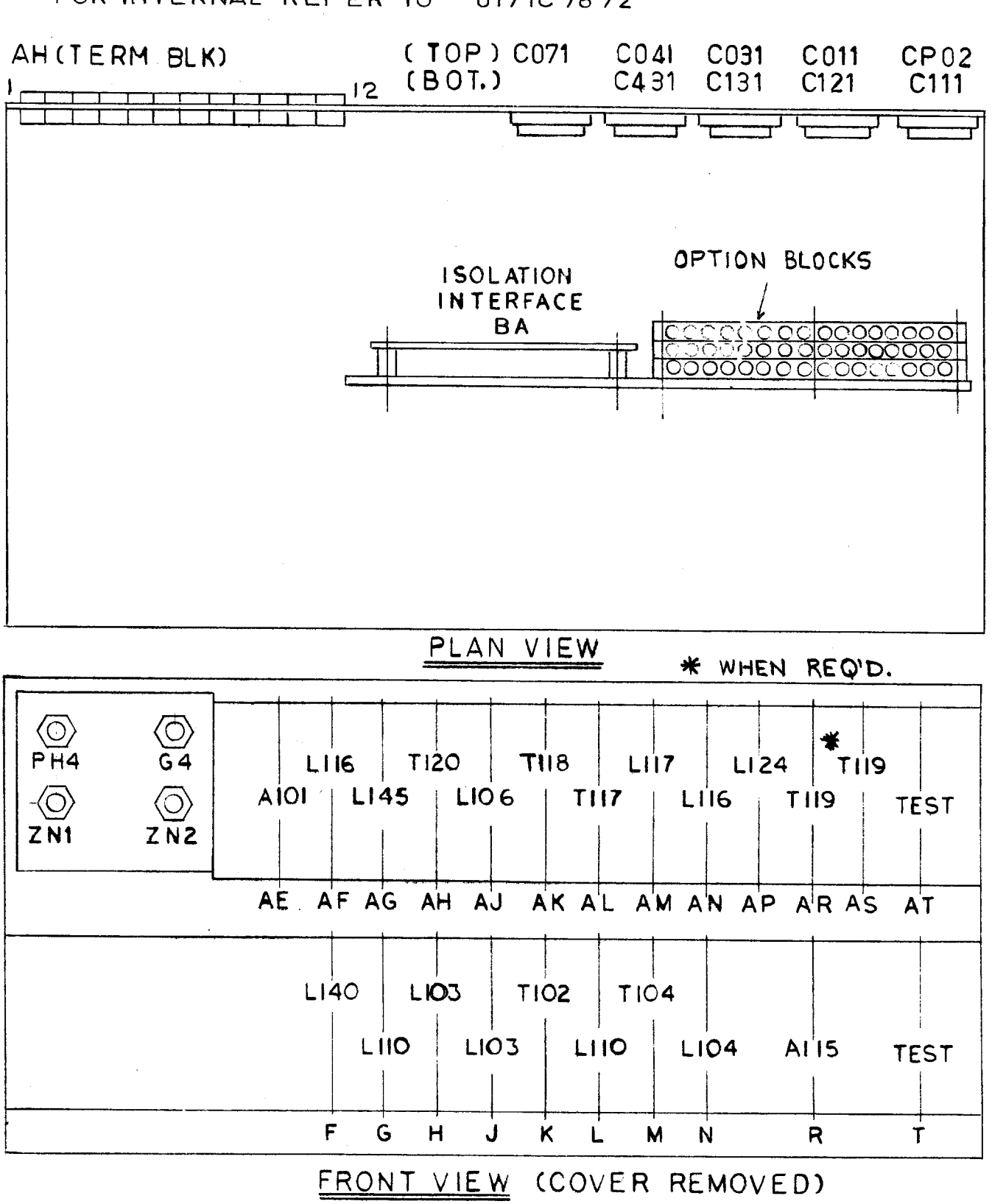


Fig. 3 (0269A3101-1) COMPONENT LOCATIONS FOR THE TYPE SLA51J RELAY

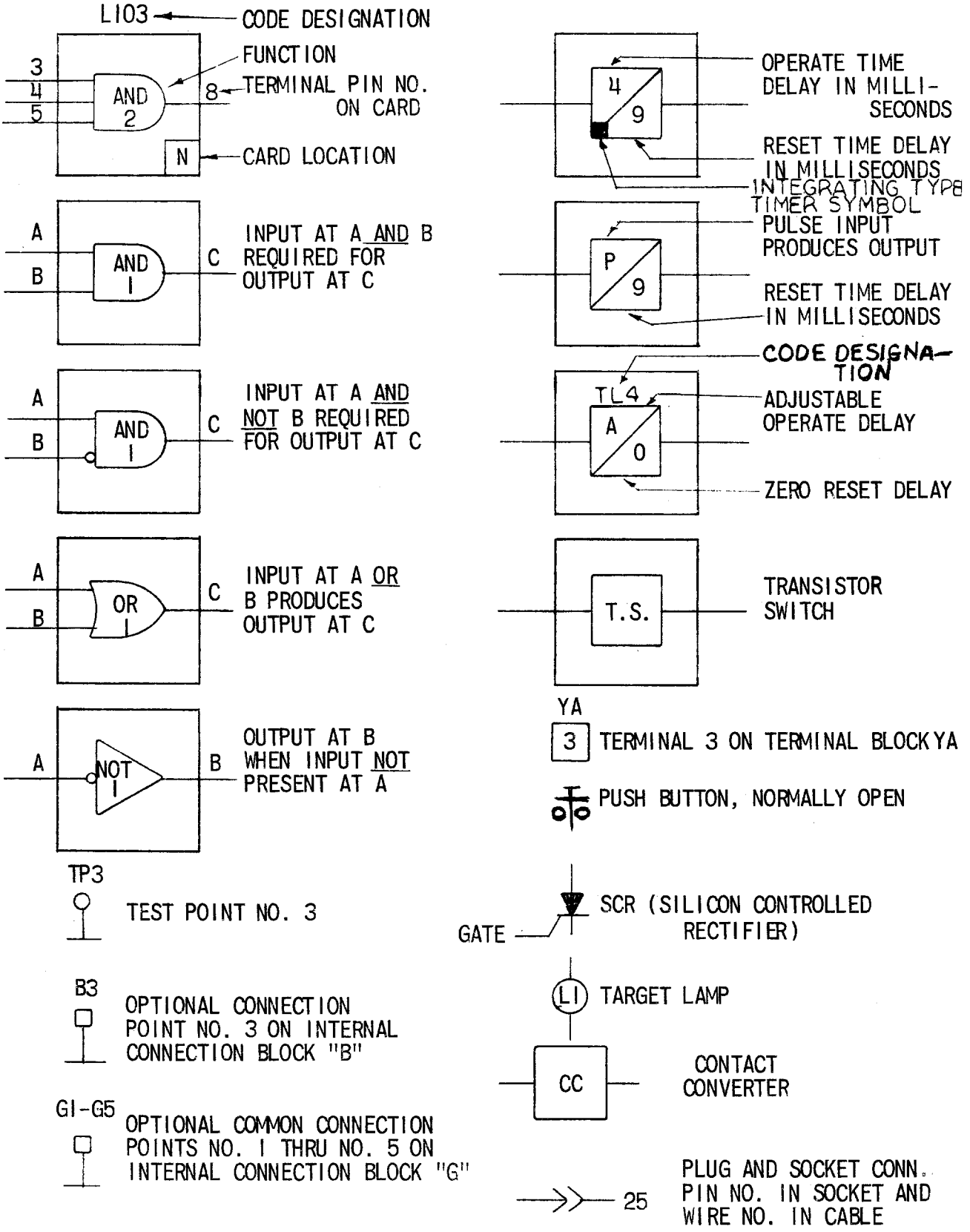


Fig. 4 (0227A2047-2) LOGIC AND INTERNAL CONNECTION DIAGRAM LEGEND

THE FOLLOWING ARE FACTORY CONNECTIONS MADE AT THE MATRIX BLOCKS INSIDE OF THE SLA RELAY ASSOCIATED WITH THIS EQUIPMENT.

SYMBOLS LISTED: PL=RELAY INTERCONNECTING CABLE LEAD
(5)=LOGIC FUNCTION CARD PIN NUMBER
‡ =3-WAY CONNECTION
✳ = DLA MONITOR CONNECTION AVAILABLE BUT NOT USED

(113)

MATRIX BLOCK JUMPERS		LOGIC FUNCTION		MATRIX BLOCK JUMPERS		LOGIC FUNCTION	
FROM	TO	FROM	TO	FROM	TO	FROM	TO
B1	PL433	OR2	DLA				
B2	PL432	OR1	DLA				
B3	PL434	PL76	DLA				
B4	B5	PL77	OR8				
B6	B7	PL74	OR9				
B8	PL435	TL3	DLA				
B9	PL437	TL1	DLA				
B10	PL438	TL5	DLA				
B11	PL439	CC1	DLA				
B12	B13	TL4	AND2				
B14	B15	TL4	AND1				
B16	B17	TL4	AND32				
B18	PL436	AND5	DLA				
B20	Y1	AND12	REF				

Fig. 5 (0227A2050-2 Sh. 113) SAMPLE OPTION CHART FOR THE TYPE SLA51J RELAY

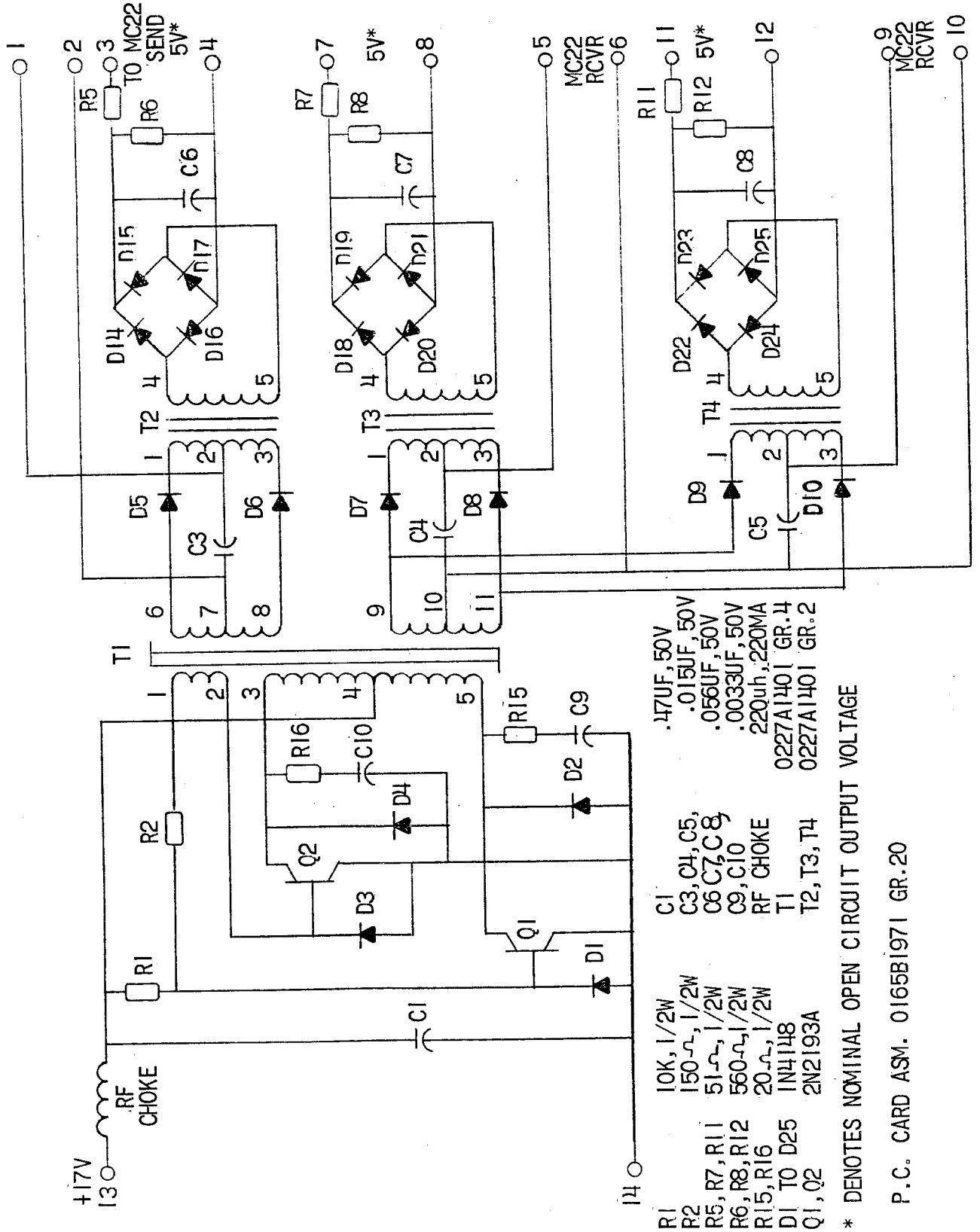
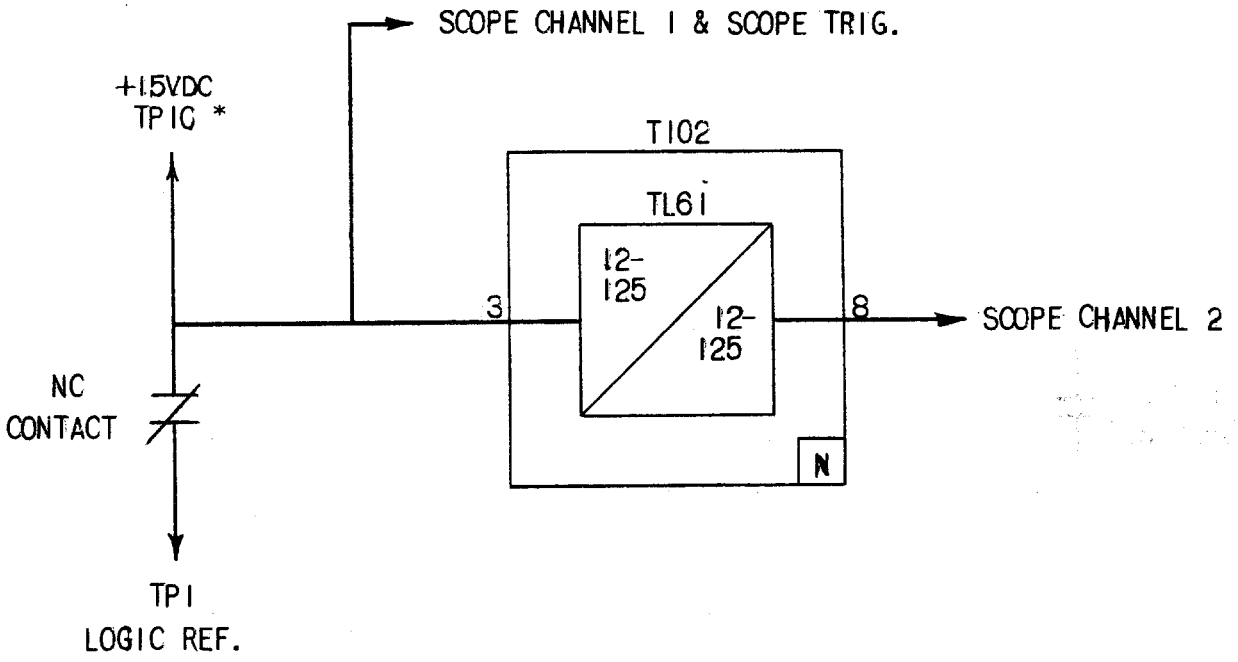
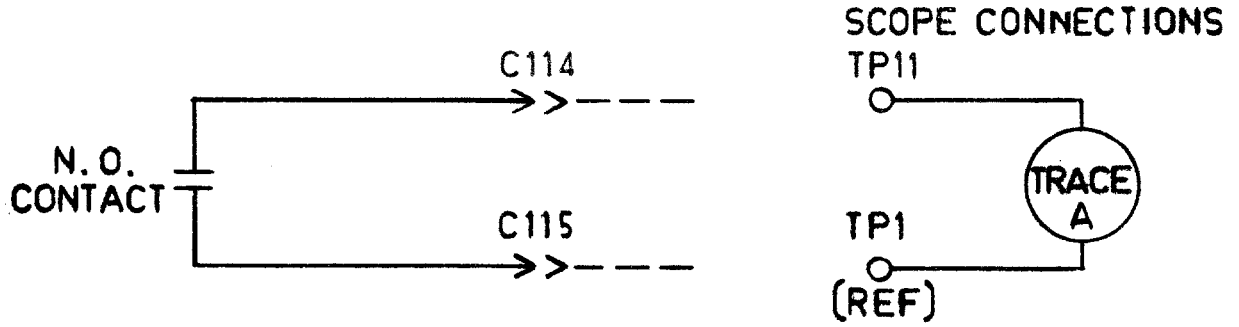


Fig. 6 (0208A5504AS-1) ISOLATION INTERFACE CIRCUIT

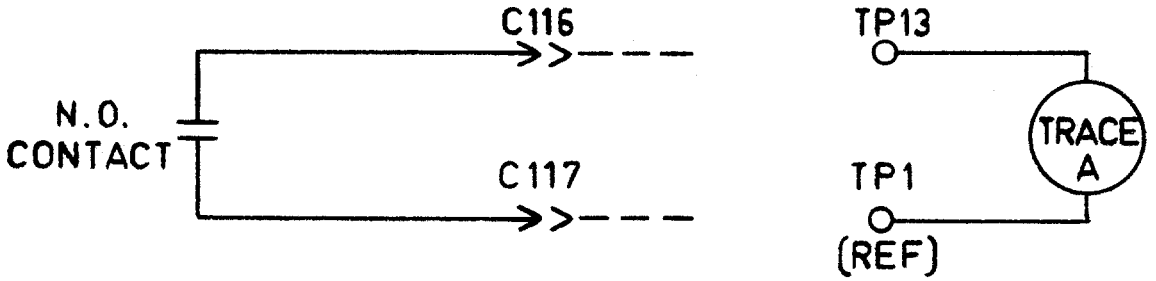


* THE 15VDC SIGNAL AT PIN 10 HAS A CURRENT LIMITING RESISTOR MOUNTED ON THE TEST CARD.

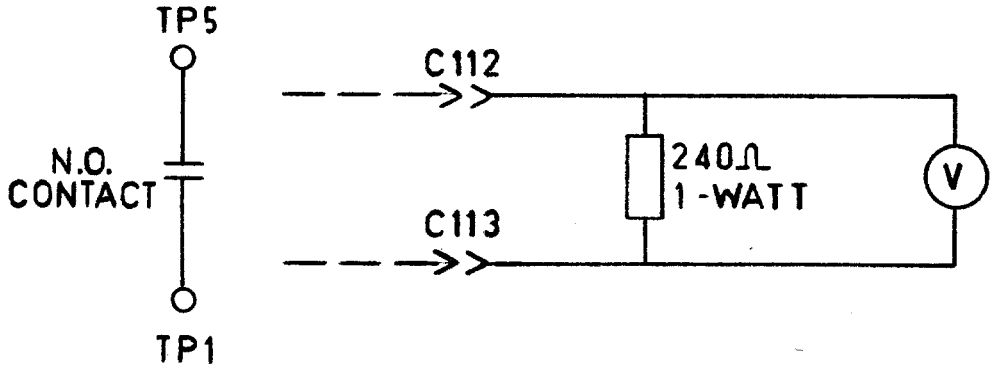
Fig. 7 (0246A7987-0) LOGIC TIMER TEST CIRCUIT



A-RECEIVE # 1 TEST CONNECTIONS



B-RECEIVE # 2 TEST CONNECTIONS



C-TRANSMITTER TEST CONNECTIONS

Fig. 8 (0257A8786-0) ISOLATION INTERFACE TEST CIRCUIT