INSTRUCTIONS

GEK-49788

AUXILIARY LOGIC RELAY

TYPE SLA51K

POWER SYSTEMS MANAGEMENT DEPARTMENT

GENERAL ELECTRIC

PHILADELPHIA PA

CONTENTS

AUXILIARY LOGIC RELAY

TYPE SLA51K

DESCRIPTION

The SLA51K relay is an auxiliary logic relay designed to be used in a directional comparison ON-OFF carrier scheme. The relay contains the necessary logic to interpret output signals from associated measuring functions and translate them to an appropriate auxiliary output and tripping relay. In addition to the SLA51K relay, appropriate ground and phase relays plus a power supply and auxiliary tripping relay are required to complete a particular relaying scheme.

The Type SLA51K relay is packaged in a four rack unit enclosed metal case. The relay is suitable for mounting in a 19 inch rack and the mounting and outline dimensions are shown in Fig. 3. Internal connections for the SLA51K relay are shown in Fig. 1, and the component card locations are shown in Fig. 2.

APPLICATION

The SLA51K relay is designed to operate in conjunction with appropriate phase and ground relays in a directional comparison ON-OFF blocking scheme, using either Type CS26B power line carrier or Type 30 audio tones as the pilot channel. Isolation interfacing provides the interconnection between the SLA logic and the transmitter and receiver of the pilot channel. The interface circuits and SLA logic is so arranged that the relay can be used if desired in an arrangement where the comparer receives a blocking signal from its own receiver and also from the receiver in another relay equipment protecting the same transmission line. The operation of such a "cross blocking " scheme can best be understood by referring to the overall logic diagram and associated logic description for a specific application.

Protection features required in a relaying scheme often vary from scheme to scheme and it is sometimes desirable to provide certain features initially with the scheme or to provide features so that they may be added at a later date in the field. To this end, the SLA51K design has incorporated circuit flexibility to permit implementation of certain optional features. Printed circuit cards L108 and T102, shown dotted in Fig. 1, are used whenever out-of-step detection is required. Matrix blocks "R", "Y", "G" and "B", each with a number of points, are provided in all SLA51K relays to permit various logic arrangements to be made simply by connecting jumper leads between appropriate points. For example, a jumper between G6 and B5, shown dotted in Fig. 11, will allow the out-of-step detection option to block all pilot tripping by applying the NOT input to the appropriate AND function in the associated SLAT tripping relay. These examples can best be understood by referring to the overall logic diagram and instruction books supplied with a particular relaying scheme.

Printed circuit cards T104 in positions G and J, and L104 in position AS, shown dotted in Fig. 1, can be added if it is desired to initiate time-delay back-up from the MT and MTG functions.

Various points in the logic can be monitored by providing jumpers from any of the available matrix points to plugs located on the rear of the SLA51K relay. The plugs may be provided initially with the equipment or added at a later date. This option is further described in paragraph "C" of this book, DATA MONITORING POINTS, under the section headed OPERATING PRINCIPLES.

For the specific options and the logic arrangement supplied with a particular scheme, refer to the logic diagram and logic descriptive write-up supplied with that scheme. If it is desired to make logic changes at a later date, the diagrams and instruction books supplied with a particular scheme should be studied to determine the means for implementing the changes. If, after study of the diagrams, further assistance is required, contact the nearest General Electric District Sales Office.

There are no measuring functions to be set in the SLA51K relay, but there are included certain timers that must be set in accordance with the demands of the particular system to be protected. Refer to the section under SETTINGS for a description of these timers and for suggestions to be used in making the settings.

RATINGS AND SPECIFICATIONS

The Type SLA51K relay is designed for use in an environment where the air temperature outside the relay case does not exceed -20°C or +65°C.

The Type SLA51K relay requires ±15 VDC power source which can be obtained from a Type SSA power supply.

Each contact converter in this relay has a link for selecting the proper voltage for the coil circuit of the contact converter. The three possible voltages are 48, 125 and 250 VDC.

The SLA51K relay contains:

Two isolation interface boards for cross blocking application, (CS26B blocked by type 30 tone, or by CS26B. Also, type 30 tone blocked by CS26B carrier and three terminal applications.

Four contact converters

Zone 2 Phase
Zone 2 Ground } Optional.

BURDENS

The SLA51K relay presents a burden of 420 milliamperes to the +15 VDC supply of the Type SSA power supply.

Each contact converter, when energized, will draw approximately 10 milliamperes from the station battery, regardless of tap setting.

OPERATING PRINCIPLES

A. LOGIC CIRCUIT

The functions of the Type SLA51K relay involve basic logic (AND, OR, and NOT) where the presence or absence of signals, rather than their magnitude, controls the operation. Signals are measured with respect to a reference bus accessible at TP1. In general, a signal below one VDC represents an OFF or LOGIC ZERO condition; an ON or LOGIC ONE condition is represented by a signal of approximately 10 to 15 VDC.

The symbols used on the internal connection diagram (Fig. 1) are explained by the legend shown in Fig. 4.

The matrix block options shown in the internal connections of the SLA51K relay are provided at the factory. The connections are shown on the associated overall logic and are listed on the associated option chart. A sample option chart for the Type SLA51K relay is shown in Fig. 5. It should be noted that the relay may require a different option chart for other applications.

B. CONTACT CONVERTERS

The purpose of this function is to convert a contact operation into a signal that is compatible with the logic circuit of the Type SLA51K relay. These contact converters, which are labeled CC1, CC2, CC3, and CC4, have a non-adjustable four-millisecond pickup delay.

CC1

Contact converter 1 is energized by an external contact to stop all carrier transmission.

CC2

Contact converter 2, when energized, prevents relay carrier tripping and relay control of carrier but permits auxiliary control of carrier.

CC3

Contact converter 3 is connected to option point W10. It is typically involved in applications with frequency shift tone channels where it is desired to shift the tone transmitter from the trip to the block frequency by means of an external contact.

CC4

Contact converter 4 is connected to option point W9. It is typically used in the so-called "cross-blocking" scheme to prevent failure of one channel from blocking the comparers in both relay equipments. This function of CC4 is best understood by referring to the overall logic of a specific scheme.

C. DATA MONITORING POINTS

Optional data monitoring points can be brought out from the matrix blocks to plugs mounted in available knockouts at the rear of the SLA51K relay. Each plug contains nine monitoring points and reference. When ordered, the selected monitoring points on the matrix block are listed on the option chart which represents the factory wiring configuration for the relay options. Changes in selection of monitored points may be easily made, but this must be done inside the relay. If monitoring points are not ordered, they may be provided at a later date by adding the cable plug(s) and associated wiring as required.

To monitor these points an additional piece of equipment termed a Data Logging Amplifier (DLA) is required.

D. CHANNEL INTERFACE

The logic of the Type SLA51K relay includes an isolation interface (Fig. 6) between the relays in the scheme and the associated channel. The circuitry of the isolation interface provides a signal path but maintains metallic isolation. This feature makes it possible to maintain isolation between the d-c supply used for the relays and that employed by the channel.

Two isolation interface board assemblies are included in the SLA51K relay, as shown in Fig. 1. Some inputs and outputs of both isolation interface boards are connected to option points to accommodate use of this relay in several relaying schemes. (See APPLICATION section.) All outputs from the isolation interface circuits are 5 volt, direct current, 20 milliamperes maximum.

SETTINGS

There are six timers in the SLA51K relay that may require field adjustment.

The 3/50 timer is part of the comparer-integrator scheme. The normal three millisecond pickup setting is intended to provide coordination between receiver input and the MT input to the comparer AND7. The pickup setting allows for the transmitter-receiver operating time plus the signal propagation time. A safety margin of at least one millisecond should be added when setting the pickup of this timer. For longer transmitter-receiver operating times, such as with a narrow band carrier, a longer pickup time should be considered. Long transmission lines (longer signal propagation time) may also require that the pickup setting be increased. It should be remembered that tripping will be delayed in accordance with the pickup setting of this timer. The purpose of the reset delay of this timer is to hold off the carrier for some time after tripping and so ensure that the remote relay will have ample time to operate.

The 2.5/16 timer in the SLY and A/40 timer in the SLA51K are part of the out-of-step detection scheme. The 2.5/16 timer forms a "tomato" (outer) characteristic; thus the distance a swing must travel before the mho (inner) characteristic is encountered is determined by the pickup setting of this timer. The A/40 timer is used to measure the time of travel between the outer and inner characteristic. An out-of-step condition will be detected when both timers are adjusted properly. The setting of both timers should be based on the results of system swing studies.

The (2-16)/0 timers in printed circuit card positions "F" and "AE" are coordinating timers necessary for the correct operation of the blocking scheme in certain applications. The timer in printed circuit card position "F" is normally set for four milliseconds to insure coordination between the carrier stop (MT) function at one end and the carrier start (MB) function at the other end of the protected line. When the SLA51K is applied in a so-called "cross-blocking " scheme where the SLA is used with a carrier channel but is also blocked by a tone receiver in another equipment, then the timer in position "F" should be set for four milliseconds plus the difference between the carrier and tone channel times.

The timer in printed circuit card position "AE" is required only in "cross-blocking" applications where the SLA51K is associated with a carrier channel but is also blocked by a tone receiver, in another equipment on the same transmission line. Its operating time in such applications should be set for the difference between the carrier and tone channel times. The TU2Ø and TU2G are zone 2 back-up timers for phase and ground faults respectively. The range of the pickup is 100 milliseconds to 2000 milliseconds. The timer setting must be such that coordination with the corresponding phase or ground remote zone 1 protection is obtained.

Further details for setting these timers can be found in the logic description provided with each static relaying scheme.

CONSTRUCTION

The SLA51K relay is packaged in an enclosed metal case with hinged front covers and removable top cover. The outline and mounting dimensions of the case and the physical location of the components are shown in Figs. 3 and 2 respectively.

The SLA51K relay contains printed circuit cards identified by a code number such as A117, T104, L104 where A designates auxiliary function, T designates time-delay function, and L designates logic function. The printed circuit cards plug in from the front of the unit. The sockets are marked with letter designations or "addresses" (D, E, F, etc.) which appear on the guide strips in front of each socket, on the component location drawing, on the internal connection diagram and on the printed circuit card. The test points (TP1, TP2, etc.) shown on the internal connection diagram are connected to instrument jacks on a test card in position T and AT with TP1 at the top of the AT card. TP10 is tied to +15 VDC through a 1.5K resistor. This resistor limits the current when TP10 is used to supply a logic signal to a card.

Other logic options are selected by means of taper tip jumpers and matrix blocks. These matrix blocks are located in the rear of the unit as shown in Fig. 2. The green (G) matrix block has ten points in two five-point common groups. The black (B) matrix block has 20 individual matrix points. The red (R) block has 20 points which are grouped in pairs. The yellow (Y) block has 20 points which are grouped in 10 common points; 1 to 10 are tied to +15 VDC, 11 to 20 are tied to reference. The white (W) matrix block has twenty individual matrix points. A tool for inserting and removing the taper tip jumpers is supplied with each relay.

RECEIVING, HANDLING AND STORAGE

The SLA51K relay will normally be supplied as a part of a static relay equipment, mounted in a rack or cabinet with other static relays and test equipment. Immediately upon receipt the static relay equipment should be unpacked and examined for any damage sustained in transit. If injury or damage resulting from rough handling is evident, file a damage claim at once with the transportation company and promptly notify the nearest General Electric Sales Office.

Reasonable care should be exercised in unpacking the equipment. If the equipment is not to be installed immediately, it should be stored indoors in a location that is free from moisture, dust, metallic chips, and severe atmospheric contaminants.

Just prior to final installation the shipping support bolt should be removed from each side of all relay units, to facilitate possible future unit removal for maintenance. These shipping support bolts are approximately eight inches back from the relay front panel.

CAUTION

STATIC RELAY EQUIPMENT, WHEN SUPPLIED IN SWING RACK CABINETS, SHOULD BE SECURELY ANCHORED TO THE FLOOR OR TO THE SHIPPING PALLET TO PREVENT THE EQUIPMENT FROM TIPPING OVER WHEN THE SWING RACK IS OPENED.

TEST INSTRUCTIONS

CAUTION

IF THE SLA51K RELAY THAT IS TO BE TESTED IS INSTALLED IN AN EQUIPMENT WHICH HAS ALREADY BEEN CONNECTED TO THE POWER SYSTEM, DISCONNECT THE OUTPUTS IN THE ASSOCIATED TYPE SLAT RELAY FROM THE SYSTEM.

A. GENERAL

The SLA51K relay is supplied from the factory either mounted in a static relay equipment or as a separate unit associated with measuring relays, a Type SSA power supply, and some form of channel equipment. All relay units for a given terminal of static relaying equipment are tested together at the factory, and each unit will have the same summary number stamped on its nameplate.

In general, when a time range is indicated on the internal connection diagram, the timer has been factory set at a mid-range value. Timers should be set for the operating or reset times indicated on the associated overall logic diagram. Where a time range is indicated on the overall logic diagram, the timer should be set for the value recommended for that function in the descriptive write-up accompanying the

overall logic diagram. Where a setting depends upon conditions encountered on a specific application, that is so stated and the factors influencing the choice of setting are described. The procedure for checking and setting the timers is described in a later section.

CAUTION

THE SLA51K RELAY UTILIZES SINKING LOGIC (SEE PRINTED CIRCUIT CARD INSTRUCTION BOOK GEK-34158). EXTREME CAUTION MUST BE EXERCISED WHEN CONNECTING ANY POINT IN THE LOGIC TO REFERENCE OR TO +15 VDC. FOR EXAMPLE, IF TP5 IS ACCIDENTALLY CONNECTED TO TP2 (-15 VDC) INSTEAD OF TP1 (REF.), THE OUTPUT STAGE OF THE CARD IN POSITION "C" AND THE INPUT STAGE OF THE CARD IN POSITION "E" WILL BURN OUT INSTANTLY. SIMILARLY, IF +15 VDC IS APPLIED TO TP5 WITHOUT A SERIES LIMITING RESISTOR (AS IS SUPPLIED WITH TP10) THE OUTPUT STAGE OF THE PRINTED CARD IN POSITION "C" WILL BURN OUT INSTANTLY.

B. OPERATIONAL CHECKS

Operation of the SLA51K unit can be checked by observing the signals at the twenty test points (TP1 to TP20) in the SLA51K or by observing the output functions in the associated Type SLAT tripping relay. The test points are located on two test cards in positions T and AT, and are numbered 1 to 20 from top to bottom. TP1 is the reference bus for the logic circuit; TP10 is at +15 VDC, and TP2 is at -15 VDC. The remaining points are located at various strategic points throughout the logic as shown on the internal connection diagram (Fig. 1). Test point voltages can be monitored with a portable high impedance voltmeter, the voltmeter on the test panel of the associated equipment, or an oscilloscope. Where a wave form other than direct current (step function) is expected, an oscilloscope should be used exclusively.

C. TEST CARD ADAPTER

The test card adapter provides a convenient means of gaining access to any pin of a particular card. Detailed information on the use of the test adapter card is included in the card instruction book GEK-34158.

D. TIMER ADJUSTMENTS AND TESTS

When the time-delay cards are to be adjusted or checked, an oscilloscope that can display two traces simultaneously and that has a calibrated horizontal sweep should be used.

In order to test the time cards it is necessary to remove the card previous to the timer (see Table I) and to place the timer card in a card adapter. The card adapter allows access to the input and output of the timer if they are not brought out on test points. The timer test circuit is shown on Fig. 8. Opening the normally closed contact causes the output to step up to +15 VDC after the pickup delay of the timer. To increase the pickup time turn the upper potentiometer on the timer card clockwise; to decrease the time turn it counterclockwise. Closing the contact causes the timer output to drop out after the reset time-delay setting of card. If the timer card is provided with a variable reset delay, it can be adjusted by the lower potentiometer on the timer card (clockwise increases reset time).

TABLE I

TIME UNDER TEST	POSITION	REMOVE CARD IN POSITION
T118 (3/50)	S	R
T103 (2-16/0)	F	D
T117 (25/35)	M	L
T104 (0.1/2 SEC.)	G	K
T104 (0.1/2 SEC.)	J	B
T103 (2-16/0)	AE	K
T102 (A/40)	E	C

E. OVERALL EQUIPMENT TESTS

After the SLA51K relay and the associated static relay units have been individually calibrated and tested for the desired settings, a series of overall operating circuit checks is advisable.

The elementary, overall logic, and logic description for the specific job will be useful for determining the overall operation of the scheme.

Overall equipment tests can be performed by applying alternating current and voltages to the measuring units as specified in the instruction book for the measuring units and checking that proper outputs are obtained from the associated SLAT when the measuring units operate.

MAINTENANCE

A. PERIODIC TESTS

It should be sufficient to check the outputs produced at test points in the SLA51K when periodic calibration tests are made on the associated measuring units, for example, the phase and ground relays in line-relaying scheme. No separate periodic tests on the SLA51K itself should be required.

B. TROUBLESHOOTING

In any troubleshooting of equipment, it should first be established which unit is functioning incorrectly. The overall logic diagram supplied with the equipment shows the combined logic of the complete equipment and the various test points in each unit. By signal tracing, using the overall logic diagram and the various test points, it should be possible to quickly isolate the trouble.

C. SPARE PARTS

To minimize possible outage time, it is recommended that a complete maintenance program should include the stocking of at least one spare card of each type. It is possible to replace damaged or defective components on the printed circuit cards, but great care should be taken in soldering so as not to damage or bridge-over the printed circuit busses, or overheat the semi-conductor components. The repaired area should be recovered with a suitable high-dielectric plastic coating to prevent possible breakdowns across the printed busses due to moisture and dust. The wiring diagrams for the cards in the SLA51K relay are included in the card book GEK-34158.

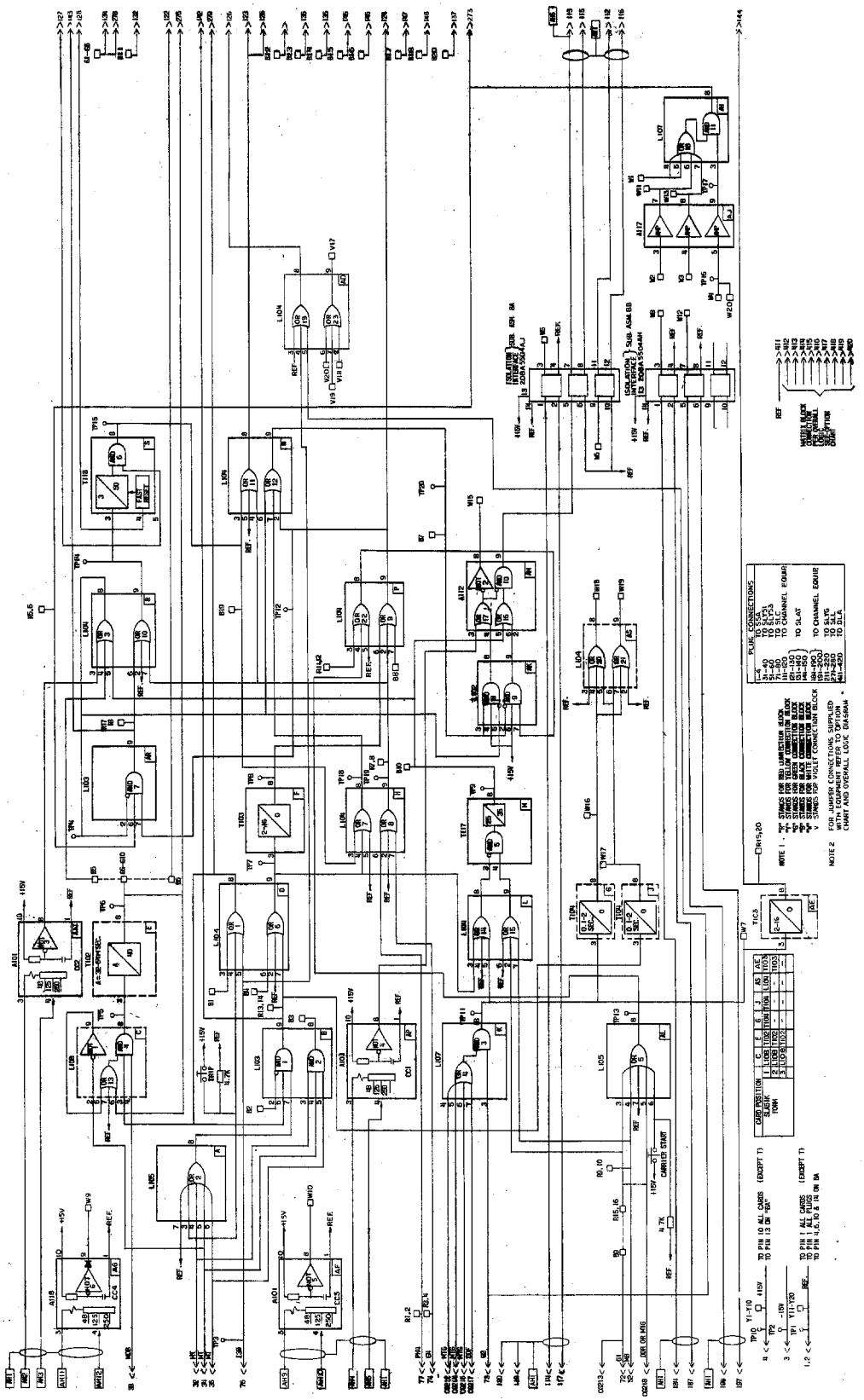

Fig. 1 (136D3500-0) INTERNAL CONNECTION DIAGRAM FOR THE SLA51K RELAY

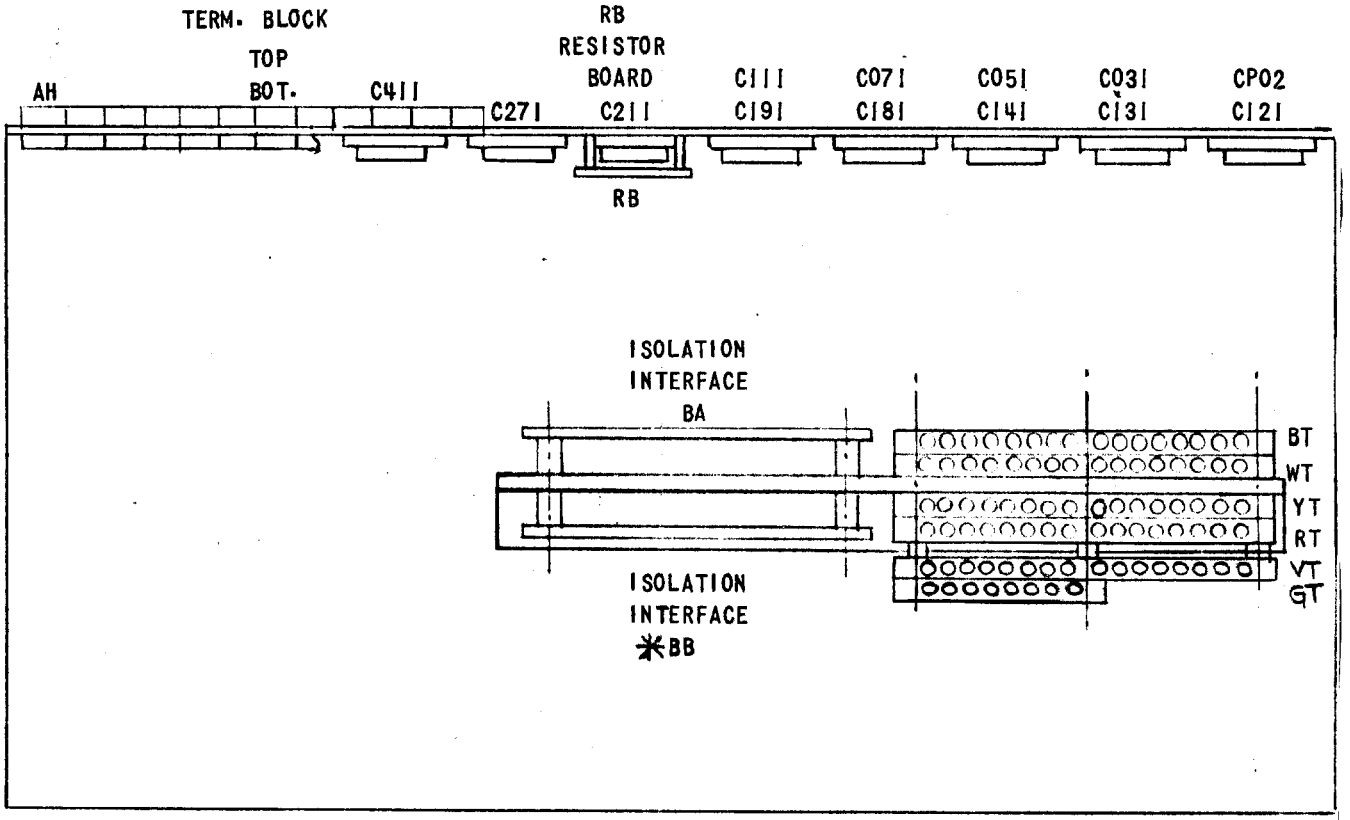

Fig. 2 (0257A8799-0) COMPONENT LOCATION DIAGRAM

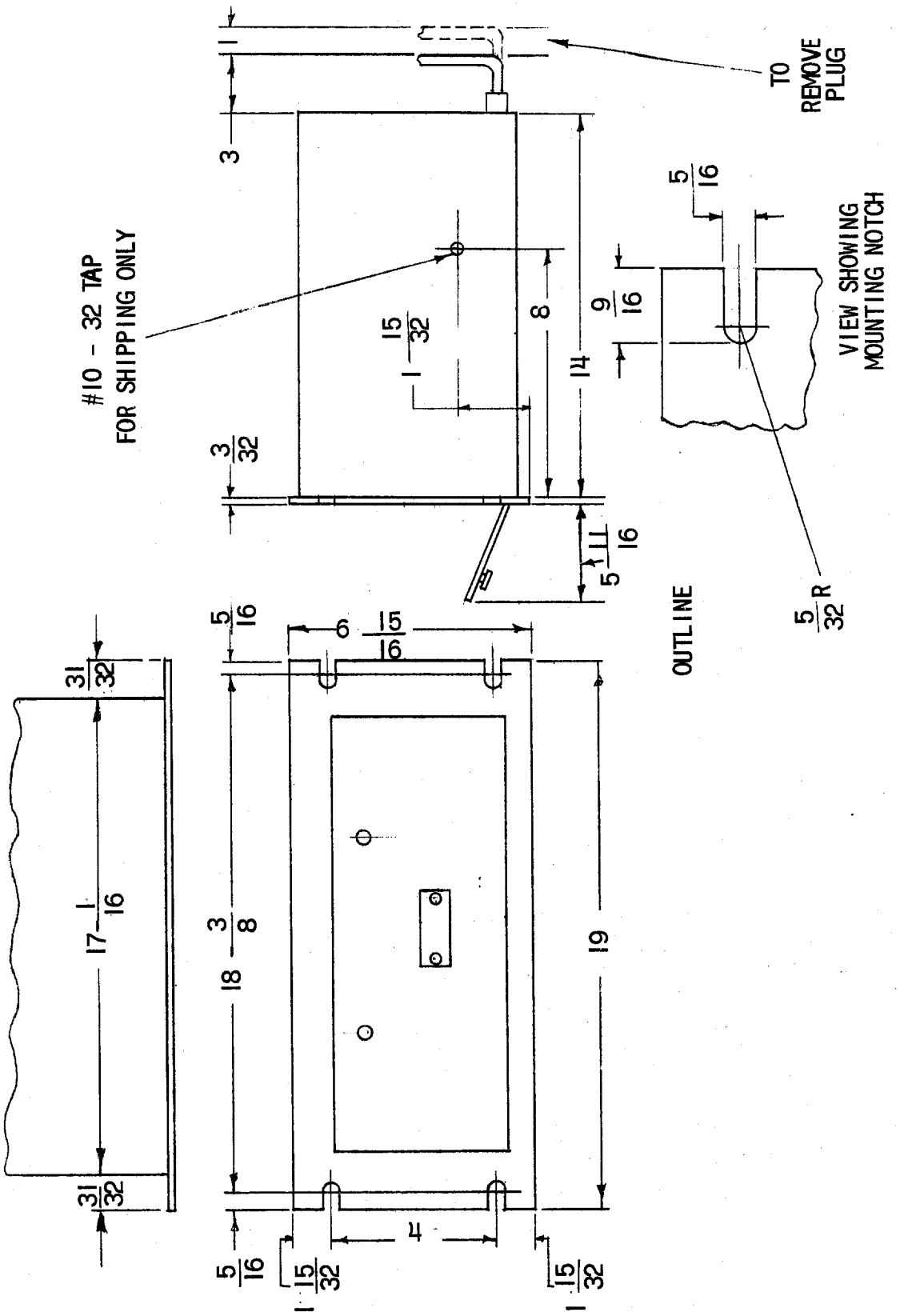

Fig. 3 (227A2037-0) OUTLINE AND MOUNTING DIMENSIONS FOR THE SLA51B RELAY

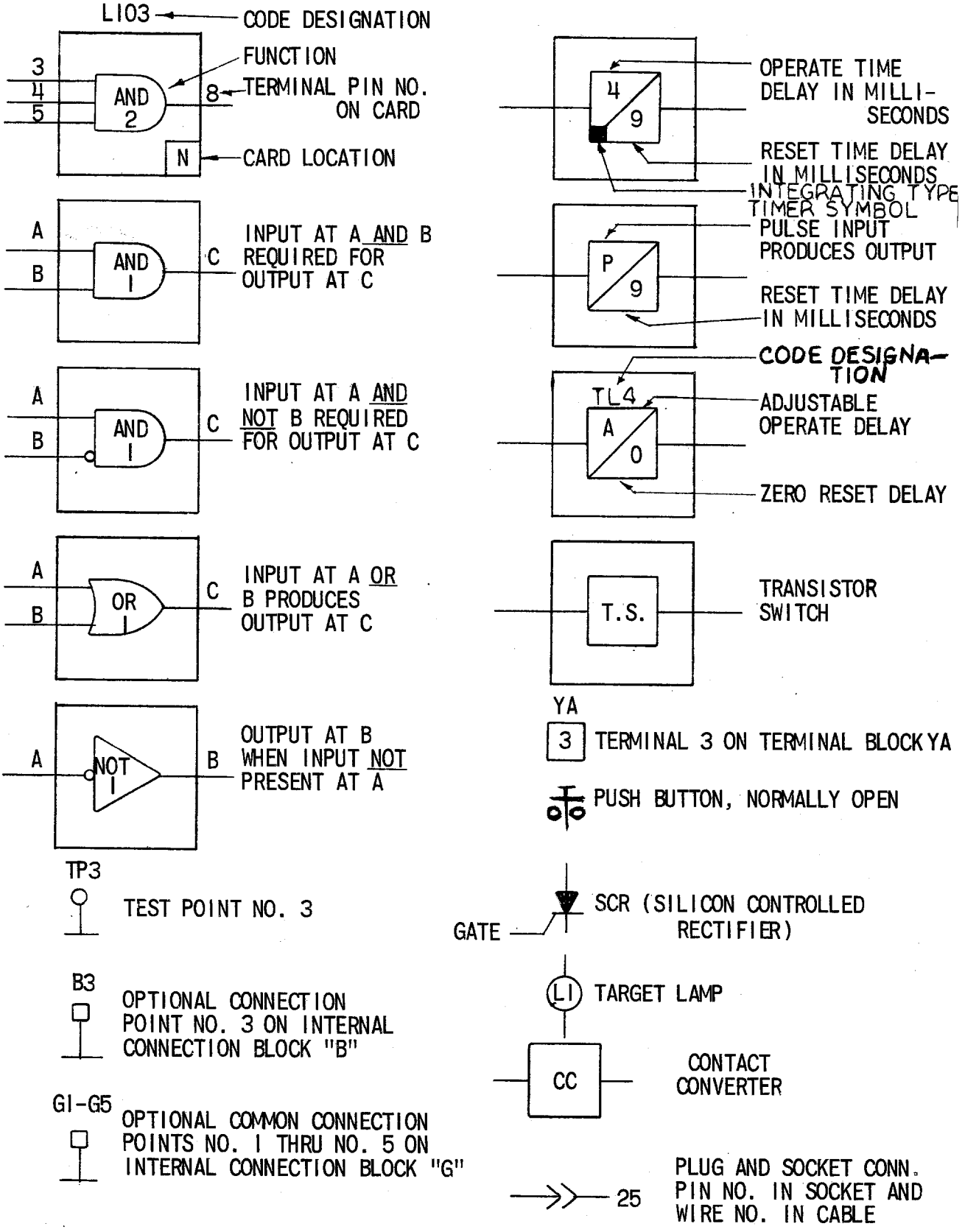

Fig. 4 (227A2047-1) LOGIC AND INTERNAL CONNECTION DIAGRAM LEGEND

THE FOLLOWING ARE FACTORY CONNECTIONS MADE AT THE MATRIX BLOCKS INSIDE OF THE SLA RELAY ASSOCIATED WITH THIS EQUIPMENT.

SYMBOLS LISTED: PL=RELAY INTERCONNECTING CABLE LEAD
(5)=LOGIC FUNCTION CARD PIN NUMBER
‡ =3-WAY CONNECTION
✳ =DLA MONITOR CONNECTION AVAILABLE BUT NOT USED

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MATRIX BLOCK JUMPERS		LOGIC FUNCTION	
FROM	TO	FROM	TO
W9	W2	CC4	AMP(AJ)
R1	B15	PL77	PL145
B9	R15	PL72	OR5
B2	Y11	AND 1	REF.
B1	Y12	OR1	REF
B4	Y14	OR6	REF
B5	Y13	OR3	REF
R3	B16	PL74	PL146
G6	B6	TL1	PL122
R11	Y15	OR22	REF
B8	R19	OR9	TL5
W5	W4	ISOL INTR	AMP
W8	W3	ISOL INTR	AMP
W15	W6	NOT 2	ISOL INTR
W1	Y17	OR18	REF
B11	Y16	PL132	REF
B14	Y18	PL135	REF
B17	Y19	PL147	REF
B18	Y20	PL148	REF
W16	W18 ⊖	TL7	OR20
W19	W17 ⊖	TL6	OR21
412	R16	PL412	OR5
413	R9	PL413	OR5
414	B7	PL414	OR12
415	R5	PL415	AND11
416	R2	PL416	PL77
417	R20	PL417	TL5
418	R13	PL418	AND1
419	B10	PL419	TL3
420	G8	PL420	TL1
V20	V17 ⊖	OR20	OR20
V19	V18 ⊖	OR20	OR20
⊖ USE	LONGEST LEADS		

MATRIX BLOCK JUMPERS		LOGIC FUNCTION	
FROM	TO	FROM	TO
FOR ZONE 2 Ø & G			
REMOVE JUMPERS			
W16	W18	TL7	OR20
W19	W17	OR21	TL6
B18	Y20	PL148	REF
B11	Y16	PL132	REF
G6	B6	TL1	PL122
V20	V17	OR23	OR23
V19	V18	OR23	OR23
ADD FOLLOWING JUMPERS			
G6	V20	TL1	OR23
B6	V17	PL122	OR23
W16	B18	TL7	PL148
W17	B17	TL6	PL147
W19	B11	OR21	PL132
W18	V19	OR20	OR23
V18	Y16	OR23	REF

Fig. 5 (227A2050-0 Sh.117) SAMPLE OPTION CHART FOR THE SLA51K RELAY

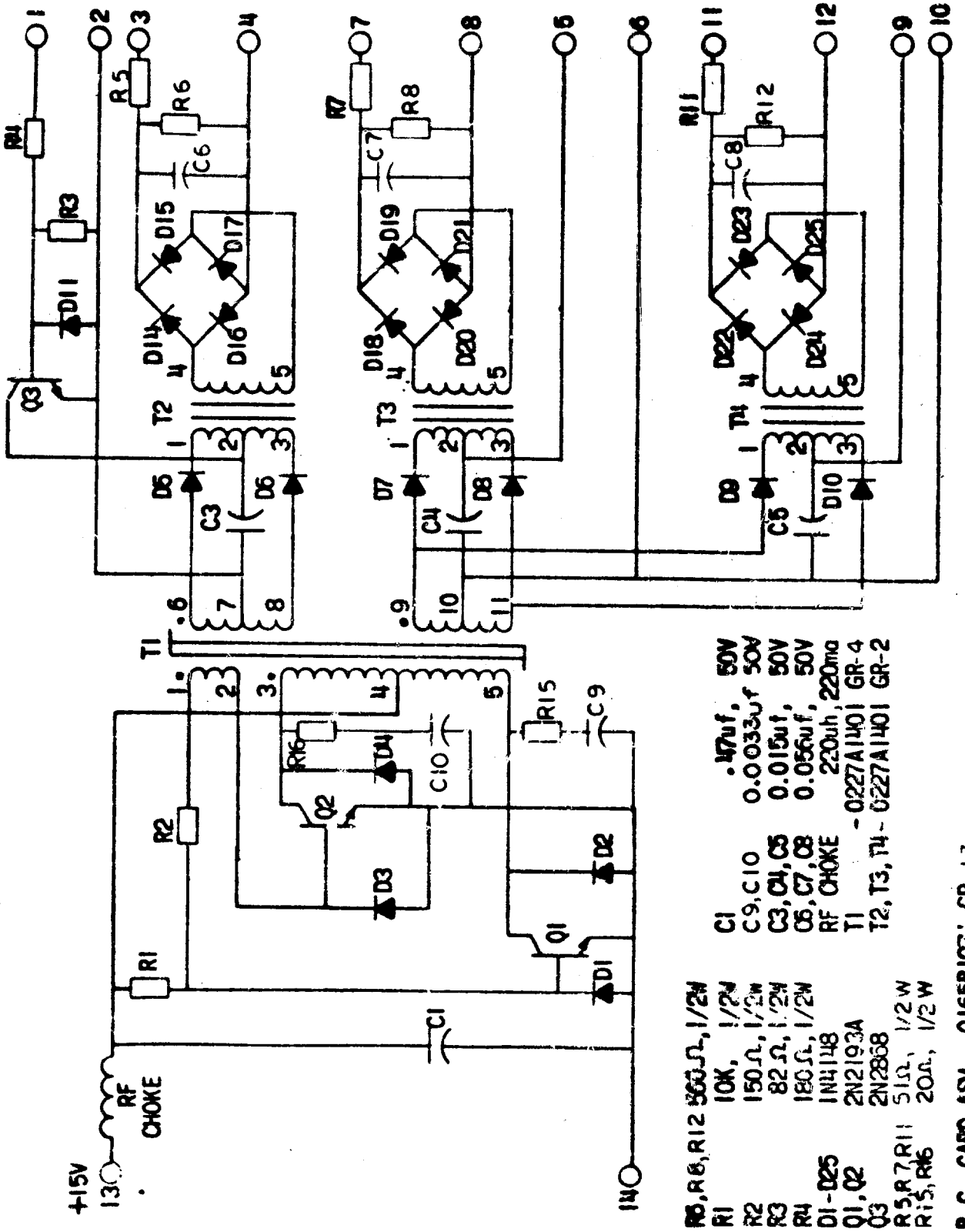


Fig. 6 (208A5504AJ-1) ISOLATION INTERFERENCE CIRCUIT

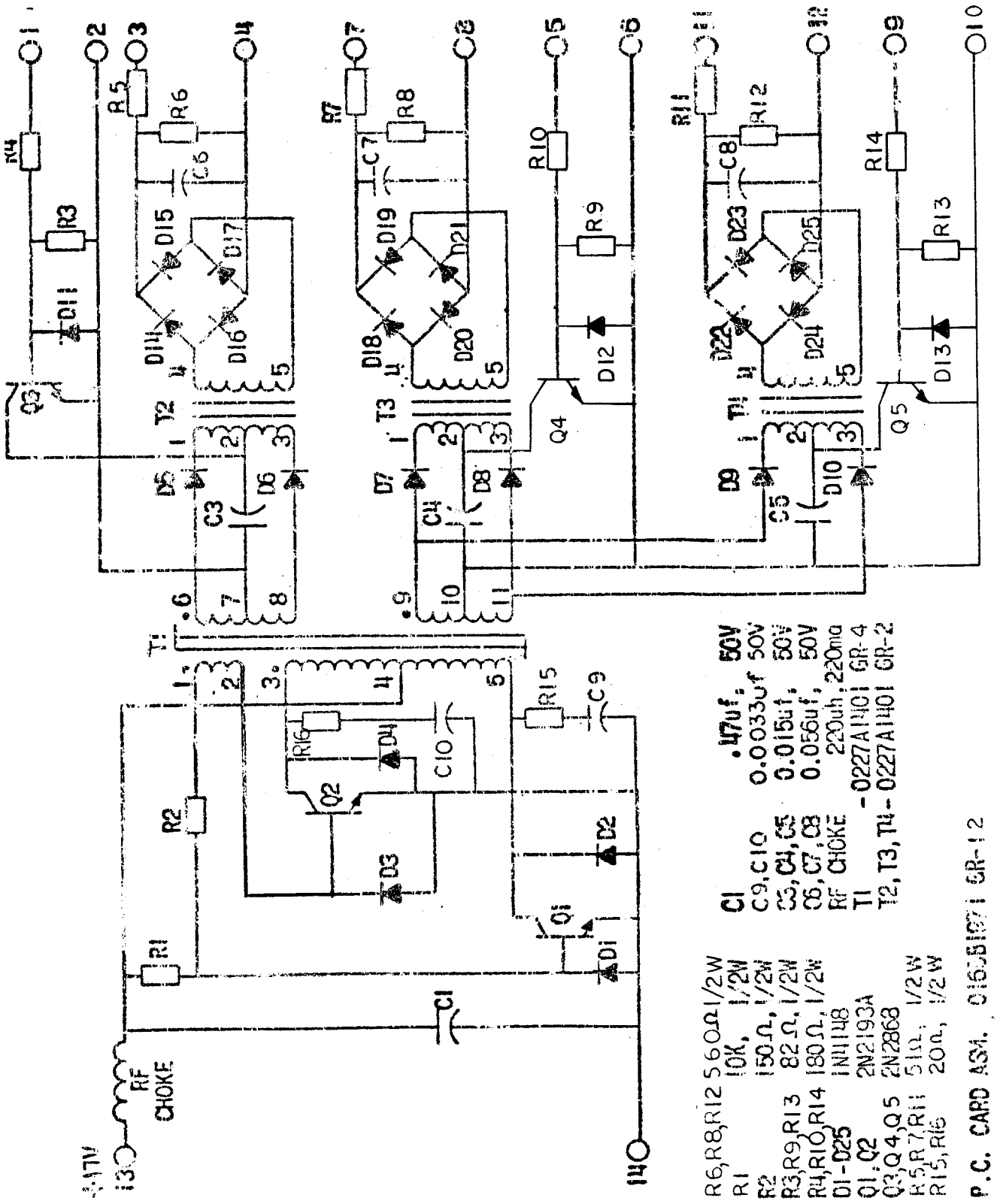
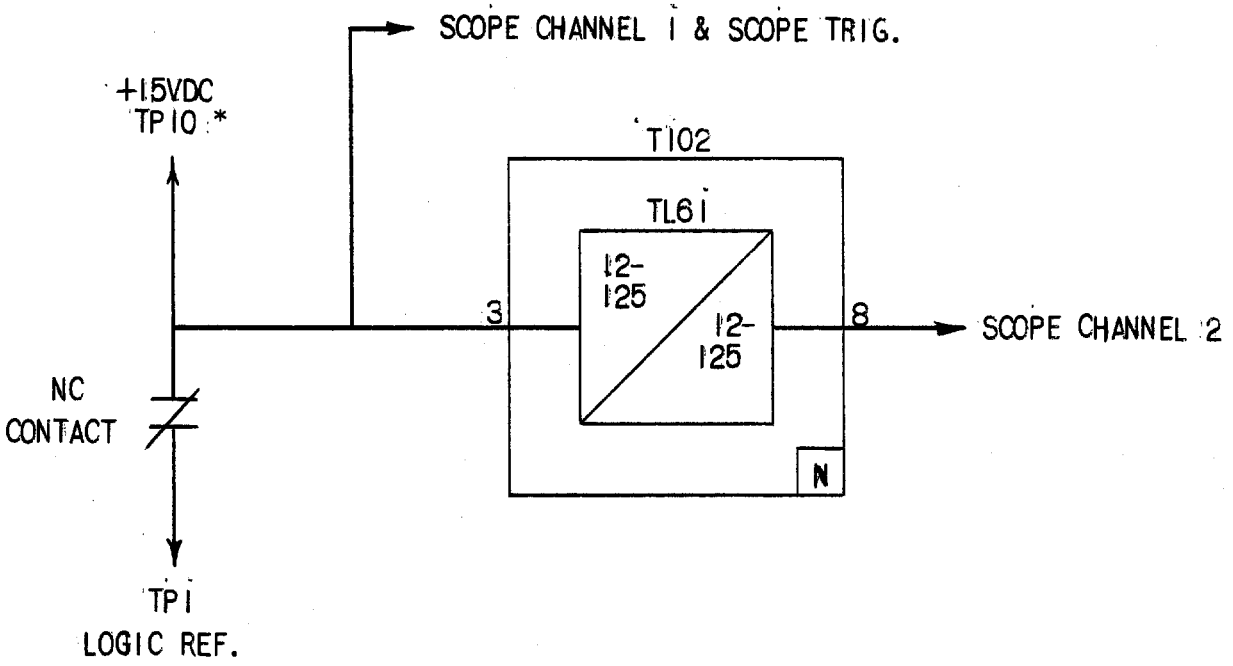


Fig. 7 (208A5504AH-1) ISOLATION INTERFACE CIRCUIT



* THE 15VDC SIGNAL AT PIN 10 HAS A CURRENT LIMITING RESISTOR MOUNTED ON THE TEST CARD.

Fig. 8 (246A7987-0) LOGIC TIMER TEST CIRCUIT