INSTRUCTIONS

GEK-49863

SOLID STATE AUXILIARY LOGIC RELAY FOR TRANSMISSION LINE PROTECTION

TYPE SLA51M

GENERAL ELECTRIC

CONTENTS

SOLID STATE AUXILIARY LOGIC RELAY

FOR TRANSMISSION LINE PROTECTION

TYPE SLA51M

DESCRIPTION

The SLA51M relay is an auxiliary logic relay designed to be used in a directional comparison ON-OFF carrier scheme. The relay contains the necessary logic to interpret output signals from associated measuring functions and translate them to an appropriate auxiliary output and tripping relay. In addition to the SLA51M relay, appropriate ground and phase relays plus a power supply and auxiliary tripping relay are required to complete a particular relaying scheme.

The type SLA51M relay is packaged in a four rack unit enclosed metal case. The relay is suitable for mounting in a 19 inch rack and the mounting and outline dimensions are shown in Fig. 3. Internal connections for the SLA51M relay are shown in Fig. 1, and the component and card locations are shown in Fig. 2.

APPLICATION

The SLA51M relay is designed to operate in conjunction with appropriate phase and ground relays in a directional comparison ON-OFF blocking scheme, using a Type CS26B power line carrier as the pilot channel. The SLA51M includes circuits to accomodate the use of first and second zone phase and ground distance back-up protection with the blocking directional comparison scheme. An isolation interface provides the interconnection between the SLA51M logic and the transmitter and receiver of the pilot channel.

Protection features required in a relaying scheme often vary from scheme to scheme and it is sometimes desirable to provide certain features initially with the scheme or to provide features so that they may be added at a later date in the field. To this end, the SLA51M design has incorporated circuit flexibility to permit implementation of certain optional features. Printed circuit cards L108 and T102, shown dotted in Fig. 1, are used whenever out-of-step detection is required. Matrix blocks "B", "G", "R", "V", "W" and "Y", each with a number of points, are provided in all SLA51M relays to permit various logic arrangements to be made simply by connecting jumper leads between appropriate points. For example, a jumper between G1 and B17 shown dotted in Fig. 1, will allow the out-of-step detection option to block all pilot tripping by applying the NOT input to AND7. On the other hand, jumpering between G2 and B16 will block reclosing by applying the NOT input to the appropriate AND function in the associated SLAT tripping relay. These examples can best be understood by referring to the overall logic diagram and instruction books supplied with a particular relaying scheme.

Various points in the logic can be monitored by providing jumpers from any of the available matrix points to plug A11 located on the rear of the SLA51M relay. This option is further described in paragraph "C", "Data Monitoring Points", under the section headed OPERATING PRINCIPLES.

For the specific options and the logic arrangement supplied with a particular scheme, refer to the logic diagram and logic descriptive writeup supplied with that scheme. If it is desired to make logic changes at a later date, the diagrams and instruction books supplied with a particular scheme should be studied to determine the means for implementing the changes. If, after study of the diagrams, further assistance is required, contact the nearest General Electric District Sales Office.

There are no measuring functions to be set in the SLA51M relay, but included are certain timers that must be set in accordance with the demands of the particular system to be protected. Refer to the section under SETTINGS for a description of these timers and for suggestions to be used in making the settings.

RATINGS

The type SLA51M relay is designed for use in an environment where the air temperature outside the relay case does not exceed -20°C or +65°C.

The type SLA51M relay requires ±15 VDC power source which can be obtained from a Type SSA power supply.

Each contact converter in this relay has a link for selecting the proper voltage for the coil circuit of the contact converter. The three possible voltages are 48 VDC, 125 VDC and 250 VDC.

BURDENS

The SLA51M relay presents a burden of 400 milliamperes to the +15 VDC supply of the Type SSA power supply.

Each contact converter, when energized, will draw approximately 10 milliamperes from the station battery, regardless of tap setting.

OPERATING PRINCIPLES

LOGIC CIRCUIT

The functions of the type SLA51M relay involve basic logic (AND, OR, and NOT) where the presence or absence of signals, rather than their magnitudes, controls the operation. Signals are measured with respect to a reference bus accessible at TP1. In general, a signal below one VDC represents an OFF or LOGIC ZERO condition; an ON or LOGIC ONE condition is represented by a signal of approximately +15 VDC.

The symbols used on the internal connection diagram (Fig. 1) are explained by the legend shown in Fig. 4.

The matrix block options shown in the internal connections of the SLA51M relay are provided at the factory. The connections are shown on the associated overall logic and are listed on the associated option chart. A sample option chart for the Type SLA51M relay is shown in Fig. 5.

CONTACT CONVERTERS

The purpose of this function is to convert a contact operation into a signal that is compatible with the logic circuit of the Type SLA51M relay. These contact converters, which are labeled CC1, CC2, and CC3 have a non-adjustable four millisecond pickup delay.

CC1

Contact converter 1 is energized by an external contact to stop all carrier transmission.

CC2

Contact converter 2, when energized, prevents relay carrier tripping and relay control of carrier but permits auxiliary control of carrier.

CC3

Contact converter 3 when included supervises trip for line energizing.

DATA MONITORING POINTS

Type SLA51M relay has provisions to provide data monitoring outputs. The data monitoring (DLA) points are selected on the matrix blocks and are listed on the option chart. Any matrix block points which are

not used for logic connections may be monitored. Key points in the logic have more than one matrix point to allow both logic and monitoring connections. A data logging amplifier (DLA) relay is used to translate these logic signals into usable outputs.

CHANNEL INTERFACE

The logic of the Type SLA51M relay includes an isolation interface (Fig. 6) between the relays in the scheme and the associated channel. The circuitry of the isolation interface provides a signal path but maintains metallic isolation. This feature makes it possible to maintain isolation between the DC supply used for the relays and that employed by the channel.

When pins 9 and 10 are both connected to relay reference, a metallically separate positive logic signal appears at pin 11 with respect to 12. The output from the isolation interface is a 5 VDC, 20 milliampere signal.

SETTINGS

There are six timers in the SLA51M relay that may require field adjustment.

The 3/50 timer is part of the comparer-integrator scheme. The normal three millisecond pickup setting is intended to provide coordination between receiver input and the MT input to the comparer AND7. The pickup setting allows for the transmitter-receiver operating time plus the signal propogation time. For longer transmitter-receiver operating times, such as with narrow band carrier, a longer pickup time should be considered. Long transmission lines (longer signal propogation time) may also require that the pickup setting be increased. It should be remembered that tripping will be delayed in accordance with the pickup setting of this timer. The purpose of the reset delay of this timer is to hold off carrier for some time after tripping and so ensure that the remote relay will have ample time to operate.

The 2.5/16 timer in the SLY and A/40 timer in the SLA51M are part of the out-of-step detection scheme. The 2.5/16 timer forms a "tomato" (outer) characteristic; thus the distance a swing must travel before the mho (inner) characteristic is encountered is determined by the pickup setting of this timer. The A/40 timer is used to measure the time of travel between the outer and inner characteristic. An out-of-step condition will be detected when both timers are adjusted properly. The setting of both timers should be based on the results of system swing studies.

The (2-16)/0 timer is a coordinating timer necessary for the correct operation of the blocking scheme. The timer is normally set for four milliseconds to insure coordination between the carrier stop (MT) function at one end and the carrier start (MB) function at the other end of the protected line.

The TU2Ø and TU2G are zone 2 backup timers for phase and ground faults respectively. The range of the pickup is 100 milliseconds to 2000 milliseconds. The timer setting must be such that coordination with the corresponding phase or ground remote zone 1 protection is obtained.

The (20-200)/(30-240) optional timer is used in a high current direct tripping scheme when the line is energized into a zero voltage fault.

Further details for setting these timers can be found in the logic description provided with each static relaying scheme.

CONSTRUCTION

The SLA51M relay is packaged in an enclosed metal case with hinged front covers and removable top cover. The outline and mounting dimensions of the case and the physical location of the components are shown in Figs. 3 and 2 respectively.

The SLA51M relay contains printed circuit cards identified by a code number such as A101, T102, L104 where A designates auxiliary function, T designates time-delay function, and L designates logic function. The printed circuit cards plug in from the front of the unit. The sockets are marked with letter designations or "addresses" (D, E, F, etc.) which appear on the guide strips in front of each socket, on the component location drawing, on the internal connection diagram and on the printed circuit card. The test points (TP1, TP2, etc.) shown on the internal connection diagram are connected to instrument jacks on a test card in position T or AT with TP1 at the top of the AT card. TP10 is tied to +15 VDC through a 1.5K resistor. This resistor limits the current when TP10 is used to supply a logic signal to a card.

Other logic options are selected by means of taper tip jumpers and matrix blocks. These matric blocks are located in the rear of the unit as shown in Fig. 2. The green (G) matrix block has twenty points in three 5-point common groups and five individual matrix points. The black (B) matrix block has 20 individual matrix points. The red (R) block has 20 points which are grouped in pairs. The yellow (Y) block has 20 points which are grouped in 10 common points; 1 to 10 are tied to +15 VDC, 11 to 20 are tied to reference. The white (W) matrix block has twenty individual matrix points. The violet (V) matrix block has twenty individual matrix points. Tools for inserting and removing taper tip jumpers are supplied with each relay.

RECEIVING, HANDLING AND STORAGE

The SLA51M relay will normally be supplied as a part of a static relay equipment, mounted in a rack or cabinet with other static relays and test equipment. Immediately upon receipt of a static relay equipment, it should be unpacked and examined for any damage sustained in transit. If injury or damage resulting from rough handling is evident, file a damage claim at once with the transportation company and promptly notify the nearest General Electric Sales Office.

Reasonable care should be exercised in unpacking the equipment. If the equipment is not to be installed immediately, it should be stored indoors in a location that is free from moisture, dust, metallic chips, and severe atmospheric contaminants.

Just prior to final installation the shipping support bolt should be removed from each side of all relay units, to facilitate possible future unit removal for maintenance. These shipping support bolts are approximately eight inches back from the relay front panel. Static relay equipment, when supplied in swing rack cabinets, should be securely anchored to the floor or to the shipping pallet to prevent the equipment from tipping over when the swing rack is opened.

TEST INSTRUCTIONS

CAUTION

THE LOGIC SYSTEM SIDE OF THE DC POWER SUPPLY USED WITH MOD III STATIC RELAY EQUIPMENT IS ISOLATED FROM GROUND. IT IS A DESIGN CHARACTERISTIC OF MOST ELECTRONIC INSTRUMENTS THAT ONE OF THE SIGNAL INPUT TERMINALS IS CONNECTED TO THE INSTRUMENT CHASSIS. IF THE INSTRUMENT USED TO TEST THE RELAY EQUIPMENT IS ISOLATED FROM GROUND, ITS CHASSIS MAY HAVE AN ELECTRICAL POTENTIAL WITH RESPECT TO GROUND. THE USE OF A TEST INSTRUMENT WITH A GROUNDED CHASSIS WILL NOT AFFECT THE TESTING OF THE EQUIPMENT. HOWEVER, A SECOND GROUND CONNECTION TO THE EQUIPMENT, SUCH AS A TEST LEAD INADVERTENTLY DROPPING AGAINST THE RELAY CASE, MAY CAUSE DAMAGE TO THE LOGIC CIRCUITRY. NO EXTERNAL TEST EQUIPMENT SHOULD BE LEFT CONNECTED TO THE STATIC RELAYS WHEN THEY ARE IN PROTECTIVE SERVICE, SINCE TEST EQUIPMENT GROUNDING REDUCES THE EFFECTIVENESS OF THE ISOLATION PROVIDED.

GENERAL

If the SLA51M relay that is to be tested is installed in an equipment which has already been connected to the power system, disconnect the outputs in the associated Type SLAT relay from the system.

The SLA51M relay is supplied from the factory either mounted in a static relay equipment or as a separate unit associated with measuring relays, a Type SSA power supply, and some form of channel equipment. All relay units for a given terminal of static relaying equipment are tested together at the factory, and each unit will have the same summary number stamped on its nameplate.

In general, when a time range is indicated on the internal connection diagram, the timer has been factory set at a mid-range value. Timers should be set for the operating or reset times indicated on the associated overall logic diagram. Where a time range is indicated on the overall logic diagram, the timer should be set for the value recommended for that function in the descriptive writeup accompanying the overall logic diagram. Where a setting depends upon conditions encountered on a specific application, that is so stated and the factors influencing the choice of setting are described. The procedure for checking and setting the timers is described in a later section.

OPERATIONAL CHECKS

Operation of the SLA51M unit can be checked by observing the signals at the twenty test points (TP1 to TP20) in the SLA51M, or by observing the output functions in the associated Type SLAT tripping relay. The

test points are located on two test cards in positions T and AT, and are numbered 1 to 20 from top to bottom. TP1 is the reference bus for the logic circuit; TP10 is at +15 VDC, and TP2 is at -15 VDC. The remaining points are located at various strategic points throughout the logic as shown on the internal connection diagram (Fig. 1). Test point voltages can be monitored with a portable high impedance voltmeter, the voltmeter on the test panel of the associated equipment, or an oscilloscope.

TEST CARD ADAPTER

The test card adapter provides a convenient means of gaining access to any pin of a particular card. Detailed information on the use of the test adapter card is included in the card instruction book GEK-34158.

TIMER ADJUSTMENTS AND TESTS

When the time-delay cards are to be adjusted or checked, an oscilloscope that can display two traces simultaneously and that has a calibrated horizontal sweep should be used.

In order to test the time cards it is necessary to remove the card previous to the timer (see Table I) and to place the timer card in a card adapter. The card adapter allows access to the input and output of the timer if they are not brought out on test points. The timer test circuit is shown in Fig. 7. Opening the normally closed contact causes the output to step up to +15 VDC after the pickup delay of the timer. To increase the pickup time turn the upper potentiometer on the timer card clockwise; to decrease the time turn it counter clockwise. Closing the contact causes the timer output to drop out after the reset time-delay setting of card. If the timer card is provided with a variable reset delay, it can be adjusted by the lower potentiometer on the timer card (clockwise increases reset time).

TABLE I

TIME UNDER TEST	POSITION	REMOVE CARD IN POSITION
T118 (3/50)	S	R
T103 (2-16/0)	F	B
T117 (25/35)	M	L
T104 (0.1/2 SEC.)	AD	AC
T104 (0.1/2 SEC.)	AF	AE
T102 (A/40)	E	C
T148 (20-200/30-240)	AH	AG

CONTACT CONVERTER TESTS

Operation of the contact converters can be checked by placing the contact converter card in a card adapter, after checking that the voltage tap selected agrees with the station battery voltage. Connect the station direct current through a switch to the appropriate pair of terminals of the terminal strip, AH, mounted on the rear of the relay. The terminal numbers and polarity of connections for each of the contact converters are shown in the internal connection diagram, Fig. 1. Output of the contact converter card may be monitored between pin 8 and pin 1 (reference) on the card adapter with either a scope or meter. Closure of the switch in the test source will provide a +15 volt DC signal at pin 8 of the card adapter.

ISOLATION INTERFACE TESTS

Operation of the three functions (received carrier, transmitter control, and transmitter auxiliary stop) of the isolation interface can be checked without direct connections to the subassembly. External test connections are made to the pins of the C111 socket mounted on the rear of the unit, see Fig. 1. Logic circuit test connections are made at the socket pins of the channel control card in position "AM".

Received carrier operation test connections are shown in Fig. 8A. For this test do not remove channel control card in position "AM". Closure of the normally open contact will simulate a received carrier signal and scope display will go from a logic "0" to a logic "1".

For the transmitter control and transmitter auxiliary stop checks remove the channel control card "AM" from its socket and replace it with a test card adapter and test card to gain access to the "AM" socket pins. Transmitter control test connections are shown in Fig. 8B. The test contact in the open position

simulates a logic "1" condition which holds off the transmitter control output of the isolation interface. Closure of the normally open contact generates a logic "0" condition initiating a transmitter control output producing a 5-6 volt DC signal across the output loading resistor. The transmitter auxiliary stop function can be tested in a similar manner using the test connections of Fig. 8C and the output again will provide a 5-6 volt DC signal across the output loading resistor.

OVERALL EQUIPMENT TESTS

After the SLA51M relay and the associated static relay units have been individually calibrated and tested for the desired settings, a series of overall operating circuit checks is advisable.

The elementary, overall logic, and logic description for the specific job will be useful for determining the overall operation of the scheme.

Overall equipment tests can be performed by applying AC current and voltages to the measuring units as specified in the instruction book for the measuring units and checking that proper outputs are obtained from the associated SLAT when the measuring units operate.

MAINTENANCE

PERIODIC TESTS

It should be sufficient to check the outputs produced at test points in the SLA51B when periodic calibration tests are made on the associated measuring units, for example, the phase and ground relays in line relaying scheme. No separate periodic tests on the SLA51M itself should be required.

TROUBLE SHOOTING

In any trouble shooting of equipment, it should first be established which unit is functioning incorrectly. The overall logic diagram supplied with the equipment shows the combined logic of the complete equipment and the various test points in each unit. By signal tracing, using the overall logic diagram and the various test points, it should be possible to quickly isolate the trouble.

SPARE PARTS

To minimize possible outage time, it is recommended that a complete maintenance program should include the stocking of at least one spare card of each type. It is possible to replace damaged or defective components on the printed circuit cards, but great care should be taken in soldering so as not to damage or bridge-over the printed circuit busses, or overheat the semi-conductor components. The repaired area should be recovered with a suitable high-dielectric plastic coating to prevent possible breakdowns across the printed busses due to moisture and dust. The wiring diagrams for the cards in the SLA51M relay are included in the card book GEK-34158.

FIGURES

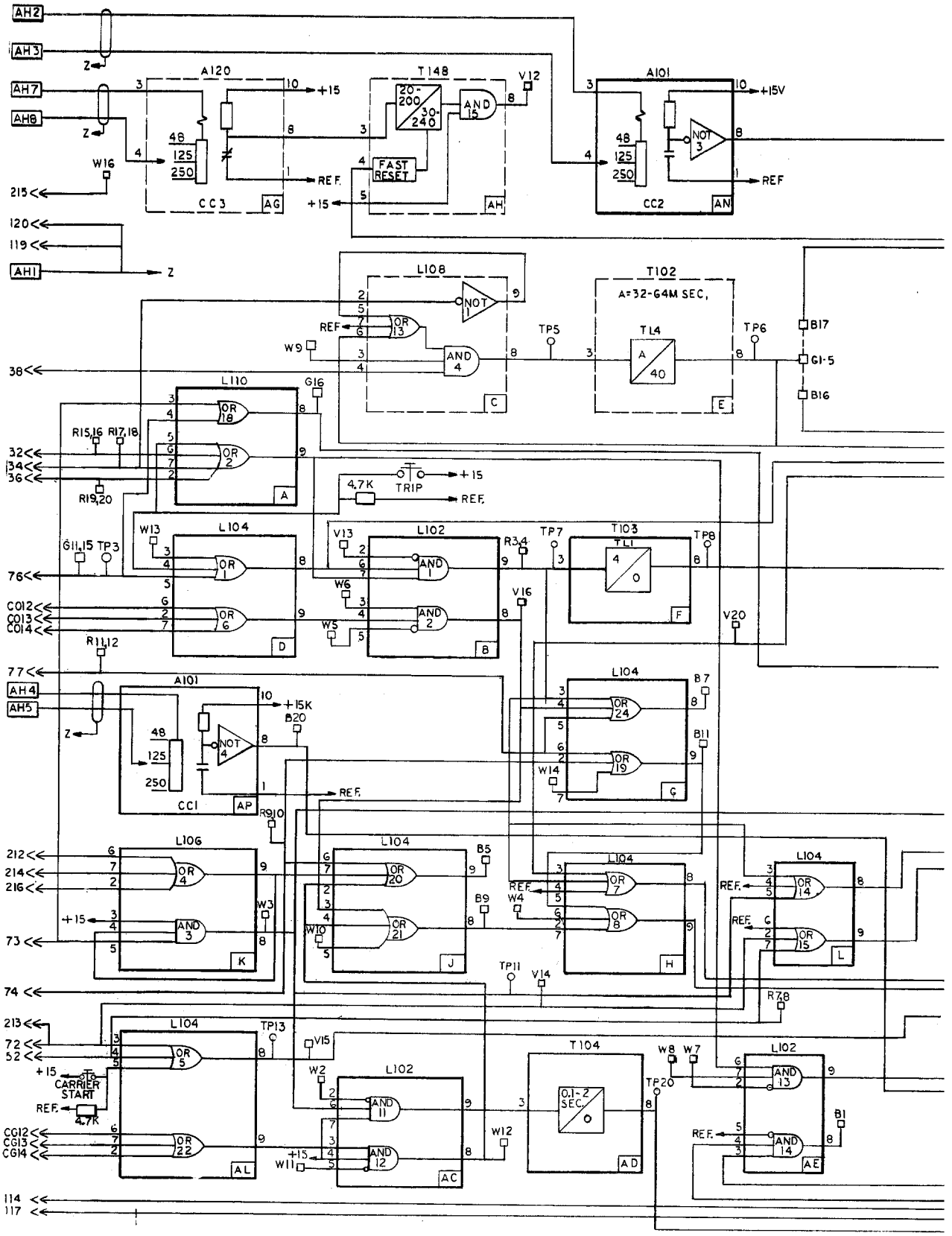


FIG. 1 (0136D3589-1) Internal Connections Diagram for the SLA51M Relay

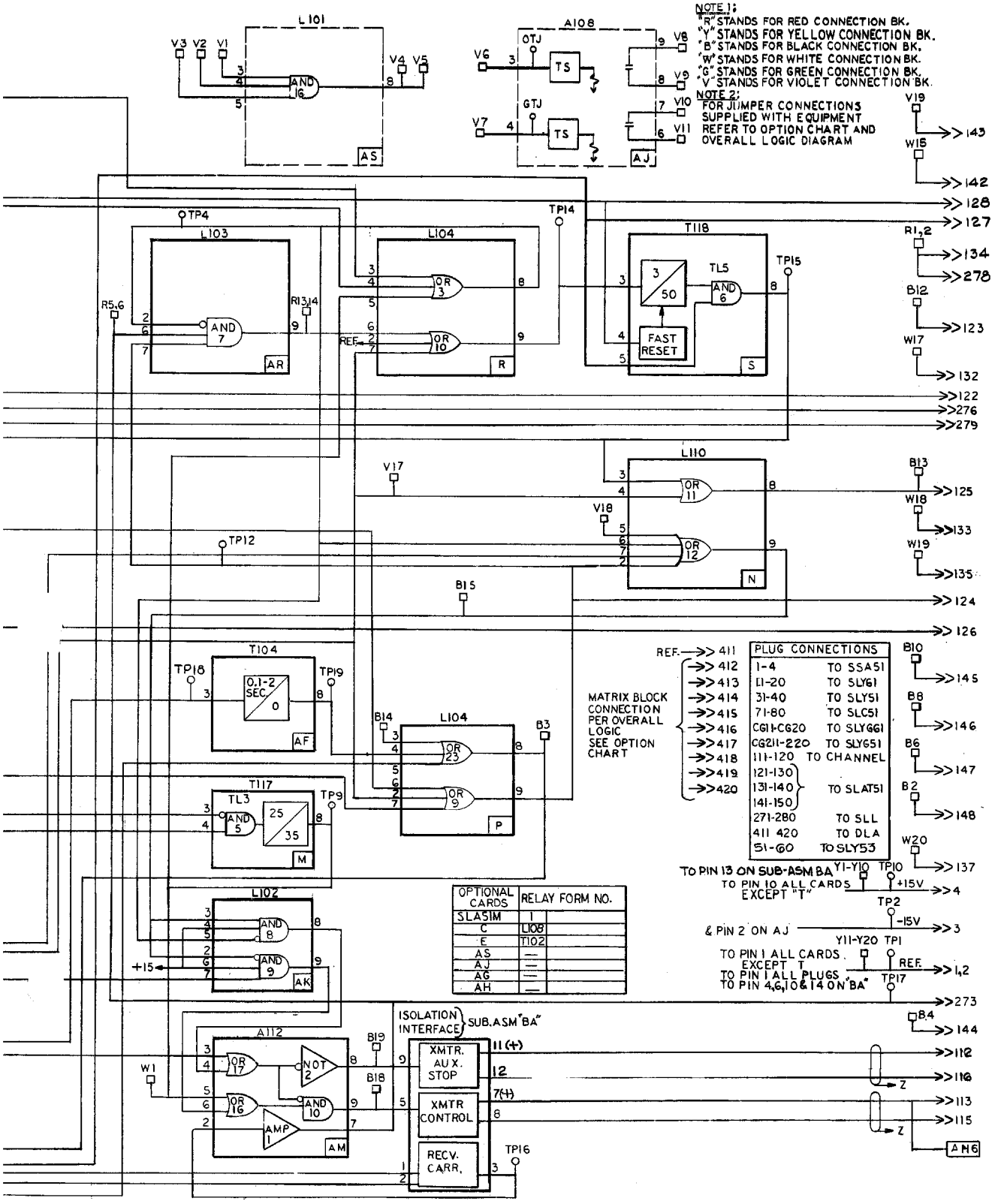
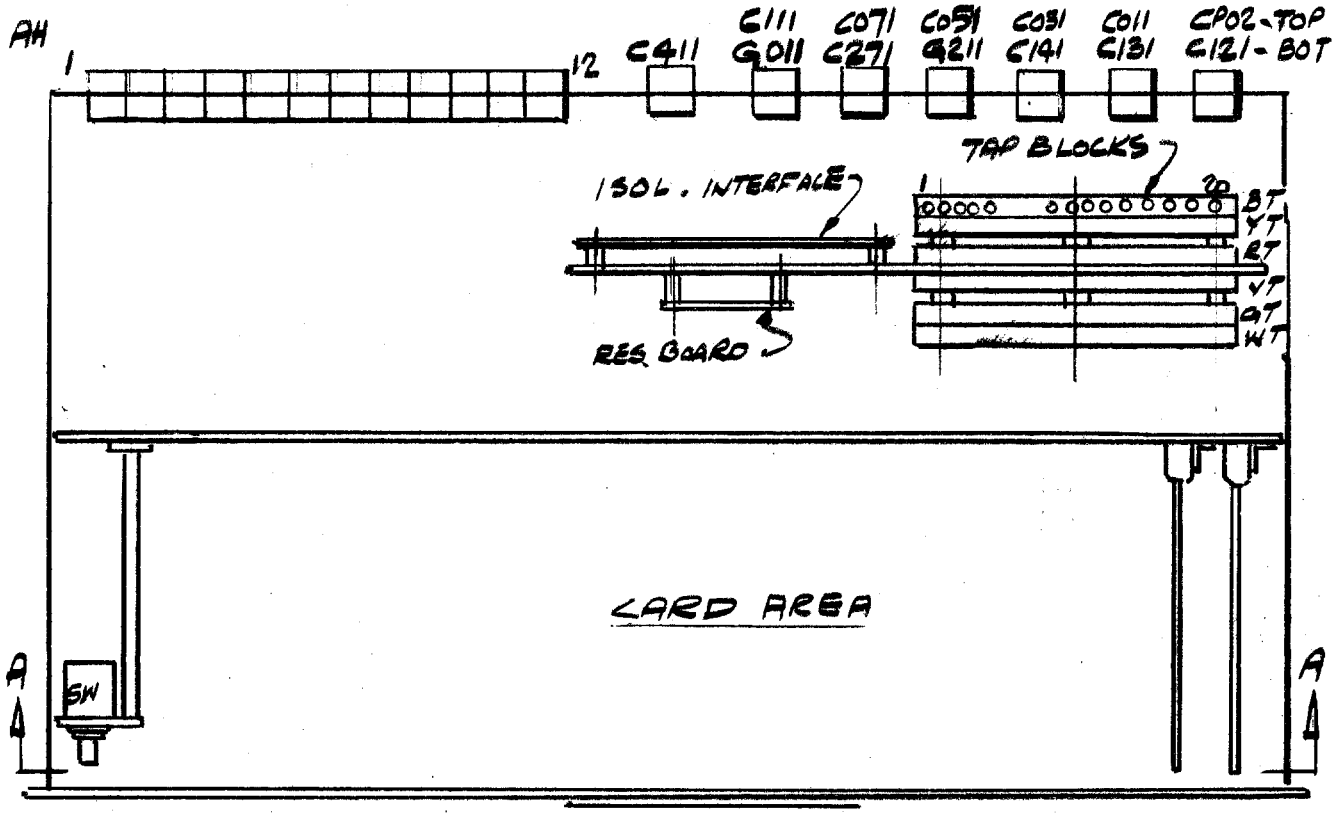


FIG. 1 (0136D3589-1) Internal Connections Diagram for the SLA51M Relay (Cont'd)



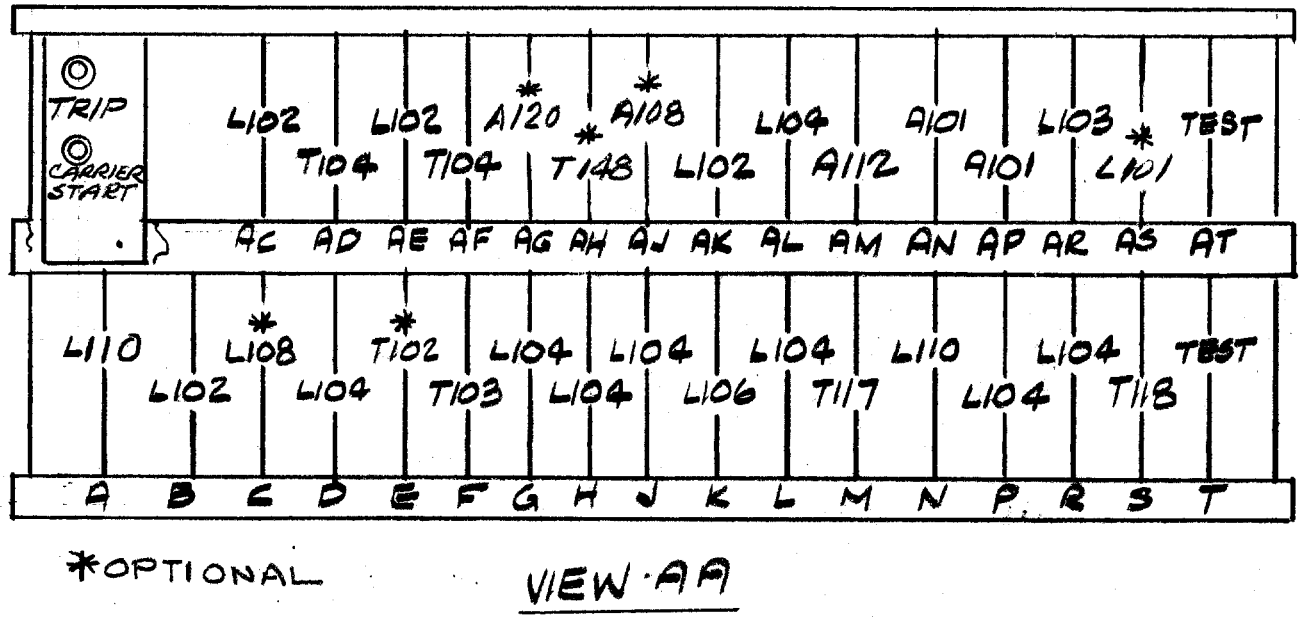


FIG. 2 (0275A1358-1) Component Location Diagram for the SLA51M Relay

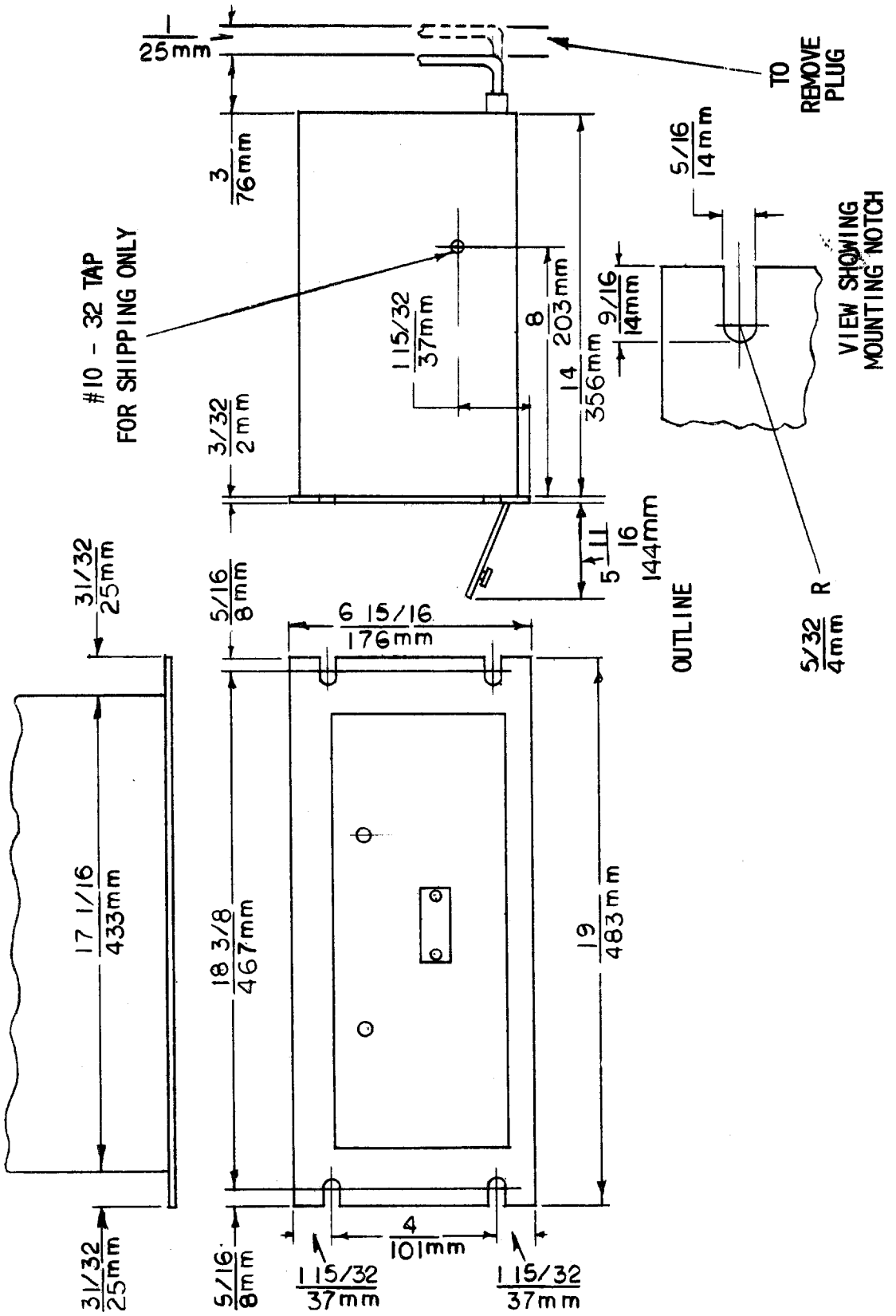


FIG. 3 (0227A2037-1) Outline and Mounting Dimensions for the SLA51M Relay

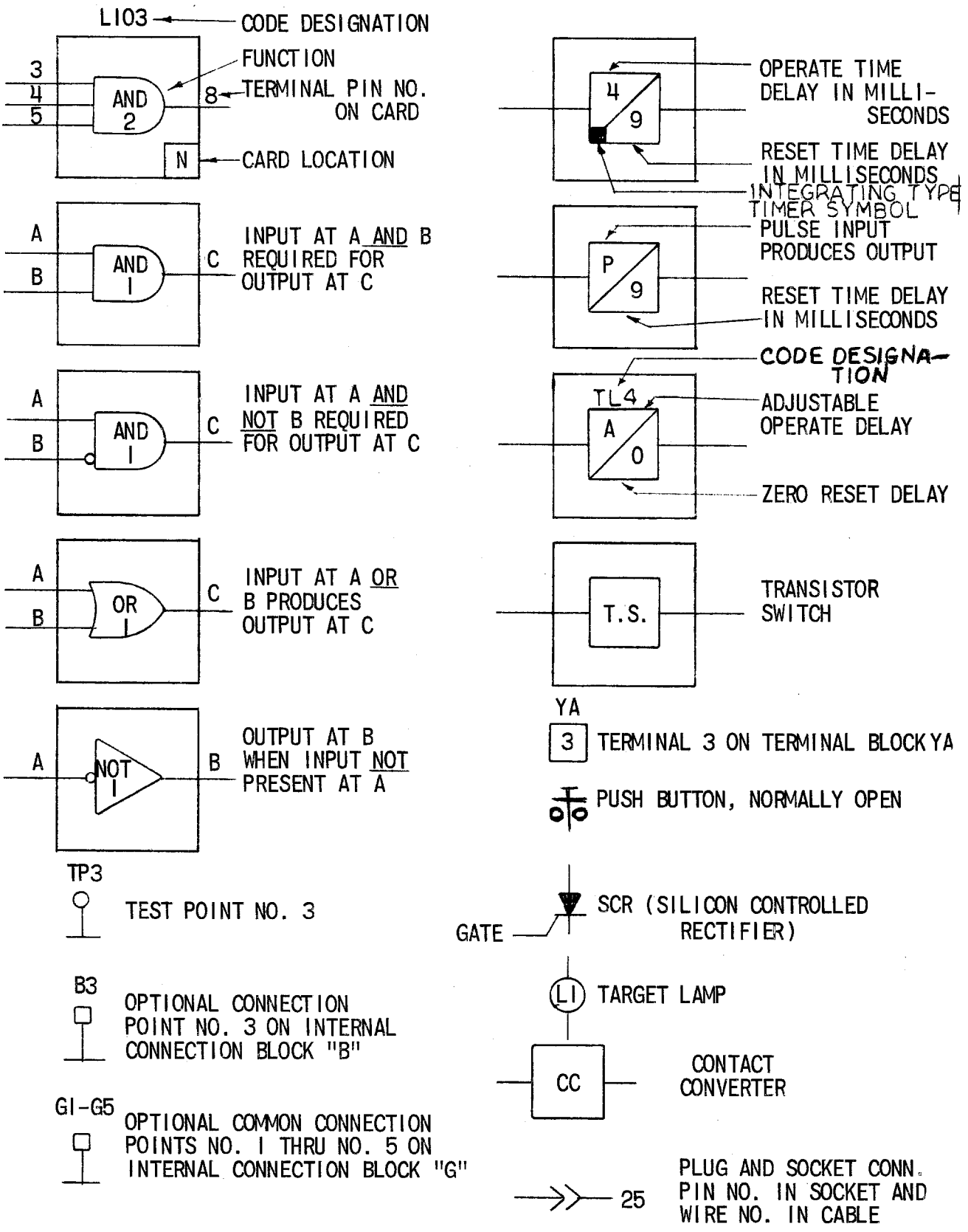


FIG. 4 (0227A2047-1) Logic and Internal Connection Diagram Legend

THE FOLLOWING ARE FACTORY CONNECTIONS MADE AT THE MATRIX BLOCKS INSIDE OF THE SLA RELAY ASSOCIATED WITH THIS EQUIPMENT.
SYMBOLS LISTED: PL=RELAY INTERCONNECTING CABLE LEAD
(5)=LOGIC FUNCTION CARD PIN NUMBER
‡ =3-WAY CONNECTION
✕ = DLA MONITOR CONNECTION AVAILABLE BUT NOT USED

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MATRIX BLOCK JUMPERS		LOGIC FUNCTION		MATRIX BLOCK JUMPERS		LOGIC FUNCTION	
FROM	TO	FROM	TO	FROM	TO	FROM	TO
W11	Y11	AND12(5)	REF				
W2	Y12	AND11(2)	REF				
W10	Y13 ‡	OR21(5)	REF				
W14	Y14 ‡	OR19(7)	REF				
W4	Y14 ‡	OR8(6)	REF				
G16	W9	OR18(8)	AND4(3)				
G11	W6	PL76	AND2(3)				
G12	W8	PL76	AND13(7)				
W5	Y16	AND2(5)	REF				
W7	Y17	AND13(2)	REF				
W13	Y18	OR1(3)	REF				
V13	Y19 ‡	AND1(2)	REF				
B17	Y20 ‡	OR3(4)	REF				
B16	Y15	PL122	REF				
B14	Y13 ‡	OR23(3)	REF				
V18	Y19 ‡	OR12(5)	REF				
B1	R1	AND14(8)	PL134				
B3	B2	OR23(8)	PL148				
B5	B4	OR20(9)	PL144				
B7	B6	OR24(8)	PL147				
B9	B8	OR21(8)	PL146				
B11	B10	OR19(9)	PL145				
R13	W15	AND7(9)	PL142				
B13	B12	OR11(8)	PL123				
PL412	✕	PL412	✕				
PL413	✕	PL413	✕				
PL414	✕	PL414	✕				
PL415	✕	PL415	✕				
PL416	✕	PL416	✕				
PL417	✕	PL417	✕				
PL418	✕	PL418	✕				
PL419	✕	PL419	✕				
PL420	✕	PL420	✕				
W19	Y20 ‡	PL135	REF				

Fig. 5 (0227A2050-0 Sh. 144) Sample Option Chart for the SLA51M Relay

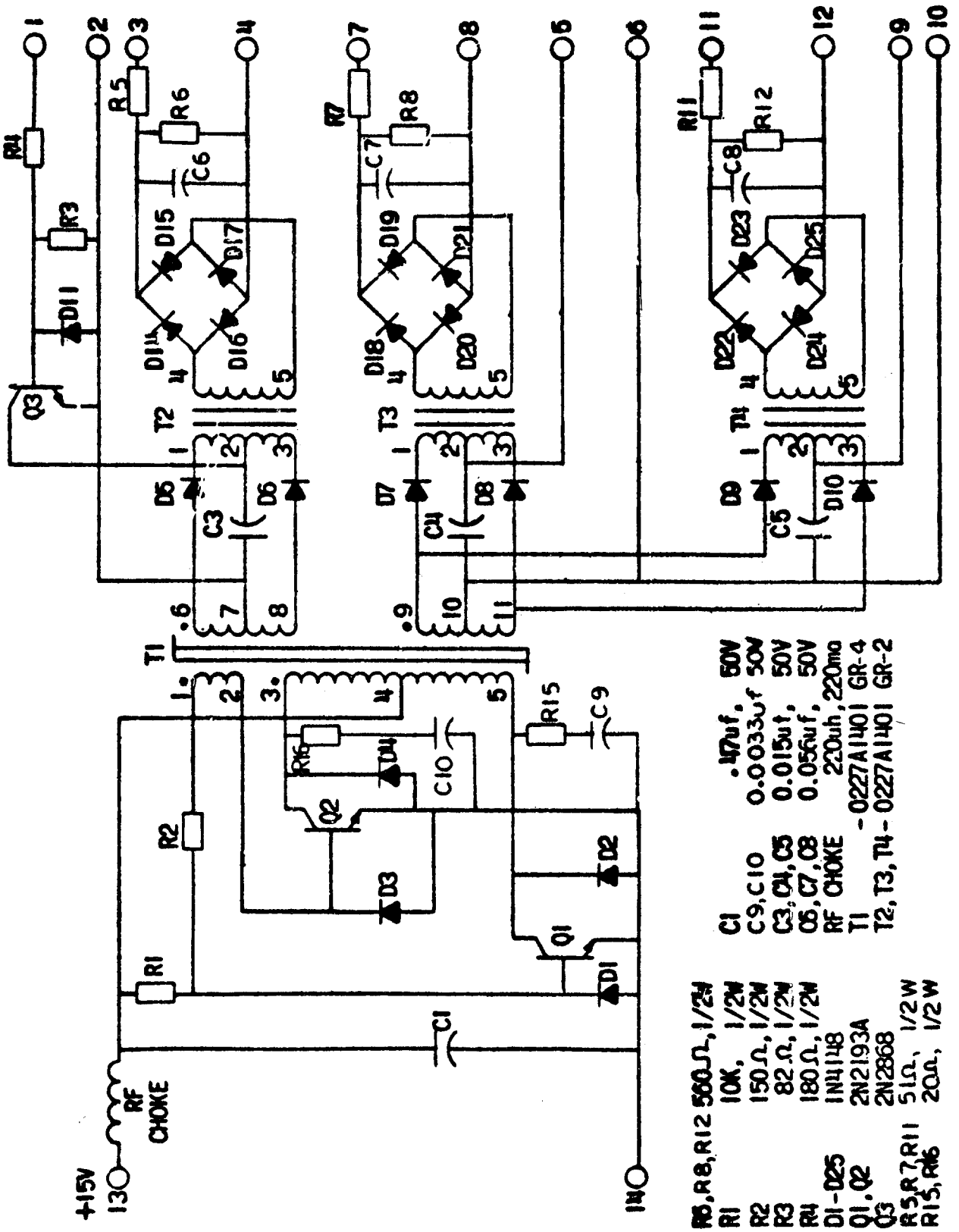
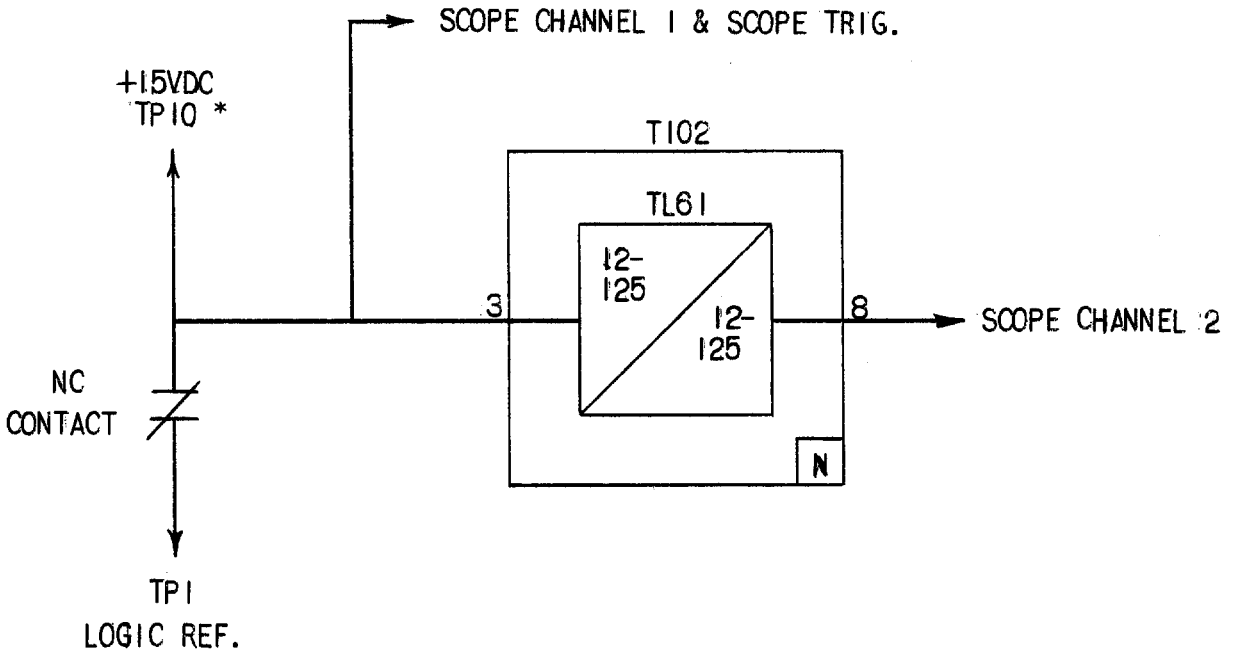
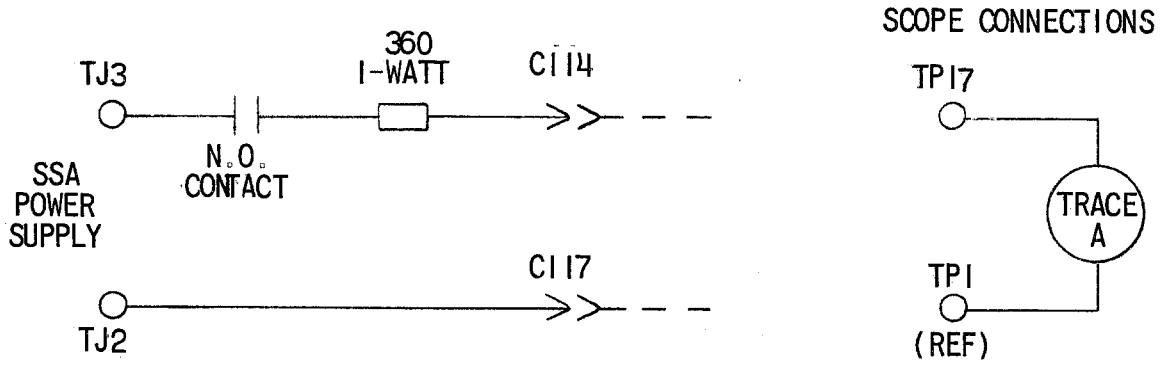


FIG. 6 (0208A5504-1 AJ) Isolation Interface Circuit

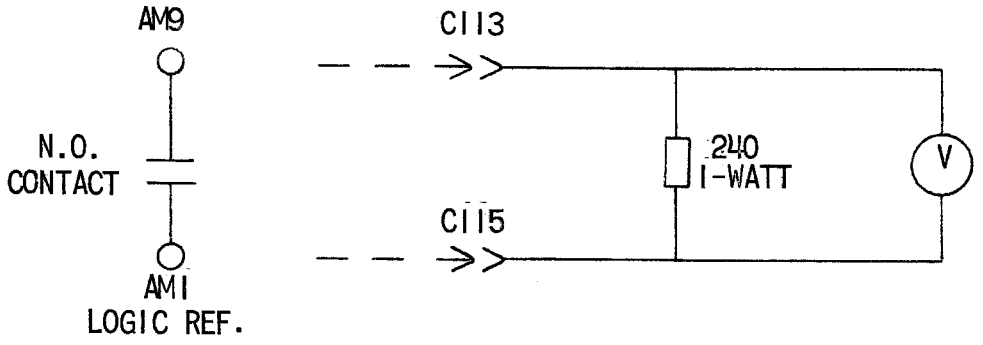


* THE 15VDC SIGNAL AT PIN 10 HAS A CURRENT LIMITING RESISTOR MOUNTED ON THE TEST CARD.

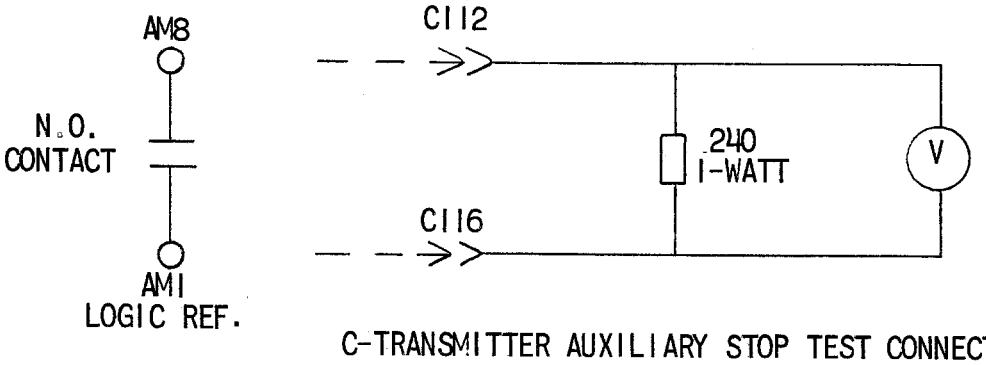
FIG. 7 (0246A7987-0) Logic Timer Test Circuits



A-RECEIVED CARRIER TEST CONNECTIONS



B-TRANSMITTER CONTROL TEST CONNECTIONS



C-TRANSMITTER AUXILIARY STOP TEST CONNECTIONS

FIG. 8 (0257A6244-0) Isolation Interface Test Circuit

GENERAL ELECTRIC COMPANY
POWER SYSTEMS MANAGEMENT BUSINESS DEPT.
PHILADELPHIA, PA. 19142

GENERAL ELECTRIC

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