STATIC AUXILIARY LOGIC RELAY

TYPE SLA54D

CONTENTS

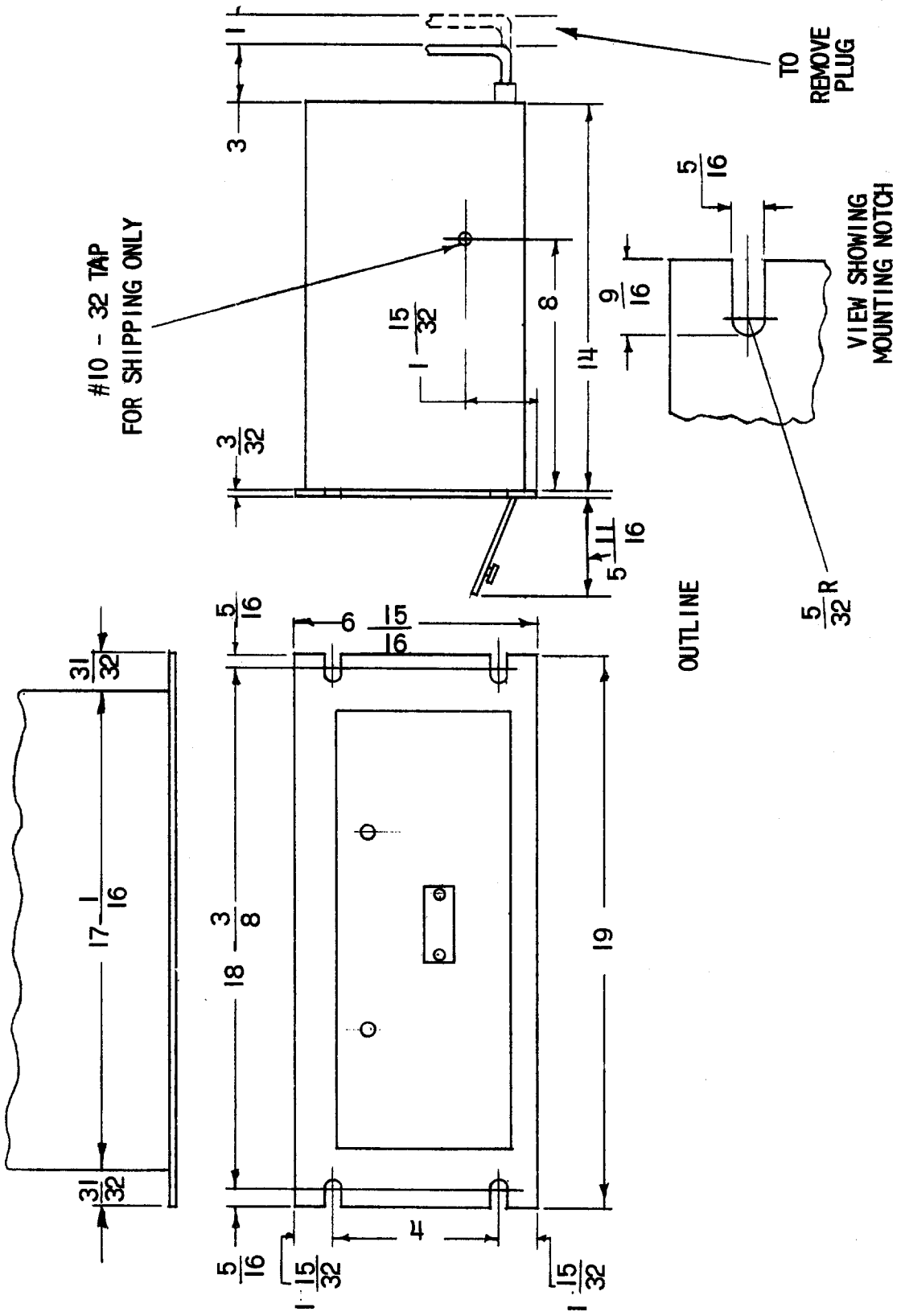


FIG. 1 (0227A2037-0) OUTLINE AND MOUNTING DIMENSIONS

STATIC AUXILIARY LOGIC RELAY

TYPE SLA54D

DESCRIPTION

The type SLA54D is a static auxiliary logic relay that was designed for use in a permissive overreaching transferred trip or directional comparison unblocking scheme via a frequency shift type channel. The relay is not intended for use by itself, but rather as part of a complement of equipment that forms a complete relaying scheme.

The SLA54D relay is packaged in a four rack unit (one rack unit = 1 3/4 inch) enclosed metal case suitable for mounting in a 19 inch rack. The outline and mounting dimensions are shown in Fig. 1. The internal connections for the relay are shown in Fig. 2. The component and card locations are shown in Fig. 3.

APPLICATION

The SLA54D relay is a static auxiliary logic relay that was designed to operate in a permissive overreaching transferred trip or directional comparison unblocking scheme via a frequency shift type channel. Appropriate phase and ground relays of the type SLY and SLYG plus a suitable type SSA power supply, a type SLC overcurrent relay, and an auxiliary output and tripping relay of the type SLAT are required to complete the scheme.

In addition to the basic logic that is required for implementation of the scheme, certain optional features are also available. For example, out-of-step blocking and out-of-step tripping logic can be provided. Provisions are also available for the addition of direct trip phase and ground overcurrent functions. These options can be provided initially with the equipment or they can be easily added at a later date. A number of logic points are brought out of the SLA54D for monitoring via a data logging amplifier (DLA). These points are designated by the cable terminations 412-430. Also included may be a number of contact converters which are used for converting external contact operations into compatible logic signals.

For a complete description of the application of this relay in a particular scheme, and of the options provided with the scheme, please refer to the logic option chart and the overall logic diagram and description supplied with the terminal.

RATINGS

The type SLA54D relay is designed for use in an environment where the air temperature outside the relay case does not exceed - 20^{o}C or +65^{o}C.

The type SLA54D relay requires $\pm$15 VDC power source which can be obtained from a Type SSA power supply.

Each contact converter in this relay has a link for selecting the proper voltage for the coil circuit of the contact converter. The three possible voltages are 48 VDC, 125 VDC, and 250 VDC.

The ratings of the reed relays used for received trip indication are listed in Table I.

TABLE I

ABSOLUTE MAXIMUM RATINGS	
100VA Resistive 35VA Inductive*	Interruption Capacity
3 Amperes make and carry continuous	
3 Amperes make and carry short time	

*The inductive rating is based on the inductance of a coil having a X_L/R ratio of 3 to 1.

BURDENS

The SLA54D relay presents a burden of 300 millamperes to the +15 VDC supply and 20 milliamperes to the -15 VDC supply of the type SSA power supply.

Each contact converter, when energized, will draw approximately 10 milliamperes from the station battery, regardless of tap setting.

OPERATING PRINCIPLES

LOGIC CIRCUIT

The functions of the type SLA54D relay involve basic logic (AND, OR, and NOT) where the presence or absence of signals, rather than their magnitudes, controls the operation. Signals are measured with respect to a reference bus accessible at TP1. In general, a signal below one VDC represents an OFF or LOGIC ZERO condition; an ON or LOGIC ONE condition is represented by a signal of approximately +15 VDC.

The symbols used on the internal connection diagram (Fig. 2) are explained by the legend shown in Fig. 4.

The matrix block options shown in the internal connections of the SLA54D relay are provided at the factory. The connections are shown on the associated overall logic and are listed on the associated option chart. A typical option chart is shown in Fig. 5.

CONTACT CONVERTERS

The purpose of this function is to convert a contact operation into a signal that is compatible with the logic circuit of the Type SLA54 relay. The contact converters are labeled CC1 through CC6. Refer to the logic description for the particular scheme for information concerning the use of each contact converter.

DATA MONITORING POINTS

Optional data monitoring points can be brought out from the matrix block to plugs mounted at the rear of the SLA54D relay. Each plug contains nine monitoring points and reference. The optional monitoring points on the matrix block are listed on the option chart which represents the factory wiring configuration for the relay options. Changes in selection of monitored points may be easily made, but this must be done inside the relay.

To monitor these points, an additional piece of equipment, termed a Data Logging Amplifier (DLA), is required. The DLA is connected to the SLA54D relay with 10 conductor shielded cables. These cables are not supplied unless the DLA unit is ordered.

CHANNEL INTERFACE

The logic of the Type SLA54D relay includes an isolation interface (Fig. 6) between the relays in the scheme and the associated channel. The circuitry of the isolation interface provides a signal path but maintains metallic isolation. This feature makes it possible to maintain isolation between the DC supply used for the relays and that employed by the channel.

SETTINGS

There are nine timers in the SLA54D that may require field adjustment.

TL1 is part of the out-of-step detection scheme. This timer is used to measure the time of travel between the outer and inner characteristic. An out-of-step condition will be detected when TL1 and the C/16 timer in the associated SLY are adjusted properly.

TL2 provides the necessary coordination to prevent relay false tripping which might otherwise result from a current reversal during the clearing of a parallel line fault. This timer can be bypassed by jumpers if not required.

TL3 forms part of the "b" switch keying with repeat circuitry. This timer is factory set to the times shown on the logic diagram and should not require further adjustment.

TL4 is the zone two back-up timer (TU2). This timer must be set such that coordination with corresponding phase and ground Zone One protection is obtained. This timer is an optional feature.

TL5 is part of the out-of-step tripping logic. This timer is factory set to the times shown on the logic diagram and should not require further adjustment.

TL6 is the trip integrator timer. The pickup delay provides coordination between the receiver input and the trip function input to the comparer. The reset delay continues keying the transmitter to insure that remote relay has ample time to operate.

TL7 is used to coordinate the operation of the circuit breaker "b" switch with the operation of the main poles of the breaker for keying the channel transmitter. This timer is an optional feature

TL8 serves the same purpose as TL4 and is used in those applications where separate timers are required for phase and ground back-up protection.

TL9 is required in some schemes to provide additional coordinating delay between the trip function input and the receiver input to the comparer.

Further details for determining the setting of these timers can be found in the logic description provided with each static relaying scheme.

CONSTRUCTION

The SLA54D relay is packaged in an enclosed metal case with hinged front covers and removable top cover. The outline and mounting dimensions of the case and the physical location of the components are shown in Figs. 1 and 3 respectively.

The SLA54D relay contains printed circuit cards identified by a code number such as A117, T102, L104, where A designates auxiliary function, T designates time-delay function, and L designates logic function. The printed circuit cards plug in from the front of the unit. The sockets are marked with letter designations or "addresses" (D, E, F, etc.) which appear on the guide strips in front of each socket, on component location drawing, on the internal connection diagram and on the printed circuit card. The test points (TP1, TP2, etc.) shown on the internal connection diagram are connected to instrument jacks on a test card in positions T and AT with TP1 at the top of the AT card. TP10 is tied to +15 VDC through a 2.2K resistor. This resistor limits the current when TP10 is used to supply a logic signal to a card.

The logic options are selected by means of taper tip jumpers and matrix blocks. These matrix blocks are located in the rear of the unit as shown in Fig. 3. The red (R), green (G), orange (OR), violet (V), and white (W) matrix blocks each have 20 individual matrix points. The yellow (Y) blocks have 20 points which are grouped in 10 common points; 1 to 10 are tied to +15 VDC, 11 to 20 are tied to reference. There are two yellow blocks in the SLA54D. The connections to both are identical and the option connections are interchangeable.

RECEIVING, HANDLING AND STORAGE

The SLA54D relay will normally be supplied as a part of a static relay equipment, mounted in a rack or cabinet with other static relays and test equipment. Immediately upon receipt of a static relay equipment, it should be unpacked and examined for any damage sustained in transit. If injury or damage resulting from rough handling is evident, file a damage claim at once with the transportation company and promptly notify the nearest General Electric Sales Office.

Reasonable care should be exercized in unpacking the equipment. If the equipment is not to be installed immediately, it should be stored indoors in a location that is free from moisture, dust, metallic chips, and severe atmospheric contaminants

Just prior to final installation the shipping support bolt should be removed from each side of all relay units to facilitate possible future unit removal for maintenance. These shipping support bolts are approximately eight inches back from the relay front panel. WARNING: STATIC RELAY EQUIPMENT, WHEN SUPPLIED IN SWING RACK CABINETS, SHOULD BE SECURELY ANCHORED TO THE FLOOR OR TO THE SHIPPING PALLET TO PREVENT THE EQUIPMENT FROM TIPPING OVER WHEN THE SWING RACK IS OPENED.

TEST INSTRUCTIONS

CAUTION

THE LOGIC SYSTEM SIDE OF THE DC POWER SUPPLY USED WITH MOD 111 STATIC RELAY EQUIPMENT IS ISOLATED FROM GROUND. IT IS A DESIGN CHARACTERISTIC OF MOST ELECTRONIC INSTRUMENTS THAT ONE OF THE SIGNAL INPUT TERMINALS IS CONNECTED TO THE INSTRUMENT CHASSIS. IF THE INSTRUMENT USED TO TEST THE RELAY EQUIPMENT IS ISOLATED FROM GROUND, ITS CHASSIS MAY HAVE AN ELECTRICAL POTENTIAL WITH RESPECT TO GROUND. THE USE OF A TEST INSTRUMENT WITH A GROUNDED CHASSIS WILL NOT AFFECT THE TESTING OF THE EQUIPMENT. HOWEVER, A SECOND GROUND CONNECTION TO THE EQUIPMENT, SUCH AS A TEST LEAD INADVERTENTLY DROPPING AGAINST THE RELAY CASE, MAY CAUSE DAMAGE TO THE LOGIC CIRCUITRY. NO EXTERNAL TEST EQUIPMENT SHOULD BE LEFT CONNECTED TO THE STATIC RELAYS WHEN THEY ARE IN PROTECTIVE SERVICE, SINCE TEST EQUIPMENT GROUNDING REDUCED THE EFFECTIVENESS OF THE ISOLATION PROVIDED.

IF THE SLA54D RELAY THAT IS TO BE TESTED IS INSTALLED IN AN EQUIPMENT WHICH HAS ALREADY BEEN CONNECTED TO THE POWER SYSTEM, DISCONNECT THE OUTPUTS IN THE ASSOCIATED TYPE SLAT RELAY FROM THE SYSTEM DURING TEST.

GENERAL

The SLA54D relay is supplied from the factory either as a separate unit, or mounted in a static relay equipment associated with measuring relays, a Type SSA power supply, and some form of channel equipment. All relay units for a given terminal of static relaying equipment are tested together at the factory and each unit will have the same summary number stamped on its nameplate.

In general, when a time range is indicated on the internal connection diagram, the timer has been factory set at a mid-range value. Timers should be set for the operating or reset times indicated on the associated overall logic diagram. Where a time range is indicated on the overall logic diagram, the timer should be set for the value recommended for that function in the descriptive write-up accompanying the overall logic diagram. Where a setting depends upon conditions encountered on a specific application, that is so stated and the factors influencing the choice of setting are described. The procedure for checking and setting the timers is described in a later section.

OPERATIONAL CHECKS

Operation of the SLA54D unit can be checked by observing the signals at the twenty test points (TP1 to TP20), or by observing the output functions in the associated type SLAT tripping relay. The test points are located on two test cards in position T and AT, and are numbered 1 to 20 from top to bottom. TP1 is the reference bus for the logic circuit; TP10 is at +15 VDC, and TP2 is at -15 VDC. The remaining points are located at various strategic points throughout the logic as shown on the internal connection diagram (Fig. 2). Test point voltages can be monitored with a portable high impedance voltmeter, the voltmeter on the test panel of the associated equipment, or an oscilloscope.

TEST CARD ADAPTER

The test card adapter provides a convenient means of gaining access to any pin of a particular card. Detailed information on the use of the test adapter card is included in the card instruction book GEK-34158.

TIMER ADJUSTMENTS AND TESTS

When the time-delay cards are to be adjusted or checked, an oscilloscope that can display two traces simultaneously and that has a calibrated horizontal sweep, should be used.

In order to test the time cards it is necessary to remove the card ahead of the timer (see Table 2) and to place the timer card in a card adapter. The card adapter allows access to the input and output of the timer if they are not brought out on test points. The timer test circuit is shown in Fig. 7. Opening the normally closed contact causes the output to step up to +15 VDC after the pickup delay of the timer. To increase the pickup time turn the upper potentiometer on the timer card clockwise; to decrease the time turn it counterclockwise. Closing the contact causes the timer output to drop out after the reset time-delay setting of card. If the timer card is provided with a variable reset delay, it can be adjusted by the lower potentiometer on the timer card (clockwise increases reset time).

TABLE 2

TIMER	CARD	RANGE	POSITION	REMOVE CARD IN POSITION
TL1	T102	10-80/10-80	AG	AF
**TL2	T103	2-16/0	G	F
TL3	T102	10-80/10-80	R	P
**TL4	T104	0.1-2 SEC/0	AN	***
TL5	T105	1-8/10-80	AJ	C
TL6	T118	1-8/10-80	K	J
**TL7	T125	25-200/25-200	AE	AC
**TL8	T104	0.1-2 SEC/0	N	***
**TL9	T104 or T111	0.1-2 SEC/0 or 1-8/0	AS	***

**When supplied
***Depends upon matrix block connections

CONTACT CONVERTER TESTS

Operation of the contact converters can be checked by placing the contact converter card in a card adapter after checking that the voltage tap selected agrees with the station battery voltage. Connect the station DC through a switch to the appropriate pair of terminals of the terminal strip, AH and AJ, mounted on the rear of the relay. The terminal numbers and polarity of connections for each of the six contact converters are shown in the internal connection diagram, Fig. 1. Output of the contact converter card may be monitored between pin 8 or pin 9 and pin 1 depending on which contact converter is being tested, with either a scope or a meter. Closure of the switch in the test source will provide a +15 DC signal at pin 8 of the card adapter.

ISOLATION INTERFACE TESTS

Operation of the isolation interface can be checked without direct connections to the subassembly. External test connections are made to the pins of the C111 socket mounted on the rear of the unit; see Fig. 3. Logic circuit test connections are made at the socket pins of the channel control card in position "L".

Receiver test connections are shown in Fig. 8A. For this test place the channel control card in the test adapter card to gain access to the card socket pins. Closure of the normally open contact will simulate a received carrier signal and scope display will go from a logic "0" to a logic "1".

For the transmitter control test, remove the channel control card "L" from its socket and replace it with a test card adapter and test card to gain access to the "L" socket pins. Transmitter control test connections are shown in Fig. 8B. The test contact in the open position simulates a logic "1" condition

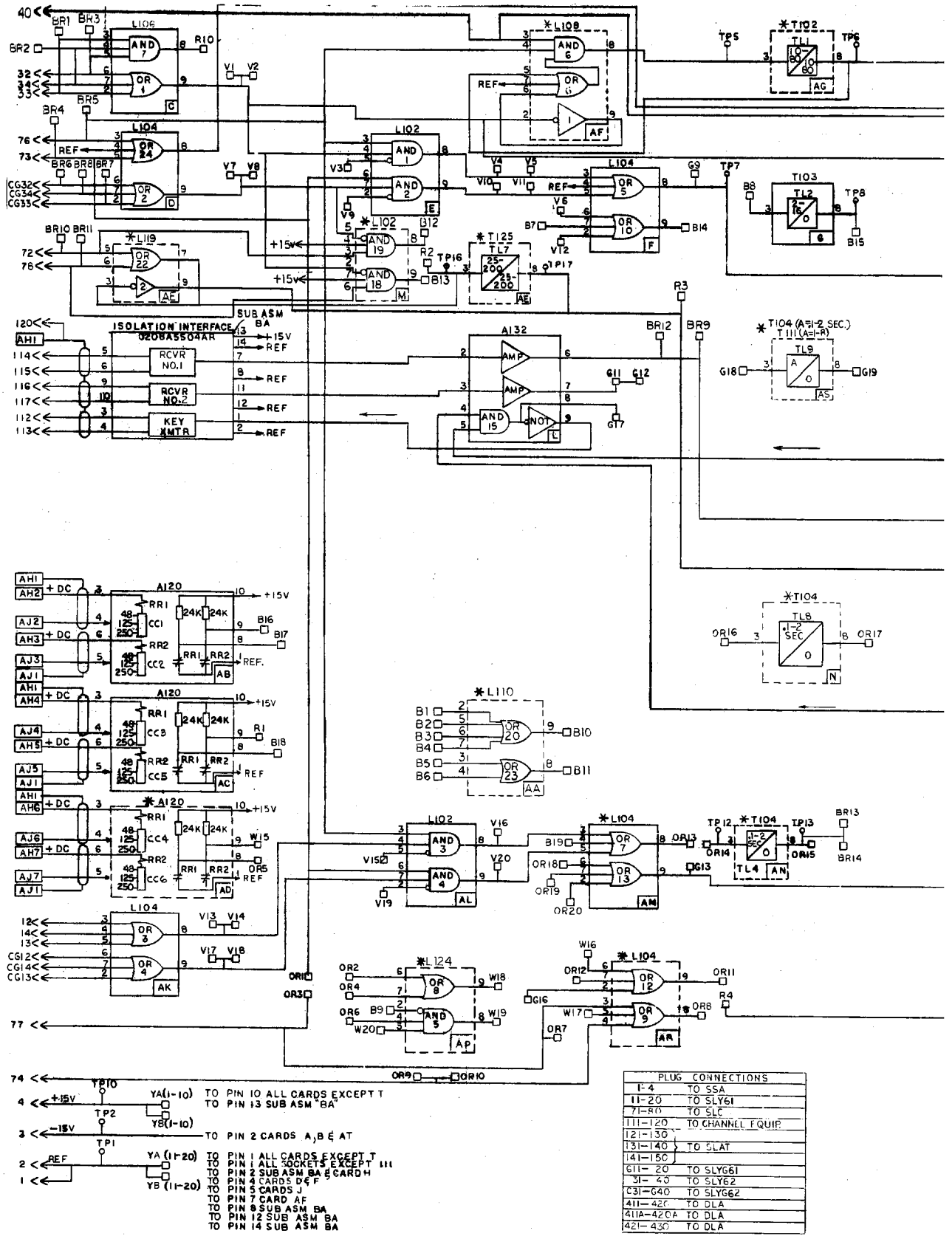
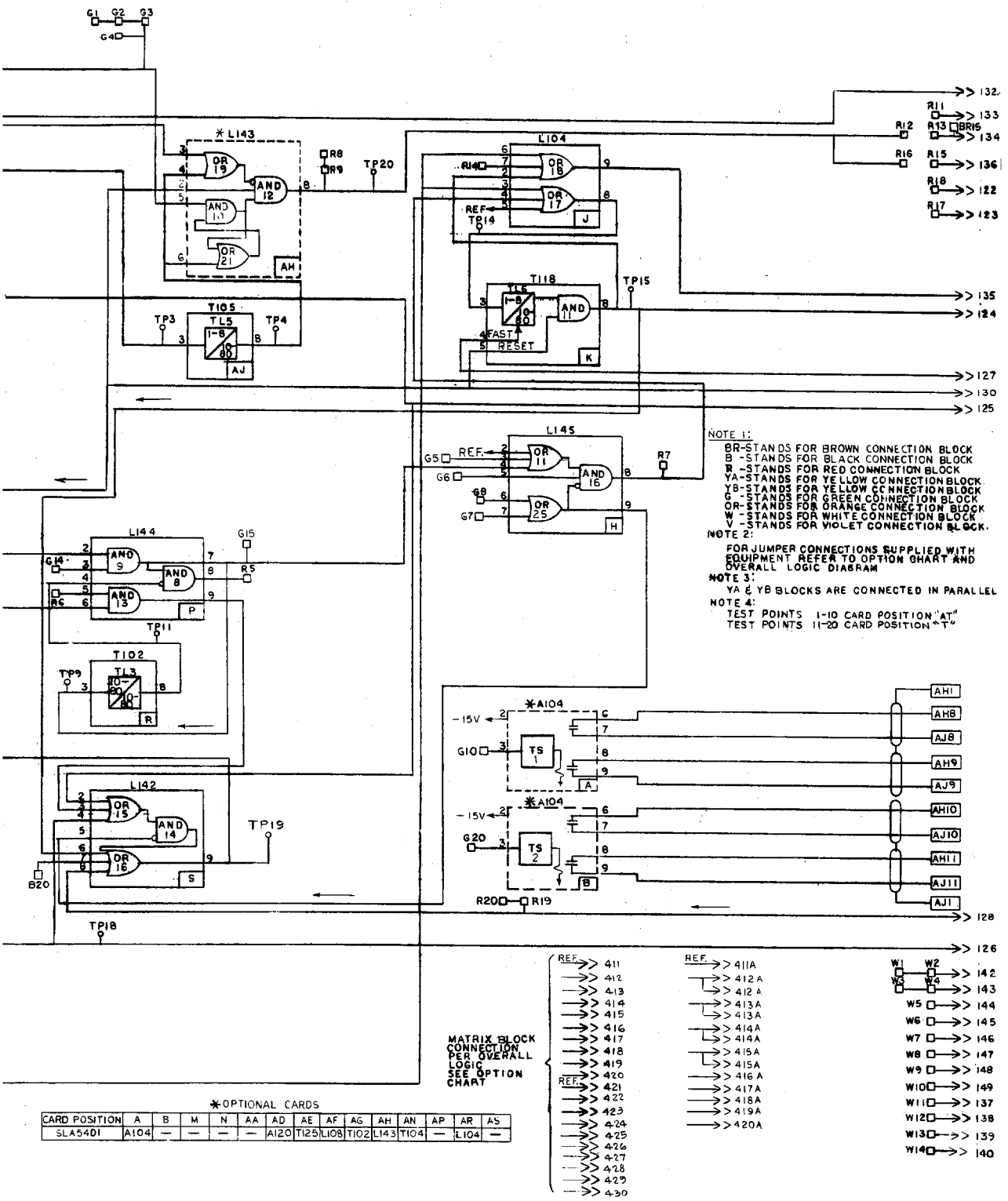


FIG. 2 (0136D4032-0) INTERNAL CO



*OPTIONAL CARDS

CARD POSITION	A	B	M	N	AA	AD	AE	AF	AG	AH	AN	AP	AR	AS
SLA54D1	A104	—	—	—	—	A120	T125	L108	T102	L143	T104	—	L104	—

which holds off the transmitter control output of the isolation interface. Closure of the normally open contact generates a logic "0" condition initiating a transmitter control output producing a 5-6 volt DC signal across the output loading resistor.

OVERALL EQUIPMENT TESTS

After the SLA54D relay and the associated static relay units have been individually calibrated and tested for the desired settings, a series of overall operating circuit checks is advisable.

The elementary, overall logic, and logic description for the specific job will be useful for determining the overall operation of the scheme.

Overall equipment tests can be performed by applying AC current and voltages to the measuring units as specified in the instruction book for the measuring units and checking that proper outputs are obtained from the associated SLAT when the measuring units operate.

MAINTENANCE

PERIODIC TESTS

It should be sufficient to check the outputs produced at test points in the SLA54D relay when periodic calibration tests are made on the associated measuring units, for example, the phase and ground relays in line relaying scheme. No separate periodic tests on theSLA54D itself should be required.

TROUBLE SHOOTING

In any trouble shooting of equipment, it should first be established which unit is functioning incorrectly. The overall logic diagram supplied with the equipment shows the combined logic of the complete equipment and the various test points in each unit. By signal tracing, using the overall logic diagram and the various test points, it should be possible to quickly isolate the trouble.

A test adapter card is supplied with each static relay equipment to supplement the pre-wired test points on the test cards. Use of the adapter card is described in the card instruction book GEK-34158.

A dual-trace oscilloscope is a valuable aid to detailed trouble shooting, since it can be used to determine phase shift, operate and reset times as well as input and output levels. A portable dual-trace oscilloscope with a calibrated sweep and trigger facility is recommended.

SPARE PARTS

To minimize possible outage time, it is recommended that a complete maintenance program should include the stocking of at least one spare card of each type. It is possible to replace damaged or defective components on the printed circuit cards, but great care should be taken in soldering so as not to damage or bridge-over the printed circuit busses, or overheat the semiconductor components. The repaired area should be recovered with a suitable high-dielectric plastic coating to prevent possible breakdowns across the printed busses due to moisture and dust. The wiring diagrams for the cards in the SLA54D relay are included in the card book GEK-34158.

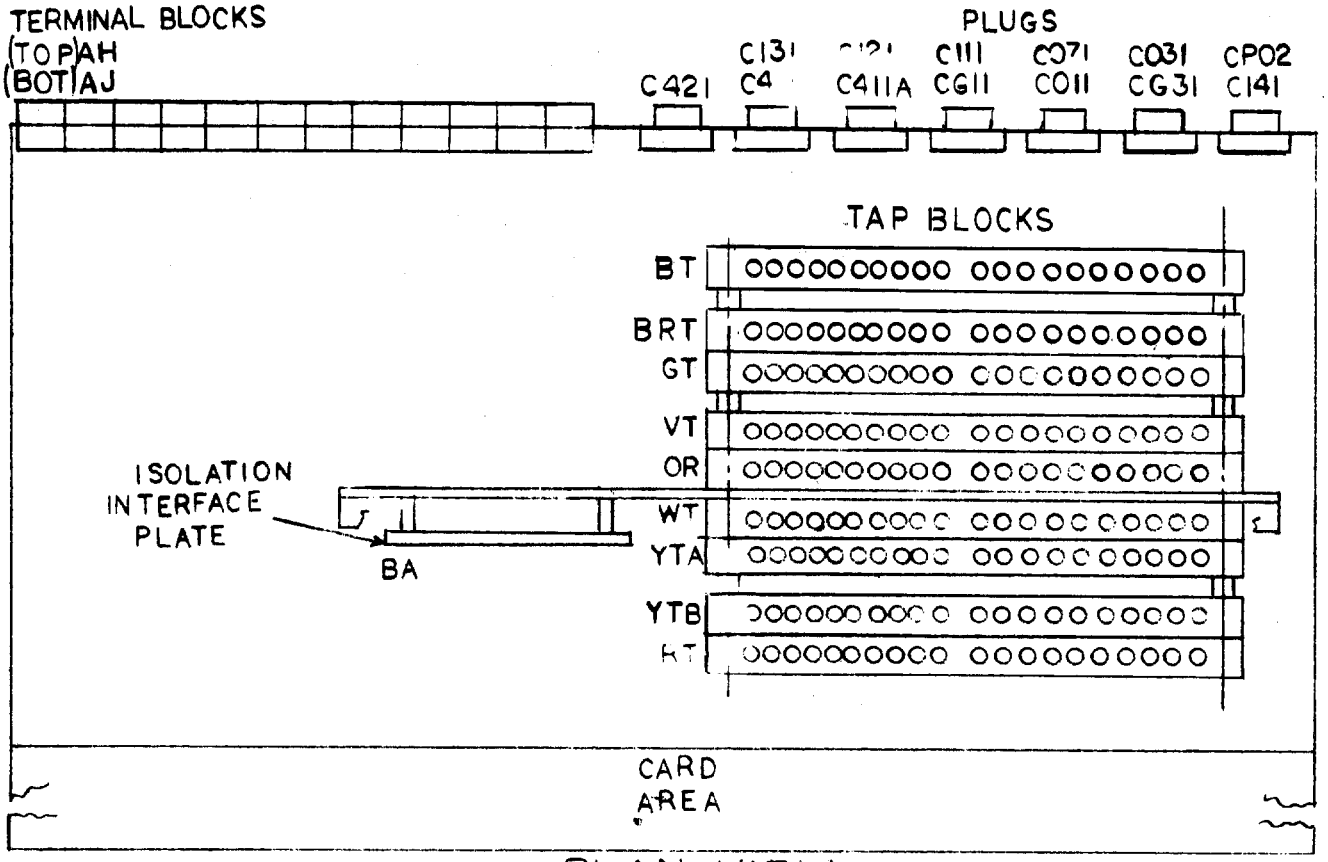


FIG. 3 (0275A1940-0) COMPONENT LOCATION DIAGRAM

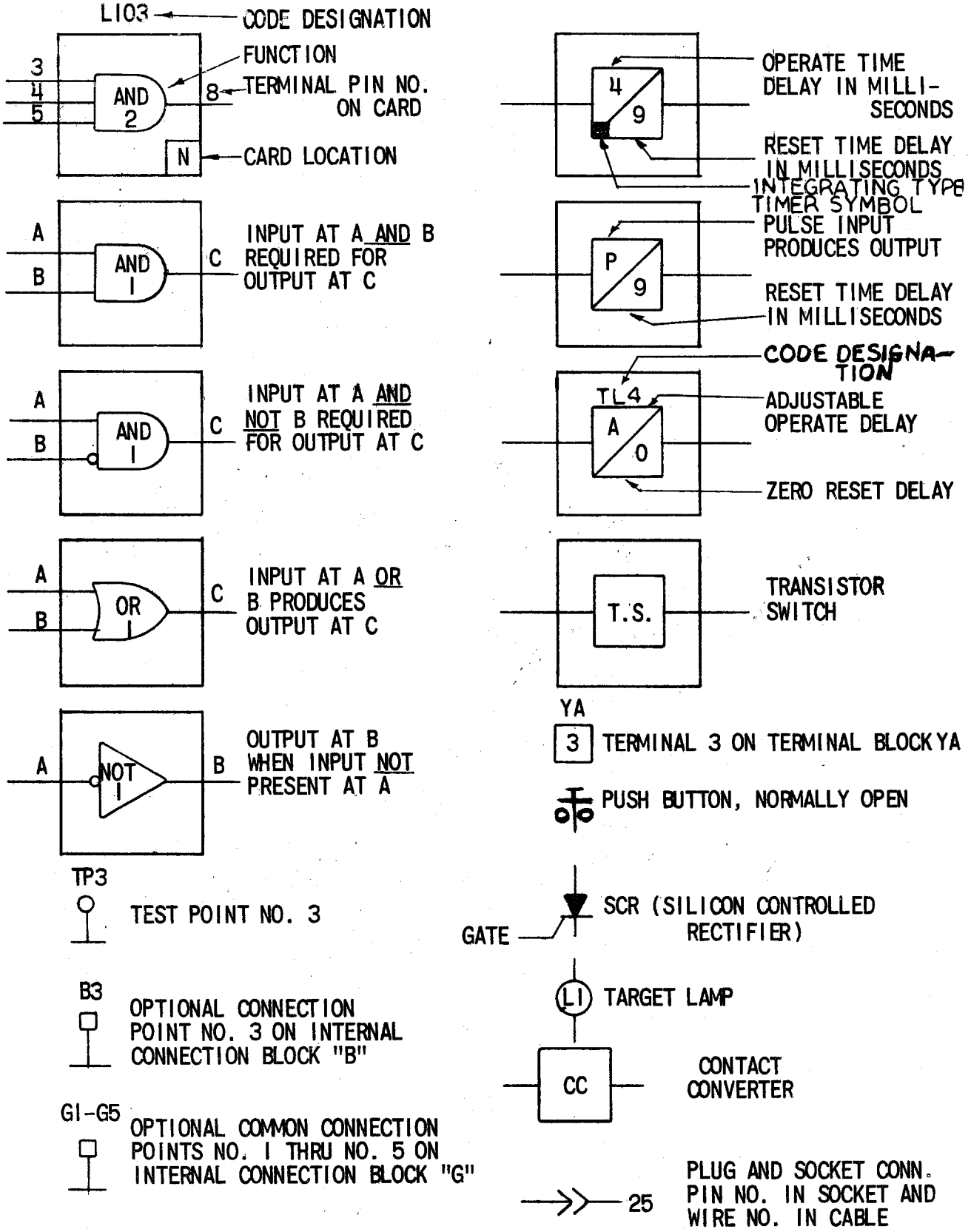


FIG. 4 (0227A2047-1) LOGIC AND INTERNAL CONNECTION DIAGRAM LEGEND

THE FOLLOWING ARE FACTORY CONNECTIONS MADE AT THE MATRIX BLOCKS INSIDE OF THE SLA RELAY ASSOCIATED WITH THIS EQUIPMENT.

SYMBOLS LISTED: PL=RELAY INTERCONNECTING CABLE LEAD
(5)=LOGIC FUNCTION CARD PIN NUMBER
‡=3-WAY CONNECTION
✳=DLA MONITOR CONNECTION AVAILABLE BUT NOT USED
†=DOUBLE JUMPER
Δ=DOUBLE DLA LEAD

147

MATRIX BLOCK JUMPERS		LOGIC FUNCTION	
FROM	TO	FROM	TO
R10	G10	AND7(8)	TS1 (3)
OR7	W14	PL77	PL140
OR10	W10	PL74	PL149
V11	V12	AND2(9)	OR10(2)
W2	W13	PL142	PL139
G1	R15	TL1 (8)	PL136
G2	V3	TL1(8)	AND1(5)
G3	V15	TL1(8)	AND3(5)
V5	V6	AND1(8)	OR10(6)
W4	W11	PL143	PL137
G9	B8	OR5(8)	TL2(3)
G9	OR14	OR5(8)	TL4(3)
B15	B7	TL2(8)	OR10(7)
B14	G6	OR10(9)	AND16(5)
OR13	W17	OR7(8)	OR9(5)
OR8	OR20	OR9(8)	OR13(2)
OR8	R4	OR9(8)	OR17(3)
B18	G5	CC3(8)	OR11(3)
R1	R2	CC5(9)	TL7(3)
R5	R6	AND8(8)	AND13(5)
B16	G7	CC2(9)	OR25(7)
B17	B20	CC1(8)	OR16(7)
R8	R11	AND12(8)	PL133
R9	W5	AND12(8)	PL144
OR15	OR18	TL4(8)	OR13(6)
BR13	W12	TL4(8)	PL138
R20	R13	PL128	PL134
V19	YA11	AND4(2)	REF
B19	YA12	OR7(4)	REF
V9	YA13	AND2(2)	REF
OR19	YA14	OR13(7)	REF
R14	YA15	OR18(7)	REF
R18	YA16	PL122	REF
R17	YA17	PL123	REF
G8	YA18	OR25(8)	REF
W6	YA1	PL145	+15

MATRIX BLOCK JUMPERS		LOGIC FUNCTION	
FROM	TO	FROM	TO
W8	YA2	PL147	+15
G14	YA3	AND9(3)	+15
BR3	412	CO32	PL412
G4	413	TL1(8)	PL413
BR15	415	PL134	PL415
BR1	417	CO33	PL417
BR2	418	CO34	PL418
BR6	419	CG32	PL419
BR7	420	CG33	PL420
BR8	422	CG34	PL422
BR12	423	RCVR1	PL423
R19	427	PL128	PL427
BR14	428	TL4(8)	PL428
OR5	429	CC4(8)	PL429
W15	430	CC6(9)	PL430
V4	412A	AND1(8)	PL412A
Δ W3	412A	PL143	PL412A
V10	413A	AND2(9)	PL413A
Δ W1	413A	PL142	PL413A
V16	414A	AND3(8)	PL414A
Δ W7	414A	PL146	PL414A
V20	415A	AND4(9)	PL415A
Δ W9	415A	PL148	PL415A
OR3	416A	PL77	PL416A
OR9	417A	PL74	PL417A
R16	418A	AND12(8)	PL418A

FIG. 5 (0227A2050-0 Sh. 147) SAMPLE OPTION CHART

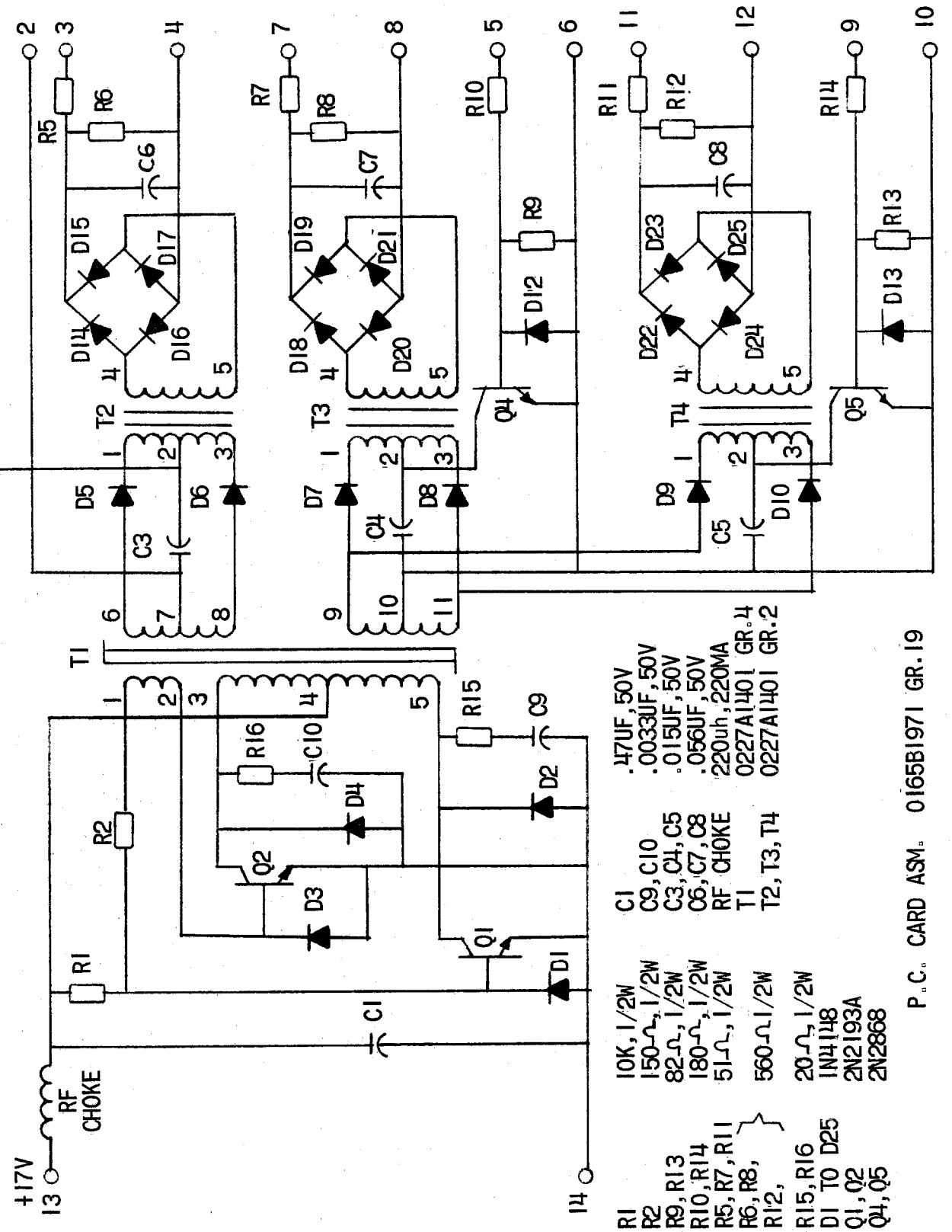
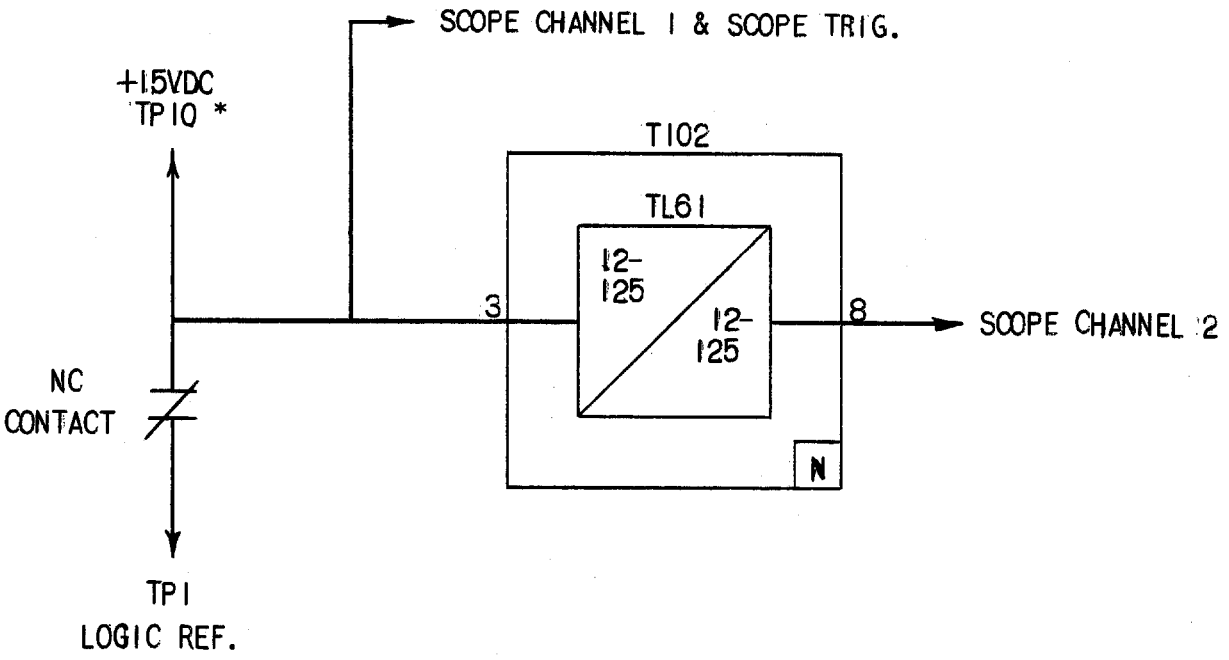
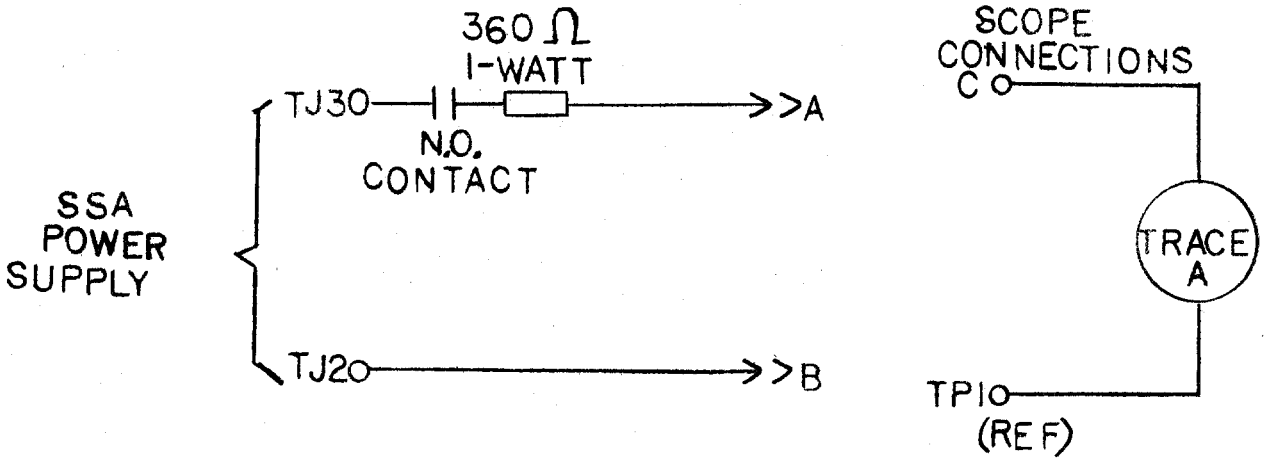


FIG. 6 (0208A5504AR-0) ISOLATION INTERFACE CIRCUIT



* THE 15VDC SIGNAL AT PIN 10 HAS A CURRENT LIMITING RESISTOR MOUNTED ON THE TEST CARD.

FIG. 7 (0246A7987-0) LOGIC TIMER TEST CIRCUIT



TEST	CONNECTIONS				RESULTS
	A	B	C		
			CARD	PIN	
RECEIVED TRIP RCVR NO 1	C114	C115	L	6	CLOSURE OF THE N.O. CONTACT WILL SIMULATE A RCVR. INPUT AND THE SCOPE DISPLAY WILL GO FROM LOGIC "O" TO LOGIC "1"
RECEIVED TRIP RCVR NO 2	C116	C117	L	7	

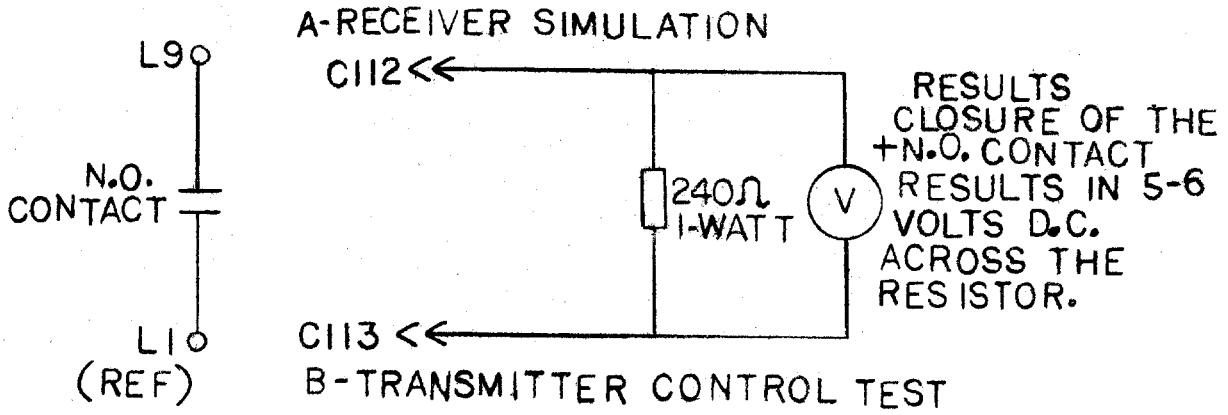


FIG. 8 (0275A2078-0) ISOLATION INTERFACE TEST CONNECTIONS