INSTRUCTIONS

GEK-49914A
Superseding GEK-49914

SOLID-STATE AUXILIARY LOGIC RELAY

FOR

TRANSMISSION LINE PROTECTION

TYPE SLA51N

GENERAL ELECTRIC

CONTENTS

SOLID-STATE AUXILIARY LOGIC RELAY FOR TRANSMISSION LINE PROTECTION

TYPE SLA51N

DESCRIPTION

The SLA51N relay is an auxiliary logic relay designed to be used in a directional comparison ON-OFF carrier scheme. The relay contains the necessary logic to interpret output signals from associated measuring functions and translate them to an appropriate output and tripping relay. To complete a particular relaying scheme, in addition to the SLA51N relay, appropriate ground and phase relays plus a power supply and auxiliary tripping relay are required .

Internal connections for the SLA51N relay are shown in Figure 1 (for relay Forms 1 through 49) and Figure 2 (for relay Forms 50 and up). Component and card locations are shown in Figure 3.

The Type SLA51N relay is packaged in a four-rack unit (4RU) enclosed metal case. The relay is suitable for mounting in a 19-inch rack. The mounting and outline dimensions are shown in Figure 4.

APPLICATION

The SLA51N relay is designed to operate in conjunction with appropriate phase and ground relays in a directional comparison ON-OFF blocking scheme, using a Type CS26B power-line carrier as the pilot channel. The SLA51N includes circuits to accommodate the use of first- and second-zone phase and ground distance backup protection with the blocking directional comparison scheme. An isolated interface provides the interconnection between the SLA51N logic and the transmitter and receiver of the pilot channel.

Considerable variations in required protection features exist among different relay schemes. It is sometimes desirable to provide certain features initially with the scheme, or provide features that may be added at a later date in the field. To this end, the SLA51N design has incorporated circuit flexibility to permit implementation of certain optional features.

For the specific options and the logic arrangement supplied with a particular scheme, refer to the logic diagram and logic descriptive text supplied with that scheme. If it is desired to make logic changes at a later date, the diagrams and instruction books supplied with a particular scheme should be studied to determine the means for implementing the changes. If, after study of the diagrams, further assistance is required, contact the nearest General Electric District Sales Office.

Various points in the logic can be monitored by providing jumpers from any of the available matrix points to plug 411, located on the rear of the SLA51N relay. This option is further described in the paragraph on "Data Monitoring Points", in the OPERATION PRINCIPLES section.

RATINGS

The Type SLA51N relay is designed for use in environments where the air temperature outside the relay case does not drop below -20° C or exceed + 65° C.

The SLA51N relay requires a ± 15 VDC power source, which can be obtained from a Type SSA power supply.

Each contact converter in this relay has a link for selecting the proper voltage for the coil circuit of the contact converter. The three possible voltages are 48 VDC, 125 VDC, and 250 VDC.

BURDENS

The SLA51N relay presents a burden of 400 milliamperes to the + 15 VDC supply of the Type SSA power supply.

Each contact converter, when energized, will draw approximately 10 milliamperes from the station battery, regardless of tap setting.

OPERATING PRINCIPLES

LOGIC CIRCUIT

The functions of the SLA51N relay involve basic logic (AND, OR, and NOT), in which operation is controlled by the presence or absence of signals, rather than their magnitudes. Signals are measured with respect to a reference bus accessible at TP1. In general, a signal below + 1 VDC represents an OFF or LOGIC ZERO condition; an ON or LOGIC ONE condition is represented by a signal of approximately + 15 VDC.

The symbols used in the internal-connections diagrams (Figures 1 and 2) are explained in Figure 5.

The matrix block options shown in the internal connection diagrams are provided at the factory. The connections are shown in the associated overall logic and listed in the associated option chart. A sample option chart for the Type SLA51N relay is shown in Figure 6.

CONTACT CONVERTERS

The purpose of a contact converter is to convert a contact operation into a signal that is compatible with the logic circuit of the Type SLA51N relay. The contact converters, labeled CC1 through CC6 in the internal-connections diagram have a nonadjustable four-millisecond (4 ms) pickup delay. To obtain information on the use of each contact converter refer to the logic description for the particular scheme.

DATA MONITORING POINTS

The Type SLA51N relay has provisions to provide data monitoring outputs. The data monitoring (DLA) points are selected on the matrix blocks and are listed on the option chart. Any matrix-block points that are not used for logic connections may be monitored. Key points in the logic have more than one matrix point to allow both logic and monitoring connections. A data logging amplifier (DLA) relay is used to translate these logic signals into usable outputs.

CHANNEL INTERFACE

The logic of the Type SLA51N relay includes an isolation interface (Figure 7) between the relays in the scheme and the associated channel. The circuitry of the isolation interface provides a signal path but maintains metallic isolation. This feature makes it possible to maintain isolation between the DC supply used for the relays and the DC supply employed by the channel.

When pins 9 and 10 are both connected to relay reference, a metallically separate positive logic signal appears at pin 11 with respect to 12. The output from the isolation interface is a 5 VDC, 20-milliampere signal.

SETTINGS

The SLA51N relay contains timers that may require field adjustment. Refer to the logic description supplied with each scheme for the settings to be made on these timers.

CONSTRUCTION

The SLA51N relay is packaged in an enclosed metal case with hinged front covers and removable top cover. The outline and mounting dimensions of the case are given in Figure 4 and the physical locations of the components are shown in Figure 3 .

The SLA51N relay contains printed-circuit cards identified by a code number such as A102, T102, or L014, where A designates auxiliary function, T designates time-delay function, and L designates logic function. The printed-circuit cards plug in from the front of the unit. The sockets are marked with letter designations, or "addresses", such as D, E, or F, which appear on the guide strips in front of each socket, on the component location drawing, on the internal-connection diagram and printed-circuit card. The test points (TP1, TP2, etc.) shown on the internal-connection diagram are connected to instrument jacks on a test card in position T or AT, with TP1 at the top of the AT card. TP10 is tied to + 15 VDC through a 1.5K resistor. This resistor limits the current when TP10 is used to supply a logic signal to a card.

Other logic options are selected by means of taper-tip jumpers and matrix blocks. These matrix blocks are located in the rear of the unit as shown in Figure 3. The green (G), red (R), black (B), orange (OR), white (W), and violet(V) matrix blocks each have 20 individual matrix points. For example the yellow (Y) block has 20 points grouped in 10 common points; 1 to 10 are tied to + 15 VDC, and 11 to 20 are tied to reference. Tools for inserting and removing taper-tip jumpers are supplied with each relay.

RECEIVING, HANDLING, AND STORAGE

The SLA51N relay is normally supplied as part of a static relay equipment, mounted in a rack or cabinet with other static relays and test equipment. Immediately upon receipt of a static relay equipment, it should be unpacked and examined for any damage sustained in transit. If damage resulting from rough handling is evident, file a damage claim at once with the transportation company and promptly notify the nearest General Electric Sales Office.

Reasonable care should be exercised in unpacking the equipment. If the equipment is not to be installed immediately, it should be stored indoors in a location that is free from moisture, dust, metallic chips, and severe atmospheric contaminants.

Just prior to final installation, the shipping support bolt should be removed from each side of all relay units, to facilitate possible future unit removal for maintenance. These shipping support bolts are approximately eight inches (8") back from the relay front panel.

CAUTION

Static relay equipment, when supplied in swing rack cabinets, should be securely anchored to the floor or shipping pallet to prevent the equipment from tipping over when the swing rack is opened.

TEST INSTRUCTIONS

CAUTION

The logic system of the DC power supply used with MODIII Static Relay Equipment is isolated from ground. It is a design characteristic of most electronic instruments that one of the signal input terminals is connected to the instrument chassis. If the instrument used to test the relay equipment is isolated from ground, its chassis may have an electric potential with respect to ground. The use of a test instrument with a grounded chassis will not affect the testing of the equipment. However, a second ground connection to the equipment, such as a test lead inadvertently dropping against the relay case, may cause damage to the logic circuitry. No external test equipment should be left connected to the static relays when they are in protective service, since test equipment grounding reduces the effectiveness of the isolation provided.

GENERAL

If the SLA51N relay to be tested is installed in equipment that has already been connected to the power system, disconnect the outputs in the associated Type SLAT relay from the system, and leave them disconnected for the duration of the tests.

The SLA51N relay is supplied from the factory either mounted in static relay equipment or as a separate unit with associated measuring relays, a Type SSA power supply, and some form of channel equipment. All relay units for a given terminal of static relay equipment are tested together at the factory, and each unit has the same summary number stamped on its nameplate.

In general, when a time range is indicated on the internal-connections diagram, the timer has been factory set at a mid-range value. Timers should be set for the operating or reset times indicated on the associated overall logic diagram. Where a time range is indicated in the overall logic diagram, the timer should be set for the value recommended for that function in the descriptive text accompanying the overall logic diagram. Where a setting depends upon conditions encountered in a specific application, it is so stated and the factors influencing the choice of setting are described. The procedure for checking and setting the timers is described below, in TIMER ADJUSTMENTS AND TESTS.

OPERATIONAL CHECKS

Operation of the SLA51N unit can be checked by observing the signals at the twenty test points (TP1 to TP20) in the relay, or by observing the output functions in the associated Type SLAT tripping relay. The test points are located on two test cards in positions T and AT, and are numbered 1 to 20 from top to bottom. TP1 is the reference bus for the logic circuit; TP10 is at +15 VDC, and TP2 is at -15 VDC. The remaining points are located at various strategic points throughout the logic, as shown on the internal connections diagram (Figures 1 and 2). Test-point voltages can be monitored with a portable high-impedance voltmeter, the voltmeter on the test panel of the associated equipment, or an oscilloscope.

TEST ADAPTER CARD

The test adapter card provides a convenient means of gaining access to any pin of a particular card. Detailed information on the use of the test adapter card is included in the instruction book GEK-34158.

TIMER ADJUSTMENTS AND TESTS

When the time-delay cards are to be adjusted or checked, an oscilloscope that can display two traces simultaneously and that has a calibrated horizontal sweep should be used.

In order to test the timer cards it is necessary to remove the card connected to the timer's input (see Table I) and to place the timer card in a adapter card. The adapter card allows access to the input and output of the timer if they are not brought out on test points. The timer test circuit is shown in Figure 8. Opening the normally-closed contact causes the output to step up to + 15 VDC after the pickup delay of the timer. To increase the pickup time turn the upper potentiometer on the timer card clockwise; to decrease the time, turn it counterclockwise. Closing the contact causes the timer output to drop out after the reset time-delay setting of the timer card. If the timer card is provided with a variable reset delay, it can be adjusted by the lower potentiometer on the timer card (clockwise increases reset time).

TABLE I

TIMER UNDER TEST	POSITION	REMOVE CARD IN POSITION
TL1, T122 (10-80/10-80)	R	P
TL2, T111 (1-8/0)	AH	(Varies)†
TL3, T118 (1-8/10-80)	G	H
TL4, T102 (10-80/10-80)	L	K
TL5, T104 (0.1-2SEC/0)	AF	(Varies)†
TL6, T104 (0.1-2SEC/0)	AG	(Varies)†
TL7, T104 (0.1-2SEC/0)	AD	(Varies)†
TL8, T118 (1-8/10-80)	N	AM

†Refer to scheme logic diagram and Figure 1or Figure 2 to determine card to remove.

CONTACT CONVERTER TESTS

Operation of the contact converters can be checked by placing the contact converter in an adapter card, after checking that the voltage tap selected agrees with the station battery voltage. Connect the station DC voltage through a switch to the appropriate pair of terminals on the terminal strip, AH, mounted on the rear of the relay. The terminal numbers and polarity of connections for each of the contact converters are shown in the internal connections diagram, Figure 1 or Figure 2. The output of the contact converter card may be monitored between pin 8 and pin 1 (reference) on the adapter card with either a scope or meter. Closure of the switch in the test source will provide a + 15 volt DC signal at pin 8 of the adapter card.

ISOLATION INTERFACE TESTS

Operation of the three functions (received carrier, transmitter control, and transmitter auxiliary stop) of the isolated interface can be checked without direct connections to the subassembly. External test connections are made to the pins of the C111 socket mounted on the rear of the unit (see Figure 1). Logic-circuit test connections are made at the socket pins of the channel control card in position "C".

Received-carrier operation test connections are shown in Figure 9A. For this test, do not remove the channel control card in position "C". Closure of the normally-open contact will simulate a received-carrier signal and the scope display will go from a logic "0" to a logic "1".

For the transmitter-control and transmitter-auxiliary-stop checks, remove the channel control card "C" from its socket and replace it with a test adapter card and test card to gain access to the "C" socket pins. Transmitter-control test connections are shown in Figure 9B. The test contact in the open position simulates a logic "1" condition, which holds off the transmitter-control output of the isolation interface. Closure of the normally-open contact generates a logic "0" condition, which indicates a transmitter-control output, producing a 5-6 VDC signal across the output loading resistor. The transmitter-auxiliary-stop function can be tested in a similar manner using the test connections of Figure 9C; the output will again provide a 5-6 VDC signal across the output loading resistor.

OVERALL EQUIPMENT TESTS

After the SLA51N relay and the associated static relay units have been individually calibrated and tested for the desired settings, a series of overall operating-circuit checks is advisable.

The elementary diagram, overall logic diagram, and logic description for the specific job will be useful for determining the overall operation of the scheme.

Overall equipment tests can be performed by applying AC current and voltages to the measuring units as specified in the instruction book for the measuring units and checking that proper outputs are obtained from the associated SLAT when the measuring units operate.

MAINTENANCE

PERIODIC TESTS

It should be suffient to check the outputs produced at test points in the SLA51N when periodic calibration tests are made on the associated measuring units; for example, when the phase and ground relays in a line relaying scheme are tested. No separate periodic tests on the SLA51N itself should be required.

TROUBLESHOOTING

In any troubleshooting of equipment, it should first be established which unit is functioning incorrectly. The overall logic diagram supplied with the equipment shows the combined logic of the complete equipment and the various test points in each unit. By signal tracing, using the overall logic diagram and the various test points, it should be possible to isolate the trouble quickly.

SPARE PARTS

To minimize possible outage time, it is recommended that a complete maintenance program include the stocking of a least one spare card of each type. It is possible to replace damaged or defective components on the printed-circuit cards, but great care should be taken in soldering so as not to damage or bridge-over the printed-circuit buses, or overheat the semiconductor components. The repaired area should be re-covered with a suitable high-dielectric plastic coating to prevent possible breakdowns across the printed buses due to moisture and dust. The wiring diagrams for the cards in the SLA51N relay are included in the card book, GEK-34158.

LIST OF FIGURES

*Revised since last issue

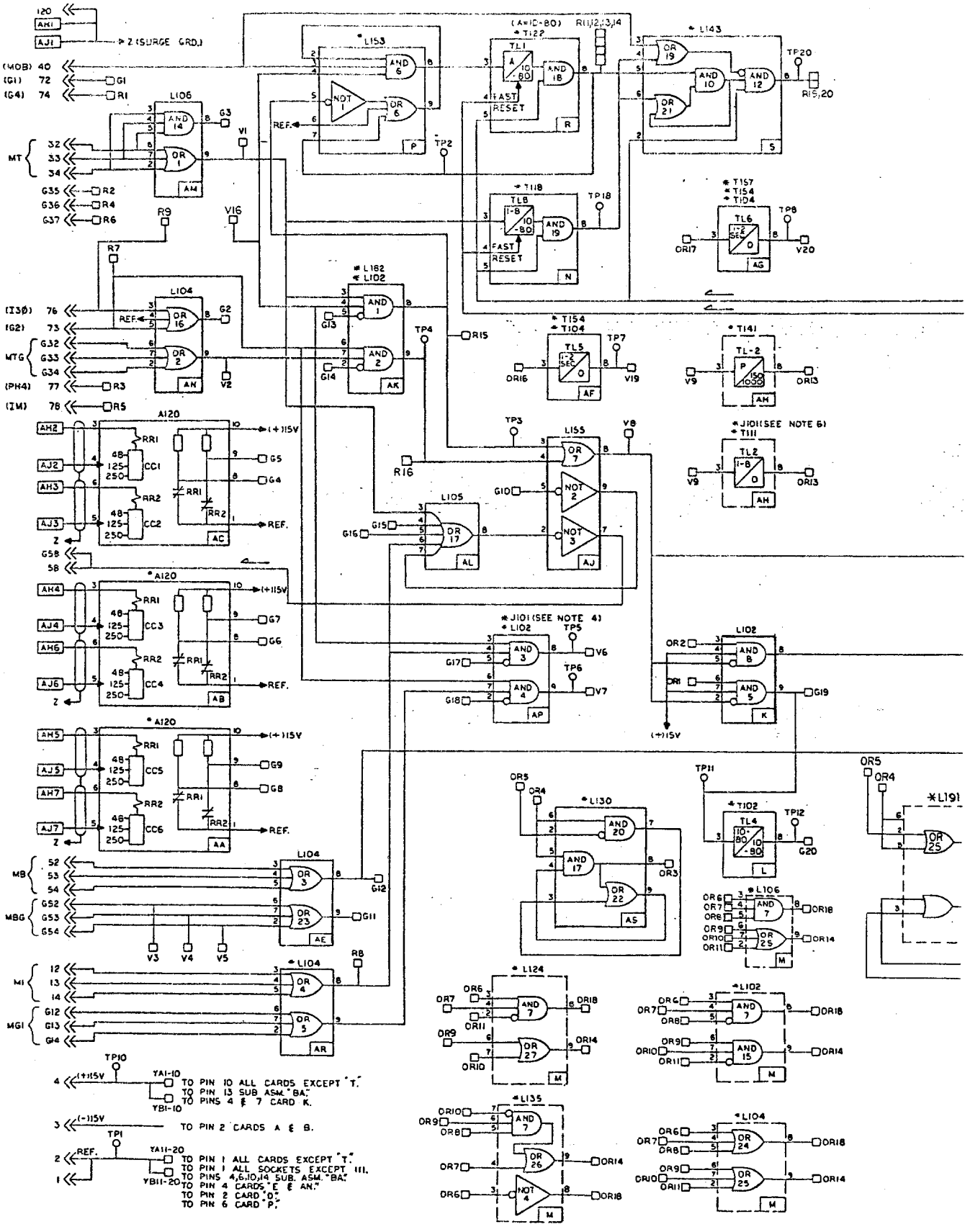
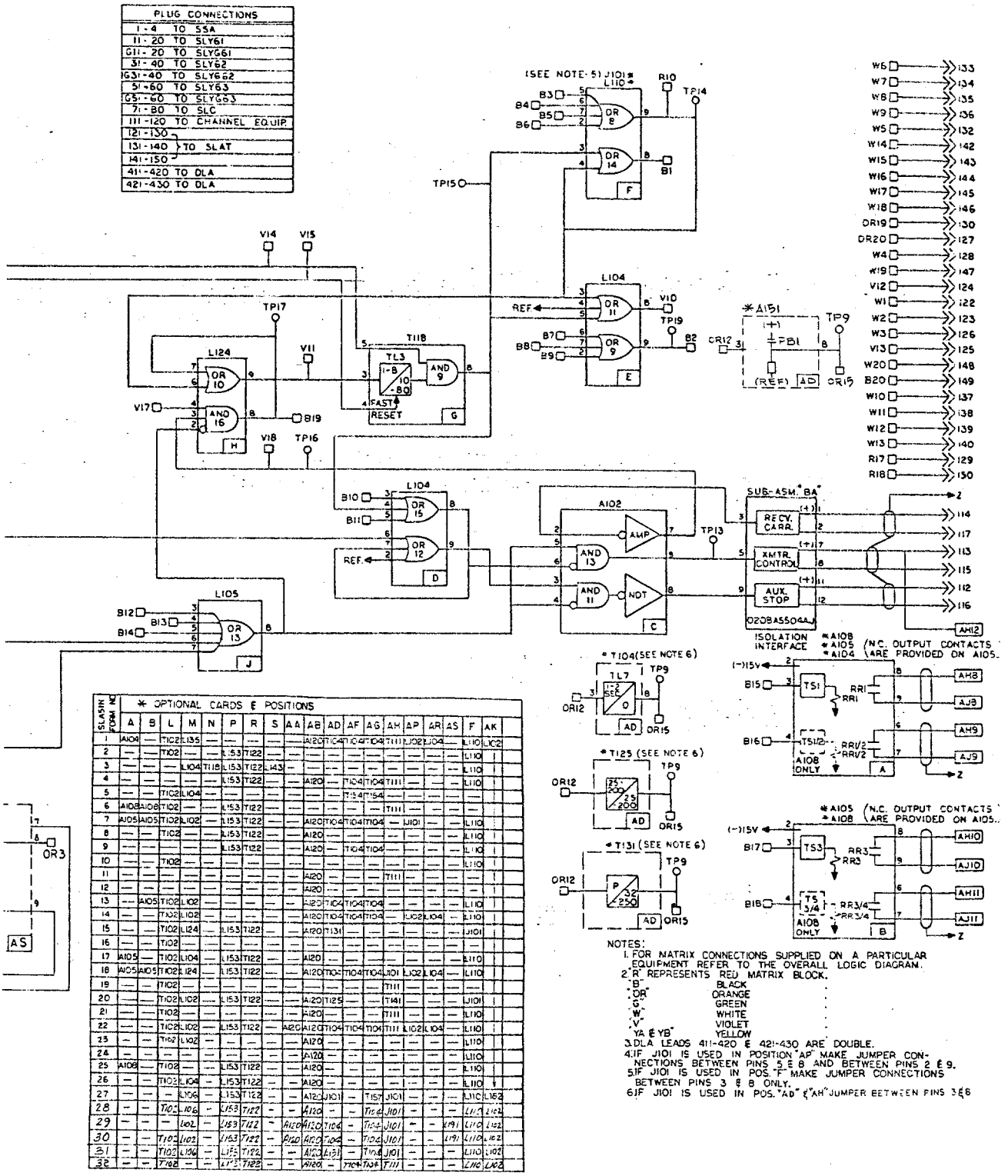


*Figure 1 (0138D2418-25) Internal-Connections Diagram for the SLA51N Relay, Forms 1-49

*Revised since last issue



* OPTIONAL CARDS & POSITIONS

SLA51N FORM NO	A	B	L	M	N	P	R	S	AA	AB	AD	AF	AG	AH	AP	AR	AS	F	AK
1	AI04	—	TI02	LI35	—	—	—	—	—	AI20	TI04	TI04	TI04	TI11	LJ02	LI04	—	LI10	LI02
2	—	—	TI02	—	—	LI53	TI22	—	—	—	—	—	—	—	—	—	—	LI10	
3	—	—	—	LI04	TI18	LI53	TI22	LI43	—	—	—	—	—	—	—	—	—	LI10	
4	—	—	—	—	—	LI53	TI22	—	—	AI20	—	TI04	TI04	TI11	—	—	—	LI10	
5	—	—	TI02	LI04	—	—	—	—	—	—	—	TI34	TI54	—	—	—	—	—	
6	AI08	AI08	TI02	—	—	LI53	TI22	—	—	—	—	—	—	TI11	—	—	—	—	
7	AI05	AI05	TI02	LI02	—	LI53	TI22	—	—	AI20	TI04	TI04	TI04	—	LJ01	—	—	LI10	
8	—	—	TI02	—	—	LI53	TI22	—	—	AI20	—	—	—	—	—	—	—	LI10	
9	—	—	—	—	—	LI53	TI22	—	—	AI20	—	TI04	TI04	—	—	—	—	LI10	
10	—	—	TI02	—	—	—	—	—	—	—	—	—	—	—	—	—	—	LI10	
11	—	—	—	—	—	—	—	—	—	AI20	—	—	—	TI11	—	—	—	—	
12	—	—	—	—	—	—	—	—	—	AI20	—	—	—	—	—	—	—	—	
13	—	AI05	TI02	LI02	—	—	—	—	—	AI20	TI04	TI04	TI04	—	—	—	—	LI10	
14	—	—	TX02	LI02	—	—	—	—	—	AI20	TI04	TI04	TI04	—	LJ02	LI04	—	LI10	
15	—	—	TI02	LI24	—	LI53	TI22	—	—	AI20	TI31	—	—	—	—	—	—	JI01	
16	—	—	TI02	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	
17	AI05	—	TI02	LI04	—	LI53	TI22	—	—	AI20	—	—	—	—	—	—	—	LI10	
18	AI05	AI05	TI02	LI24	—	LI53	TI22	—	—	AI20	TI04	TI04	TI04	JI01	LJ02	LI04	—	LI10	
19	—	—	TI02	—	—	—	—	—	—	—	—	—	—	TI11	—	—	—	—	
20	—	—	TI02	LI02	—	LI53	TI22	—	—	AI20	TI25	—	—	TI41	—	—	—	JI01	
21	—	—	TI02	—	—	—	—	—	—	AI20	—	—	—	TI11	—	—	—	LI10	
22	—	—	TI02	LI02	—	LI53	TI22	—	A20	AI20	TI04	TI04	TI04	TI11	LJ02	LI04	—	LI10	
23	—	—	TI02	LI02	—	—	—	—	—	AI20	—	—	—	—	—	—	—	LI10	
24	—	—	—	—	—	—	—	—	—	AI20	—	—	—	—	—	—	—	LI10	
25	AI08	—	TI02	—	—	LI53	TI22	—	—	AI20	—	—	—	—	—	—	—	LI10	
26	—	—	TI02	LI04	—	LI53	TI22	—	—	AI20	—	—	—	—	—	—	—	LI10	
27	—	—	—	LI06	—	LI53	TI22	—	—	AI20	JI01	—	TI57	JI01	—	—	—	LI10	LI62
28	—	—	TI02	LI06	—	LI53	TI22	—	—	AI20	—	—	TI04	JI01	—	—	—	LI10	LI62
29	—	—	—	LI02	—	LI53	TI22	—	AI20	AI20	TI04	—	TI04	JI01	—	—	LJ91	LI10	LI62
30	—	—	TI02	LI02	—	LI53	TI22	—	AI20	AI20	TI04	—	TI04	JI01	—	—	LJ91	LI10	LI62
31	—	—	TI02	LI06	—	LI53	TI22	—	—	AI20	LI31	—	TI04	JI01	—	—	—	LI10	LI02
32	—	—	TI02	—	—	LI53	TI22	—	—	AI20	—	TI04	TI04	TI11	—	—	—	LI10	LI02

Figure 1 (0138D2418-25) Internal-Connections Diagram for the SLA51N Relay, Forms 1-49

*Revised since last issue

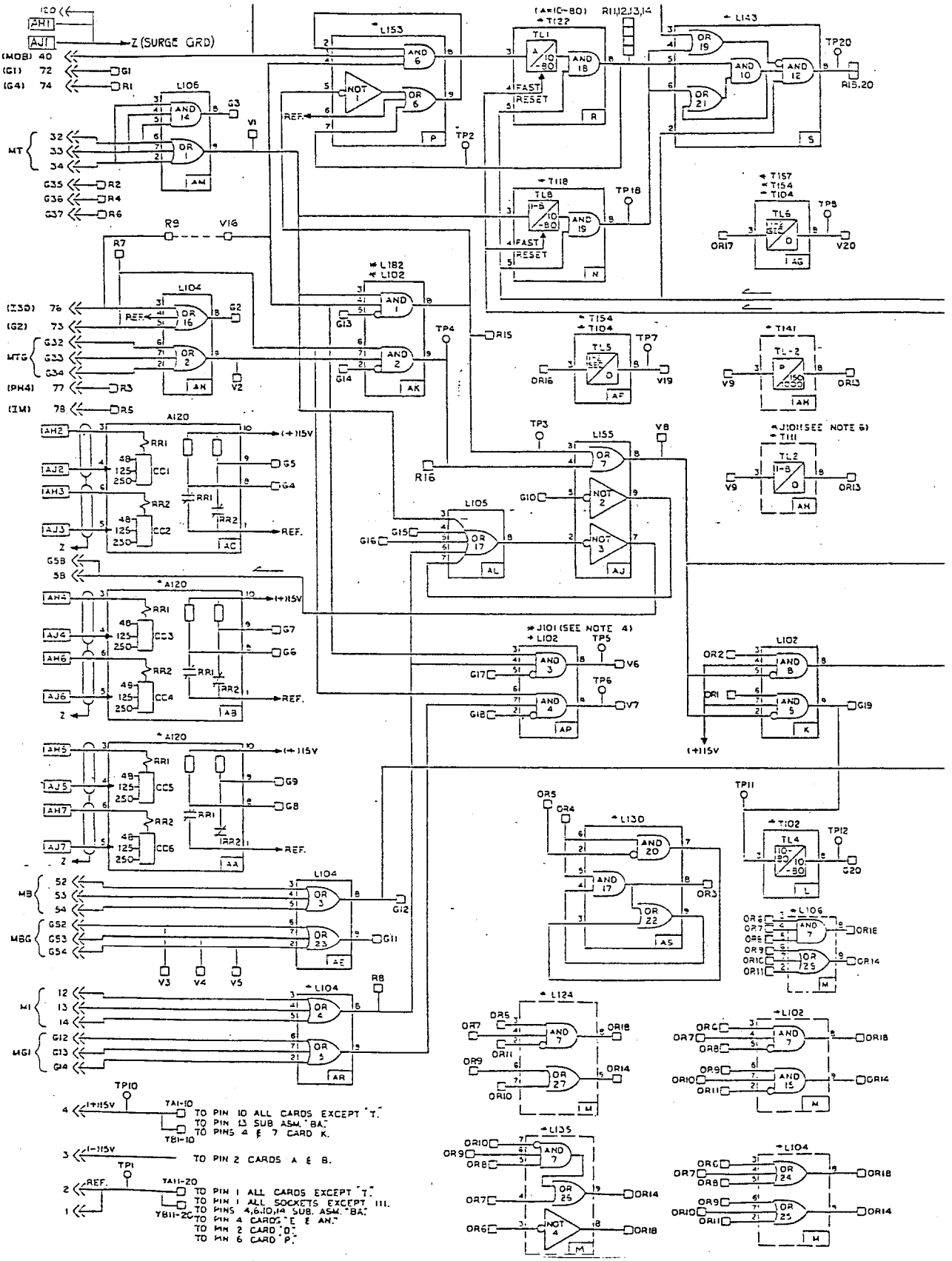


*Figure 2 (0153D6638-1) Internal-Connections Diagram for the SLA51N Relay, Forms 50 and Up

*Revised since last issue

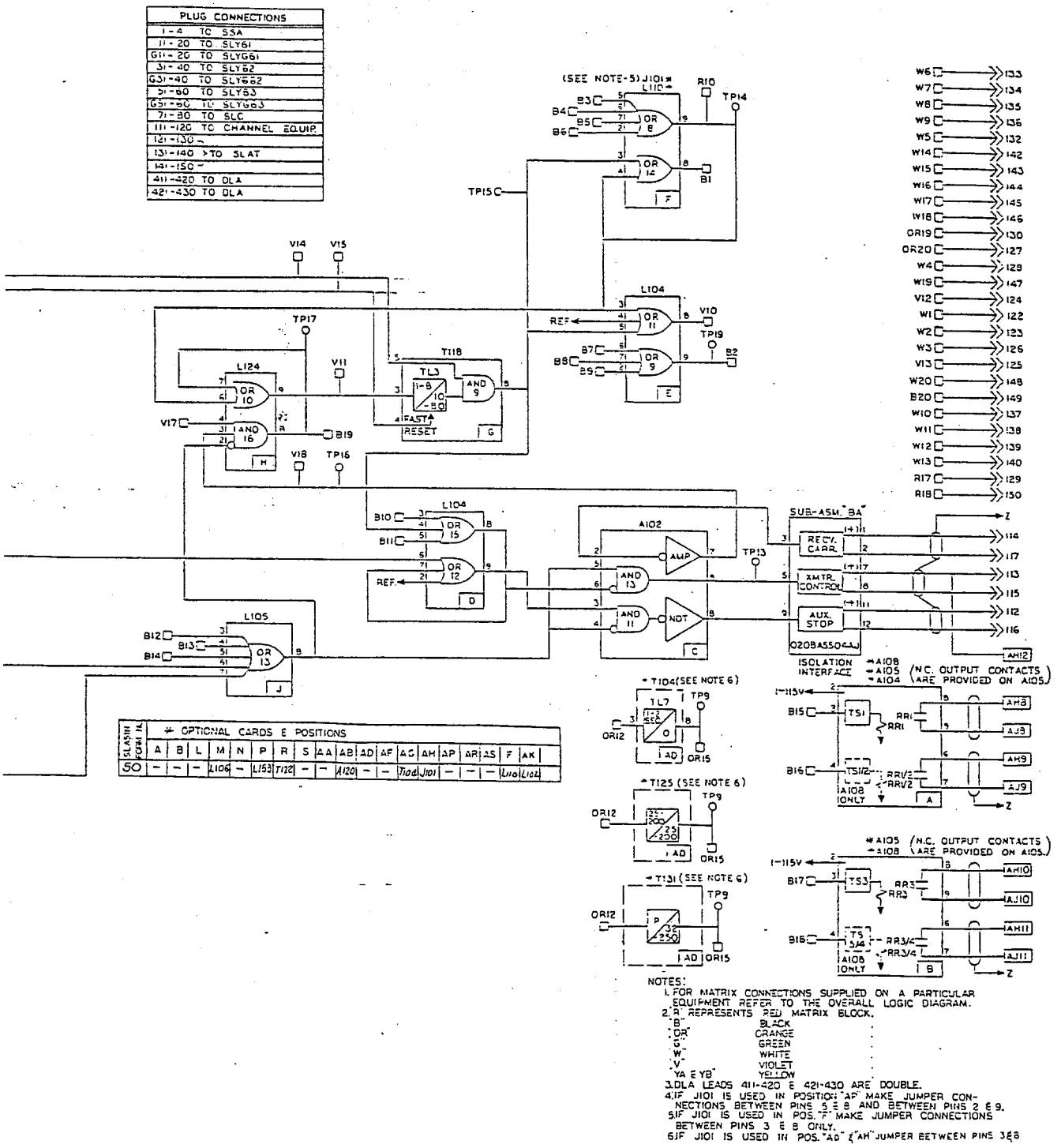
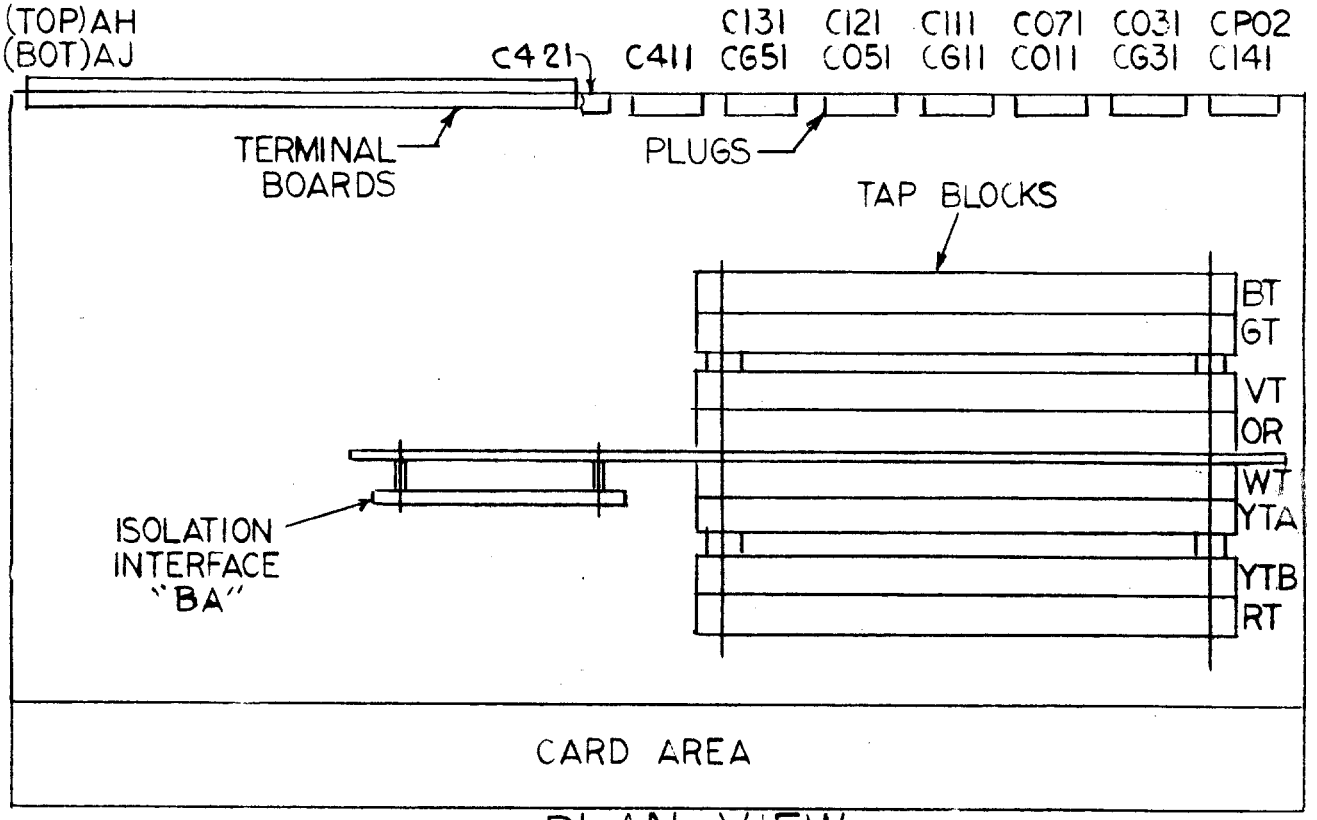


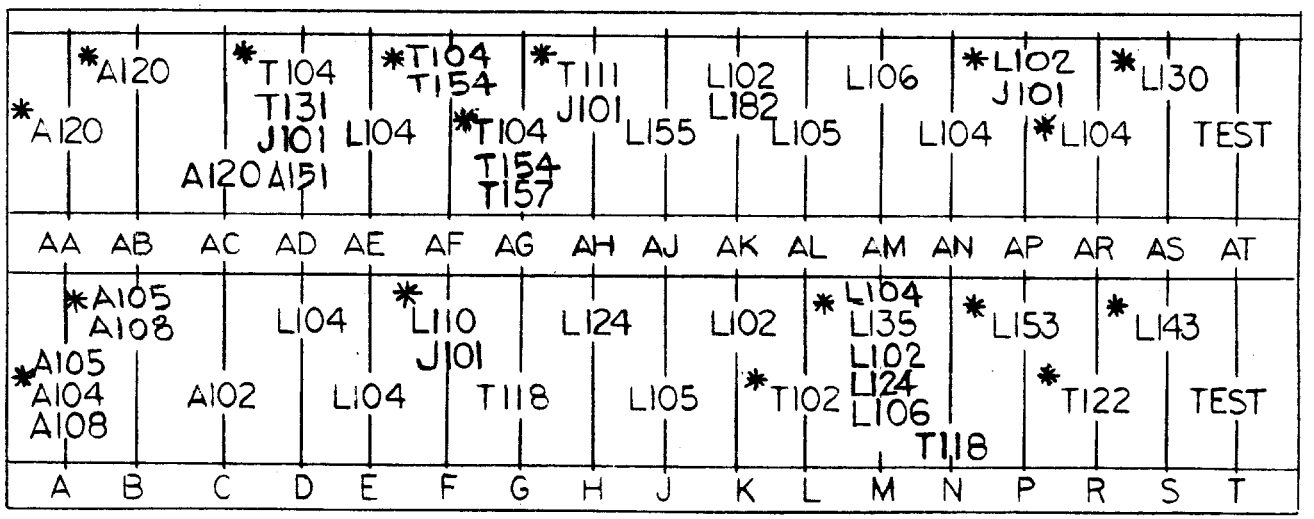
*Figure 2 (0153D6638-1) Internal-Connections Diagram for the SLA51N Relay, Forms 50 and Up

*Revised since last issue



PLAN VIEW

* OPTIONAL CARDS



FRONT VIEW

*Figure 3 (0273A9106-4) Component Location Diagram

*Revised since last issue

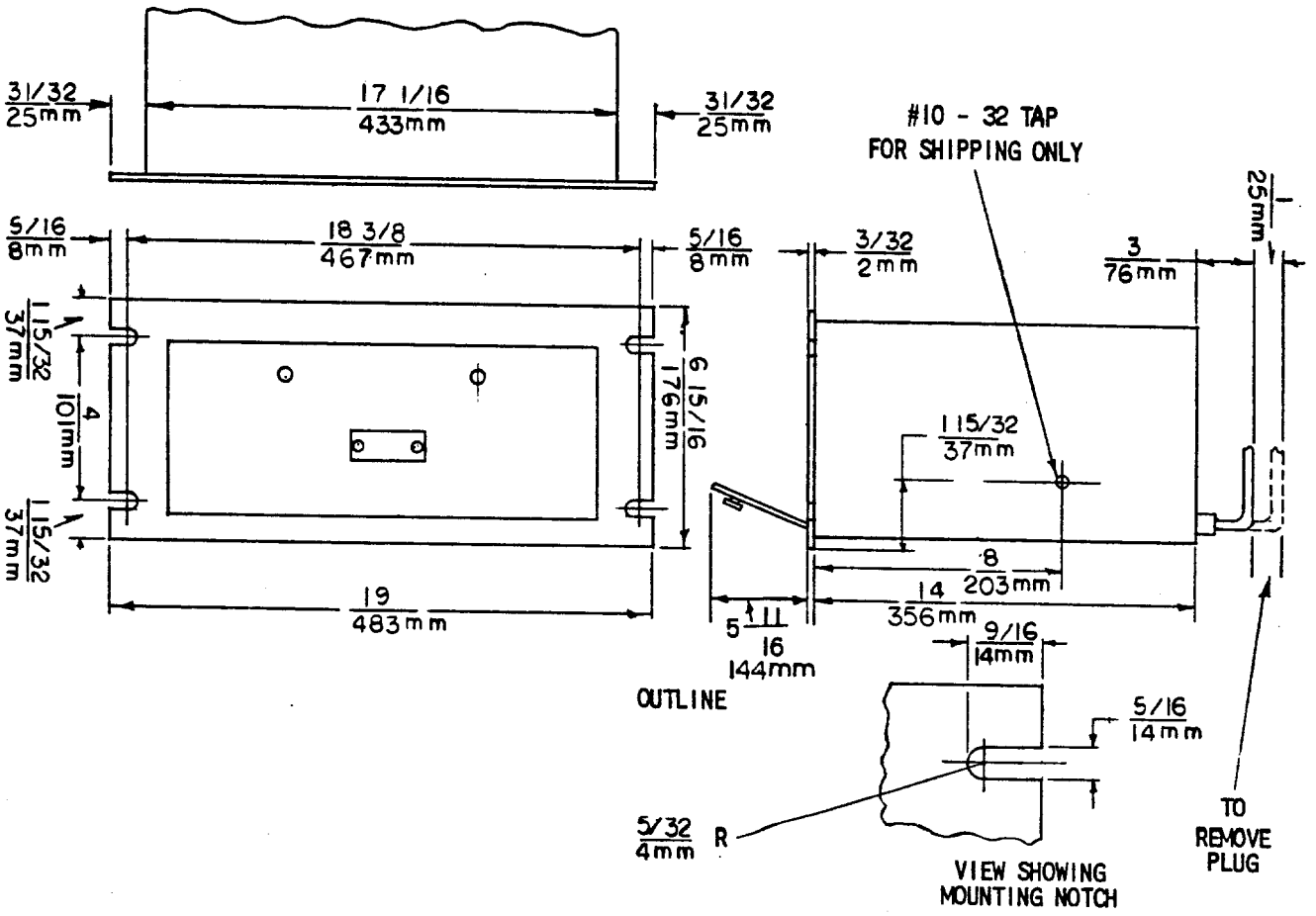


Figure 4 (0227A2037-1) Outline and Mounting Dimensions

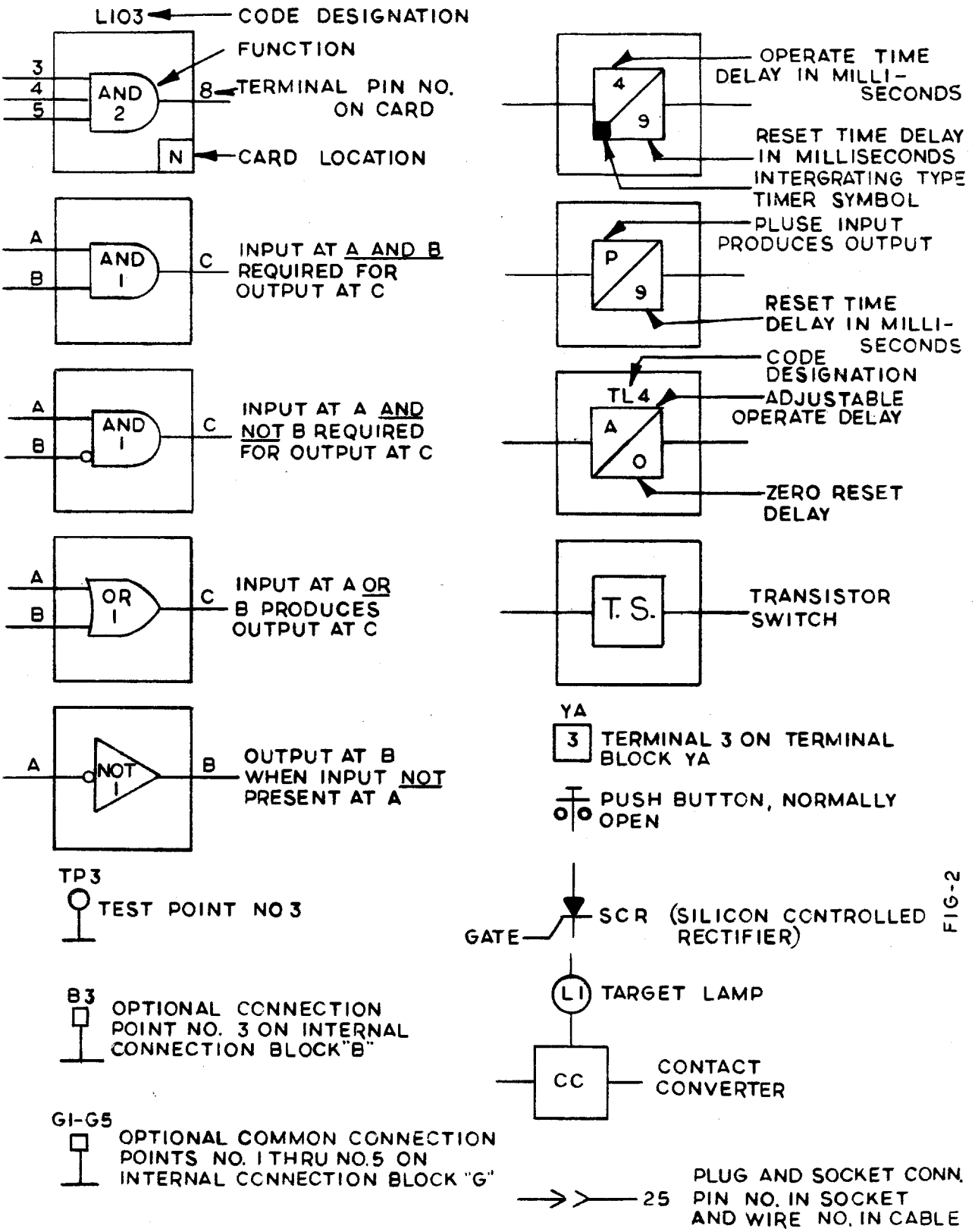


*Figure 5 (0227A2047-1) Logic and Internal-Connection Diagram Legend

*Revised since last issue

THE FOLLOWING ARE FACTORY CONNECTIONS MADE AT THE MATRIX BLOCKS INSIDE OF THE SLA RELAY ASSOCIATED WITH THIS EQUIPMENT.
SYMBOLS LISTED: PL=RELAY INTERCONNECTING CABLE LEAD
(5)=LOGIC FUNCTION CARD PIN NUMBER
‡=3-WAY CONNECTION
✳=DLA MONITOR CONNECTION AVAILABLE BUT NOT USED

158

MATRIX BLOCK JUMPERS		LOGIC FUNCTION	
FROM	TO	FROM	TO
G13	YB13	AND1 (5)	REF.
G14	YB14	AND2 (2)	REF.
G15	YB15	OR17 (4)	REF.
G16	YB16	OR17 (5)	REF.
G17	YB17	AND3 (5)	REF.
G18	YB18	AND4 (2)	REF.
B3	YA12	OR8 (5)	REF.
B5	YA14	OR8 (7)	REF.
OR7	YA15	OR23 (4)	REF.
W1	YA11	PL122	REF.
W3	YA13	PL126	REF.
W9	YA16	PL136	REF.
W11	YA10	PL138	+15V.
OR13	V17	TL2(8)	AND16(4)
R5	G10	PL78	NOT2(5)
R9	OR8	PL76	AND7(5)
G2	W5	OR16(8)	PL132
V8	V9	OR7(8)	TL2(3)
G6	OR2	CC3(8)	AND8(3)
G1	OR1	PL72	AND5(6)
G19	B13	AND5(9)	OR13(4)
G20	B14	TL4(8)	OR13(5)
B2	W2	OR9(9)	PL123
G5	B11	CC2(9)	OR15(5)

MATRIX BLOCK JUMPERS		LOGIC FUNCTION	
FROM	TO	FROM	TO
B19	W19	AND16(8)	PL147
V18	OR6	RCVR.	NOT4(3)
OR18	B15	NOT4(8)	TS1(3)
B1	W8	OR14(8)	PL135
W4	W16	PL128	PL144
OR15	OR10	TL7(8)	AND7(7)
V10	V12	OR11(8)	PL124
V11	V13	OR10(9)	PL125
V14	OR19	D.C.SUPV.	PL130
V15	OR20	FAST RESET	PL127
‡ G4	B12	CC1 (8)	OR13(3)
‡ G4	B10	CC1 (8)	OR15 (3)
‡ V19	W13	TL5 (8)	PL140
‡ V19	B7	TL5 (8)	OR9 (6)
‡ V20	B8	TL6 (8)	OR9 (7)
‡ V20	B20	TL6 (8)	PL149
‡ OR14	B9	AND7 (9)	OR9 (2)
‡ OR14	W17	AND7 (9)	PL145
‡ G7	OR12	CC4 (9)	TL7 (3)
‡ G7	OR9	CC4 (9)	AND7 (6)
‡ V7	B6	AND4 (9)	OR8 (2)
‡ V7	W12	AND4 (9)	PL139
‡ R15	OR17	AND1 (8)	TL6 (3)
‡ R15	W20	AND1 (8)	PL148
‡ R16	OR16	AND2 (9)	TL5 (3)
‡ R16	W18	AND2 (9)	PL146
‡ V6	W10	AND3(8)	PL137
‡ V6	B4	AND3(8)	OR8 (6)

Figure 6 (0227A2050 Sh.158 1) Sample Option Chart

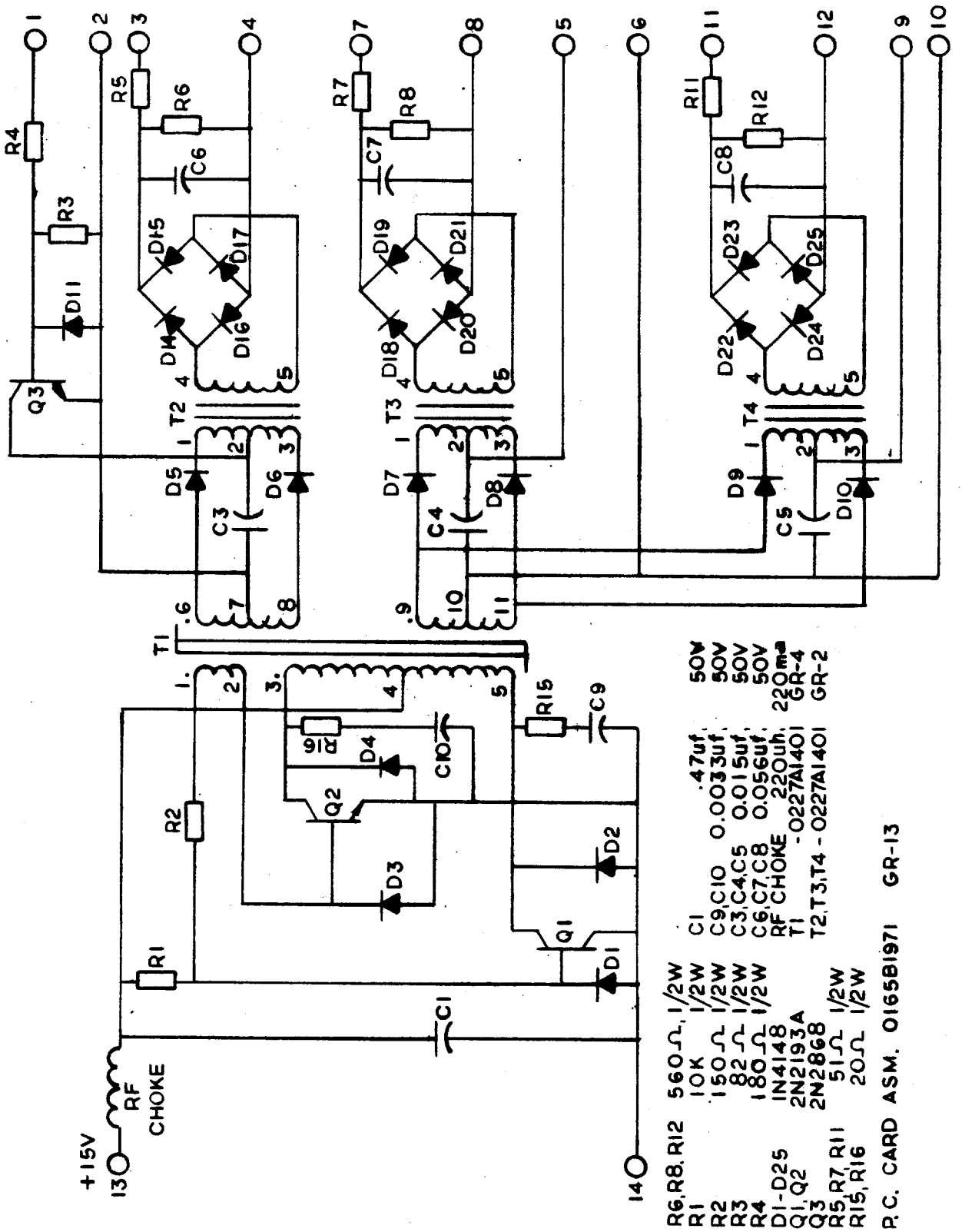
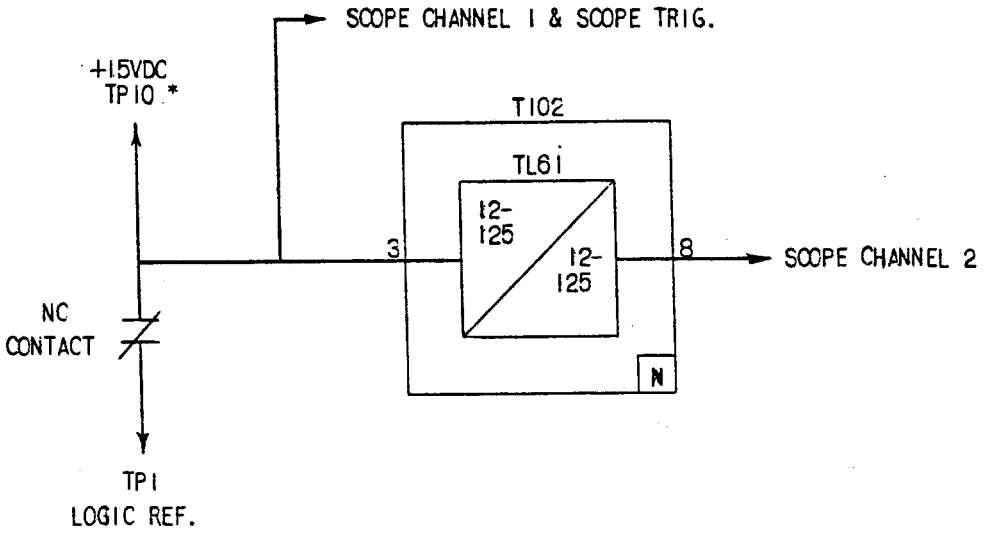


*Figure 7 (0208A5504AJ-1) Isolation Interface Circuit

Revised since last issue



* THE 15VDC SIGNAL AT PIN 10 HAS A CURRENT LIMITING RESISTOR MOUNTED ON THE TEST CARD.

Figure 8 (0246A7987) Logic Timer Test Circuit

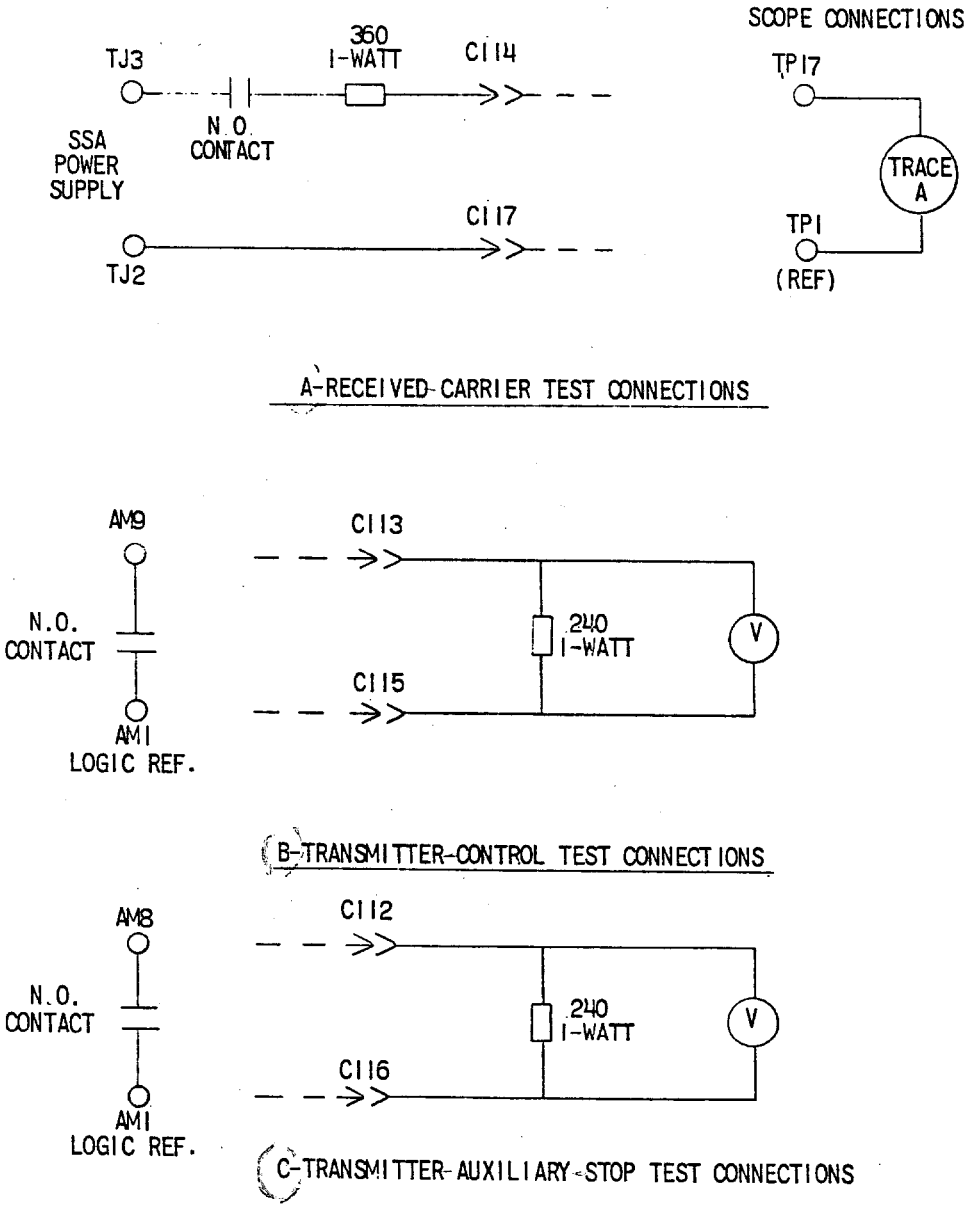


Figure 9 (0257A6244-0) Isolation Interface Test Circuit

Meter and Control
Business Department

General Electric Company

4/89