INSTRUCTIONS

GEK-49917

AUXILIARY LOGIC RELAY

TYPE SLA51P

GENERAL ELECTRIC

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AUXILIARY LOGIC RELAY

TYPE SLA51P

DESCRIPTION

The SLA51P relay is an auxiliary logic relay designed to be used in a directional comparison ON-OFF carrier scheme. The relay contains the necessary logic to interpret output signals from associated measuring functions and translate them to an appropriate auxiliary output and tripping relay. In addition to the SLA51P relay, appropriate ground and phase relays plus a power supply and auxiliary tripping relay are required to complete a particular relaying scheme.

The type SLA51P relay is packaged in a four-rack unit enclosed metal case. The relay is suitable for mounting in a 19-inch rack and the mounting and outline dimensions are shown in Fig. 3. Internal connections for the SLA51P relay are shown in Fig. 1, and the component and card locations are shown in Fig. 2.

APPLICATION

The SLA51P relay is designed to operate in conjunction with appropriate phase and ground relays in a directional comparison ON-OFF blocking scheme, using either Type CS26B power line carrier or Type 30 audio tones as the pilot channel. Isolation interfacing provides the interconnection between the SLA logic and the transmitter and receiver of the pilot channel.

Protection features required in a relaying scheme often vary from scheme to scheme and it is sometimes desirable to provide certain features initially with the scheme or to provide features so that they may be added at a later date in the field. To this end, the SLA51P design has incorporated circuit flexibility to permit implementation of certain optional features. Printed circuit cards L101, L106, L110, L104, L102, T102 and T107 in Position G, J, AJ, AC, AD, AF, AE and AH respectively, shown dotted in Fig. 1, are used whenever a single phase fault selector is required. Matrix blocks "R", "Y", "O", "B" and "W", each with a number of points, are provided in all SLA51P relays to permit various logic arrangements to be made simply by connecting jumper leads between appropriate points. For example, a jumper between O6 and B5 will allow the out-of-step detection option to block all pilot tripping by applying the NOT input to the appropriate AND function in the associated SLAT tripping relay. These examples can best be understood by referring to the overall logic diagram and instruction books supplied with a particular relaying scheme.

Various points in the logic can be monitored by providing jumpers from any of the available matrix points to plugs located on the rear of the SLA51P relay. The plugs may be provided initially with the equipment or added at a later date. This option is further described in DATA MONITORING POINTS under the section headed OPERATING PRINCIPLES.

For the specific options and the logic arrangement supplied with a particular scheme, refer to the logic diagram and logic descriptive writeup supplied with that scheme. If it is desired to make logic changes at a later date, the diagrams and instruction books supplied with a particular scheme should be studied to determine the means for implementing the changes. If, after study of the diagrams, further assistance is required, contact the nearest General Electric District Sales Office.

There are no measuring functions to be set in the SLA51P relay, but certain timers are included that must be set in accordance with the demands of the particular system to be protected. Refer to the section under SETTINGS for a description of these timers and for suggestions to be used in making the settings.

RATINGS

The type SLA51P relay is designed for use in an environment where the air temperature outside the relay case does not vary more than -20°C to +65°C.

The type SLA51P relay requires ±15 volt DC power source which can be obtained from a Type SSA power supply.

Each contact converter in this relay has a link for selecting the proper voltage for the coil circuit of the contact converter. The three possible voltages are 48 volt DC, 125 volt DC and 250 volt DC.

BURDENS

The SLA51P relay presents a burden of 330 milliamperes to the +15 volt DC supply of the Type SSA power supply, and about 40 milliamperes to the -15 volt DC supply.

Each contact converter, when energized, will draw approximately 10 milliamperes from the station battery, regardless of tap setting.

OPERATING PRINCIPLES

LOGIC CIRCUIT

The functions of the type SLA51P relay involve basic logic (AND, OR, and NOT) where the presence or absence of signals, rather than their magnitude, controls the operation. Signals are measured with respect to a reference bus accessible at TP1. In general, a signal below one volt DC represents an OFF or LOGIC ZERO condition; an ON or LOGIC ONE condition is represented by a signal of 10 to 15 volt DC.

The symbols used on the internal connection diagram (Fig. 1) are explained by the legend shown in Fig. 4.

The matrix block options shown in the internal connections of the SLA51P relay are provided at the factory. The connections are shown on the associated overall logic and are listed on the associated option chart. A sample option chart for the Type SLA51P relay is shown in Fig. 5.

CONTACT CONVERTERS

The purpose of this function is to convert a contact operation into a signal that is compatible with the logic circuit of the Type SLA51P relay. These contact converters, which are labeled CC1, CC2 and CC3 have a non-adjustable four-millisecond pickup delay.

CC1

Contact converter 1 is energized by an external contact to stop all carrier transmission.

CC2

Contact converter 2, when energized, prevents relay carrier tripping and relay control of carrier but permits auxiliary control of carrier.

CC3

Contact converter 3, when energized by a breaker "a" contact, will start a timer (50-400 milliseconds) which disables the output of "AND 28". In a typical scheme, the other input to "AND 28" comes from PH4 (instantaneous phase overcurrent) or G4 (instantaneous ground unit).

DATA MONITORING POINTS

Optional data monitoring points can be brought out from the matrix block to plugs mounted in available knockouts at the rear of the SLA51P relay. Each plug contains nine monitoring points and reference. When ordered, the selected monitoring points on the matrix block are listed on the option chart which represents the factory wiring configuration for the relay options. Changes in selection of monitored points may be

easily made, but this must be done inside the relay. If monitoring points are not ordered, they may be provided at a later date by adding the cable plug(s) and associated wiring as required.

To monitor these points an additional piece of equipment termed a Data Logging Amplifier (DLA) is required.

CHANNEL INTERFACE

The logic of the type SLA51P relay includes an isolation interface (Fig. 6) between the relays in the scheme and the associated channel. The circuitry of the isolation interface provides a signal path but maintains metallic isolation. This feature makes it possible to maintain isolation between the DC supply used for the relays and that employed by the channel. All outputs from the isolation interface circuits are 5 volt DC 20 milliamperes maximum.

SETTINGS

There are seven timers in the SLA51P that may require field adjustment.

TL1 (A/40)

The TL1 timer, Pos. "E", is part of the out-of-step detection scheme. This timer has a pickup range of 10-80 milliseconds and a similar drop-out range. In a typical directional comparison relaying scheme the drop-out time is factory set to 40 milliseconds. The pickup time should be field set to anywhere between two-to-four cycles depending on the application.

TL2 (4/0)

This timer, Pos. "F", is normally not supplied with the relay. In its place, a jumper card is used to short pins 3 and 8 together. When coordination with an electromechanical relay on the other end of the line is required, this timer should replace the jumper card. A typical pickup setting should be four milliseconds with a drop-out time of zero.

TL3 (25/35)

The TL3 timer, Pos. "M", is part of the transient blocking circuit. This timer has a pickup range of 10-80 milliseconds and a similar drop-out range. This timer is factory set to pick up at 25 milliseconds and drop out at 35 milliseconds when the SLA51P is supplied as part of a protective relaying scheme.

TL4 (3/50)

The TL4 timer, Pos. "S", is part of the comparer-integrator circuit. This timer has a pickup range of one-to-eight milliseconds and a drop-out range of 10-80 milliseconds. This timer is factory set to pick up at three milliseconds and drop out at 50 milliseconds when the SLA51P is part of a protective relaying scheme. The TL4 timer is provided with a fast reset DC supervision to prevent operations on application or removal of DC power.

TL5 and TL6 (10-40/70, 10-32/70)

TL5 and TL6 are part of the logic circuit which initiates reclosing following single phase-to-ground faults and blocks reclosing on all multi-phase faults.

TL5 and TL6 have a pickup range of 10-80 milliseconds and a similar drop-out range. These timers (when supplied) are factory set to drop out at 70 milliseconds. When the SLA51P is part of a protective relaying scheme the pickup of TL5 is set by the user at a value between 10-40 milliseconds and that of TL6, between 10-32 milliseconds.

TL7 (50-400/0)

The TL7 timer, Pos. "AG" is part of the line pickup circuit, which in a typical relaying scheme, will block the instantaneous, phase and ground, overcurrent trips within a set time after the breaker "a" switch closes. The pickup range of this timer is 50 to 400 milliseconds, and the drop-out time is zero milliseconds.

For further details concerning these timers, see the logic description provided with each static relaying scheme.

CONSTRUCTION

The SLA51P relay is packaged in an enclosed metal case with hinged front covers and removable top cover. The outline and mounting dimensions of the case and the physical location of the components are shown in Figs. 3 and 2 respectively.

The SLA51P relay contains printed circuit cards identified by a code number such as A112, T102, L104 where A designates auxiliary function, T designates time-delay function, and L designates logic function. The printed circuit cards plug in from the front of the unit. The sockets are marked with letter designations or "addresses" (D, E, F, etc.) which appear on the guide strips in front of each socket, on the component location drawing, on the internal connection diagram and on the printed circuit card. The test points (TP1, TP2, etc.) shown on the internal connection diagram are connected to instrument jacks on a test card in position T or AT with TP1 at the top of the AT card. TP10 is tied to +15 volt DC through a 1.5K resistor. This resistor limits the current when TP10 is used to supply a logic signal to a card.

Other logic options are selected by means of taper tip jumpers and matrix blocks. These matrix blocks are located in the rear of the unit as shown in Fig. 2. The orange (O) matrix blocks has ten points in two 5-point common groups. The black (B) matrix block has 20 individual matrix points. The red (R) block has 20 points which are grouped in pairs. The yellow (Y) block has 20 points which are grouped in 10 common points; 1 to 10 are tied to +15 volt DC, 11 to 20 are tied to reference. The white (W) matrix block has twenty individual matrix points. A tool for inserting and removing the taper tip jumpers is supplied with each relay.

RECEIVING, HANDLING AND STORAGE

The SLA51P relay will normally be supplied as a part of a static relay equipment, mounted in a rack or cabinet with other static relays and test equipment. Immediately upon receipt of a static relay equipment, it should be unpacked and examined for any damage sustained in transit. If injury or damage resulting from rough handling is evident, file a damage claim at once with the transportation company and promptly notify the nearest General Electric Sales Office.

Reasonable care should be exercised in unpacking the equipment. If the equipment is not to be installed immediately, it should be stored indoors in a location that is free from moisture, dust, metallic chips, and severe atmospheric contaminants.

Just prior to final installation the shipping support bolt should be removed from each side of all relay units, to facilitate possible future unit removal for maintenance. These shipping support bolts are approximately eight inches back from the relay front panel. Static relay equipment, when supplied in swing rack cabinets, should be securely anchored to the floor or to the shipping pallet to prevent the equipment from tipping over when the swing rack is opened.

TEST INSTRUCTIONS

CAUTION

IF THE SLA51P RELAY THAT IS TO BE TESTED IS INSTALLED IN AN EQUIPMENT WHICH HAS ALREADY BEEN CONNECTED TO THE POWER SYSTEM, DISCONNECT THE OUTPUTS IN THE ASSOCIATED TYPE SLAT RELAY FROM THE SYSTEM.

GENERAL

The SLA51P relay is supplied from the factory either mounted in a static relay equipment or as a separate unit associated with measuring relays, a Type SSA power supply and some form of channel equipment. All relay units for a given terminal of static relaying equipment are tested together at the factory, and each unit will have the same summary number stamped on its nameplate.

In general, when a time range is indicated on the internal connection diagram, the timer has been factory set at a mid-range value. Timers should be set for the operating or reset times indicated on the associated overall logic diagram. Where a time range is indicated on the overall logic diagram, the timer

should be set for the value recommended for that function in the descriptive writeup accompanying the overall logic diagram. Where a setting depends upon conditions encountered on a specific application, that is so stated and the factors influencing the choice of setting are described. The procedure for checking and setting the timers is described in a later section.

OPERATIONAL CHECKS

Operation of the SLA51P unit can be checked by observing the signals at the twenty test points (TP1 to TP20) in the SLA51P or by observing the output functions in the associated Type SLAT tripping relay. The test points are located on two test cards in positions T and AT, and are numbered 1 to 20 from top to bottom. TP1 is the reference bus for the logic circuit; TP10 is at +15 volt DC and TP2 is at -15 volt DC. The remaining points are located at various strategic points throughout the logic as shown on the internal connection diagram (Fig. 1). Test point voltages can be monitored with a portable high impedance voltmeter, the voltmeter on the test panel of the associated equipment, or an oscilloscope.

TEST CARD ADAPTER

The test card adapter provides a convenient means of gaining access to any pin of a particular card. Detailed information on the use of the test adapter card is included in the card instruction book GEK-34158.

TIMER ADJUSTMENTS AND TESTS

When the time-delay cards are to be adjusted or checked, an oscilloscope that can display two traces simultaneously and that has a calibrated horizontal sweep should be used.

In order to test the time cards it is necessary to remove the card previous to the timer (see Table 1) and to place the timer card in a card adapter. The card adapter allows access to the input and output of the timer if they are not brought out on test points. The timer test circuit is shown in Fig. 7. Opening the normally closed contact causes the output to step up to +15 volt DC after the pickup delay of the timer. To increase the pickup time turn the upper potentiometer on the timer card clockwise; to decrease the time turn it counterclockwise. Closing the contact causes the time output to drop out after the reset time-delay setting of card. If the timer card is provided with a variable reset delay, it can be adjusted by the lower potentiometer on the timer card (clockwise increases reset time).

TABLE I

Timer Under Test	Location	Remove Card in Location
T102 (A/40) - TL1	E	C
T103 (4/0) - TL2	F	D
T117 (25/35) - TL3	M	L
T118 (3/50) - TL4	S	R*
T102 (10-40/70) - TL5	AE	Plug C131
T117 (10-32/70) - TL6	AH	AJ, AR**
T146 (50-400) - TL7	AG	AP

*Connect Pin 4 of T118 to reference and Pin 5 to +15 volt (TP10).
**Connect Pin 3 of T117 to reference.

OVERALL EQUIPMENT TESTS

After the SLA51P relay and the associated static relay units have been individually calibrated and tested for the desired settings, a series of overall operating circuit checks is advisable.

The elementary, overall logic, and logic description for the specific job will be useful for determining the overall operation of the scheme.

Overall equipment tests can be performed by applying alternating current and voltages to the measuring units as specified in the instruction book for the measuring units and checking that proper outputs are obtained from the associated SLAT when the measuring units operate.

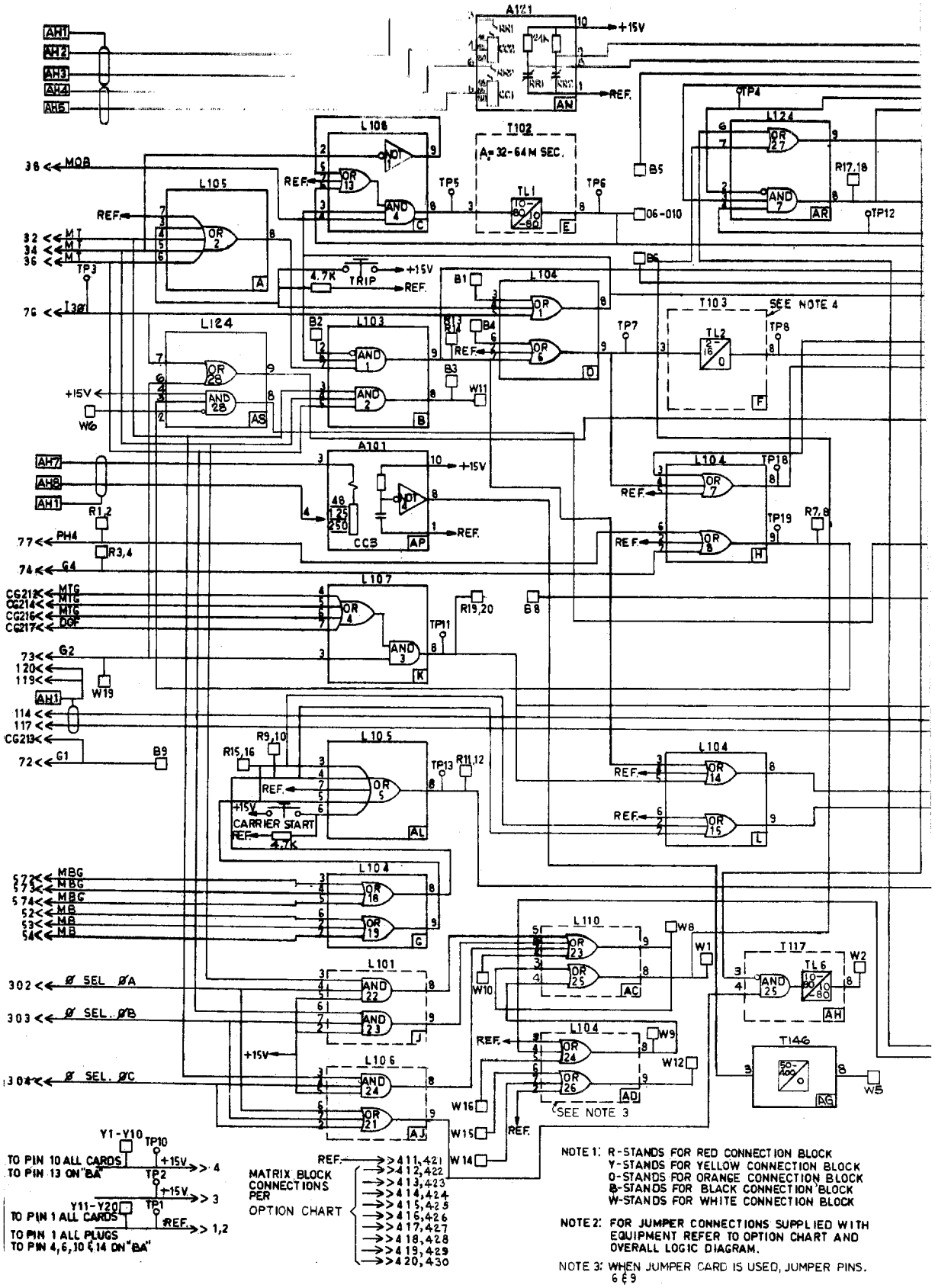
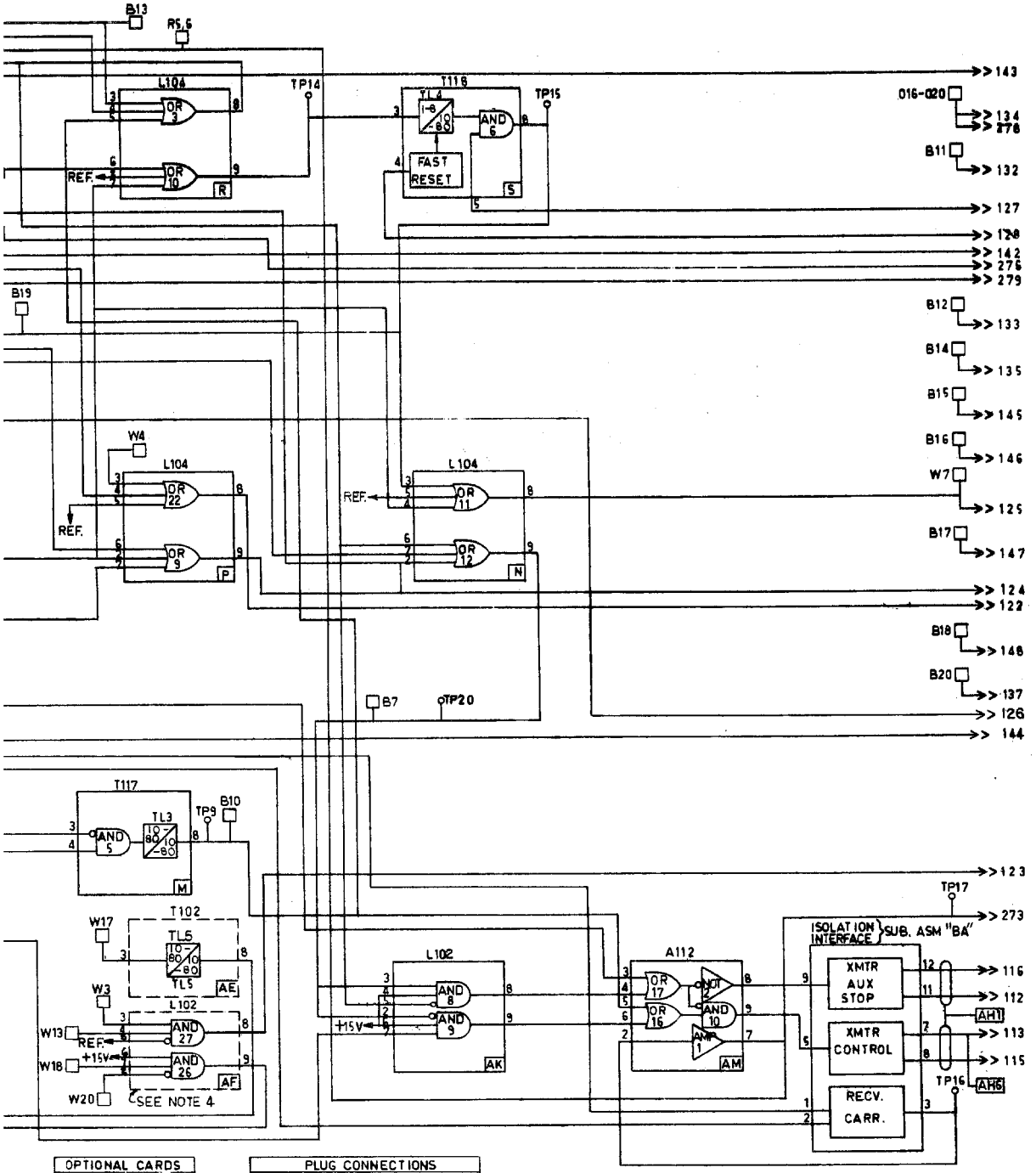


Fig. 1 (0138D2446-0) Interr



OPTIONAL CARDS		
FORM #	1	2
J101		AD,AF
L110	AC	—
L104	AD	—
T 102	AE	—
L 102	AF	—
T 117	AH	—
L 106	AJ	—
L 108	C	C
T 102	E	E
L 101	J	—
J 101	F	F

PLUG CONNECTIONS		
1-4	TO	SSA
31-40	TO	SLY51
51-60	TO	SLY53
71-80	TO	SLC51
111-120	TO	CHANNEL
121-130, 131-140, 141-150	TO	SLAT51
211-220	TO	SLYG51
271-280	TO	SLL
301-310	TO	SLON52
411-420	TO	DLA
571-580	TO	SLYG53
421-430	TO	DLA

NOTE 4: WHEN JUMPER CARD IS USED, JUMPER PINS 3 & 8.

Diagram for the SLA51P Relay

MAINTENANCE

PERIODIC TESTS

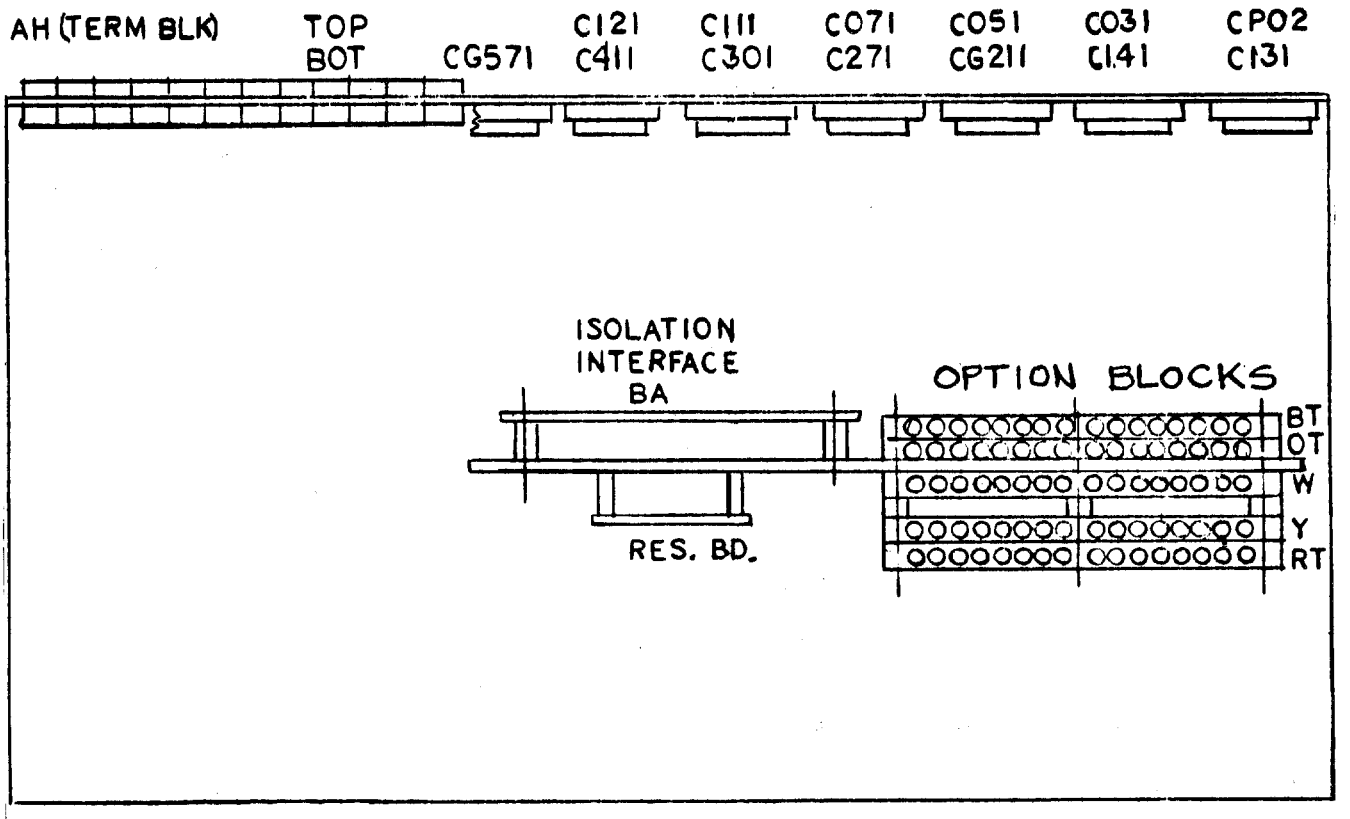
It should be sufficient to check the outputs produced at test points in the SLA51P when periodic calibration tests are made or the associated measuring units, for example, the phase and ground relays in line relaying scheme. No separate periodic tests on the SLA51P itself should be required.

TROUBLE SHOOTING

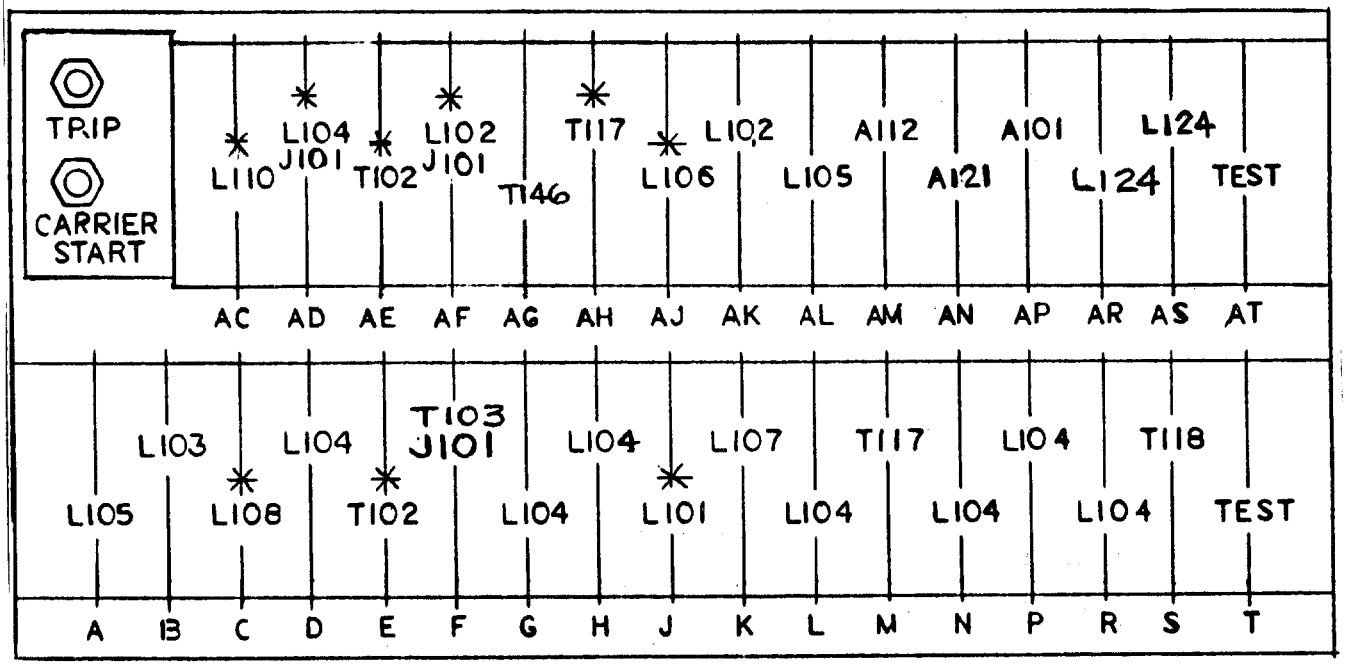
In any trouble shooting of equipment, it should first be established which unit is functioning incorrectly. The overall logic diagram supplied with the equipment shows the combined logic of the complete equipment and the various test points in each unit. By signal tracing, using the overall logic diagram and the various test points, it should be possible to quickly isolate the trouble.

SPARE PARTS

To minimize possible outage time, it is recommended that a complete maintenance program should include the stocking of at least one spare card of each type. It is possible to replace damage or defective components on the printed circuit cards, but great care should be taken in soldering so as not to damage or bridge-over the printed circuit buses, or overheat the semi-conductor components. The repaired area should be recovered with a suitable high-dielectric plastic coating to prevent possible breakdowns across the printed buses due to moisture and dust. The wiring diagrams for the cards in SLA51P relay are included in the card book GEK-34158.



PLAN VIEW



✳ OPTIONAL

Fig. 2 (0273A9089-0) Component Location Diagram for the SLA51P Relay

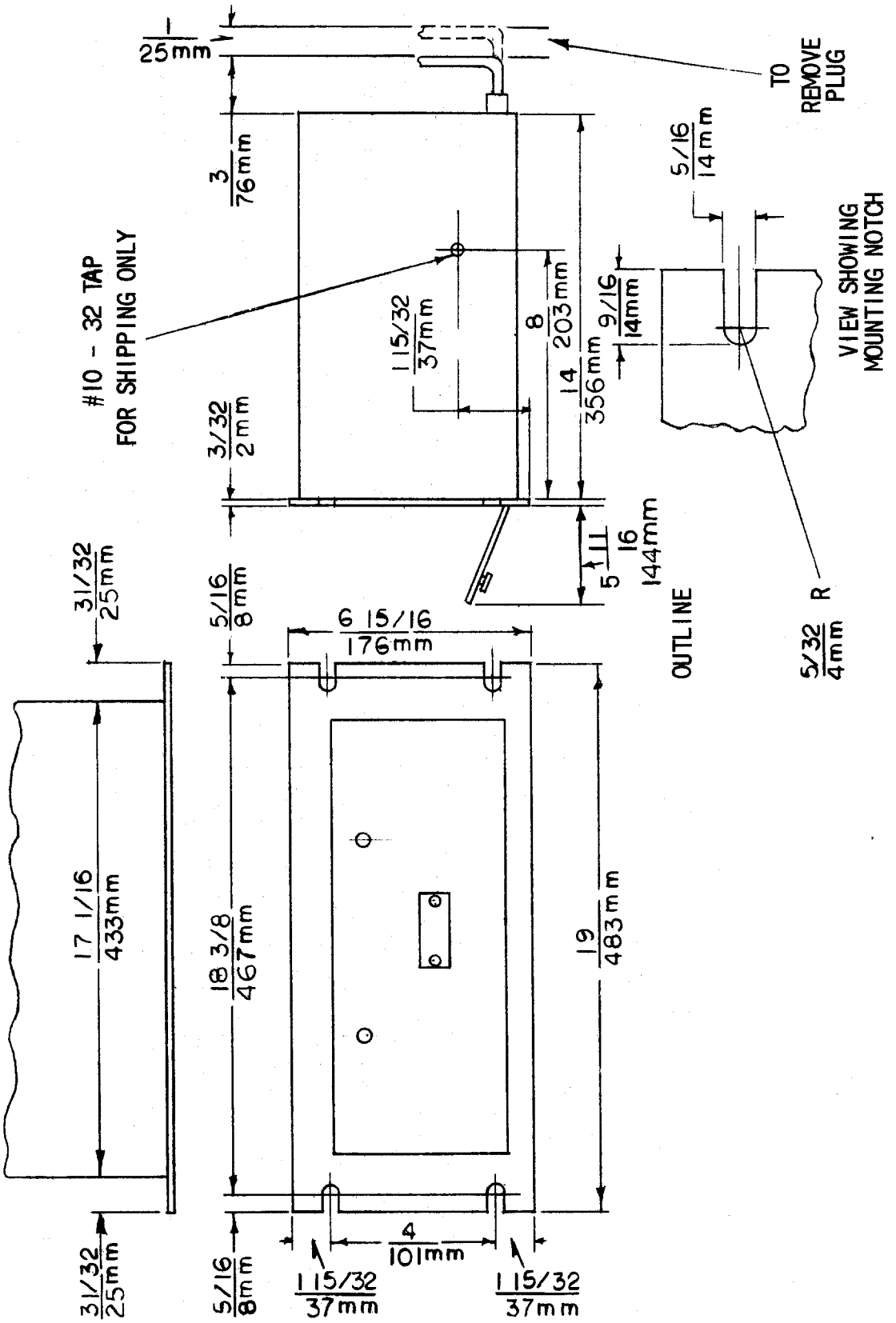


Fig. 3 (227A2037-1) Outline and Mounting Dimensions for the SLA51P Relay

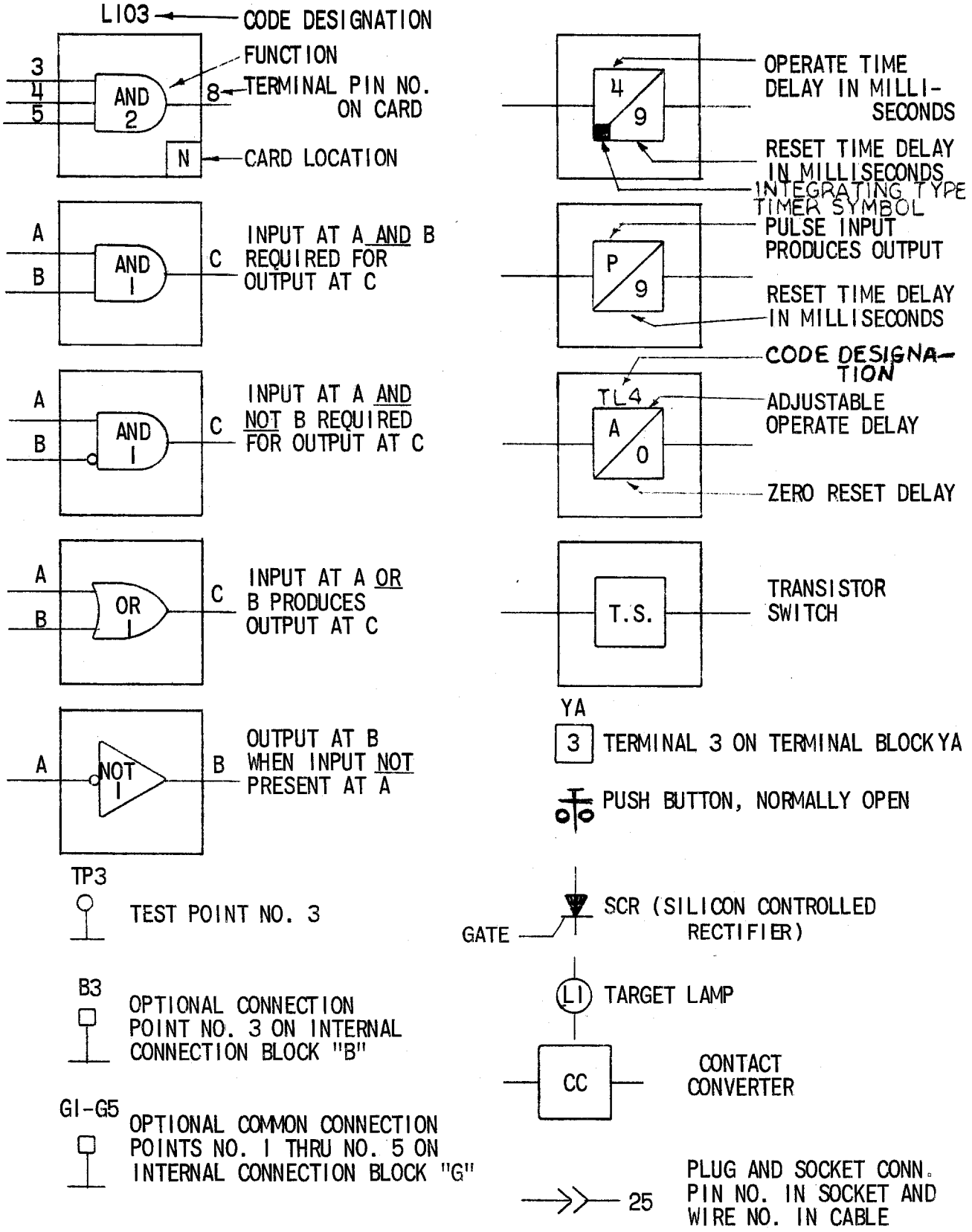


Fig. 4 (227A2047-1) Logic and Internal Connection Diagram Legend

THE FOLLOWING JUMPER CONNECTIONS ARE MADE AT THE MATRIX BLOCKS INSIDE OF THE RELAY REFERENCED IN ABOVE TITLE BLOCK

PL=CABLE PLUG
(5)=LOGIC FUNCTION CARD PIN NUMBER

MATRIX BLOCK JUMPERS		LOGIC FUNCTION		FUNCTION
FROM	TO	FROM	TO	
B1	Y12	OR1(5)	REF	1 3Ø SUPERVISION
B2	Y11	AND1(2)	REF	REQ'D LOGIC CONNECTION
B3	W15	AND2(8)	OR26(6)	3Ø FAULT DETECTOR
B4	Y13	OR6(6)	REF	REQ'D LOGIC CONNECTION
B5	Y14	OR3(4)	REF	O.S.B OUT
B8	R19	OR9(7)	AND3(8)	GROUND RELAY INPUT TO COMPUTER
B14	Y19	PL135	REF	OPTIONAL TRIP SUPERVISION
R1	B15	PL77	PL145	PH4 TARGET LIGHT
R3	B16	PL74	PL146	G4 TARGET LIGHT
R4	W16	PL74	DR24(5)	G4 INPUT TO PHASE SELECTOR LOGIC
W7	W3	PL125	AND27(3)	G4, PH4 OR TRIP INPUT TO PHASE SELECTOR LOGIC
R13	W18	AND1(9)	AND26(7)	PHASE RELAY INPUT TO PHASE SELECTOR LOGIC
W1	W14	OR25(8)	AND27(4)	PHASE SELECTOR LOGIC INPUT TO 3Ø DETECTOR
W2	W13	TL6(8)	AND27(4)	PHASE SELECTOR LOGIC SUPERVISION OF R.I.
W4	Y18	OR22(3)	REF	R.I. SUPERVISION
W11	W10	AND2(8)	OR23(2)	3Ø FAULT DETECTOR INPUT TO Ø SELECTOR LOGIC
W12	B12	OR26(9)	PL133	3Ø DETECTOR OUTPUT SUPERVISION
W19	W20	PL73	AND26(2)	G2 INPUT TO PHASE SELECTOR LOGIC
07	B6	TL1(8)	OR22(4)	R.I. BLOCKING IN
06	B11	TL1(8)	PL132	O.S.D. SELECTOR
016	W17	PL134	TL5(3)	TRIP BUS INPUT TO PHASE SELECTOR LOGIC
PL413	R5	PL413	AMP1(7)	RCV'D CARRIER MONITOR
PL412	017	PL412	PL134	TRIP BUS MONITOR
PL414	B7	PL414	OR12(9)	CARRIER STOP MONITOR
PL415	B10	PL415	OR16(5)	TRANSIENT BLOCK MONITOR
PL416	R7	PL416	OR8(9)	PH4 OR G4 MONITOR
PL417	B19	PL417	AND6(8)	PILOT TRIP MONITOR
PL418	R2	PL418	PL77	PH4 MONITOR
PL419	W8	PL419	OR23(9)	3Ø AND Ø-Ø-G FAULT MONITOR
PL420	08	PL420	TL1(8)	O.S.B. MONITOR
W5	W6	TL7,8	AND28(2)	LINE PICK-UP-INHIBITS PH4 & G4

Fig. 5 (227A2050-0 Sh. 154) Sample Option Chart for the SLA51P Relay

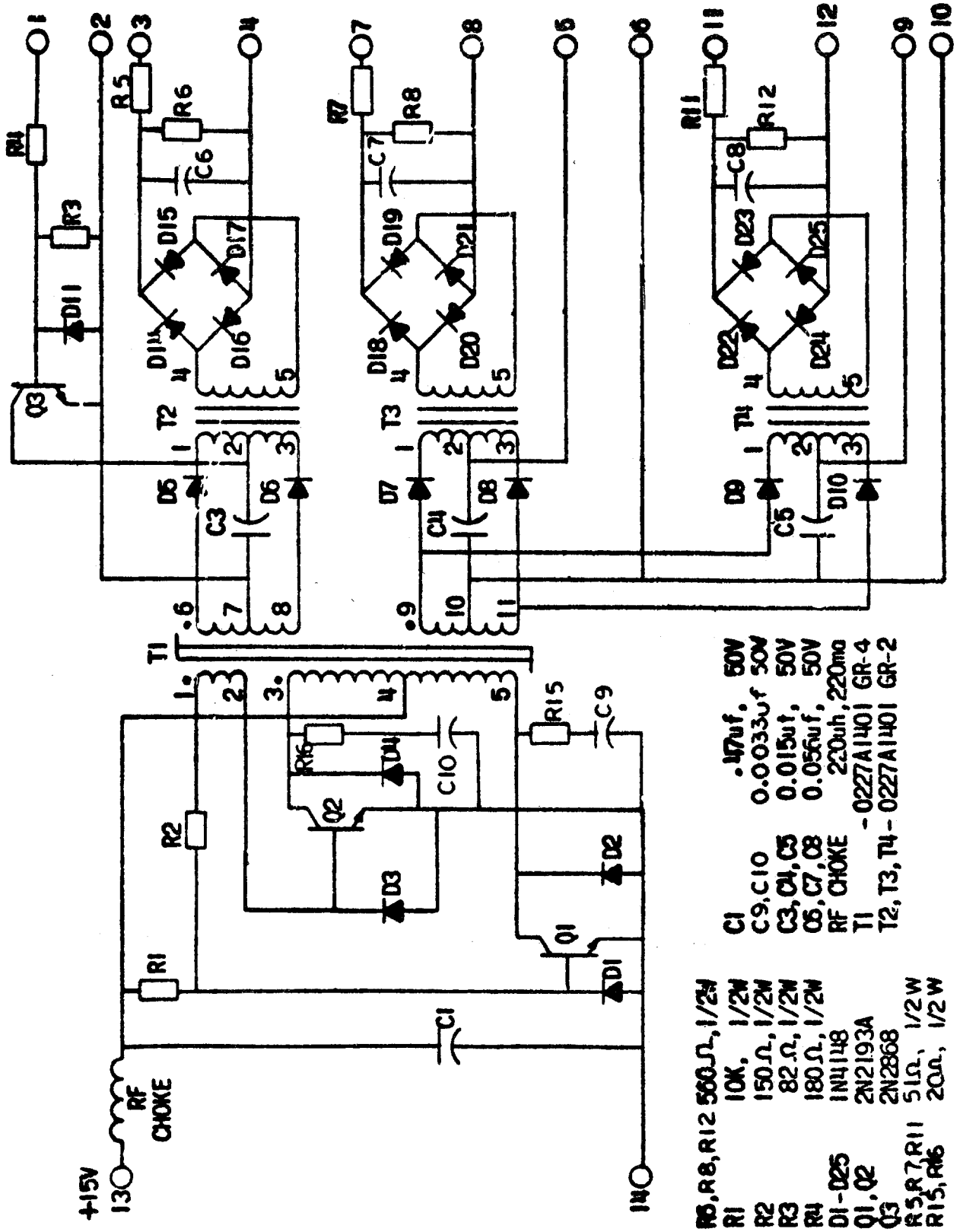
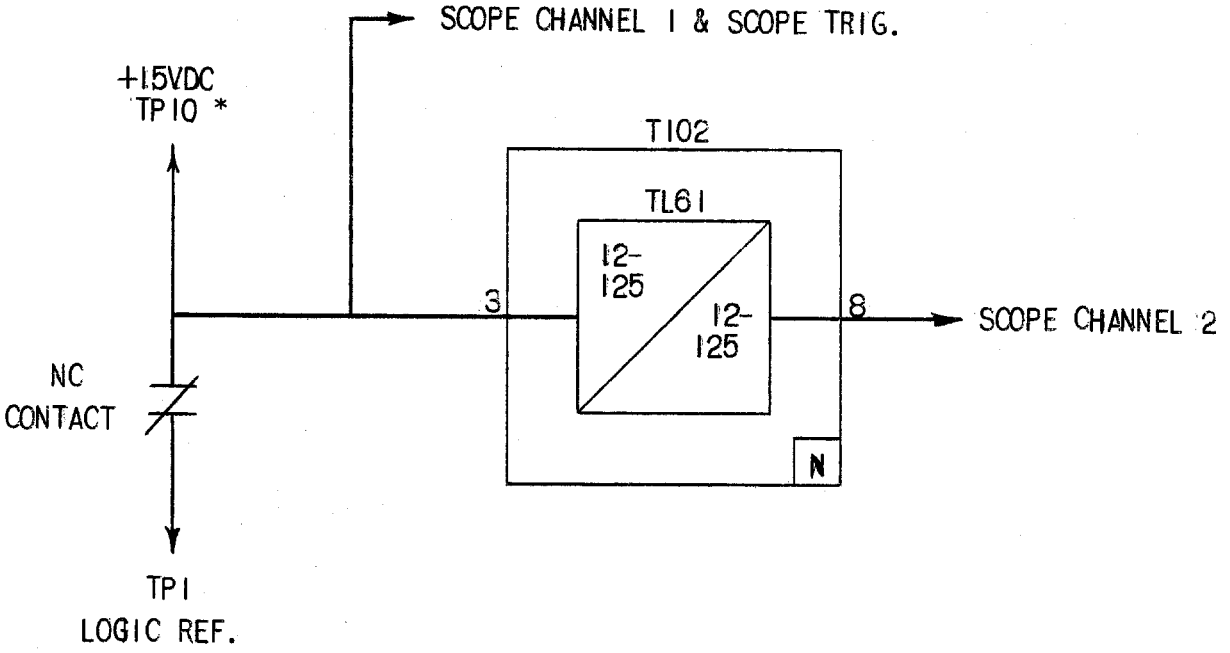


Fig. 6 (208A5504AJ-1) Isolation Interface Circuit



* THE 15VDC SIGNAL AT PIN 10 HAS A CURRENT LIMITING RESISTOR MOUNTED ON THE TEST CARD.

Fig. 7 (246A7987-0) Logic Timer Test Circuit