

AUXILIARY LOGIC RELAY

TYPE SLA55B

### GEK-49954

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#### AUXILIARY LOGIC RELAY

TYPE SLA55B

#### DESCRIPTION

The SLA55B is a solid state auxiliary logic relay that was designed specifically for use in a combined phase and directional comparison transmission line relaying scheme. The relay is intended to be used with a type SLDY51A relay which contains the necessary measuring functions that are required to implement the scheme. A suitable auxiliary tripping relay of the SLAT type and an SSA power supply are also required to complete the scheme. A C326B type carrier equipment is required for use with the SLA55B relay. For a complete description of the scheme in which the relay is applied, refer to the logic diagram and associated description supplied with the scheme.

The SLA55B relay is packaged in a four rack unit case suitable for mounting in a standard 19 inch rack. Outline and mounting dimensions are illustrated in Fig. 2. The internal connections for the complete SLA55B relay are shown in Fig. 1 while the component printed circuit card locations are shown in Fig. 3.

#### APPLICATION

The SLA55B is an auxiliary logic relay that is meant to be used with an SLDY51A relay in a combined phase and directional comparison transmission line relaying scheme. The SLA55B contains the necessary scheme logic and channel interface whereas the SLDY51A contains the necessary measuring functions for implementation of the scheme. Positive sequence distance functions are used to initiate directional comparison operation for three phase faults and negative sequence overcurrent functions are used to initiate phase comparison protection for all unbalanced faults. A suitable tripping relay and power supply are also required to complete the scheme.

All the functions shown in the SLA55B relay may not be included in every scheme. Some of the functions are optional and their uses will be dependent on the user's requirements or the specific requirements of the application. Where functions are omitted, they may easily be added at a future date by the insertion of appropriated printed circuit cards and/or jumpers if the need for them arises. It should be noted that other optional functions may also be required in the other relays when optional functions are added to the SLA55B. These too are readily added via appropriate printed circuit cards. Please refer to the associated logic diagram supplied with each scheme to determine the functions that are supplied with that scheme.

#### RATINGS

The Type SLA55B relay is designed for use in an environment where the air temperature outside the relay case does not exceed  $-20^{\circ}\text{C}$  or  $+65^{\circ}\text{C}$ .

The Type SLA55B relay requires +15VDC power source which can be obtained from a Type SSA power supply.

Each contact converter in this relay has a link for selecting the proper voltage for the coil circuit of the contact converter. The three possible voltages are 48 VDC, 125 VDC and 250 VDC.

These instructions do not purport to cover all details or variations in equipment nor to provide for every possible contingency to be met in connection with installation, operation or maintenance. Should further information be desired or should particular problems arise which are not covered sufficiently for the purchaser's purposes, the matter should be referred to the General Electric Company.

To the extent required the products described herein meet applicable ANSI, IEEE and NEMA standards; but no such assurance is given with respect to local codes and ordinances because they vary greatly.

#### BURDENS

The SLA55B relay presents a burden of 460 milliamperes to the +15 VDC supply and 60 milliamperes to the -15 VDC supply of the Type SSA power supply.

Each contact converter, when energized, will draw approximately 10 milliamperes from the station battery, regardless of tap setting.

#### OPERATING PRINCIPLES

#### LOGIC CIRCUIT

The functions of the Type SLA55B relay involve basic logic (AND, OR, and NOT) where the presence or absence of signals, rather than their magnitudes, controls the operation. Signals are measured with respect to a reference bus accessible at TP1. In general, a signal below one VDC represents an OFF or LOGIC ZERO condition; an ON or LOGIC ONE condition is represented by a signal of approximately +15 VDC.

The symbols used on the internal connection diagram (Fig. 1) are explained by the legend shown in Fig. 4.

The matrix block options shown in the internal connections of the SLA55B relay are provided at the factory. The connections are shown on the associated overall logic and are listed on the associated option chart. A sample option chart for the Type SLA55B relay is shown in Fig. 8.

#### CONTACT CONVERTERS

The purpose of this function is to convert a contact operation into a signal that is compatible with the logic circuit of the Type SLA55B relay. Those contact converters are labeled CC1, CC2, CC3 and CC4.

The contact converter output signals are wired to matrix blocks permitting selection to accommodate external control of such functions as transmitter keying, block pilot tripping or stop all carrier. When used to provide one input to AND2 whose second input comes from the positive sequence overcurrent function the contact converter becomes part of the line pickup scheme.

#### DATA MONITORING POINTS

Type SLA55B relay has provisions to provide data monitoring outputs. Some of the data monitoring (DLA) points are hard wired into the logic as shown in Fig. 1. Other data monitoring points are selected on the matrix blocks and are listed on the option chart. Any matrix block points which are not used for more than one connection may be monitored using the double leads 412, 414, 415 and 420.

#### CHANNEL INTERFACE

The logic of the Type SLA55B relay includes an isolation interface (Fig. 5) between the relays in the scheme and the associated channel. The circuitry of the isolation interface provides a signal path but maintains metallic isolation. This feature makes it possible to maintain isolation between the DC supply used for the relays and that employed by the channel.

#### TIMER CARDS

There are a number of timers in the SLA55B relay, some of which are meant to be set in the field, and others which are factory set and should need no further adjustment except in connection with corrective maintenance. All of them may not be included in every scheme. Refer to the logic description supplied with each scheme to determine which timers are included. Following is a brief description of the timers along with a general discussion of the various settings.

- $\overline{\text{TL-1}}$  This timer forms part of the out-of-step detection and is supplied only when out-of-step detection is required. The pickup setting determines the amount of time that the swing impedance must be in the out-of-step characteristic before an output will be permitted. In general, the lowest setting will permit the fastest swing to be detected. Longer pickup times will in general permit slower swings to be detected but will add to the scheme security. Pickup is adjustable over the range of two-to-four cycles. The dropout time is set at 40 milliseconds and needs no further adjustment.
- $\frac{\text{TL-2}}{\text{ment}}$  This timer is used to compensate for any phase delay that may be introduced by the channel equipment and signal propagation time. It permits an accurate comparison to be made at the COMPARER between the locally derived signal and the signal received from the remote terminal. Pickup and dropout times are adjustable over the range of one-to-eight milliseconds. The pickup and dropout setting are set equal to each other and must be made in the field after the equipment is installed.
- $\frac{\text{TL-3}}{\text{pickup}}$ . This timer follows the COMPARER and is commonly referred to as the TRIP INTEGRATOR timer. Its pickup, factory set at four milliseconds, has been selected to provide security and dependability to the scheme. Its dropout setting will depend on the particular application.
- $\overline{\text{TL-4}}$  This timer follows the receiver output and is used to adjust for any dissymetries that may be introduced by the channel equipment. Pickup and dropout time is adjustable over the range of 0.3-3.0 seconds. The pickup or dropout must be adjusted so that the output signal is symmetrical for a symmetrically applied keying signal to the transmitter at the remote end of the line. This adjustment must be made in the field after the equipment is installed.
- $\overline{\text{TL}-6}$  This timer is generally required when the scheme is applied on long lines with shunt reactors. It is used in conjunction with a low set level detector to provide very sensitive protection. Pickup time is adjustable over the range of 5-15 milliseconds. The dropout is factory set at 100 milliseconds. The timer measures the coincidence between the output of AND 9 (the comparer) and  $\overline{\text{TL}-3}$ , but this measuring will only take place if the low set level detector is picked up. The timer integrates and sums up the signals applied to it.

The output of TL-3 is the output of AND 9 delayed by four milliseconds, therefore TL-6 measures the coincidence between the output of AND 9 and the same signal delayed by four milliseconds. The coincidence signal is therefore the output of AND 9 minus four milliseconds. Since the maximum signal that AND 9 can produce is 8.33 milliseconds, the maximum coincidence that can be measured is 4.33 milliseconds and it occurs only once per cycle. If the pickup time of TL-6 is set at five milliseconds, at least two consecutive cycles must be compared before the timer can produce an output. Therefore with a timer pickup setting of five milliseconds, a delay of at least one cycle will be introduced into the trip path. Longer delays in the tripping can be attained by setting the pickup time of the timer accordingly.

- $\frac{\mathsf{TL-7}}{\mathsf{The}}$  This timer is meant to be used with a positive sequence voltage detector located in the SLDY relay. The two functions can be used to either provide a line pickup option or loss of voltage indication. The pickup and dropout time will depend on the particular application.
- $\frac{TL-8}{blocking}$  This timer is provided only when additional coordination time is required between the tripping and blocking functions at each end of the line. The pickup time is adjustable over the range of one-to-eight milliseconds. Dropout is set at zero milliseconds.
- $\overline{\text{TL-9}}$  This timer is used in conjunction with the phase-delay timer TL-2. It is required only in those applications where the combination of channel time and propagation are too long to be compensated for by a single phase delay timer. When this timer is used it is effectively in series with TL-2 and the total phase delay will be equal to the sum of the two individual timer settings. The dropout time of each timer must be set equal to its particular pickup time. Each individual timer setting should be approximately half the total setting.

#### CONSTRUCTION

The SLA55B relay is packaged in an enclosed metal case with hinged front covers and removable top cover. The outline and mounting dimensions of the case and the physical location of the components are shown in Figs. 2 and 3 respectively.

The SLA55B relay contains printed circuit cards identified by a code number such as All1, T102, L104 where A designates auxiliary function, T designates time-delay function, and L designates logic function. The printed circuit cards plug in from the front of unit. The sockets are marked with letter designations or "addresses" (D,E,F, etc.) which appear on the guide strips in front of each socket, on the component

location drawing, on the internal connection diagram and on the printed circuit card. The test points (TP1, TP2, etc.) shown on the internal connection diagram are connected to instrument jacks on a test card in position T or AT with TP1 at the top of the AT card. TP10 is tied to  $\pm 15$  VDC through a 1.5K resistor. This resistor limits the current when TP10 is used to supply a logic signal to a card.

Other logic options are selected by means of taper tip jumpers and matrix blocks. These matrix blocks are located in the rear of the unit as shown in Fig. 1. The green (G) matrix block has twenty individual points with points eight, nine and ten wired together. The yellow (Y) block has twenty points which are grouped in ten common points; 1 to 10 are tied to +15 VDC, 11 to 20 are tied to reference. The white, red, black and violet matrix blocks have 20 individual matrix points. A tool for inserting and removing the taper tip jumpers is supplied with each relay.

#### RECEIVING, HANDLING AND STORAGE

These relays will normally be supplied as a part of a static relay equipment, mounted in a rack or cabinet with other static relays and test equipment. Immediately upon receipt of a static relay equipment, it should be unpacked and examined for any damage sustained in transit. If injury or damage resulting from rough handling is evident, file a damage claim at once with the transportation company and promptly notify the nearest General Electric Sales Office.

Reasonable care should be exercised in unpacking the equipment. If the equipment is not to be installed immediately, it should be stored indoors in a location that is free from moisture, dust, metallic chips, and severe atmospheric contaminants.

Just prior to final installation the shipping support bolt should be removed from each side of all relay units, to facilitate possible future unit removal for maintenance. These shipping support bolts are approximately eight inches back from the relay front panel. Static relay equipment, when supplied in swing rack cabinets, should be securely anchored to the floor or to the shipping pallet to prevent the equipment from tipping over when the swing rack is opened.

#### **INSTALLATION TESTS**

#### CAUTION

LOGIC SYSTEM SIDE OF THE DC POWER SUPPLY USED WITH MOD III STATIC RELAY EQUIPMENT IS ISOLATED FROM GROUND. IT IS A DESIGN CHARACTERISTIC OF MOST ELECTRONIC INSTRUMENTS THAT ONE OF THE SIGNAL INPUT TERMINALS IS CONNECTED TO THE INSTRUMENT CHASSIS. IF THE INSTRUMENT USED TO TEST THE RELAY EQUIPMENT IS ISOLATED FROM GROUND, ITS CHASSIS MAY HAVE AN ELECTRICAL POTENTIAL WITH RESPECT TO GROUND. THE USE. OF A TEST INSTRUMENT WITH A GROUNDED CHASSIS WILL NOT AFFECT THE TESTING OF THE EQUIPMENT. HOWEVER, A SECOND GROUND CONNECTION TO THE EQUIPMENT, SUCH AS A TEST LEAD INADVERTENTLY DROPPING AGAINST THE RELAY CASE, MAY CAUSE DAMAGE TO THE LOGIC CIRCUITRY. NO EXTERNAL TEST EQUIPMENT SHOULD BE LEFT CONNECTED TO THE STATIC RELAYS WHEN THEY ARE IN PROTECTIVE SERVICE, SINCE TEST EQUIPMENT GROUNDING REDUCES THE EFFECTIVENESS OF THE ISOLATION PROVIDED.

#### GENERAL

If the SLA55B relay that is to be tested is installed in an equipment which has already been connected to the power system, disconnect the outputs in the associated Type SLAT relay from the system.

The SLA55B relay is supplied from the factory either mounted in a static relay equipment or as a separate unit associated with measuring relays, a Type SSA power supply, and some form of channel equipment. All relay units for a given terminal of static relaying equipment are tested together at the factory, and each unit will have the same summary number stamped on its nameplate.

In general, when a time range is indicated on the internal connection diagram, the timer has been factory set at a mid-range value. Timers should be set for the operating or reset times indicated on the associated overall logic diagram. Where a time range is indicated on the overall logic diagram, the timer should be set for the value recommended for that function in the descriptive writeup accompanying the overall logic diagram. Where a setting depends upon conditions encountered on a specific application, this is so stated and the factors influencing the choice of setting are described. The procedure for checking and setting the timers is described in a later section.

#### OPERATIONAL CHECKS

Operation of the SLA55B unit can be checked by observing the signals at the twenty test points (TP1 to TP20) in the SLA55B, by observing the operation of the associated channel equipment, or by observing the output functions in the associated Type SLAT tripping relay. The test points are located on two test cards in positions T and AT, and are numbered 1 to 20 from top to bottom. TP1 is the reference bus for the logic circuit; TP10 is at +15 VDC. The remaining points are located at various strategic points throughout the logic as shown on the internal connection diagram (Fig. 1). Test point voltages can be monitored with a portable high impedance voltmeter, the voltmeter on the test panel of the associated equipment, or an oscilloscope.

#### TEST CARD ADAPTER

The test card adapter provides a convenient means of gaining access to any pin of a particular card. Detailed information on the use of the test adapter card is included in the card instruction book, GEK-34158.

#### EQUIPMENT ADJUSTMENTS AND TESTS

The SLA55B relay is usually supplied from the factory, mounted and wired as part of a complete static relay equipment. There are several adjustments that must be made to this equipment in the field. The field adjustments that directly involve the SLA55B are indicated below.

- A. CT Phasing, Polarity and Sequence Check B. Channel Signal Symmetry Adjustment C. Phase Delay Adjustment

#### TESTING INSTRUCTIONS

#### CT Phasing, Polarity and Sequence Check

This test should be performed according to the instructions given in the instruction book for the measuring unit (SLDY relay). That book states that in making this check, one oscilloscope channel should be used to observe the received channel signal in the SLA. This signal can be observed at TP18 or TP19 in the SLA55B. Note that the voltage level at TP18 is zero when the received channel signal is in the BLOCKING half cycle. There is a positive signal at TP18 when the received channel signal is in the TRIP half cycle.

#### Channel Signal Symmetry Adjustment

The TL-4 timer located in position AE is provided for symmetry adjustment; it is used to compensate for any asymmetries that may be introduced by the channel equipment. The final settings for this timer must be made in the field after the transmitters, receivers and coupling equipment have been tuned and adjusted for proper sensitivity per the channel instructions. Operation of the squaring amplifier and fault detectors is required for accomplishment of the final symmetry adjustment; refer to the measuring unit instruction book for the recommended procedure.

In order to adjust these timer cards it is necessary to monitor the card's output with an oscilloscope. This can be accomplished by putting the card in a card adapter and connecting the oscilloscope input to Pin 8. Check the overall logic diagram to determine whether or not there is a test point that can be used to monitor the output of the symmetry timers. If a test point is used, it is not necessary to put the card in a card adapter.

#### Phase Delay Adjustment

After the symmetry adjustment has been accomplished, the phase alignment must be made. The purpose of this adjustment is to obtain the proper alignment of the local signal with the received signal; refer to the measuring unit instruction book for the recommended procedure.

Before the phase delay adjustment can be made, TP17 in the SLA55B of the local equipment must be connected to TP1; this causes a continuous blocking signal to be applied to the channel control logic and prevents the local transmission of a trip signal. There must also be a connection made in the SLAŠ5B of the remote equipment between TP1; this prevents the transmission of a continuous trip signal at the remote end.

In order to adjust the phase delay, the output of the phase delay timers (TL-2, position AL and TL-9, position G) must be monitored with an oscilloscope and compared to the received signal. A dual trace oscilloscope must be used and one of its inputs must be connected to the output of the symmetry timer; use the same monitoring point that was used during the symmetry adjustment. The second oscilloscope input must be connected to the output of the phase delay timer. The output of timer TL-2 can be monitored at TP6. If timer TL-9 is used in this equipment, the card in position "G" must be placed in a card adapter and the output monitored at Pin 8; check the overall logic diagram to determine whether or not there is a test point that can be used to monitor the output of timer TL-9.

When timers TL-2 and TL-9 are both used, they are effectively in series. The drop-out time of each timer must be set equal to its particular pickup time. The total phase delay will be equal to the sum of the two individual timer settings. Each individual timer setting should be approximately half the total setting.

#### TIMER ADJUSTMENTS AND TESTS

When the time delay cards are to be adjusted or checked, an oscilloscope that can display two traces simultaneously and that has a calibrated horizontal sweep should be used.

In order to test the timer cards it is necessary to remove the card previous to the timer (see Table I) and to place the timer card in a card adapter. The card adapter allows access to the input and output of the timer if they are not brought out on test points. The timer test circuit is shown in Fig. 6. Opening the normally closed contact causes the output to step up to +15 VDC after the pickup delay of the timer. To increase the pickup time turn the upper potentiometer on the timer card clockwise; to decrease the time turn it counterclockwise. Closing the contact causes the timer output to drop out after the reset time delay setting card. If the timer card is provided with a variable reset delay, it can be adjusted by the lower potentiometer on the timer card (clockwise increases reset time).

TABLE I

| TIME UNDER<br>TEST | POSITION | REMOVE CARD IN POSITION |
|--------------------|----------|-------------------------|
| TL1                | J        | H                       |
| TL2                | AL       | *                       |
| TL3                | AN       | AM                      |
| TL4                | AE       | **                      |
| TL6                | M        | AN,AM,AK                |
| TL7                | AS       | ***                     |
| TL8                | AC       | L                       |
| TL9                | G        | *                       |

- \* See the section on PHASE DELAY ADJUSTMENT for details on the adjustment of this timer.
- \*\* See the section on CHANNEL SIGNAL SYMMETRY ADJUSTMENT for details on the adjustment of this timer.
- \*\*\* Remove wires connected to Pins 3 and 4 on the card adapter. Connect the test circuit shown in Fig. 6 to Pins 3 and 4 of the card, through the terminals on the card adapter.

#### CONTACT CONVERTER TESTS

Operation of the contact converters can be checked by placing the contact coverter card in a card adapter, after checking that the voltage tap selected agrees with the station battery voltage. Connect the station DC through a switch to the appropriate pair of terminals of the terminal strip, AH, mounted on the rear of the relay. The terminal numbers and polarity of connections for each of the contact converters are shown in the internal connection diagram, Fig. 3. Output of the contact converter card may be monitored between Pin 8 and Pin 1 (reference) on the card adapter with either a scope or meter. Closure of the switch in the test source will provide a +15 volt DC signal at Pin 8 of the card adapter.

#### ISOLATION INTERFACE TESTS

Operation of the three functions (received carrier #1, auxiliary stop and transmitter control) of the isolation interface can be checked without direct connections to the subassembly. External test connections are made to the pins of the C111 socket mounted on the rear of the unit, see Fig. 3. Logic circuit test connections are made using a card adapter in position "AR".

#### ISOLATION INTERFACE TESTS

Received carrier operation test connections are shown in Fig. 7A. For this test do not remove channel control card in position "AR". Closure of the normally open contact will simulate a received carrier signal and scope display will go from a logic Zero to logic One.

For the transmitter control checks, remove the channel control card "AJ" from its socket and make the test connections shown in Figs. 7B and C. The test contact in the open position simulates a logic One condition, which initiates a transmitter control output producing a five-to-six volt DC signal across the output loading resistor. Closure of the normally open contact generates a logic Zero condition which holds off the transmitter control output of the isolation interface.

#### OVERALL EQUIPMENT TESTS

After the SLA55B relay and the associated static relay units have been individually calibrated and tested for the desired settings, a series of overall operating circuit checks is advisable.

The elementary, overall logic, and logic description for the specific job will be useful for determining the overall operation of the scheme.

Overall equipment tests can be per formed by applying AC current and voltages to the measuring units as specified in the instruction book for the measuring units and checking that proper outputs are obtained from the associated SLAT when measuring units operate.

#### MAINTENANCE

#### PERIODIC TESTS

It should be sufficient to check the outputs produced at test points in the SLA55B when periodic calibration tests are made on the associated measuring units, for example, the phase and ground relays in line relaying scheme. No separate periodic tests on the SLA55B itself should be required.

#### TROUBLESHOOTING

In any troubleshooting of equipment, it should first be established which unit is functioning incorrectly. The overall logic diagram supplied with the equipment shows the combined logic of the complete equipment and the various test points in each unit. By signal tracing, using the overall logic diagram and the various test points, it should be possible to quickly isolate the trouble.

A test adapter card is supplied with each static relay equipment to supplement the prewired test points on the test cards. Use of the adapter card is described in the card instruction book GEK-34158.

A dual-trace oscilloscope is a valuable aid to detailed troubleshooting, since it can be used to determine phase shift, operate and reset times as well as input and output levels. A portable dual-trace oscilloscope with a calibrated sweep and trigger facility is recommended.

#### SPARE PARTS

To minimize possible outage time, it is recommended that a complete maintenance program should include the stocking of at least one spare card of each type. It is possible to replace damaged or defective components on the printed circuit cards, but great care should be taken in soldering so as not to damage or bridge-over the printed circuit buses, or overheat the semi-conductor components. The repaired area should be recovered with a suitable high-dielectric plastic coating to prevent possible breakdowns across the printed buses due to moisture and dust. The wiring diagrams for the cards in the SLA55 relay are included in the card book, GEK-34158.

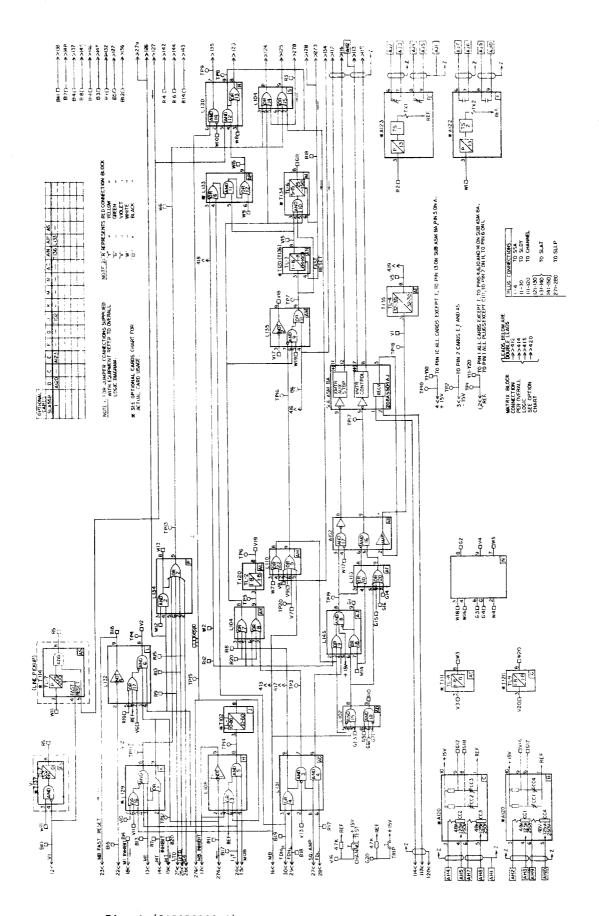


Fig. 1 (0138D3844-0) Internal Connections for the Type SLA55B Relay

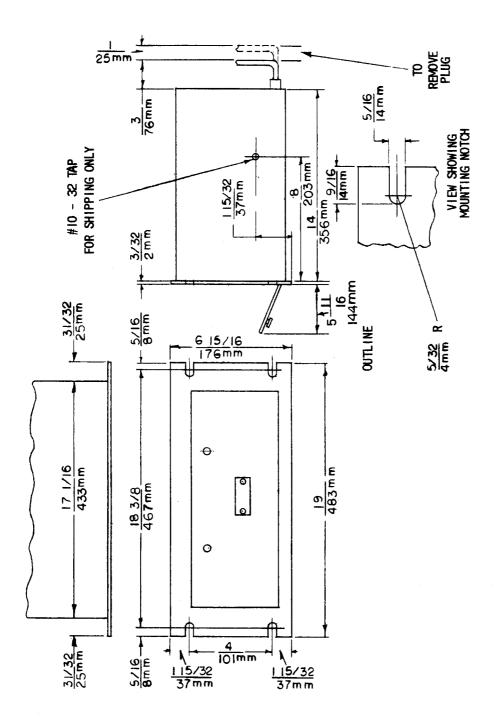


Fig. 2 (0227A2037-0) Outline and Mounting Dimensions for the Type SLA55B Relay

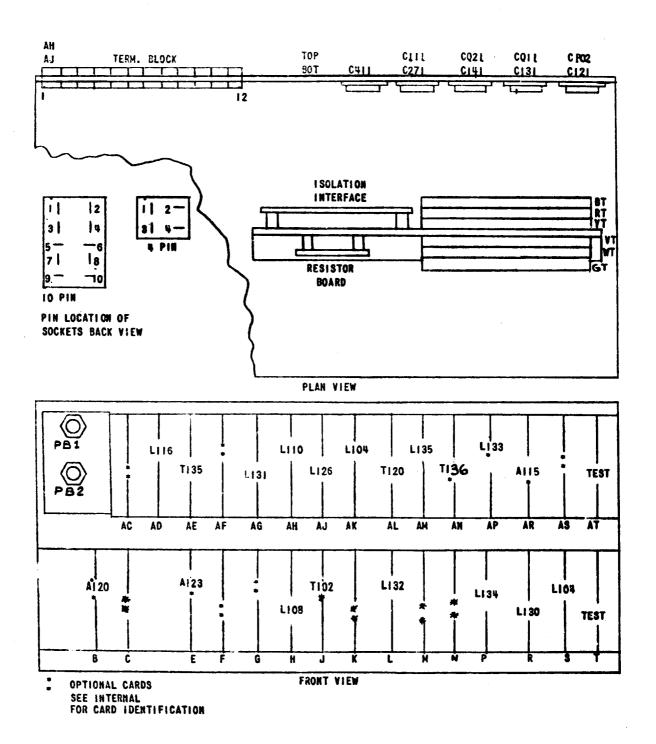


Fig. 3 (0275A3266-0) Component Location Diagram for the Type SLA55B Relay

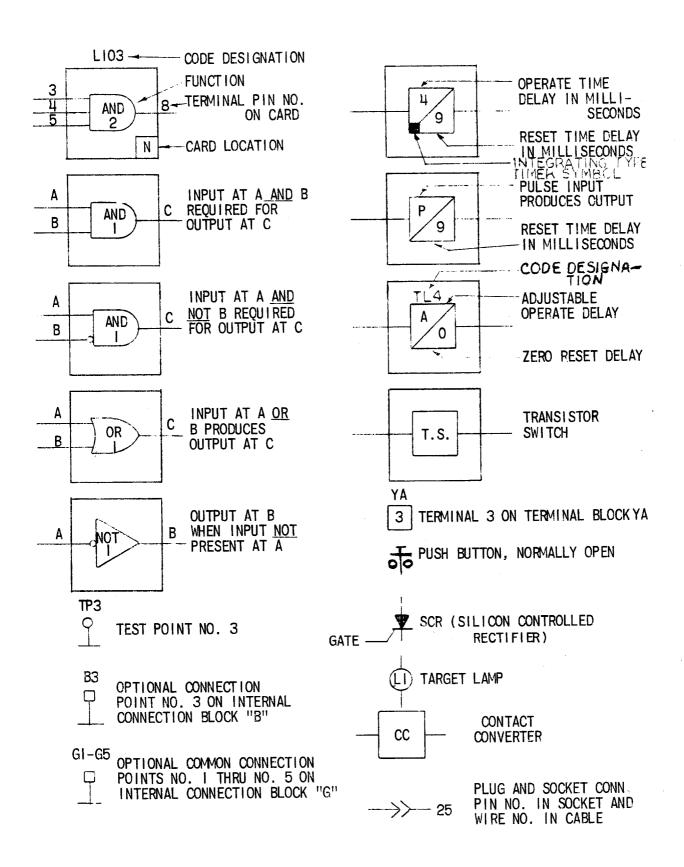


Fig. 4 (0227A2047-1) Logic and Internal Connection Diagram Legend

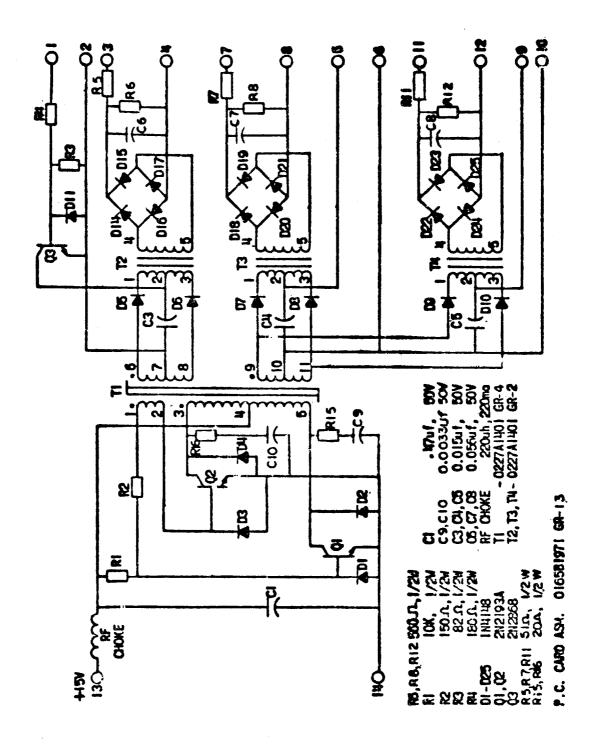
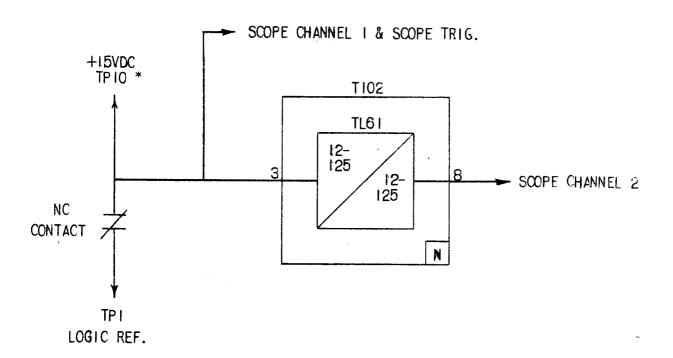
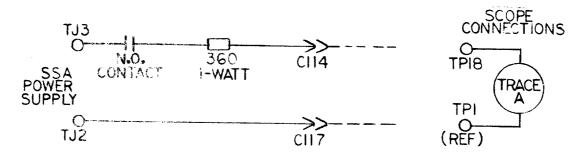


Fig. 5 (0208A5504AJ-1) Internal Connections for the Isolation Interface

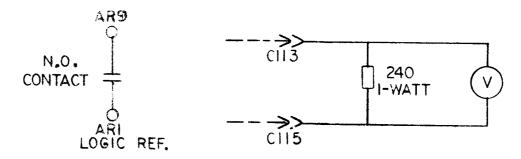


\* THE LOVDC SIGNAL AT PIN TO HAS A CURRENT LIMITING RESISTOR MOUNTED ON THE TEST CARD.

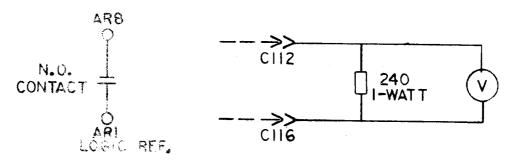
Fig. 6 (0246A7987-0) Logic Timer Test Circuit



## A-RECIEVED CARRIER TEST CONNECTIONS



## B-TRANSMITTER CONTROL TEST CONNECTIONS



C-TRANSMITTER AUXILIARY STOP TEST CONNECTIONS

Fig. 7 (0275A3275-0) Isolation Interface Test Circuit

THE FOLLOWING ARE FACTORY CONNECTIONS MADE AT THE MATRIX BLOCKS INSIDE OF THE SLA RELAY ASSOCIATED WITH THIS EQUIPMENT. SYMBOLS LISTED: PL=RELAY INTERCONNECTING CABLE LEAD
(5)=LOGIC FUNCTION CARD PIN NUMBER

= 3-WAY CONNECTION

X = DLA MONITOR CONNECTION AVAILABLE BUT NOT USED

| MATRIX<br>JUMPS | BLOCK<br>RS | LOGIC FU         | NCTION               | MATRIX<br>JUMPE  | BLOCK<br>RS  | LOGIC FU     | NCTION   |
|-----------------|-------------|------------------|----------------------|--|--------------|--------------|--|
| FROM            | ТО          | FROM             | TO                   | FROM   | TO           | FROM         | TO   |
| W7              | YII         | OR22(3)          | REF                  | G13  | Y10          | AND 15(3)    | +15  |
| <b># v8</b>     | Y12         | OR5(7)           | A                    | WIO  | Y 9          | ANDI4 (Z)    | +15  |
| <b>+</b> V9     | 412         | OR5(2)           |                      |  |              |              |  |
| #WB             | Y13         | OR13(3)          |                      |  |              |              |  |
|                 | 413         | OR12 (6)         |                      |  |              |              |  |
| <b>主 Y12</b>    | Y16         | OR 2 (5)         |                      |  |              |              |  |
| ± V13           | 416         | AND3(2)          |                      |  |              |              |  |
| # R13           | Y17         | JORZ (7)         |                      |  |              |              |  |
| # R15           | Y17         | OR2(2)           |                      |  |              |              |  |
|                 | Y18         | AND 17(4)        |                      |  |              |              |  |
| <b>‡</b> G14    | Y18         | OR20(2)          |                      |  |              |              |  |
| # B18           | 419         | OR4 (4)          | Y                    |  |              |              |  |
| <b>FR19</b>     | 419         | OR17(5)          | REF                  |  |              |              |  |
|                 |             | ļ                |                      |  |              |              |  |
|                 |             | <b> </b>         |                      |  |              | ļ            |  |
|                 |             |                  |                      |  |              | <del> </del> | ·····  |
| <del>- VI</del> | R2          | RCVR             | TX-1(3)<br>OR7(5)    |  |              |              |  |
| ‡ V2            | W2          | AND6(8)          |                      | <u> </u>   | <b> </b>     | <del> </del> |  |
| ‡ V2<br>V5      | R4          | ANDG(B)          | PL 142               |  |              |              |  |
|                 | V17         | TL4 (8)          | NOT 2(3)<br>AND 2(3) | <u> </u>   |              |              |  |
| <u> </u>        | W12<br>R14  | CC4(9)<br>TL3(8) | ANDZ                 |  | ļ            |              |  |
| V15             |             |                  | PL143                |  |              |              |  |
| V16             | G15         | PBI              | OR 20(6)             | and the same of th |              |              |  |
| <u> V18</u>     | V7          | NOT 2 (8)        | OR5 (6)<br>AND9 (5)  |  |              |              | r: Appliging Spellings, rest, risk sugar, Clarinum problem, 100 derignes relablishensa 2   |
| V19<br>G8       | W19<br>B5   | TL-2 (8)         | PL122                |  |              |              |  |
| <u> </u>        | V6          | TL-1(8)          | AND6(7)              | A ST SE OF SECTION SEC |              |              |  |
| <u>G17</u>      | W14         | (2)              | OR18(7)              |  |              |              |  |
| 620             | RZO         | PB2              | OR7 (4)              |  |              |              | THE RESERVE THE PARTY OF THE PA |
| RIT             | G16         | PL28             | OR 20(7)             |  |              | <b>†</b>     |  |
| WG              | 88          | OR2 (9)          | PL 145               |  | <del> </del> |              |  |
| R 8             | R6          |                  | PL144                | <b></b>  | <b>†</b>     |              | CONTRACTOR  |
|                 | RII         | PL14             | ANO6(3)              |  | <u> </u>     |              |  |
|                 | 1 1511      | 17614            | 14406(3)             | L  | L            | L            |  |

Fig. 8 (0227A2050-0 Sh. 183) Sample Option Chart for the Type SLA55 Relay

# GENERAL ELECTRIC COMPANY POWER SYSTEMS MANAGEMENT BUSINESS DEPT.

