



INSTRUCTIONS

GEK-65590

STATIC LOGIC AUXILIARY RELAY

TYPE SLA52N

GENERAL  ELECTRIC

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**STATIC LOGIC AUXILIARY RELAY
TYPE SLA52N**

DESCRIPTION

The Type SLA52N relay is a solid state, rack mounted auxiliary logic unit which provides the logic for a directional comparison scheme. Other solid state relays, a power supply, and a test panel are required for a complete protective system.

APPLICATION

Refer to the overall logic diagram and its associated logic description for the particular scheme in which this relay is employed for an application guide.

RATINGS

The Type SLA52N relay is designed for use in an environment where the air temperature outside the relay case does not exceed minus 20°C or plus 65°C.

The Type SLA52N relay requires a plus or minus 15 VDC power source which can be obtained from a Type SSA power supply.

Each contact converter in this relay has a link for selecting the proper voltage for the coil circuit of the contact converter. The three possible voltages are 48 VDC, 125 VDC and 250 VDC.

BURDENS

The SLA52N relay presents a maximum burden of 250 milliamperes to the plus 15 VDC supply of the Type SSA power supply.

Each contact converter, when energized, will draw ten milliamperes from the station battery, regardless of tap setting.

OPERATING PRINCIPLES

LOGIC CIRCUIT

The functions of the Type SLA52N involve basic logic (AND, OR, and NOT) where the presence or absence of signals, rather than their magnitude, controls the operation. Signals are measured with respect to a reference bus accessible at TP1. In general, a signal below one VDC represents an OFF or LOGIC ZERO condition; an ON or LOGIC ONE is represented by a signal of approximately plus 15 VDC.

These instructions do not purport to cover all details or variations in equipment nor to provide for every possible contingency to be met in connection with installation, operation or maintenance. Should further information be desired or should particular problems arise which are not covered sufficiently for the purchaser's purposes, the matter should be referred to the General Electric Company.

To the extent required the products described herein meet applicable ANSI, IEEE and NEMA standards; but no such assurance is given with respect to local codes and ordinances because they vary greatly.

The symbols used on the internal connection diagram (Fig. 1) are explained by the legend shown in Fig. 2.

The matrix blocks shown on the internal connections diagram of the SLA52N are connected by jumpers at the factory. These connections are used to implement the logic arrangement shown on the associated overall logic diagram. These matrix jumpers are listed on the associated option chart. A typical option chart for the Type SLA52N relay is shown in Fig. 3. Some of the matrix block connections may be customer options. These connections will then be shown as optional connections on the overall logic and must be selected by the user before the unit is placed in service.

CONTACT CONVERTERS

The purpose of the contact converters (CC1, CC2, CC3, CC4) included in the Type SLA52N relay is to convert a contact operation into a signal that is compatible with the logic circuitry of the relay. When the external contact is closed, a plus 15 VDC signal is produced by the contact converter.

The function of contact converters (CC1, CC2, CC3, CC4) depends upon the scheme in which the relay is employed.

The contact converters are incorporated into the relay through matrix point connections. This type of incorporation provides many specialized circuit arrangements to individual customer's present and future needs.

DATA MONITORING POINTS

The Type SLA52N relay has provision for eighteen data monitoring outputs. The data monitoring (DLA) points are connected to key points in the relay logic via matrix block connections. A data logging amplifier (Type DLA) relay is used to translate the logic signals into usable outputs.

CONSTRUCTION

The SLA52N relay is packaged in an enclosed metal case with hinged front covers and removable top cover. The outline and mounting dimensions of the case and the physical location of the components are shown in Fig. 4 and 5, respectively.

The SLA52N relay contains printed circuit cards identified by a code number, such as A111, T102, L104; where A designates auxiliary function, T designates time-delay function, and L designates logic function. The printed circuit cards plug in from the front of the unit. The sockets are marked with letter designations or "addresses" (D, E, F, etc.) which appear on the guide strips in front of each socket, on the component location drawing, on the unit internal connection diagram, and on the printed circuit card. The test points (TP1, TP2, etc.) shown on the internal connection diagram are connected to instrument jacks on a test card in position T or AT with TP1 at the top of the AT card. TP10 is tied to plus 15 VDC through a 1.5K resistor. This resistor limits the current when TP10 is used to supply a logic signal.

Logic options in the SLA52N relay are selectable by means of jumper wires with taper tip pins on each end which are used to interconnect the matrix block points. These matrix blocks are located in the rear of the unit as shown in Fig. 5. The top cover of the relay must be removed to make the blocks accessible. The taper tip jumpers should be inserted and removed using the special tools which are supplied with each equipment. Red (R), orange (O), green (G), violet (V), white (W), black (B) and brown (BR) matrix points are connected as indicated on the internal connection diagram, Fig. 1; Y1 to Y10 are connected to plus 15 VDC, Y11 to Y20 are connected to reference.

RECEIVING, HANDLING AND STORAGE

These relays will normally be supplied as part of a static relay equipment, mounted in a rack or cabinet with other static relays and test equipment. Immediately upon receipt of a static relay equipment, it should be unpacked and examined for any damage sustained in transit. If injury or damage resulting from rough handling is evident, file a damage claim at once with the transportation company and promptly notify the nearest General Electric Sales Office.

Reasonable care should be exercised in unpacking the equipment. If the equipment is not to be installed immediately, it should be stored indoors in a location that is free from moisture, dust, metallic chips, and severe atmospheric contaminants.

Just prior to final installation the shipping support bolt should be removed from each side of all relay units, to facilitate possible future unit removal for maintenance. These shipping support bolts are approximately eight inches back from the relay front panel. Static relay equipment, when supplied in swing rack cabinets, should be securely anchored to the floor or to the shipping pallet to prevent the equipment from tipping over when the swing rack is opened.

INSTALLATION TESTS

CAUTION

THE LOGIC SYSTEM SIDE OF THE DC POWER SUPPLY USED WITH MOD III STATIC RELAY EQUIPMENT IS ISOLATED FROM GROUND. IT IS A DESIGN CHARACTERISTIC OF MOST ELECTRONIC INSTRUMENTS THAT ONE OF THE SIGNAL INPUT TERMINALS IS CONNECTED TO THE INSTRUMENT CHASSIS. IF THE INSTRUMENT USED TO TEST THE RELAY EQUIPMENT IS ISOLATED FROM GROUND, ITS CHASSIS MAY HAVE A ELECTRICAL POTENTIAL WITH RESPECT TO GROUND. THE USE OF A TEST INSTRUMENT WITH A GROUNDED CHASSIS WILL NOT AFFECT THE TESTING OF THE EQUIPMENT. HOWEVER, A SECOND GROUND CONNECTION TO THE EQUIPMENT, SUCH AS A TEST LEAD INADVERTENTLY DROPPING AGAINST THE RELAY CASE, MAY CAUSE DAMAGE TO THE LOGIC CIRCUITRY. NO EXTERNAL TEST EQUIPMENT SHOULD BE LEFT CONNECTED TO THE STATIC RELAYS WHEN THEY ARE IN PROTECTIVE SERVICE, SINCE TEST EQUIPMENT GROUNDING REDUCES THE EFFECTIVENESS OF THE ISOLATION PROVIDED.

GENERAL

If the SLA52N relay that is to be tested is installed in an equipment which has already been connected to the power system, disconnect the outputs in the associated Type SLAT relay from the system.

The SLA52N relay is supplied from the factory either mounted in a static relay equipment or as a separate unit associated with measuring relays, a Type SSA power supply, and some form of channel equipment. All relay units for a given terminal of static relaying equipment are tested together at the factory, and each unit will have the same summary number stamped on its nameplate.

In general, when a time range is indicated on the internal connection diagram, the timer has been factory set at a mid-range value. Timers should be set for the operating or reset times indicated on the associated overall logic diagram. Where a time range is indicated on the overall logic diagram, the timer should be set for the value recommended for that function in the descriptive write-up accompanying the overall logic diagram. Where a setting depends upon conditions encountered on a specific application, this is so stated and the factors influencing the choice of setting are described. The procedure for checking and setting the timers is described in a later section.

OPERATIONAL CHECKS

Operation of the SLA52N unit can be checked by observing the signals at the twenty test points (TP1 to TP20) in the SLA52N, by observing the operation of the associated channel equipment, or by observing the output functions in the associated Type SLAT tripping relay. The test points are located on two test cards in positions T and AT, and are numbered 1 to 20 from top to bottom. TP1 is the reference bus for the logic circuit; TP10 is at plus 15 VDC. The remaining points are located at various strategic points throughout the logic as shown on the internal connection diagram (Fig. 1). Test point voltages can be monitored with a portable high impedance voltmeter, the voltmeter on the test panel of the associated equipment, or an oscilloscope.

TEST CARD ADAPTER

The test card adapter provides a convenient means of gaining access to any pin of a particular card. Detailed information on the use of the test adapter card is included in the card instruction book, GEK-34158.

TIMER ADJUSTMENTS AND TESTS

When the time-delay cards are to be adjusted or checked, an oscilloscope that can display two traces simultaneously, and that has a calibrated horizontal sweep, should be used.

In order to test the timer cards it is necessary to remove the card previous to the timer and to place the timer card in a card adapter. The card adapter allows access to the input and output of the timer if they are not brought out on test points. The timer test circuit is shown in Fig. 6. Opening the normally closed contact causes the output to step up to plus 15 VDC after the pickup delay of the timer. To increase the pickup time, turn the upper potentiometer on the timer card clockwise; to decrease the time, turn it counterclockwise. Closing the contact causes the timer output to drop out after the reset time-delay setting of the card. If the timer card is provided with a variable reset delay, it can be adjusted by the lower potentiometer on the timer card (clockwise increases reset time).

CONTACT CONVERTER TESTS

Operation of the contact converters can be checked by placing the contact converter card in a card adapter, after checking that the voltage tap selected agrees with the station battery voltage. Connect the station direct current through a switch to the appropriate pair of terminals of the terminal strip, AH, mounted on the rear of the relay. The terminal numbers and polarity of connections for each of the contact converters are shown in the internal connection diagram, Fig. 1. Output of the contact converter card may be monitored between pins 8 or 9 and pin 1 (reference) on the card adapter with either a scope or meter. Closure of the switch in the test source will provide a plus 15 VDC signal at the output of the contact converter.

OVERALL EQUIPMENT TESTS

After the SLA52N relay and the associated static relay units have been individually calibrated and tested for the desired settings, a series of overall operating circuit checks is advisable.

The elementary, overall logic and logic description for the specific job will be useful for determining the overall operation of the scheme.

Overall equipment tests can be performed by applying alternating current and voltages to the measuring units as specified in the instruction book for the measuring units and checking that proper outputs are obtained from the associated SLAT when measuring units operate.

MAINTENANCE

PERIODIC TESTS

It should be sufficient to check the outputs produced at test points in the SLA52N when periodic calibration tests are made on the associated measuring units, for example, the positive and negative sequence relays in line-relaying scheme. No separate periodic tests on the SLA52N itself should be required.

TROUBLESHOOTING

In any troubleshooting of equipment, it should first be established which unit is functioning incorrectly. The overall logic diagram supplied with the equipment shows the combined logic of the complete equipment and the various test points in each unit. By signal tracing, using the overall logic diagram and the various test points, it should be possible to quickly isolate the trouble.

A test adapter card is supplied with each static relay equipment to supplement the prewired test points on the test cards. Use of the adapter card is described in the card instruction book, GEK-34158.

A dual trace oscilloscope is a valuable aid to detailed troubleshooting, since it can be used to determine phase shift, operate and reset times, as well as input and output levels. A portable dual-trace oscilloscope with a calibrated sweep and trigger facility is recommended.

SPARE PARTS

To minimize possible outage time, it is recommended that a complete maintenance program should include the stocking of a least one spare card of each type. It is possible to replace damaged or defective components on the printed circuit cards, but great care should be taken in soldering so as not to damage or bridge-over the printed circuit buses, or overheat the semiconductor components. The repaired area should be recovered with a suitable high-dielectric plastic coating to prevent possible breakdowns across the printed buses due to moisture and dust. The wiring diagrams for the cards in the SLA52N relay are included in the card book, GEK-34158.

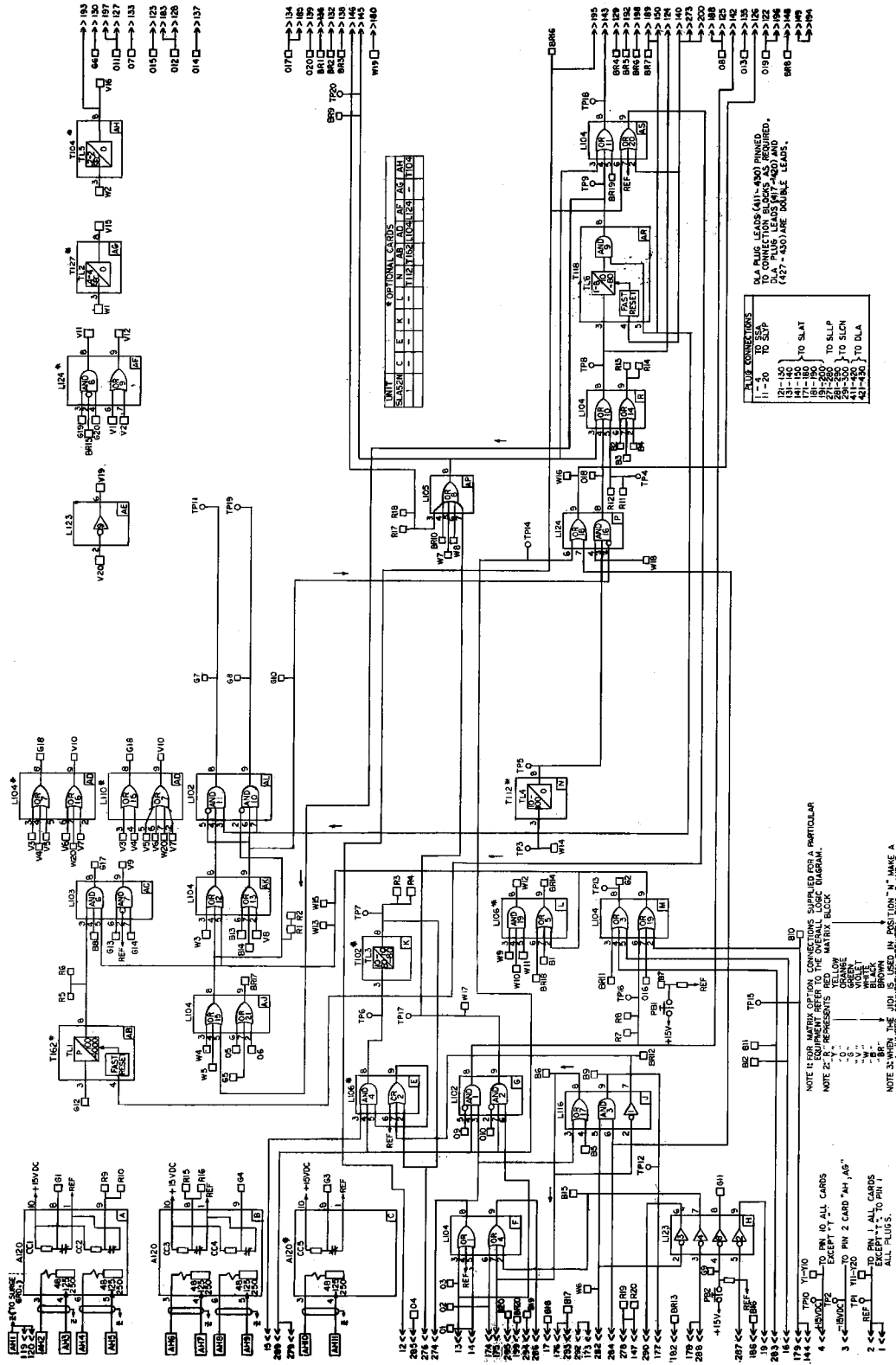


Fig. 1 (0145D7168-0) Internal Connection Diagram for the Type SLA52N Relay

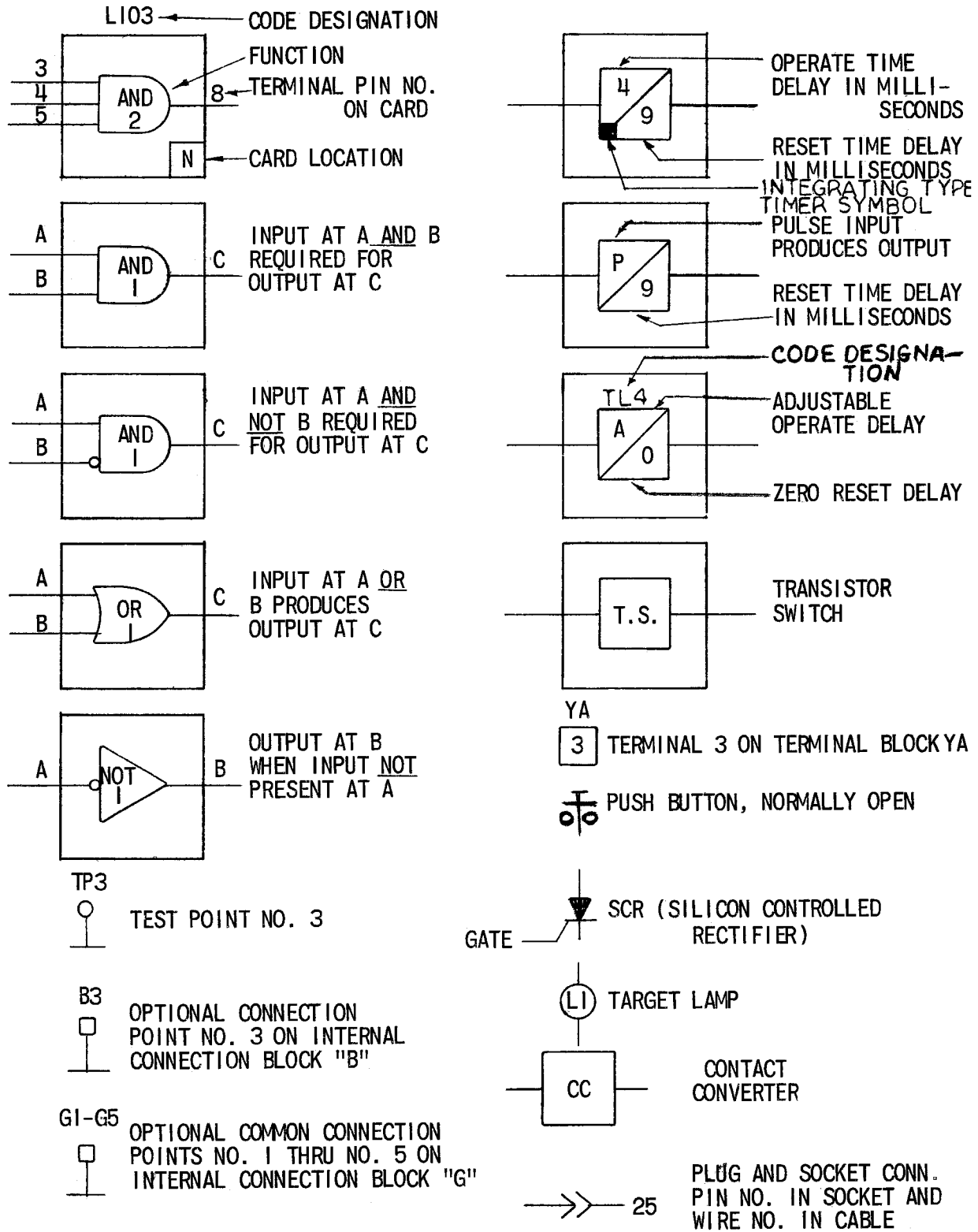


Fig. 2 (0227A2047-1) Internal Connection Diagram Legend

THE FOLLOWING ARE FACTORY CONNECTIONS MADE AT THE MATRIX BLOCKS INSIDE OF THE SLA RELAY ASSOCIATED WITH THIS EQUIPMENT.
 SYMBOLS LISTED: PL=RELAY INTERCONNECTING CABLE LEAD
 (5)=LOGIC FUNCTION CARD PIN NUMBER
 ‡=3-WAY CONNECTION
 * =DLA MONITOR CONNECTION AVAILABLE BUT NOT USED
 Δ= 4 WAY CONNECTION (0227A 2024 G-31) 223

MATRIX BLOCK JUMPERS		LOGIC FUNCTION		MATRIX BLOCK JUMPERS		LOGIC FUNCTION	
FROM	TO	FROM	TO	FROM	TO	FROM	TO
B12	O10	PL016	AND2	W20	Y14	OR16	REF.
O9	Y11	AND1	REF	#B9	V6	AND3	OR16
B11	BR15	PL2B3	AND8	#B9	B10	AND3	OR19
R5	B5	TL1	OR17	V11	BR10	AND8	OR8
V12	G19	OR9	AND8	G18	R18	OR7	OR8
W6	G20	PL2B2	AND8	R17	BR2	OR7	PL132
O4	V1	PL2B5	OR9	W7	Y15	OR8	REF.
B19	V2	PL296	OR9	W8	Y16	OR8	REF.
O2	Y12	OR4	REF	BR19	Y17	OR11	REF.
BR16	O15	PL012	PL123	O18	BR1	AND16	PL136
G4	G12	CC4	TL1	R11	Y18	OR10	REF.
R6	G13	TL1	AND7				
W16	G14	OR18	AND7				
V9	V3	AND7	OR7	O17	O14	PL134	PL137
G17	V4	AND6	OR7	BR8	BR5	PL148	PL192
#V16	V5	TL5	OR7	W13	BR3	OR19	PL138
#V16	R20	TL5	PL147	#G7	O12	AND11	PL128
#V10	W2	OR16	TL5	G8	O8	AND10	PL125
#V10	O7	OR16	PL133				
R10	BR11	CC2	OR3				
G1	W5	CC1	OR15				
B8	Y1	AND6	+15VDC				
W15	W14	OR19	TL4	O13	Y19	PL135	REF
AG2	G10	OR3	AND16	#O19	Y20	PL122	REF
AG2	O20	OR3	PL139	#W4	Y20	OR15	REF
#R15	V20	CC3	NOT9				
#R15	BR4	CC3	PL129				
R16	O5	CC3	OR21				
V19	W18	NOT9	AND16	BR12	B18	NOT1	PL017
BR17	G6	OR21	PL130				
AG2	G5	OR3	OR21				
#G7	O6	AND11	OR21				
W3	Y13	OR12	REF.				
B7	O16	FB1	OR19				
R8	V7	AND1	OR16				

Fig. 3 (0227A2050-1, Sh. 223) Typical Option Chart for the Type SLA52N Relay

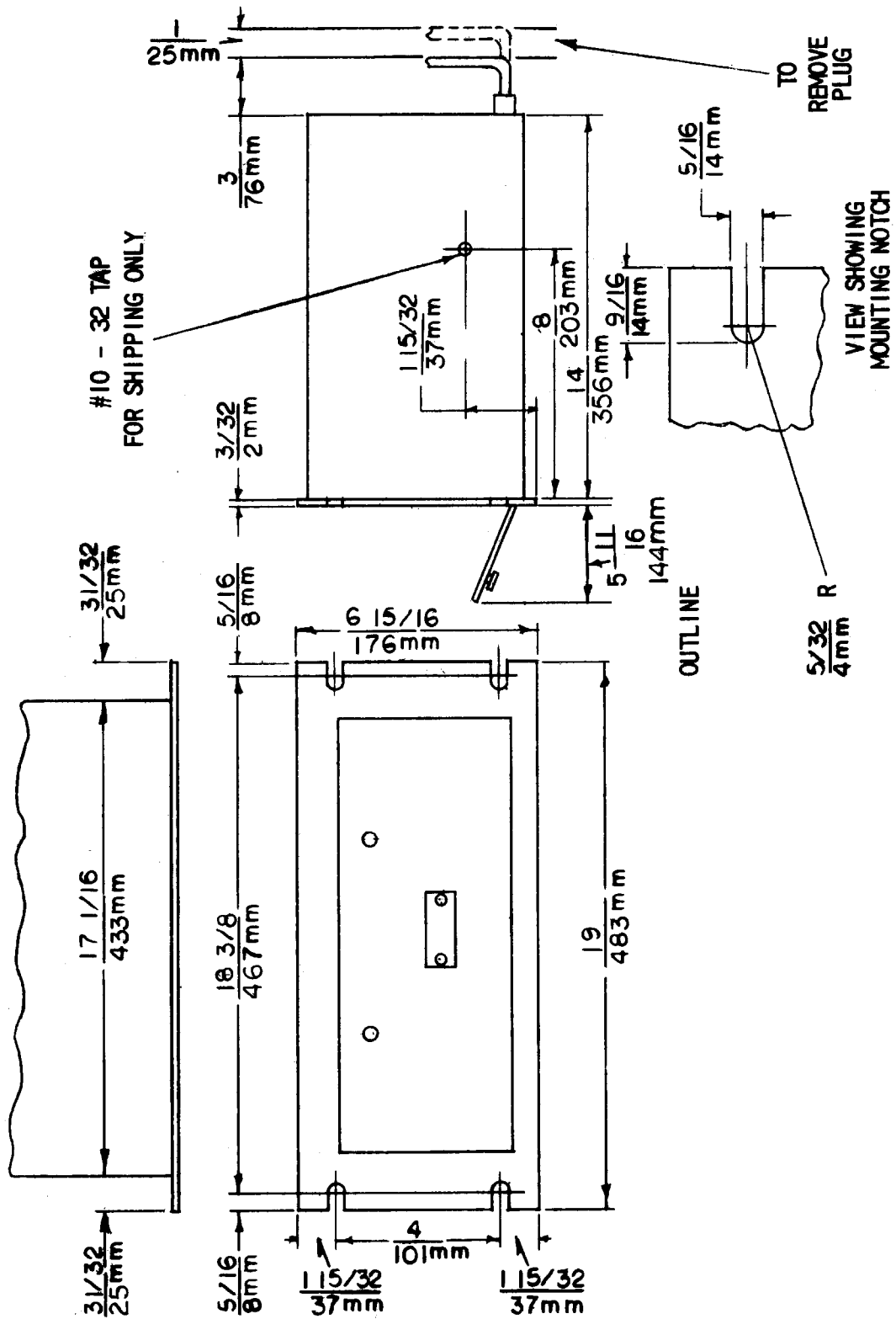
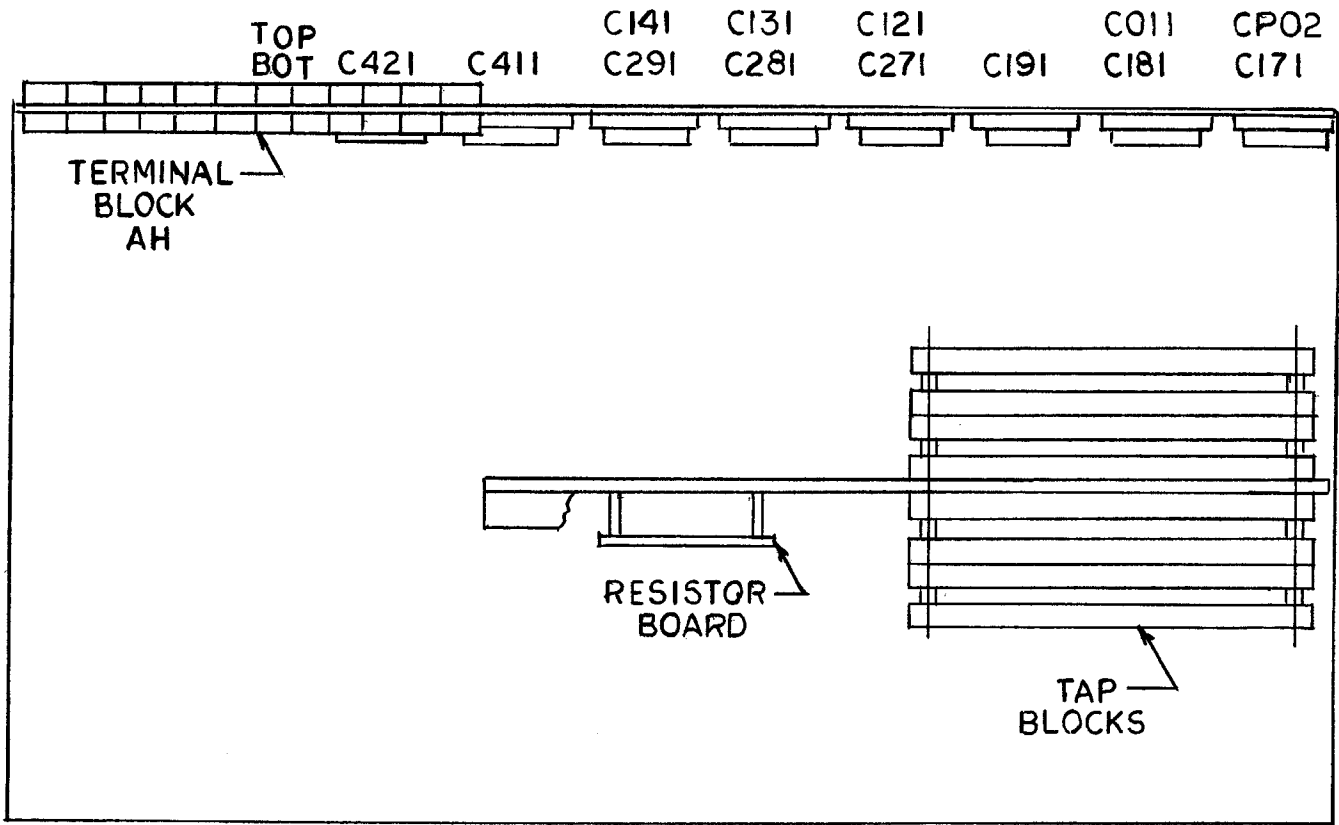
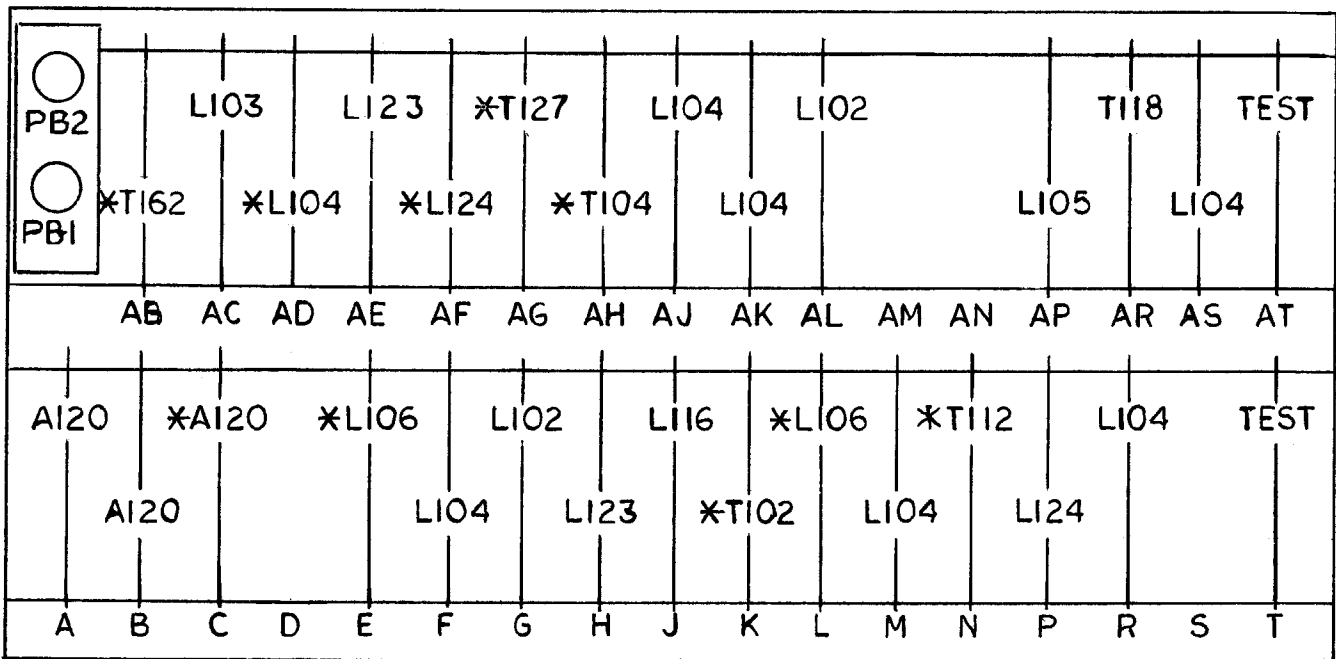


Fig. 4 (0227A2037-0) Outline and Mounting Dimensions



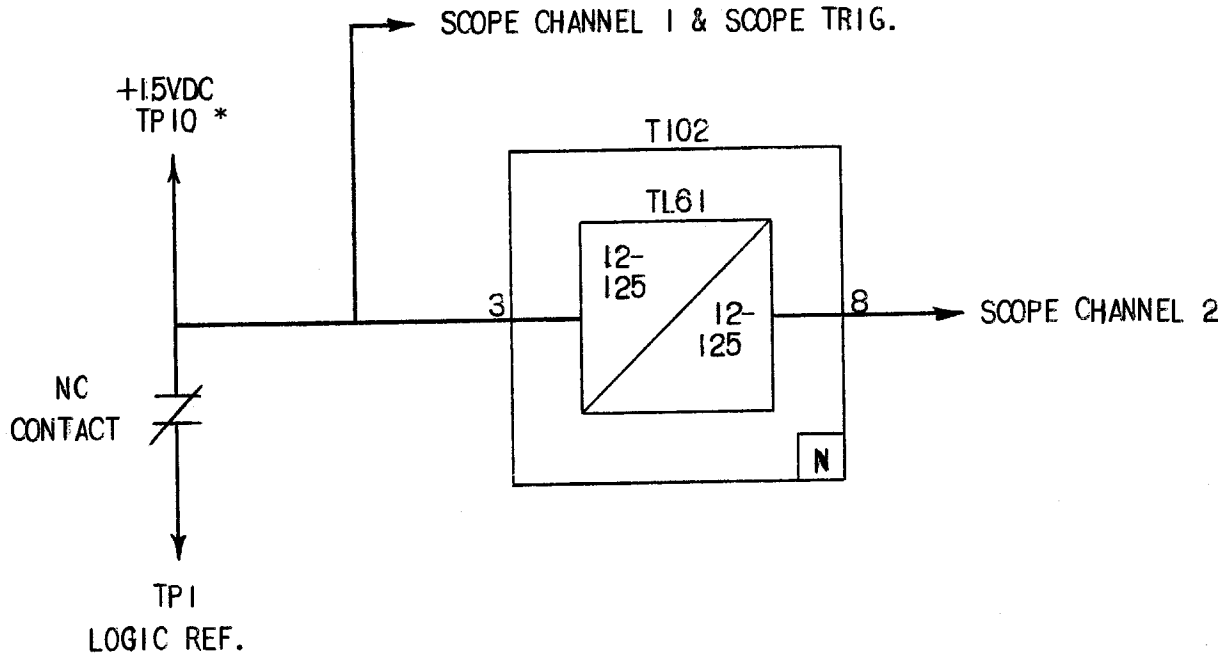
PLAN VIEW



* OPTIONAL

FRONT VIEW

Fig. 5 (0285A5604-0) Component Location Diagram for the SLA52N Relay



* THE 15VDC SIGNAL AT PIN 10 HAS A CURRENT LIMITING RESISTOR MOUNTED ON THE TEST CARD.

Fig. 6 (0246A7987-0) Logic Timer Test Circuit

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