INSTRUCTIONS

GEK-65667

AUXILIARY LOGIC RELAY

TYPE SLA54G

GENERAL ELECTRIC

CONTENTS

AUXILIARY LOGIC UNIT

TYPE SLA54G

DESCRIPTION

The SLA54G is an auxiliary logic relay designed for use in permissive overreaching transferred trip schemes. The relay contains the necessary logic to interpret output signals from associated measuring functions and translate them to an appropriate auxiliary output and tripping relay. In addition to the SLA54G relay, proper phase and ground relays, a power supply, and auxiliary tripping relay are required to complete a particular relaying scheme.

The SLA54G relay is packaged in a four-rack unit enclosed metal case. The relay is suitable for mounting in a 19-inch rack; the outline and mounting dimensions are shown in Fig. 1. Internal connections for the SLA54G relay are shown in Fig. 2, and the component location drawing is shown in Fig. 3.

APPLICATION

The SLA54G auxiliary logic relay is designed to operate in conjunction with appropriate phase and ground relays and a suitable communication channel to provide a permissive overreaching transferred tripping scheme for transmission line protection. For complete information on this scheme refer to the overall logic diagram and the accompanying logic description in which this relay is used.

Protection features required in a relay scheme often vary with the particular application. It is sometimes desirable to initially provide certain features in a relaying scheme and simultaneously to make provisions for adding or changing features should it later become necessary. To this end, this relay design has incorporated circuit flexibility to permit implementation of certain optional features. To implement these features the relay is equipped with matrix connection blocks designated R, Y, OR, V, W, G and B. Appropriate jumper connections are made between the various points to modify the logic. A typical option chart is shown in Fig. 5. Some examples of functional logic available are:

1. The choice of out-of-step blocking of either tripping or reclosing.

2. Bypassing of overcurrent supervision of phase MT functions.

3. The addition of I_W and I_{0W} overcurrent detectors for weak source terminal applications.

Various points in the logic can be monitored by connecting jumpers from the cable plug 411-420 to the selected matrix points. This option is further described under the heading DATA MONITORING POINTS in the section entitled **OPERATING PRINCIPLES.**

For the specific options and the logic arrangement supplied for a particular relaying scheme, refer to the logic diagram and the logic description supplied with that scheme. If it is desired to make logic changes, the diagrams and instruction books supplied with the equipment should be studied to determine the means for implementing the changes. If further assistance is required, contact the nearest General Electric District Sales Office.

There are no measuring functions to be set in this relay but there are certain timers included that must be set in accordance with the demands of the particular protection scheme being employed and the power system on which it is being used. Refer to the section of this book entitled **SETTINGS** for a description of these timers and for suggestions to be used in making appropriate settings.

RATINGS

The Type SLA54G relay is designed for use in an environment where the air temperature outside the relay case does not exceed minus 20°C or plus 65°C.

The Type SLA54G relay requires a plus or minus 15 volt DC power source which can be obtained from a Type SSA power supply.

Each contact converter in this relay has a link for selecting the proper voltage for the coil circuit on the contact converter. The three possible voltages are 48 VDC, 125 VDC and 250 VDC.

BURDENS

The SLA54G relay presents a burden of 300 milliamperes to the plus 15 VDC supply of the Type SSA power supply.

Each contact converter, when energized, will draw ten milliamperes from the station battery, regardless of tap setting.

OPERATING PRINCIPLES

LOGIC CIRCUIT

The functions of the Type SLA54G relay involve basic logic (AND, OR, and NOT) where the presence or absence of signals, rather than their magnitude, controls the operation. Signals are measured with respect to a reference bus accessible at TP1. In general, a signal below one VDC represents an OFF or LOGIC ZERO condition; an ON or LOGIC ONE condition is represented by a signal of approximately plus 15 VDC.

The symbols used on the internal connection diagram (Fig. 2) are explained by the legend shown in Fig. 4.

The matrix block options shown in the internal connections of the SLA54G relay are prewired at the factory. The connections are shown on the associated overall logic and are listed on the associated option chart. A sample option chart for the Type SLA54G relay is shown in Fig. 5.

CONTACT CONVERTERS

Eight contact converters are provided in the SLA54G relay. A contact converter provides an interface between the logic circuits in the SLA54G and the external signals.

CC1 is hard wired to key the channel transmitter via "OR16" and "AND16."

CC2 is hard wired to block "AND7" via "OR20," and to block "AND15" directly.

CC3 through CC8 are connected to option points (see Fig. 2) and can be connected as desired. To determine the connections used on a particular equipment, see the corresponding option chart drawing.

MONITORING POINTS

Various points within the relay logic are brought out to a cable plug mounted on the back of the SLA54G relay. This plug provides nine monitoring points plus one point for a voltage reference. Specific points that have been preselected are shown on the logic diagram marked with a number series of 411 to 420. These points may be augmented or readily changed at the matrix boards located inside the SLA relay. To monitor these points, an additional piece of equipment called a DLA (data logging amplifier) is required. The dry contact outputs from the DLA can be fed to an oscillograph to record selected function responses. A typical selection of monitoring points is shown below:

413 - Phase overcurrent

414 - Ground overcurrent

415 - Phase overcurrent

416 - Phase distance measurement output

417 - Ground distance measurement output

418 - Local comparer input

419 - Remote comparer input

420 - Comparer output

CHANNEL INTERFACE

The logic of the Type SLA54G relay includes an isolation interface (Fig. 6) between the relays in the scheme and the associated channel. The circuitry of the isolation interface provides a signal path but maintains metallic isolation. This feature makes it possible to maintain isolation between the DC supply used for the relays and that employed by the channel.

When pins 9 and 10 are both connected to relay reference, a metallically separate positive logic signal appears at pin 11 with respect to 12. The output from the isolation interface is a 5 VDC, 20 milliampere signal.

SETTINGS

The following timers in the SLA54G relay may require field adjustments.

A/40 (TL1 - Location AG)

The 2.5/16 timer found in the SLY62A and the A/40 timer are part of the out-of-step detection scheme. The 2.5/16 timer forms a "tomato" (outer) characteristic; thus the distance a swing must travel before the mho (inner) characteristic is encountered is determined by the pickup setting of this timer. The A/40 timer is used to measure the time of travel between the outer and inner characteristic. An out-of-step condition will be detected when both timers are adjusted properly. The setting of both timers should be based on the results of system swing studies. However, lower pickup settings of the 2.5/16 timer (larger tomato characteristic) in conjunction with short pickup settings on the A/40 timer will enable the out-of-step protection to detect faster swings. The pickup setting of the 2.5/16 timer should not be made too low so that it may operate on load or minor swings.

B/O - C/O (TL2 - Location AB and TL4 - Location AC)

These timers may be used to provide the necessary coordination to prevent relay false tripping which might otherwise result from a current reversal occurring during the clearing of a parallel line fault. An analysis of the conditions and the necessary timer settings will be found in the logic description for the particular relay scheme being used. If these timers are not needed, they should be removed and replaced with jumper cards.

D/D (TL7 - Location AE)

The D/D timer is used to coordinate the operation of the circuit breaker "b" switch with the operation of the main poles of the breaker for keying the channel transmitter. Refer to the analysis of these conditions and the suggested timer settings discussed in the logic description for the particular relay scheme being used.

E/O (TL3 - Location AF and TL5 - Location AD)

These are generally used as Zone 2 timers. Refer to the logic description of the particular equipment for a detailed discussion on these timers.

TL8 (Location S)

This is the trip integrating timer following the comparer. This timer delays tripping for security margin against false tripping.

TL6 (Location AM)

This timer can be used in the line energizing, direct tripping circuit. Refer to the logic description of the particular equipment for a detailed discussion on this timer.

TIMER SETTINGS

In general, when a time range is indicated on the internal connection diagram, the timer has been factory set at a mid-range value. Timers should be set for the operating or reset times indicated on the associated overall logic diagram. When a time range is indicated on the overall logic diagram, the timer should be set at the value recommended for that function in the descriptive writeup accompanying the overall logic diagram. When a setting depends upon conditions encountered on a specific application, this is so stated and the factors influencing the choice of setting are described. The procedure for checking and setting the timers is described below.

When the time-delay cards are to be adjusted or checked, an oscilloscope that can display two traces simultaneously and that has a calibrated sweep should be used.

In order to test the timer cards it is necessary (due to the "sinking logic" technique used in this equipment) to remove the card previous to the timer under test (see Table I) and to place the timer card in a card adapter. The card adapter allows access to the input and output of the timer if they are not brought out on test points. The timer test circuit is shown in Fig. 7. Opening the normally closed contact causes the output to step up to plus 15 VDC after the pickup delay of the timer. To increase the pickup time, turn the upper potentiometer on the timer card clockwise; to decrease the time, turn it counterclockwise. Closing the contact causes the timer output to drop out after the reset time-delay setting of the card. If the timer card is provided with a variable reset relay, it can be adjusted by the lower potentiometer on the timer card (clockwise increases reset time).

A timer tester card (0172C5151G-1) can be obtained to be used instead of the test circuit of Fig. 7. This card is equipped with an "ON" and "OFF" push-button switch, an "ON" indicating LED, and two parallelled test jacks. This test card can be plugged into any printed circuit card socket (except the "T" location). One test jack connects, via a test lead, to the input of the timer under test. The second test jack connects to trigger the timing device used. This timer test card provides a bounceless switching action, ease of operation and consistent results.

TABLE I

TIMER UNDER TEST	POSITION	REMOVE CARD IN POSITION
TL1 33-67/40	AG	SEE OPTION CHART
TL2 2-16/0	AB	SEE OPTION CHART
TL3 0.1-2 sec/0	AF	SEE OPTION CHART
TL4 2-16/0	AC	SEE OPTION CHART
TL5 0.1-2 sec/0	AD	SEE OPTION CHART
TL6 25-50/0	AM	SEE OPTION CHART
TL7 25-200/25-200	AE	SEE OPTION CHART
TL8 1-8/10-80	S	AH

OPERATIONAL CHECKS

Operation of the SLA54G unit can be checked by observing the signals at the twenty test points (TP1 to TP20) in the SLA54G, by observing the operation of the associated channel equipment, or by observing the output functions in the associated Type SLAT tripping relay. The test points are located on two test cards in positions T and AT and are numbered 1 to 20 from top to bottom. TP1 (on card AT) is at reference bus for the logic circuit; TP10 is at plus 15 VDC. The remaining points are located at various strategic points throughout the logic as shown on the internal connection diagram (Fig. 2). Test point voltages can be monitored with a portable high impedance voltmeter, the voltmeter on the test panel of the associated equipment, or an oscilloscope.

OVERALL EQUIPMENT TESTS

After the SLA54G relay and the associated static relay units have been individually calibrated and tested for the desired settings, a series of overall operating circuit checks is advisable.

The elementary, overall logic, and logic description for the specific job will be useful for determining the overall operation of the scheme.

Overall equipment tests can be performed by applying alternating currents and voltages to the measuring units as specified in the instruction books for the measuring units and checking that proper outputs are obtained from the associated SLAT when the measuring units operate.

CONSTRUCTION

The SLA54G relay is packaged in an enclosed metal case with hinged front covers and removable top cover. The outline and mounting dimensions of the case and the physical location of the components are shown in Fig. 1 and 3, respectively.

The SLA54G relay contains printed circuit cards identified by a code number, such as A120, T102, L104 where A designates auxiliary function, T designates time-delay function, and L designates logic function. The printed circuit cards plug in from the front of the unit. The sockets are marked with letter designations or "addresses" (D, E, F, etc.) which appear on the guide strips in front of each socket, on the component location drawing, on the internal connection diagram, and on the printed circuit card. The test points (TP1, TP2, etc.) shown in the internal connection diagram are connected to instrument jacks on a test card in position T or AT with TP1 at the top of the AT card. TP10 is tied to plus 15 VDC through a 1.5K resistor. This resistor limits the current when TP10 is used to supply a logic signal to a card.

Other logic options are selected by means of taper tip jumpers and matrix blocks. These matrix blocks are located inside the unit as shown in Fig. 3. The red (R) matrix block has 20 points in ten two-point common groups. The black (B) matrix block has 20 individual matrix points. The yellow (Y) matrix block has 20 matrix points which are grouped in ten common points: one to ten are tied to plus 15 VDC, 11 to 20 are tied to reference. The orange (OR) block has 20 individual points identical to the black (B). The violet (V) is also identical to the black (B). Tools for inserting and removing the taper tip jumpers are supplied with each relay.

RECEIVING, HANDLING AND STORAGE

These relays will normally be supplied as part of a static relay equipment, mounted in a rack or cabinet with other static relays and test equipment. Immediately upon receipt of a static relay equipment, it should be unpacked and examined for any damage sustained in transit. If injury or damage resulting from rough handling is evident, file a damage claim at once with the transportation company and promptly notify the nearest General Electric Sales Office.

Reasonable care should be exercised in unpacking the equipment. If the equipment is not to be installed immediately, it should be stored indoors in a location that is free from moisture, dust, metallic chips, and severe atmospheric contaminants.

Just prior to final installation the shipping support bolt should be removed from each side of all relay units, to facilitate possible future unit removal for maintenance. These shipping support bolts are approximately eight inches back from the relay front panel. STATIC RELAY EQUIPMENT, WHEN SUPPLIED IN SWING RACK CABINETS, SHOULD BE SECURELY ANCHORED TO THE FLOOR OR TO THE SHIPPING PALLET TO PREVENT THE EQUIPMENT FROM TIPPING OVER WHEN THE SWING RACK IS OPENED.

INSTALLATION TESTS

CAUTION

THE LOGIC SYSTEM SIDE OF THE DC POWER SUPPLY USED WITH MOD III STATIC RELAY EQUIPMENT IS ISOLATED FROM GROUND. IT IS A DESIGN CHARACTERISTIC OF MOST ELECTRONIC INSTRUMENTS THAT ONE OF THE SIGNAL INPUT TERMINALS IS CONNECTED TO THE INSTRUMENT CHASSIS. IF THE INSTRUMENT USED TO TEST THE RELAY EQUIPMENT IS ISOLATED FROM GROUND, ITS CHASSIS MAY HAVE A ELECTRICAL POTENTIAL WITH RESPECT TO GROUND. THE USE OF A TEST INSTRUMENT WITH A GROUNDED CHASSIS WILL NOT AFFECT THE TESTING OF THE EQUIPMENT. HOWEVER, A SECOND GROUND CONNECTION TO THE EQUIPMENT, SUCH AS A TEST LEAD INADVERTENTLY DROPPING AGAINST THE RELAY CASE, MAY CAUSE DAMAGE TO THE LOGIC CIRCUITRY. NO EXTERNAL TEST EQUIPMENT SHOULD BE LEFT CONNECTED TO THE STATIC RELAYS WHEN THEY ARE IN PROTECTIVE SERVICE, SINCE TEST EQUIPMENT GROUNDING REDUCES THE EFFECTIVENESS OF THE ISOLATION PROVIDED.

MAINTENANCE

PERIODIC TESTS

It should be sufficient to check the outputs produced at test points in the SLA54G when periodic calibration tests are made on the associated measuring units, for example, the phase and ground relays in the line relaying scheme. No separate periodic tests on the SLA54G itself should be required.

TROUBLESHOOTING

In any troubleshooting of equipment, it should first be established which unit is functioning incorrectly. The overall logic diagram supplied with the equipment shows

the combined logic of the complete equipment and the various test points in each unit. By signal tracing, using the overall logic diagram and the various test points, it should be possible to quickly isolate the trouble.

A test adapter card is supplied with each static relay equipment to supplement the prewired test points on the test cards. Use of the adapter card is described in the card instruction book, GEK-34158.

A dual-trace oscilloscope is a valuable aid to detailed troubleshooting, since it can be used to determine phase-shift, operate and reset times, as well as input and output levels. A portable dual-trace oscilloscope with a calibrated sweep and trigger facility is recommended.

SPARE PARTS

To minimize possible outage time, it is recommended that a complete maintenance program should include the stocking of at least one spare card of each type. It is possible to replace damaged or defective components on the printed circuit cards, but great care should be taken in soldering so as not to damage or bridge-over the printed circuit buses, or overheat the semiconductor components. The repaired area should be recovered with a suitable high-dielectric plastic coating to prevent possible breakdowns across the printed buses due to moisture and dust. The wiring diagrams for the cards in the SLA54G relay are included in the card book, GEK-34158.

GENERAL

The SLA54G relay is supplied from the factory either mounted in a static relay equipment or as a separate unit associated with measuring relays, a Type SSA power supply, and some form of channel equipment. All relay units for a given terminal of static relaying equipment are tested together at the factory, and each unit will have the same summary number stamped on its nameplate.

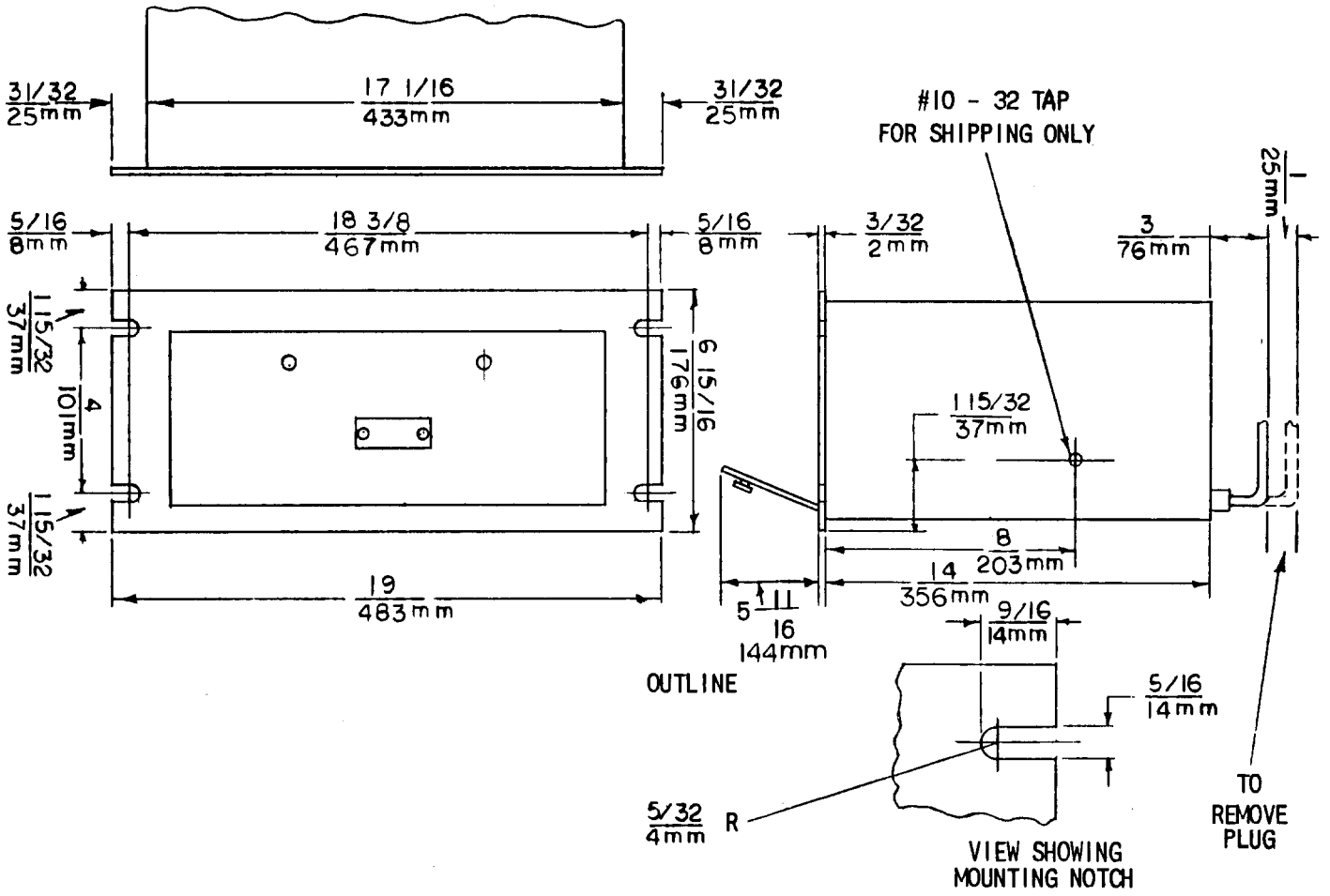


Fig. 1 (0227A2037-1) Outline and Mounting Dimensions
for the SLA54G Relay

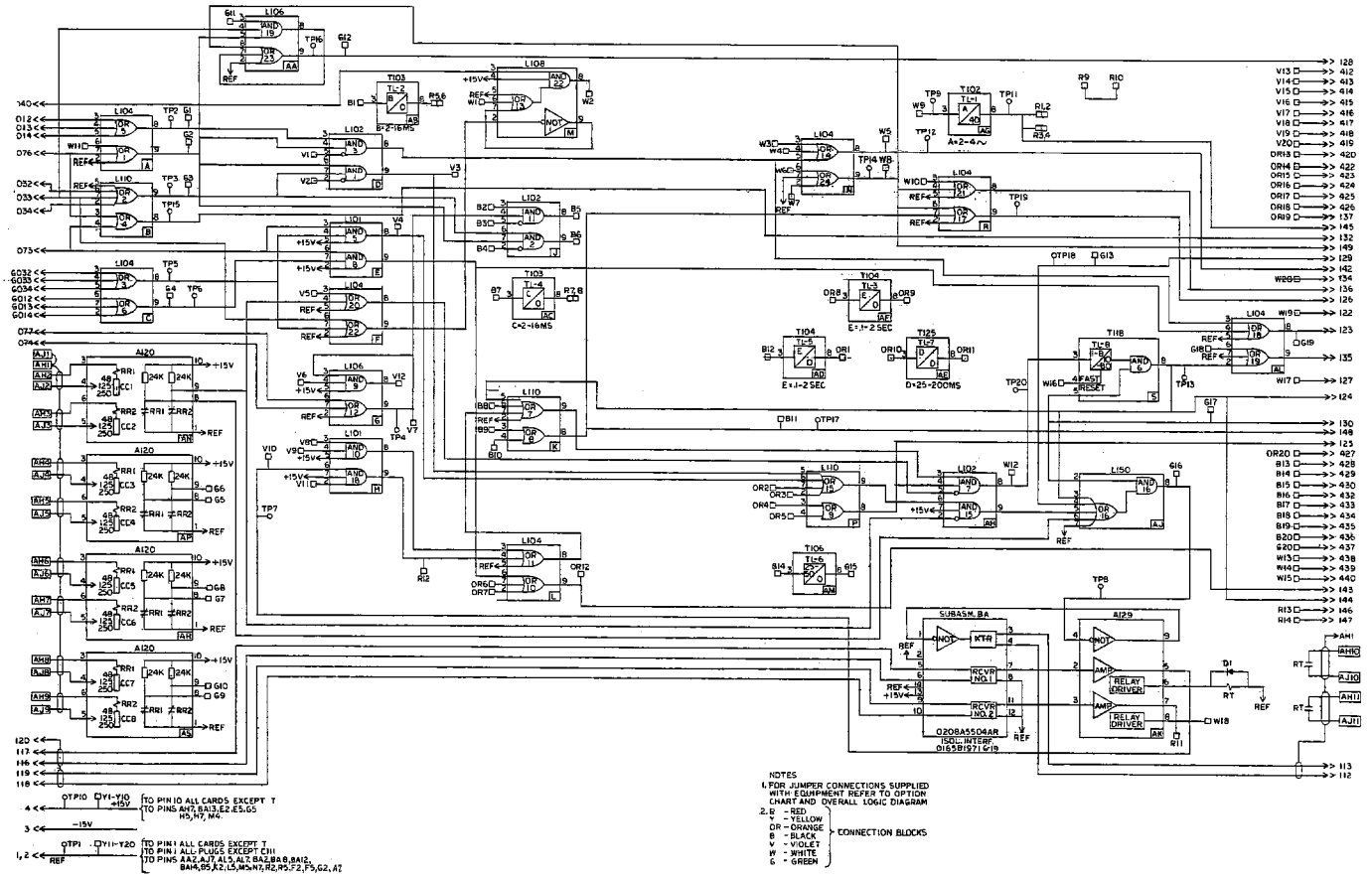


Fig. 2 (0145D8084-1) Internal Connections for the Type SLA54G Relay

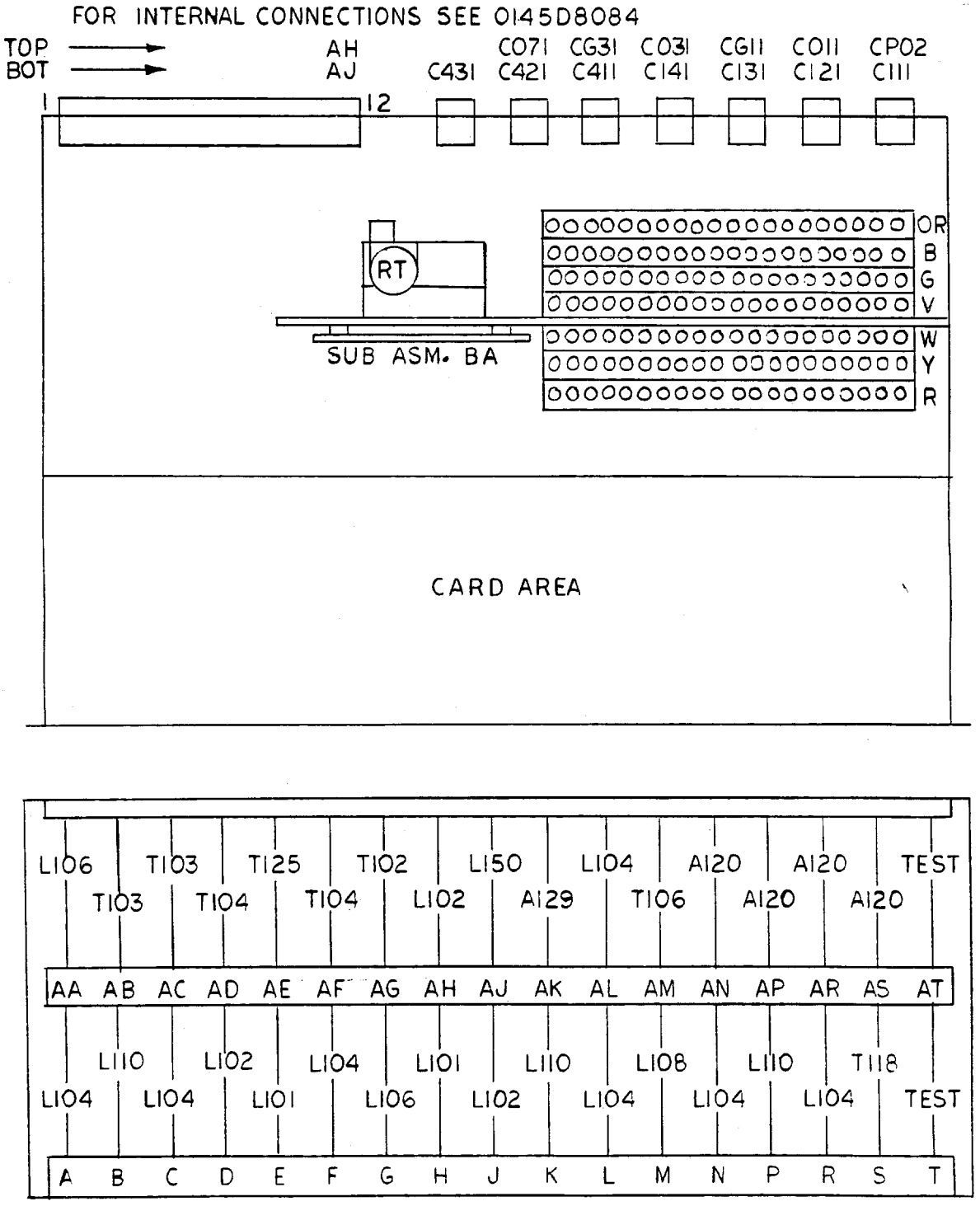


Fig. 3 (0285A5756-0) Component Location Diagram for the Type SLA54G Relay

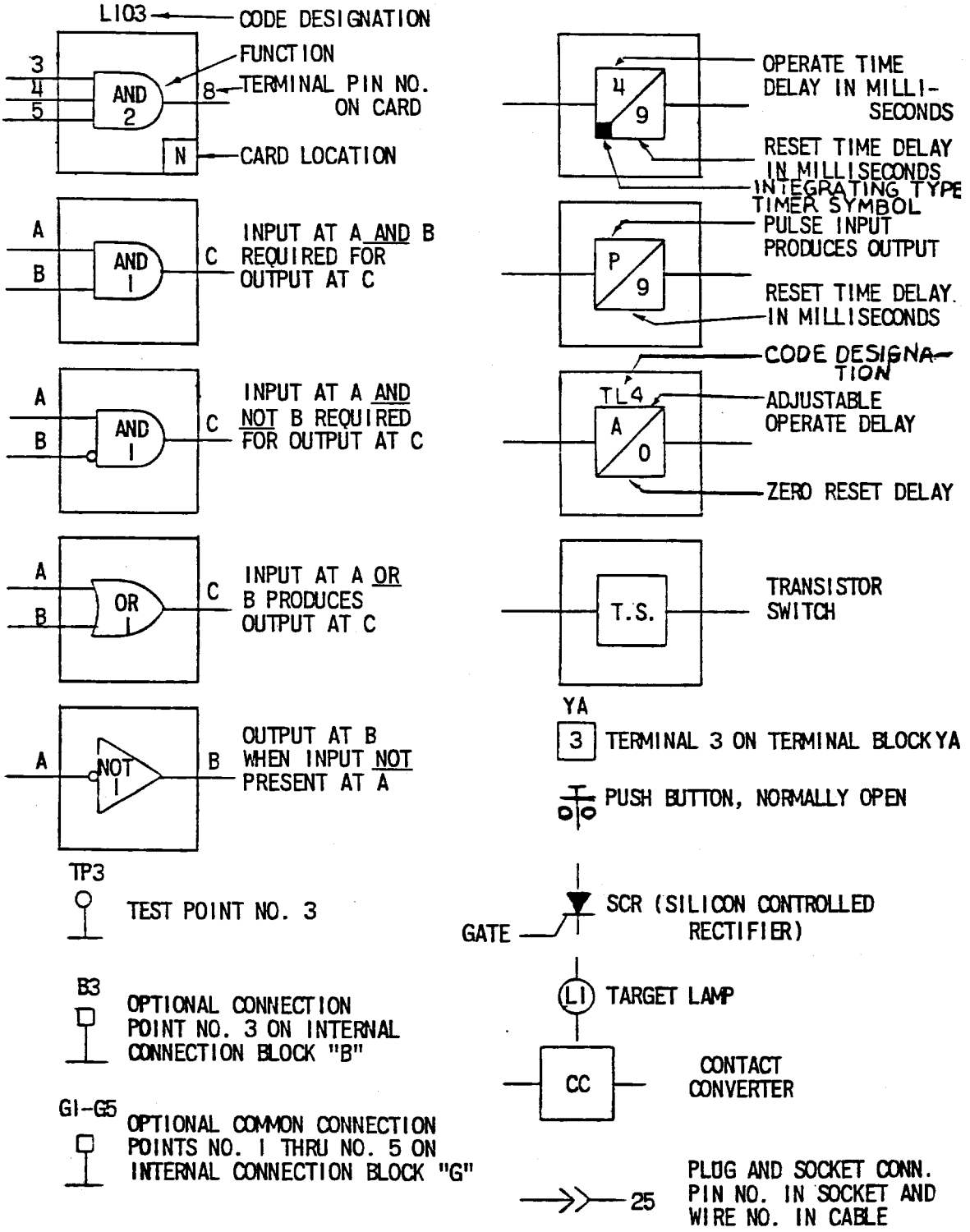


Fig. 4 (0227A2047-1) Logic and Internal Connection Diagram Legend

THE FOLLOWING ARE FACTORY CONNECTIONS MADE AT THE MATRIX BLOCKS INSIDE OF THE SLA RELAY ASSOCIATED WITH THIS EQUIPMENT.

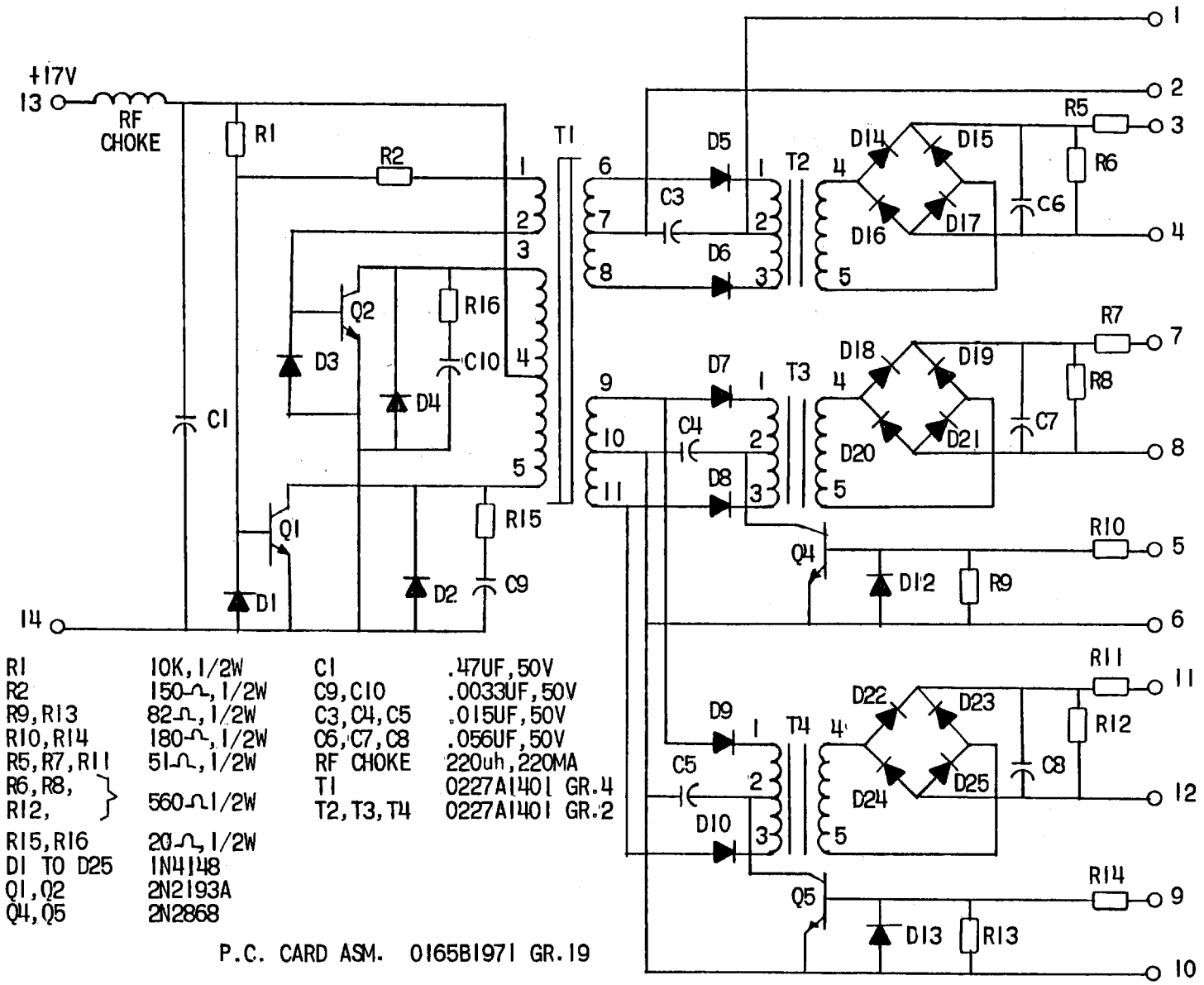
SYMBOLS LISTED: PL=RELAY INTERCONNECTING CABLE LEAD
(5)=LOGIC FUNCTION CARD PIN NUMBER
‡=3-WAY CONNECTION
✳=DLA MONITOR CONNECTION AVAILABLE BUT NOT USED

(244)

MATRIX BLOCK JUMPERS		LOGIC FUNCTION	
FROM	TO	FROM	TO
W2	W9	AND22(8)	TL1(3)
R1	G11	TL1(8)	AND19(3)
R2	W1	TL1(8)	OR13(6)
V3	B1	AND1(9)	TL2(3)
R5‡	OR4	TL2(8)	OR9(3)
R3	W10	TL1(8)	OR21(3)
R6	W3	TL2(8)	OR14(3)
B6	OR8	AND2(9)	TL3(3)
OR9‡	W4	TL3(8)	OR14(4)
OR9‡	B9	TL3(8)	OR8(3)
V4‡	B7	AND5(8)	TL4(3)
V4‡	B12	AND5(8)	TL5(3)
R7‡	OR5	TL4(8)	OR9(4)
R8	OR6	TL4(8)	OR10(9)
OR1‡	B10	TL5(8)	OR8(4)
OR1‡	OR7	TL5(8)	OR10(2)
G7	B2	CC5(8)	AND11(3)
B5	G14	AND11(8)	TL6(3)
G15‡	W7	TL6(8)	OR24(2)
G5	V6	CC3(8)	AND9(4)
V12‡	W6	AND9(8)	OR24(6)
R11‡	V9	A129(7)	AND10(4)
G8	V8	CC6(9)	AND10(3)
G9	B8	CC7(8)	OR7(6)
G6	OR10	CC4(9)	TL7(3)
OR11	OR2	TL7(8)	OR15(7)
V1	Y11‡	AND3(5)	REF.
V2	Y11‡	AND1(2)	REF.
B3	Y12‡	AND11(5)	REF.
B4	Y12‡	AND2(2)	REF.
OR3	Y13‡	OR15(2)	REF.
V5	Y13‡	OR20(3)	REF.
G18	Y14‡	OR19(6)	REF.
W20	Y14‡	PL134	REF.
W19	Y15‡	PL122	REF.
R13	Y15‡	PL146	REF.

MATRIX BLOCK JUMPERS		LOGIC FUNCTION	
FROM	TO	FROM	TO
R5‡	V13	TL2(8)	PL412
R7‡	V14	TL4(8)	PL413
R12	V15	AND18(9)	PL414
G16	V16	AND16(8)	PL415
G13	V17	OR16(4)	PL416
W12	V18	AND7(8)	PL417
V7	V19	OR12(9)	PL418
G19	V20	OR18(8)	PL419
R4	OR13	TL1(8)	PL420
OR19	OR14	PL137	PL422
W5	OR15	OR14(8)	PL423
V12‡	OR16	AND9(8)	PL424
B11	OR17	OR8(8)	PL425
OR12	OR18	OR10(9)	PL426
G15	OR20	TL6(8)	PL427
R11‡	B13	A129(7)	PL428
V10	B14	AND18(6)	PL429
W8	B15	AND24(9)	PL430
G1	B16	OR5(8)	PL432
G3	B17	OR2(9)	PL433
G2	B18	OR1(9)	PL434
G12	B19	OR23(9)	PL435
G17	B20	PL130	PL436
G4	G20	OR6(9)	PL437
V11	Y1	AND18(2)	+15V
W17	W16	PL127	TL8(4)
R14	Y16	PL147	REF.
W11	Y15	OR1(2)	REF.

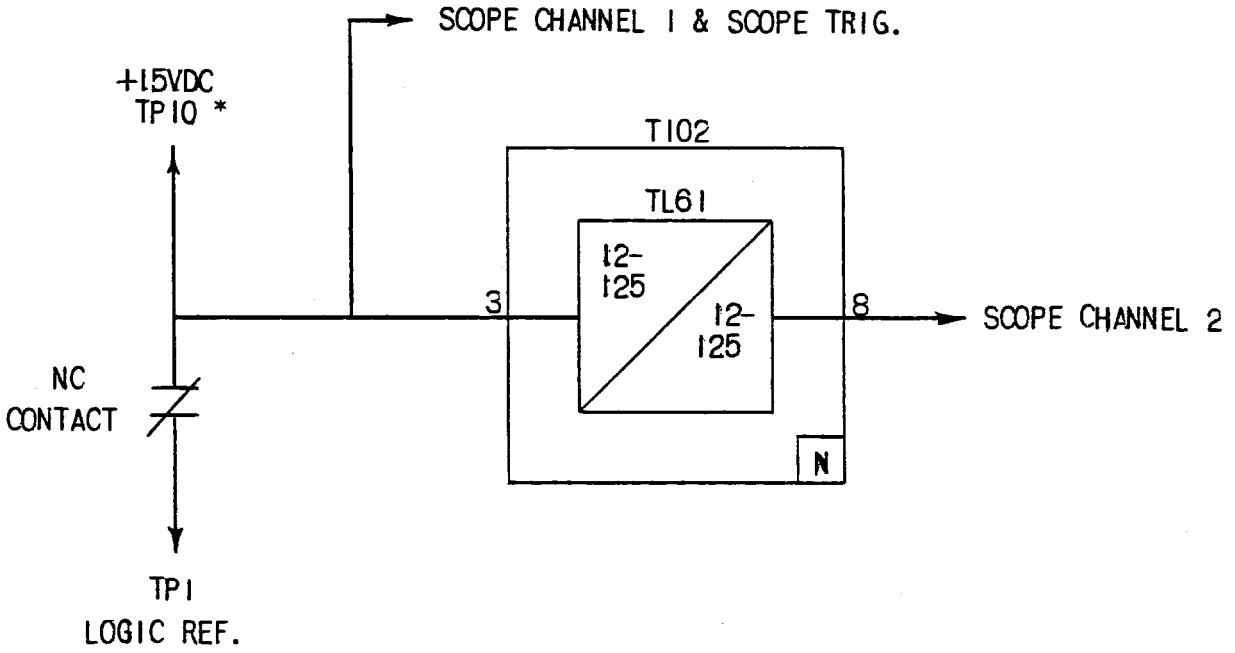
Fig. 5 (0227A2050-1, Sh. 244) Typical Option Chart for the Type SLA54G Relay



R1	10K, 1/2W	C1	.47UF, 50V
R2	150Ω, 1/2W	C9, C10	.0033UF, 50V
R9, R13	82Ω, 1/2W	C3, C4, C5	.015UF, 50V
R10, R14	180Ω, 1/2W	C6, C7, C8	.056UF, 50V
R5, R7, R11	51Ω, 1/2W	RF CHOKE	220uh, 220MA
R6, R8, R12,	560Ω 1/2W	T1	0227A1401 GR.4
		T2, T3, T4	0227A1401 GR.2
R15, R16	20Ω, 1/2W		
D1 TO D25	IN4148		
Q1, Q2	2N2193A		
Q4, Q5	2N2868		

P.C. CARD ASM. 0165B1971 GR.19

Fig. 6 (0208A5504AR-0) Internal Connections for the Isolation Interface Used in the Type SLA54G Relay



* THE 15VDC SIGNAL AT PIN 10 HAS A CURRENT LIMITING RESISTOR MOUNTED ON THE TEST CARD.

Fig. 7 (0246A7987-0) Timer Test Circuit for Setting Timer Cards in the Type SLA54G Relay

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