INSTRUCTIONS

GEK-86047

AUXILIARY LOGIC UNIT

TYPE SLA53K

GENERAL ELECTRIC

CONTENTS

AUXILIARY LOGIC UNIT

TYPE SLA53K

DESCRIPTION

The SLA53K is a static auxiliary logic relay designed for use in a directional comparison transmission line protection scheme with single pole trip and reclose capability. It includes the necessary scheme logic and the channel interface and control circuits for a Type CS26 on-off power line carrier.

The SLA53K is packaged in a four rack unit (one rack unit equals 1-3/4 inches) enclosed metal case suitable for mounting on a 19-inch rack. The case outline and mounting dimensions are shown in Figure 1. The internal connections for the SLA53K are shown in Figure 2. The component and printed circuit card locations are shown in Figure 3.

APPLICATION

The SLA53K is intended for application with Type SLY61, SLY62, SLY63, SLYG61 and SLYG62 directional distance relays, and SLC51 overcurrent relays in a directional comparison blocking scheme with Type CS26 power line carrier. Circuits are included to permit single pole switching. An SLAT53 output relay with individual pole control and an isolated plus or minus 15 VDC power supply, Type SSA51, are also required for a complete equipment for one terminal of a transmission line.

For a complete description of the overall scheme in which the SLAT53G relay is employed, refer to the overall logic diagram and the associated logic description which are supplied with each terminal of the equipment. The only user adjustments which should be required are the following three timer settings:

TL4 - B/O second zone timer for delayed tripping by MT or MTG. Set B pickup time delay long enough to coordinate with clearing of faults in the next line section.

TL5 - 3/50 trip integrator. The three millisecond pickup time delay is based on proper coordination between local trip and received channel blocking signal at the comparer with a 1.5 millisecond CS26C channel. For longer channel times due to the use of narrow band carrier or longer than one millisecond propagation time (100 mile line), the pickup time should be increased accordingly. Refer to the specific logic description for details. The 50 millisecond reset time is to hold off blocking carrier transmission to the remote terminal once a local trip is initiated.

TL6 - 1/A is the comparer bypass timer. The A (2-20 cycle) drop-out time represents the duration of time for which direct tripping by MTG (or MT) is permitted following single pole reclosing. The minimum two cycle drop-out time will assure tripping on a sustained fault. Longer drop-out settings will accomodate operation of other output control circuits. Refer to the logic description for detailed considerations.

The other timers in the SLAT53G should be applied with the settings shown on the overall logic diagram, and no user adjustment should be required.

RATINGS

The Type SLA53K relay is designed for use in an environment where the air temperature outside the relay case is between minus 20°C or plus 65°C.

The Type SLA53K relay requires a plus or minus 15 VDC power source which can be obtained from a Type SSA power supply.

BURDENS

The SLA53K relay presents a burden of 390 milliamperes to the plus 15 VDC supply of the Type SSA power supply.

Each contact converter, when energized, draws ten milliamperes from the station battery, regardless of tap setting.

OPERATING PRINCIPLES

LOGIC CIRCUIT

The functions of the Type SLA53K relay involve basic logic (AND, OR, and NOT) where the presence or absence of signals, rather than their magnitude, controls the operation. Signals are measured with respect to a reference bus accessible at TP1. In general, a signal below one VDC represents an OFF or LOGIC ZERO condition; an ON or LOGIC ONE is represented by a signal of approximately plus 15 VDC.

The symbols used on the internal connection diagram (Figure 2) are explained by the legend shown in Figure 4.

The matrix block connections shown in the internal connections of the SLA53K relay are prewired at the factory. The connections are shown on the associated overall logic and are listed on the associated option chart. A sample option chart for the Type SLA53K relay is shown in Figure 5.

Some of the matrix block connections may be user options. In this instance, they will be shown as options on the overall logic and must be selected by the user before the unit is placed in service.

CONTACT CONVERTERS

The purpose of this function is to convert an external contact operation into a signal that is compatible with the logic circuit of the Type SLA53K relay. These contact converters are labeled CC1, CC2 and CC3.

$\overline{CC1}$ Contact converter 1 stops all carrier transmission.
$\overline{CC2}$ Contact converter 2 blocks carrier tripping and carrier transmission.

CC3 This contact converter is connected to matrix block points. Refer to the logic diagram for its use in a particular scheme.

DATA MONITORING POINTS

The Type SLA53K relay has provisions to provide up to 20 data monitoring points; the 20 points are brought out on two sockets C411 and C421. These data monitoring (DLA) points are selected by connecting the movable lead from the DLA socket pin (412-420, C422-C430) to one of the available points on the matrix blocks. These connections are listed on the option chart (refer to the sample option chart, Figure 5). Any matrix points which are not being used for logic connections may be monitored; key points in the logic have more than one matrix point to allow both logic and monitoring connections.

A data loggic amplifier (DLA) unit is used to convert the logic signals into usable outputs. The associated DLA unit determines the number of points which can be monitored at the same time.

CHANNEL INTERFACE

The logic of the Type SLA53K relay includes an isolation interface (Figure 6) between the relays in the scheme and the associated channel equipment. The circuitry of the isolation interface provides a signal path but maintains metallic isolation. This feature makes it possible to maintain isolation between the DC supply used for the relays and that employed by the channel.

CALCULATION OF SETTINGS

This section covers those timers in the SLA53K which require field adjustment.

TL4 (B/O) This timer is for delaying tripping by MT or MTG. This delay time must be set long enough to allow time for faults in the next line section to be cleared.

TL6 (1/A) The drop delay of this timer controls the amount of time which direct tripping by MT or MTG is permitted following single pole reclosing. Refer to the logic description for a discussion on how to determine the drop-out delay setting of the TL6 timer.

CONSTRUCTION

The SLA53K relay is packaged in an enclosed metal case with hinged front covers and removable top cover. The outline and mounting dimensions of the case and the physical location of the components are shown in Figure 1 and 3, respectively.

The SLA53K relay contains printed circuit cards identified by a code number, such as A112, T102, L104 where A designates auxiliary function, T designates timing function, and L designates logic function. The printed circuit cards plug in from the front of the unit. The sockets are marked with letter designations or "addresses" (D, E, F, etc.) which appear on the guide strips in front of each socket, on the component location drawing, on the unit internal connection diagram, and on the printed circuit

card. The test points (TP1, TP2, etc.) shown in the internal connection diagram are connected to instrument jacks on a test card in position T or AT with TP1 at the top of the AT card. TP10 is tied to plus 15 VDC through a 2.3K resistor. This resistor limits the current when TP10 is used to supply a logic signal to a card.

Logic options and data monitoring points are selected by means of taper tip jumpers and matrix blocks. These matrix blocks are located in the rear of the unit as shown in Figure 3. Twenty point blocks are supplied. Each block is a different color and its points are numbered from 1 to 20. The matirx points appear on the internal connections (Figure 2) as small squares identified with a letter and a number such as G18. G18 is the eighteenth position on the green block. The matrix blocks supplied are Y (yellow), B (black), G (green), R (red), V (violet), O (orange), and W (white). Tools for inserting and removing the taper tip jumpers are supplied with each equipment. The factory matrix connections are listed on the option chart. (Figure 5 is a typical option chart.)

RECEIVING, HANDLING AND STORAGE

These relays will normally be supplied as a part of a static relay equipment, mounted in a rack or cabinet with other static relays and test equipment. Immediately upon receipt of a static relay equipment, it should be unpacked and examined for any damage sustained in transit. If injury or damage resulting from rough handling is evident, file a damage claim at once with the transportation company and promptly notify the nearest General Electric Sales Office.

Reasonable care should be exercised in unpacking the equipment. If the equipment is not to be installed immediately, it should be stored indoors in a location that is free from moisture, dust, metallic chips, and severe atmospheric contaminants.

Just prior to final installation the shipping support bolts should be removed from each side of all relay units, to facilitate possible future unit removal for maintenance. These shipping support bolts are approximately eight inches back from the relay front panel. WARNING: STATIC RELAY EQUIPMENT, WHEN SUPPLIED IN SWING RACK CABINETS, SHOULD BE SECURELY ANCHORED TO THE FLOOR OR TO THE SHIPPING PALLET TO PREVENT THE EQUIPMENT FROM TIPPING OVER WHEN THE SWING RACK IS OPENED.

INSTALLATION TESTS

If the SLA53K relay that is to be tested is installed in an equipment which has already been connected to the power system, disconnect the trip outputs in the associated Type SLAT relay from the system.

CAUTION

THE LOGIC SYSTEM SIDE OF THE DC POWER SUPPLY USED WITH MOD III STATIC RELAY EQUIPMENT IS ISOLATED FROM GROUND. IT IS A DESIGN CHARACTERISTIC OF MOST ELECTRONIC INSTRUMENTS THAT ONE OF THE SIGNAL INPUT TERMINALS IS CONNECTED TO THE INSTRUMENT CHASSIS. IF THE INSTRUMENT USED TO TEST THE RELAY EQUIPMENT IS ISOLATED FROM GROUND, ITS CHASSIS MAY HAVE A ELECTRICAL POTENTIAL WITH RESPECT TO GROUND. THE USE OF A TEST INSTRUMENT WITH A GROUNDED CHASSIS WILL NOT AFFECT THE TESTING OF THE EQUIPMENT. HOWEVER, A SECOND GROUND CONNECTION TO THE EQUIPMENT, SUCH AS A TEST LEAD INADVERTENTLY

DROPPING AGAINST THE RELAY CASE, MAY CAUSE DAMAGE TO THE LOGIC CIRCUITRY. NO EXTERNAL TEST EQUIPMENT SHOULD BE LEFT CONNECTED TO THE STATIC RELAYS WHEN THEY ARE IN PROTECTIVE SERVICE, SINCE TEST EQUIPMENT GROUNDING REDUCES THE EFFECTIVENESS OF THE ISOLATION PROVIDED.

GENERAL

The SLA53K relay is supplied from the factory either mounted in a static relay equipment or as a separate unit associated with measuring relays, a Type SSA power supply, and some form of channel equipment. All relay units for a given terminal of static relaying equipment are tested together at the factory, and each unit will have the same summary number stamped on its nameplate.

Timers should be set for operating on reset times indicated on the associated overall logic diagram. Where a time range is indicated on the overall logic diagram, the timer should be set for the value recommended for that function in the descriptive writeup accompanying the overall logic diagram. Where a setting depends upon conditions encountered on a specific application, this is so stated and the factors influencing the choice of setting are described. The procedure for checking and setting the timers is described in a later section.

OPERATIONAL CHECKS

Operation of the SLA53K unit can be checked by observing the signals at the twenty test points (TP1 to TP20) in the SLA53K, by observing the operation of the associated channel equipment, or by observing the output functions in the associated Type SLAT tripping relay. The test points are located on the test cards in position T and AT and are numbered 1 to 20 from top to bottom. TP1 is the reference bus for the logic circuit; TP10 is at plus 15 VDC. The remaining points are located at various strategic points throughout the logic as shown on the internal connection diagram (Figure 2). Test point voltages can be monitored with a portable high impedance voltmeter, the voltmeter on the test panel of the associated equipment, or an oscilloscope.

TEST CARD ADAPTER

The test card adapter provides a convenient means of gaining access to any pin of a particular card. Detailed information on the use of the test adapter card is included in the card instruction book, GEK-34158.

TIMER ADJUSTMENTS AND TESTS

When the time-delay cards are to be adjusted or checked, an oscilloscope that can display two traces simultaneously and that has a calibrated sweep should be used.

In order to test the timer cards it is necessary to remove the card which supplies the input to the timer and to place the timer card in a card adapter (see Table I). The card adapter allows access to the input and output of the timer if they are not brought out on test points. The timer test circuit is shown in Figure 7. Opening the normally closed contact causes the output to step up to plus 15 VDC after the pickup delay of the timer. To increase the pickup time, turn the upper potentiometer on the timer card clockwise; to decrease the time, turn it counterclockwise. Closing the contact causes the timer output to drop out after the reset time-delay setting of the card. If the

timer card is provided with a variable reset relay, it can be adjusted by the lower potentiometer on the timer card (clockwise increases reset time).

TABLE I

TIMER UNDER TEST	POSITION	REMOVE CARD IN POSITION
TL3	R	L
TL4	AM	F
TL5	J	H
TL6	AH	AG
TL8	AS	AG
TL9	AF	AP (in SLAT53E)

CONTACT CONVERTER TESTS

Operation of the contact converters can be checked by connecting the station DC through a switch to the appropriate pair of terminals of the terminal strip, AH, mounted on the rear of the relay. The terminal numbers and polarity of connections for each of the three contact converters are shown in the internal connection diagram, Figure 2. The output of CC1 can be monitored at pin 3 of card AP. The output of CC2 can be monitored at pin 7 of card F, and the output of CC3 can be monitored at the input to the function which it drives (refer to the logic diagram).

ISOLATION INTERFACE TESTS

Operation of the three functions (received carrier, transmitter control, and transmitter auxiliary stop) of the isolation interface can be checked without direct connections to the subassembly. External test connections are made to the pins of the C111 socket mounted on the rear of the unit, see Figure 3. Logic circuit test connections are made at the socket pins of the channel control card in position "AP."

Received carrier operation test connections are shown in Figure 8A. For this test do not remove channel control card in position "AP." Closure of the normally open contact will simulate a received carrier signal and scope display will go from a LOGIC ZERO to a LOGIC ONE.

For the transmitter control and transmitter auxiliary stop checks, remove the channel control card "AP" from its socket and replace it with a test card adapter and test card to gain access to the "AP" socket pins. Transmitter control test connections are shown in Figure 8B. The test contact in the open position simulates a LOGIC ONE condition which holds off the transmitter control output of the isolation interface. Closure of the normally open contact generates a LOGIC ZERO condition, initiating a transmitter control output producing a five-to-six volt DC signal across the output loading resistor. The transmitter auxiliary stop function can be tested in a similar manner using the test connections of Figure 8C and the output again will provide a five-to-six volt DC signal across the output loading resistor.

OVERALL EQUIPMENT TESTS

After the SLA53K relay and the associated static relay units have been individually calibrated and tested for the desired settings, a series of overall operating circuit checks is advisable.

The elementary, overall logic, and logic description for the specific job will be useful for determining the overall operation of the scheme.

Overall equipment tests can be performed by applying alternating currents and voltages to the measuring units as specified in the instruction book for the measuring units and checking that proper outputs are obtained from the associated SLAT when the measuring units operate.

MAINTENANCE

PERIODIC TESTS

It should be sufficient to check the outputs produced at test points in the SLA53K when periodic calibration tests are made on the associated measuring units, for example, the phase and ground relays in the line relaying scheme. No separate periodic tests on the SLA53K itself should be required.

TROUBLESHOOTING

In any troubleshooting of equipment, it should first be established which unit is functioning incorrectly. The overall logic diagram supplied with the equipment shows the combined logic of the complete equipment and the various test points in each unit. By signal tracing, using the overall logic diagram and the various test points, it should be possible to quickly isolate the trouble.

A test adapter card is supplied with each static relay equipment to supplement the prewired test points on the test cards. Use of the adapter card is described in the card instruction book, GEK-34158.

A dual trace oscilloscope is a valuable aid to detailed troubleshooting, since it can be used to determine phase-shift, operate and reset times, as well as input and output levels. A portable dual-trace oscilloscope with a calibrated sweep and trigger facility is recommended.

SPARE PARTS

To minimize possible outage time, it is recommended that one spare card of each type be carried in stock. It is possible to replace damaged or defective components on the printed circuit cards, but great care should be taken in soldering so as not to damage or bridge-over the printed circuit buses, or overheat the semiconductor components. The repaired area should be recovered with a suitable high-dielectric plastic coating to prevent possible breakdowns across the printed buses due to moisture and dust. The wiring diagrams for the cards in the SLA53K relay are included in the card book, GEK-34158.

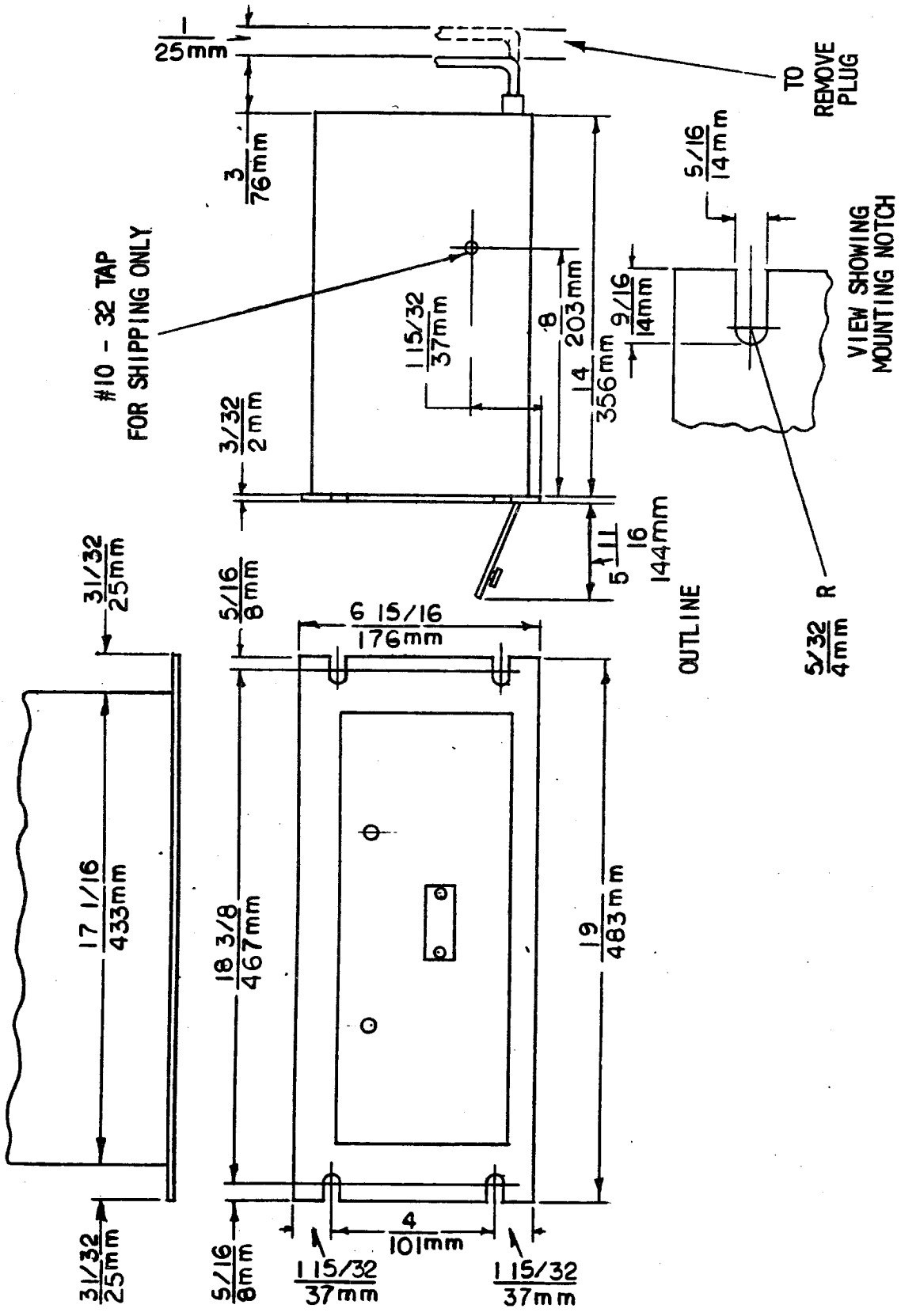


Figure 1 (0227A2037-0) Outline and Mounting Dimensions

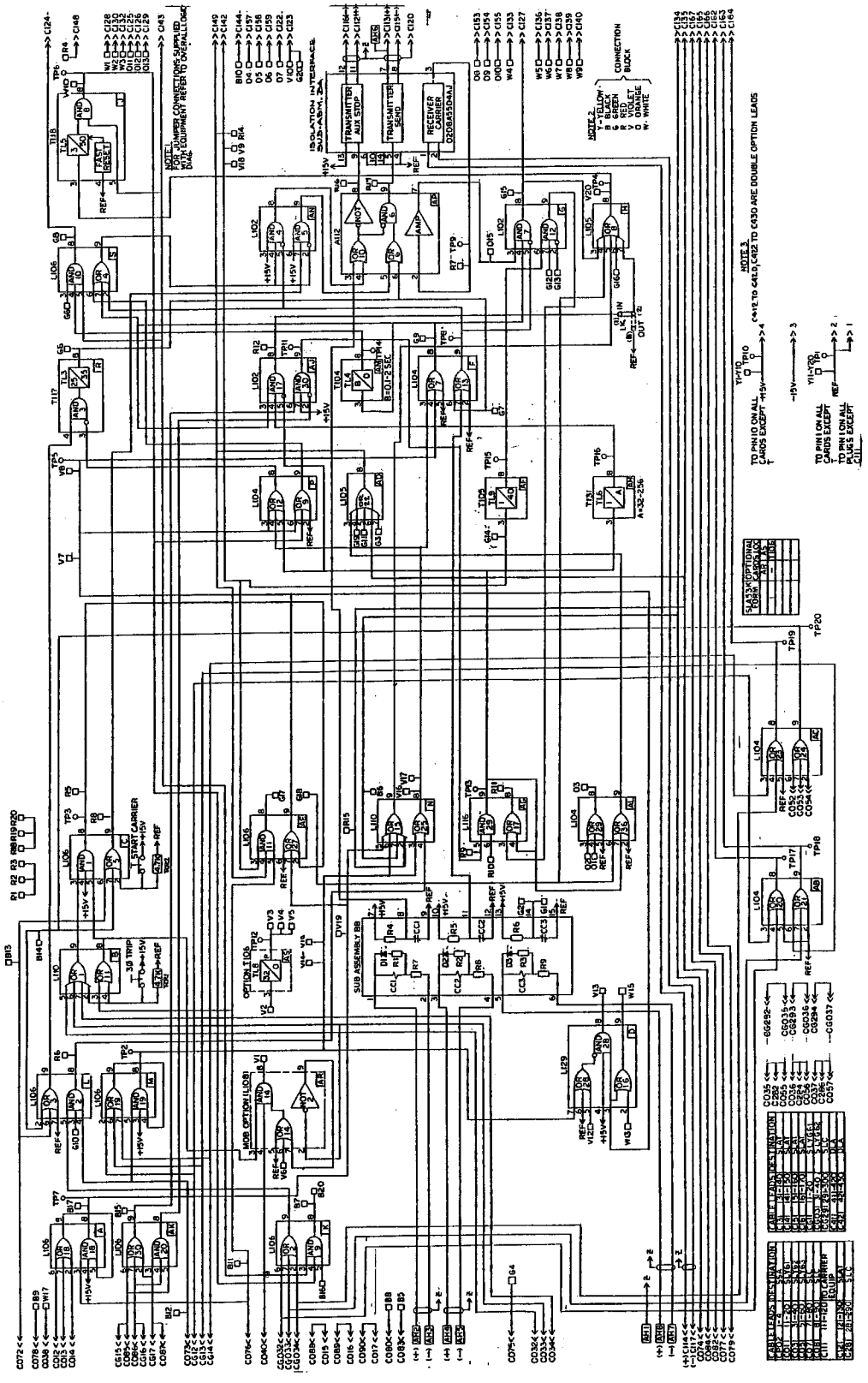
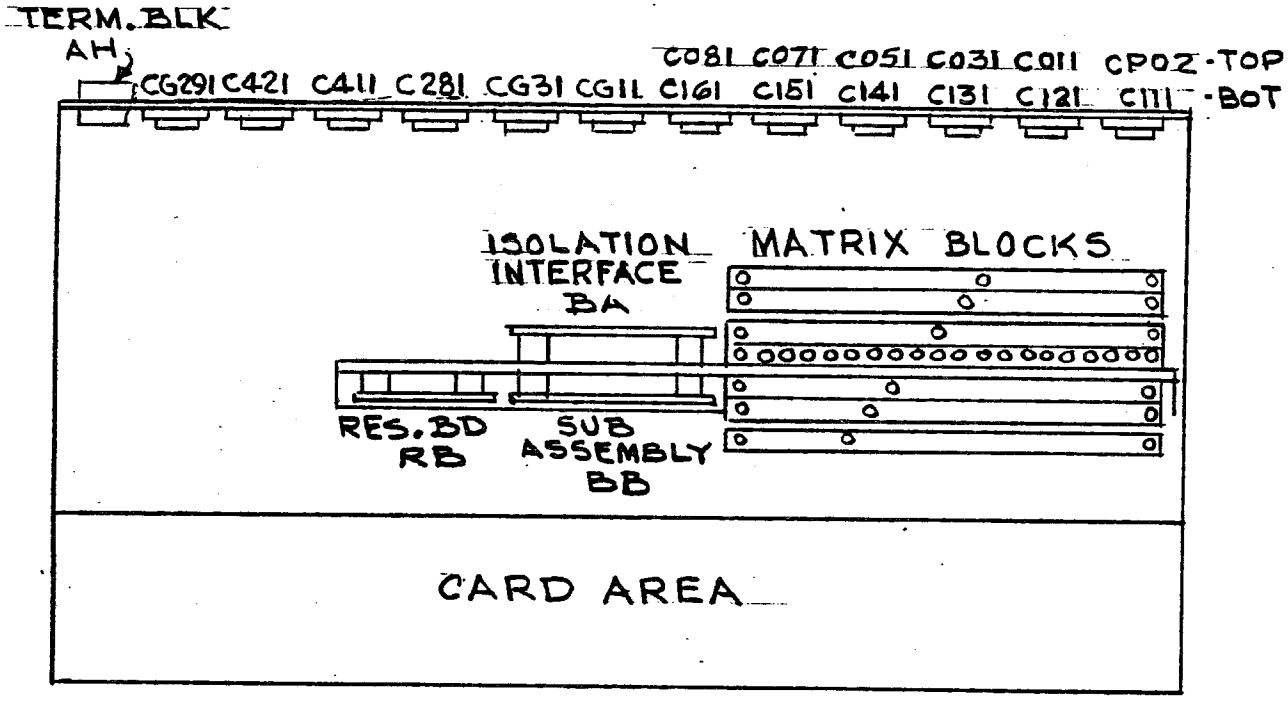
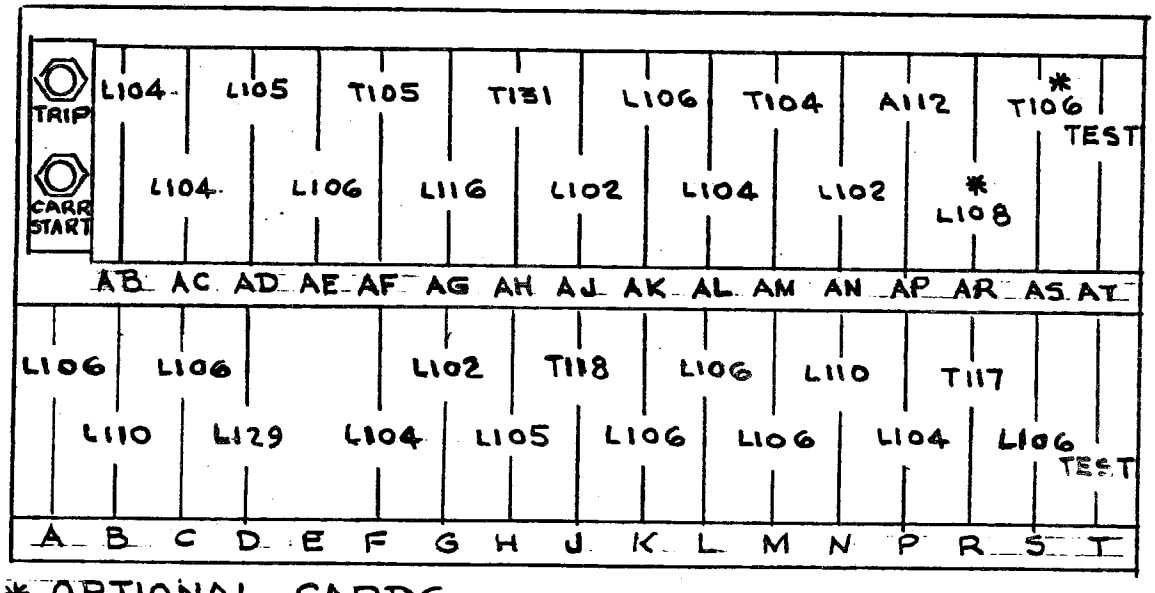


Figure 2 (0145D8793-0) Internal Connections for the Type SLA53K Relay



PLAN VIEW



* OPTIONAL CARDS

Figure 3 (0285A6645-0) Component Location Diagram for the Type SLA53K Relay

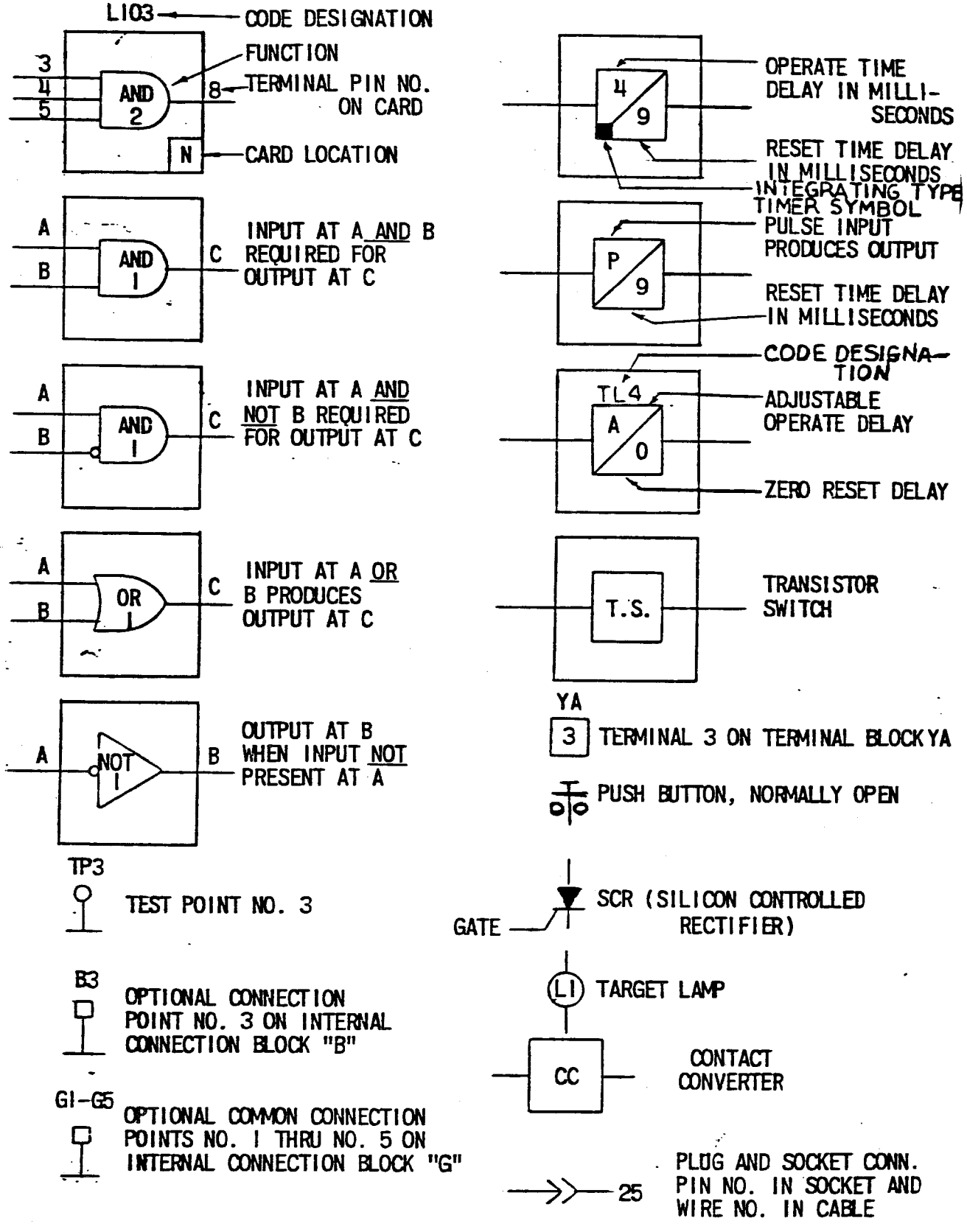


Figure 4 (0227A2047-1) Internal Connections Diagram Legend

THE FOLLOWING ARE FACTORY CONNECTIONS MADE AT THE MATRIX BLOCKS INSIDE OF THE SLA RELAY ASSOCIATED WITH THIS EQUIPMENT.

SYMBOLS LISTED: PL=RELAY INTERCONNECTING CABLE LEAD
(5)=LOGIC FUNCTION CARD PIN NUMBER
‡=3-WAY CONNECTION
✳=DLA MONITOR CONNECTION AVAILABLE BUT NOT USED

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MATRIX BLOCK JUMPERS		LOGIC FUNCTION	
FROM	TO	FROM	TO
B17	PL426	AND18	DLA
V19	W6	AND18	AND56(2)
G4	V12	IO	OR28(5)
R9	PL428	AND30	DLA
V7	PL412	OR27(9)	DLA
V8	W3	OR27(9)	AND51(4)
G9	02	OR7(8)	OR29(3)
03	B16	OR29(8)	AND9(5)
B20	PL415	AND9(8)	DLA
B7	‡R18	AND9(8)	COM
R19	G20	COM	TL31
V18	‡PL422	OR31(8)	DLA
G13	V9	AND12(2)	TL9(3)
G12	Y1	AND12(7)	+15VDC
R11	V2	OR17(8)	TL8(3)
V3	R10	TL8(8)	AND29(6)
G10	Y2	AND2(3)	+15VDC
G17	G18	AND11(8)	OR36(6)
08	PL416	OR33(8)	DLA
09	PL417	OR34(8)	DLA
010	PL418	OR35(8)	DLA
B10	R20	PL144	AND9(8)
B13	PL420	G1	DLA
B14	PL419	MB	DLA
B6	PL424	G4	DLA
R15	PL425	OR81(9)	DLA
V14	PL427	AND19(8)	DLA
V15	W5	AND19(8)	AND55(6)
V13	G19	AND28(8)	OR22(4)
G1	G11	CC3(14)	OR22(5)
V16	PL413	OR25(8)	DLA
V17	W4	OR25(8)	AND52(6)
015	PL414	RECAMP(7)	DLA
V20	01	OR8(8)	OR29(4)
G6	Y3	AND10(3)	+15VDC
G16	Y11	OR8(6)	REF

MATRIX BLOCK JUMPERS		LOGIC FUNCTION	
FROM	TO	FROM	TO
G8	W7	AND10(8)	AND57(4)
‡PL422	R1	DLA	COM(OR31)
R2	012	COM(OR31)	AND51(3)
R3	W1	COM(OR31)	AND57(5)
07	PL423	OR32(9)	DLA
‡R18	011	COM	AND31(6)
W15	Y17	OR16(9)	REF.
G3	R4	OR22(7)	PL148

Figure 5 (0227A2050-0, Sh. 278) Typical Option Chart

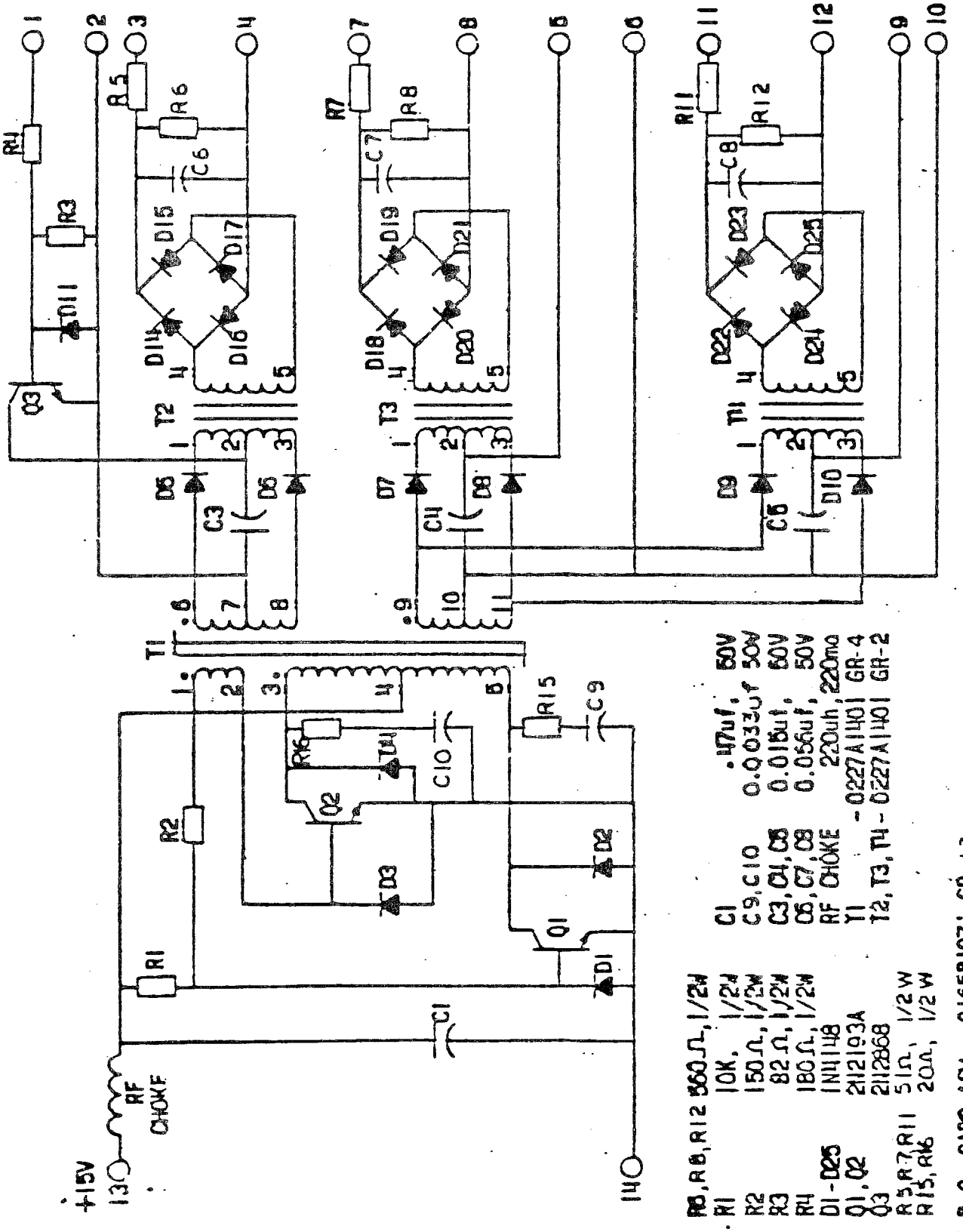
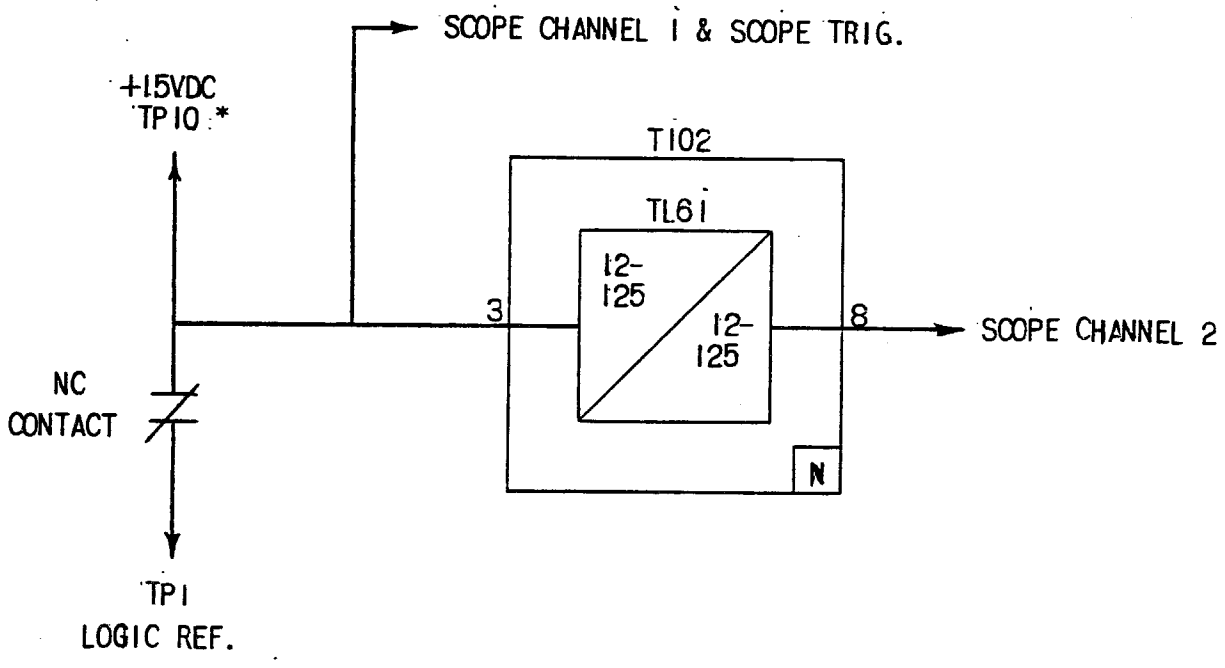


Figure 6 (0208A5504AJ-1) Isolation Interface Internal Connections



* THE 15VDC SIGNAL AT PIN 10 HAS A CURRENT LIMITING RESISTOR MOUNTED ON THE TEST CARD.

Figure 7 (0246A7987-0) Logic Timer Test Circuit

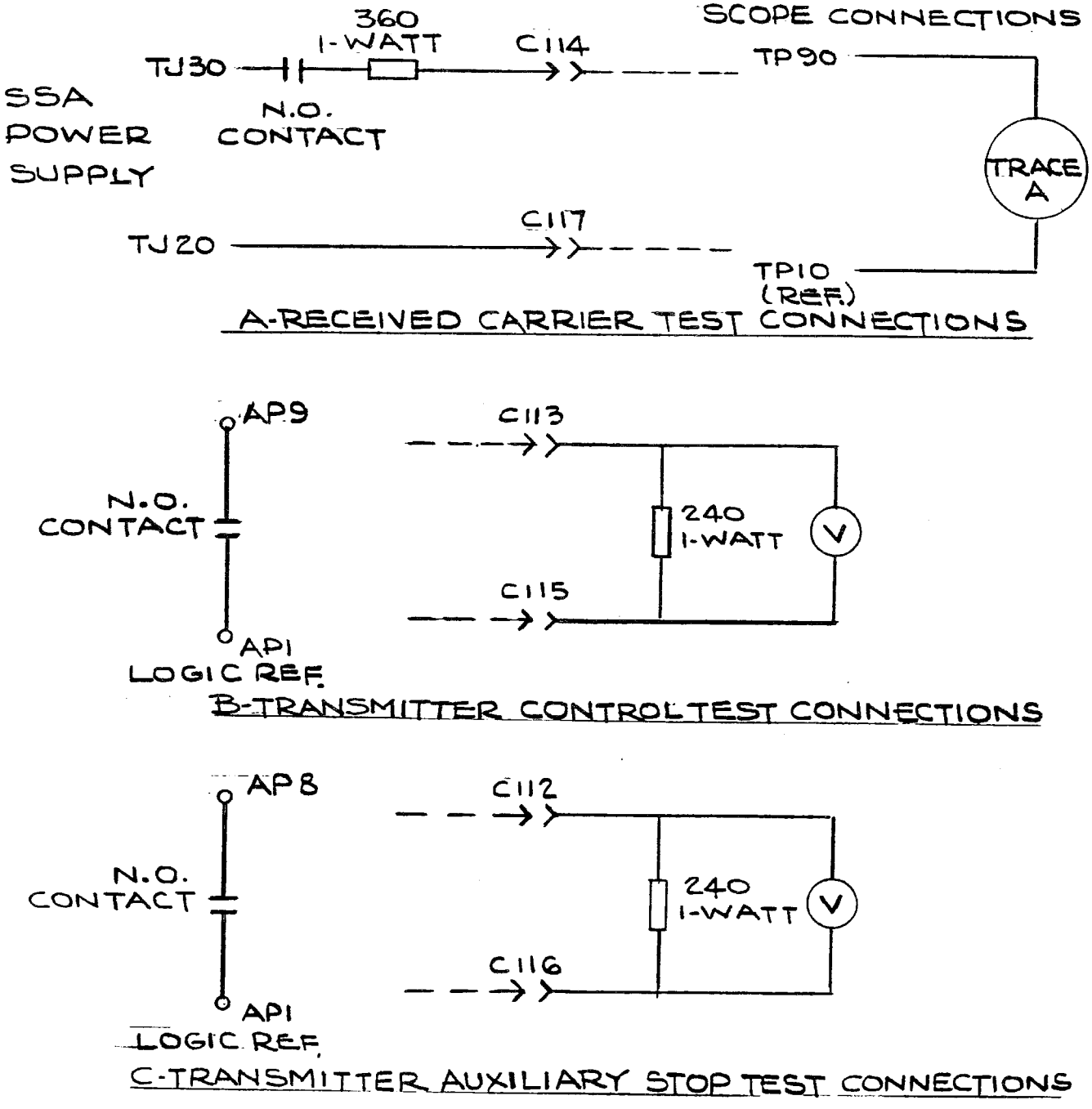


Figure 8 (0285A5717-0) Isolation Interface Test Circuit

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