INSTRUCTIONS

GEK-86060

SOLID STATE AUXILIARY LOGIC RELAY

FOR

TRANSMISSION LINE PROTECTION

TYPE SLA53L

GENERAL ELECTRIC

CONTENTS

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TYPE SLA53L

DESCRIPTION

The SLA53L is an auxiliary logic relay designed for use in a directional comparison scheme. The relay contains the necessary logic to interpret output signals from associated measuring functions and translate them to an appropriate auxiliary output and tripping relay. In addition to the SLA53L relay, appropriate ground and phase relays, plus a power supply and auxiliary tripping relay are required to complete a particular relaying scheme.

The Type SLA53L is packaged in a four-rack unit enclosed metal case. The relay is suitable for mounting in a 19-inch rack. The case outline and mounting dimensions are shown in Figure 3. The internal connections for this relay are shown in Figure 1 and the component and printed circuit card locations are shown in Figure 2.

APPLICATION

The SLA53L is designed to operate in conjunction with appropriate phase and ground relays in a directional comparison scheme using a pilot channel. The SLA53L includes circuits to accomodate the use of first and second zone phase and ground distance back-up protection with the blocking directional comparison scheme. An isolation interface provides the interconnection between the SLA53L logic, and the associated channel equipment.

Protection features required in a relaying scheme often vary from scheme to scheme, and it is sometimes desirable to provide certain features initially with the scheme or to provide features so that they may be added at a later date in the field. To this end, the SLA53L design has incorporated circuit flexibility to permit implementation of certain optional features.

For the specific options and the logic arrangement supplied with a particular scheme, refer to the logic diagram and the logic descriptive write-up supplied with that scheme. If it is desired to make logic changes at a later date, the diagrams and instruction books supplied with the equipment should be studied to determine the means for implementing the changes. If after study of the diagrams, further assistance is required, contact the nearest General Electric District Sales Office.

Various points in the logic can be monitored by providing jumpers from any of the available matrix points to plugs 411 and 421 located on the rear of the SLA53L relay. This option is further described in paragraph, DATA MONITORING POINTS, in the section entitled **OPERATING PRINCIPLES.**

RATINGS

The Type SLA53L relay is designed for use in an environment where the air temperature outside the relay case is between minus 20°C or plus 65°C.

The Type SLA53L relay requires a plus or minus 15 VDC power source which can be obtained from a Type SSA50/51 power supply.

Each contact converter in this relay has a link for selecting the proper voltage for the coil circuit of the contact converter. The three possible voltages are 48 VDC, 125 VDC and 250 VDC.

BURDENS

The SLA53L relay presents a burden of approximately 400 milliamperes to the plus 15 VDC supply of the Type SSA50/51 power supply.

Each contact converter, when energized, draws approximately ten milliamperes from the station battery, regardless of tap setting.

OPERATING PRINCIPLES

LOGIC CIRCUIT

The functions of the Type SLA53L relay involve basic logic (AND, OR, and NOT) where the presence or absence of signals, rather than their magnitude, controls the operation. Signals are measured with respect to a reference bus accessible at TP1. In general, a signal below one VDC represents an OFF or LOGIC ZERO condition; an ON or LOGIC ONE is represented by a signal of approximately plus 15 VDC.

The symbols used on the internal connection diagram (Figure 1) are explained by the legend shown in Figure 4.

The matrix block connections shown in the internal connections of the SLA53L relay are prewired at the factory. The connections are shown on the associated overall logic and are listed on the associated option chart. A sample option chart for the Type SLA53L relay is shown in Figure 5.

CONTACT CONVERTERS

The purpose of this function is to convert a contact operation into a signal that is compatible with the logic circuit of the Type SLA53L relay. These contact converters which are labeled CC1 through CC3 have a non-adjustable four millisecond pickup delay. Refer to the logic description for the particular scheme for information concerning the use of each contact converter.

DATA MONITORING POINTS

The Type SLA53L relay has provisions to provide data monitoring outputs. The data monitoring (DLA) points are selected on the matrix blocks and are listed on the option

chart. Any matrix block points which are not being used for logic connections may be monitored. Key points in the logic have more than one matrix point to allow both logic and monitoring connections. A data logging amplifier (DLA) relay is used to translate these logic signals into usable outputs.

CHANNEL INTERFACE

The logic of the Type SLA53L relay includes an isolation interface (Figure 6) between the relays in the scheme and the associated channel equipment. The circuitry of the isolation interface provides a signal path but maintains metallic isolation. This feature makes it possible to maintain isolation between the DC supply used for the relays and that employed by the channel.

When pins 1 and 2 of the interface are both connected to relay reference, a positive voltage appears at pin3 with respect to pin 4. This output is a five volt DC, 20 milliampere signal.

When a five volt DC signal is applied to pin 5 with respect to pin 6, an output signal (five volts DC, 20 milliamperes) appears between pins 7 and 8. This signal is made compatible with the relay logic by the A115 channel control card in card position A.

SETTINGS

There are certain timers in the SLA53L that may require field adjustment. Refer to the logic description supplied with each scheme for the settings to be made on these timers.

CONSTRUCTION

The SLA53L relay is packaged in an enclosed metal case with hinged front covers and removable top cover. The outline and mounting dimensions of the case and the physical location of the components are shown in Figure 3 and 2, respectively.

The SLA53L relay contains printed circuit cards identified by a code number, such as A102, T102, L104 where A designates auxiliary function, T designates time-delay function, and L designates logic function. The printed circuit cards plug in from the front of the unit. The sockets are marked with letter designations or "addresses" (D, E, F, etc.) which appear on the guide strips in front of each socket, on the component location drawing, on the internal connection diagram, and on the printed circuit card. The test points (TP1, TP2, etc.) shown on the internal connection diagram are connected to instrument jacks on a test card in position T or AT with TP1 at the top of the AT card. TP10 is tied to plus 15 VDC through a 1.5K resistor. This resistor limits the current when TP10 is used to supply a logic signal to a card.

Other logic options are selected by means of taper tip jumpers and matrix blocks. These matrix blocks are located in the rear of the unit as shown in Figure 2. The green (G), red (R), black (B), orange (O), white (W), brown (BR), blue (BL) and violet (V) matrix blocks each have 20 points. The yellow (Y) matrix block also has 20 points, which are grouped in ten common points; 1 to 10 are tied to plus 15 VDC, 11 to 20 are tied to reference. Tools for inserting and removing the taper tip jumpers are supplied with each static terminal.

RECEIVING, HANDLING AND STORAGE

The SLA53L relay will normally be supplied as part of a static relay equipment, mounted in a rack or cabinet with other static relays and test equipment. Immediately upon receipt of a static relay equipment, it should be unpacked and examined for any damage sustained in transit. If injury or damage resulting from rough handling is evident, file a damage claim at once with the transportation company and promptly notify the nearest General Electric Sales Office.

Reasonable care should be exercised in unpacking the equipment. If the equipment is not to be installed immediately, it should be stored indoors in a location that is free from moisture, dust, metallic chips, and severe atmospheric contaminants.

Just prior to final installation the shipping support bolt should be removed from each side of all relay units, to facilitate possible future unit removal for maintenance. These shipping support bolts are approximately eight inches back from the relay front panel. Static relay equipment, when supplied in swing rack cabinets, should be securely anchored to the floor or to the shipping pallet to prevent the equipment from tipping over when the swing rack is opened.

TEST INSTRUCTIONS

CAUTION

THE LOGIC SYSTEM SIDE OF THE DC POWER SUPPLY USED WITH MOD III STATIC RELAY EQUIPMENT IS ISOLATED FROM GROUND. IT IS A DESIGN CHARACTERISTIC OF MOST ELECTRONIC INSTRUMENTS THAT ONE OF THE SIGNAL INPUT TERMINALS IS CONNECTED TO THE INSTRUMENT CHASSIS. IF THE INSTRUMENT USED TO TEST THE RELAY EQUIPMENT IS ISOLATED FROM GROUND, ITS CHASSIS MAY HAVE AN ELECTRICAL POTENTIAL WITH RESPECT TO GROUND. THE USE OF A TEST INSTRUMENT WITH A GROUNDED CHASSIS WILL NOT AFFECT THE TESTING OF THE EQUIPMENT. HOWEVER, A SECOND GROUND CONNECTION TO THE EQUIPMENT, SUCH AS A TEST LEAD INADVERTENTLY DROPPING AGAINST THE RELAY CASE, MAY CAUSE DAMAGE TO THE LOGIC CIRCUITRY. NO EXTERNAL TEST EQUIPMENT SHOULD BE LEFT CONNECTED TO THE STATIC RELAYS WHEN THEY ARE IN PROTECTIVE SERVICE, SINCE TEST EQUIPMENT GROUNDING REDUCES THE EFFECTIVENESS OF THE ISOLATION PROVIDED.

GENERAL

If the SLA53L relay that is to be tested is installed in an equipment which has already been connected to the power system, disconnect the trip outputs in the associated Type SLAT relay from the system.

The SLA53L relay is supplied from the factory either mounted in a static relay equipment or as a separate unit associated with measuring relays, a Type SSA power supply, and some form of channel equipment. All relay units for a given terminal of static relaying equipment are tested together at the factory, and each unit will have the same summary number stamped on its nameplate.

In general, when a time range is indicated on the internal connection diagram, the timer has been factory set at a mid-range value. Timers should be set for the operating or reset times indicated on the associated overall logic diagram. Where a time range is indicated on the overall logic diagram, the timer should be set for the value recommended for that function in the descriptive write-up accompanying the overall logic diagram. Where a setting depends upon conditions encountered on a specific application, this is so stated and the factors influencing the choice of setting are described. The procedure for checking and setting the timers is described in a later section.

OPERATIONAL CHECKS

Operation of the SLA53L unit can be checked by observing the signals at the twenty test points (TP1 to TP20), or by observing the output functions in the associated Type SLAT tripping relay. The test points are located on two test cards in positions T and AT and are numbered 1 to 20 from top to bottom. TP1 is the reference bus for the logic circuit and TP10 is at plus 15 VDC. The remaining points are located at various strategic points throughout the logic as shown on the internal connection diagram (Figure 1). Test point voltages can be monitored with a portable high impedance voltmeter, the voltmeter on the test panel of the associated equipment, or an oscilloscope.

TEST CARD ADAPTER

The test card adapter provides a convenient means of gaining access to any pin of a particular card. Detailed information on the use of the test adapter card is included in the card instruction book, GEK-34158.

TIMER ADJUSTMENTS AND TESTS

When the time-delay cards are to be adjusted or checked, an oscilloscope that can display two traces simultaneously and that has a calibrated sweep should be used.

In order to test the timer cards it is necessary to remove the card previous to the timer (see Table I) and to place the timer card in a card adapter. The card adapter allows access to the input and output of the timer if they are not brought out on test points. The timer test circuit is shown in Figure 7. Opening the normally closed contact causes the output to step up to plus 15 VDC after the pickup delay of the timer. To increase the pickup time, turn the upper potentiometer on the timer card clockwise; to decrease the time, turn it counterclockwise. Closing the contact causes the timer output to drop out after the reset time-delay setting of the card. If the timer card is provided with a variable reset relay, it can be adjusted by the lower potentiometer on the timer card (clockwise increases reset time).

TABLE I

TIMER UNDER TEST	POSITION	REMOVE CARD IN POSITION
TL1 T118 (1-8/10-80)	AC	K
TL2 T104 (100-2000/0)	J	**
TL3 T104 (100-200/0)	L	**
TL4 T142 (20-200/20-200)	S	F
TL5 T103 (2-16/0)	AM	**
TL6 T102 (10-80/10-80)	M	**
TL7 T118 (1-8/10-80)	AA	**
TL8 T131 (P/32-250)	B	**
TL9 T102 (10-80/10-80)	R	AR

**Refer to scheme logic diagram and Figure 1 to determine which card to remove.

CONTACT CONVERTER TESTS

Operation of the contact converters can be checked by connecting the station direct current through a switch to the appropriate pair of terminals of the terminal strip, AH, mounted on the rear of the relay. The terminal numbers and polarity of connections for each of the contact converters are shown in the internal connection diagram, Figure 1. Output of the contact converter card may be monitored between pins 8 and 9, 11 and 12, and 14 and 15 on the subassembly card with either a scope or meter. Closure of the switch in the test source will provide a plus 15 VDC signal at pins 8, 11 and 14 with respect to reference.

OVERALL EQUIPMENT TESTS

After the SLA53L relay and the associated static relay units have been individually calibrated and tested for the desired settings, a series of overall operating circuit checks is advisable.

The elementary, overall logic, and logic description for the specific job will be useful for determining the overall operation of the scheme.

Overall equipment tests can be performed by applying alternating currents and voltages to the measuring units as specified in the instruction book for the measuring units and checking that proper outputs are obtained from the associated SLAT when the measuring units operate.

MAINTENANCE

PERIODIC TESTS

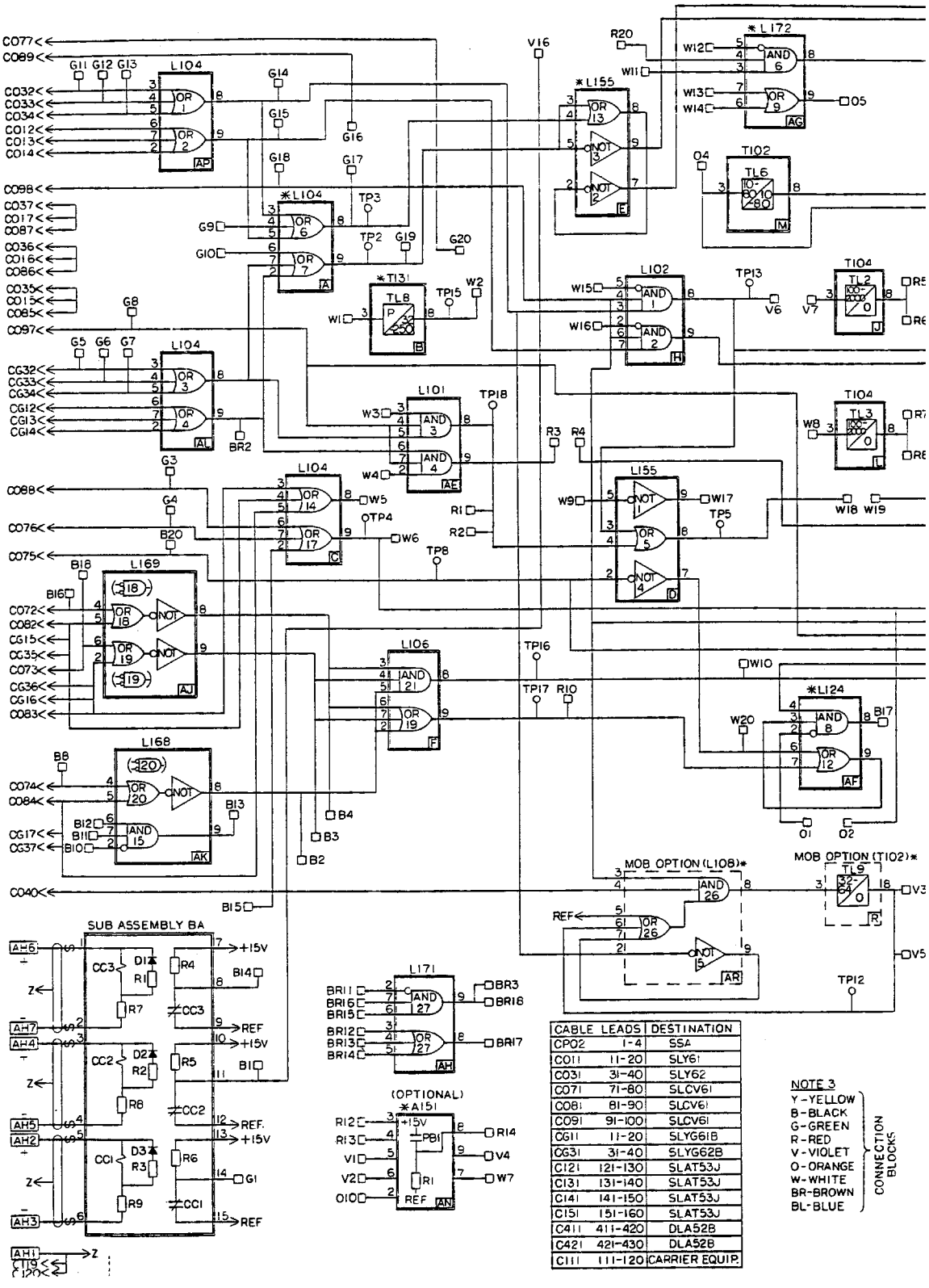
It should be sufficient to check the outputs produced at test points in the SLA53L when periodic calibration tests are made on the associated measuring units, for example, the phase and ground relays in the line relaying scheme. No separate periodic tests on the relay should be required.

TROUBLESHOOTING

In any troubleshooting of equipment, it should first be established which unit is functioning incorrectly. The overall logic diagram supplied with the equipment shows the combined logic of the complete equipment and the various test points in each unit. By signal tracing, using the overall logic diagram and the various test points, it should be possible to quickly isolate the trouble.

SPARE PARTS

To minimize possible outage time, it is recommended that one spare card of each type be carried in stock. It is possible to replace damaged or defective components on the printed circuit cards, but great care should be taken in soldering so as not to damage or bridge-over the printed circuit buses, or overheat the semiconductor components. The repaired area should be recovered with a suitable high-dielectric plastic coating to prevent possible breakdowns across the printed buses due to moisture and dust. The wiring diagrams for the cards in the SLA53L relay are included in the card book, GEK-34158.



CABLE LEADS		DESTINATION
CP02	1-4	SSA
C011	11-20	SLY61
C031	31-40	SLY62
C071	71-80	SLCV61
C081	81-90	SLCV61
C091	91-100	SLCV61
CG11	11-20	SLYG61B
CG31	31-40	SLYG62B
C121	121-130	SLAT53J
C131	131-140	SLAT53J
C141	141-150	SLAT53J
C151	151-160	SLAT53J
C411	411-420	DLA52B
C421	421-430	DLA52B
C111	111-120	CARRIER EQUIP.

NOTE 3
Y-YELLOW
B-BLACK
G-GREEN
R-RED
V-VIOLET
O-ORANGE
W-WHITE
BR-BROWN
BL-BLUE
CONNECTION BLOCKS

Figure 1A (0145D8959-0) Internal Connections for the Type SLA53L Relay

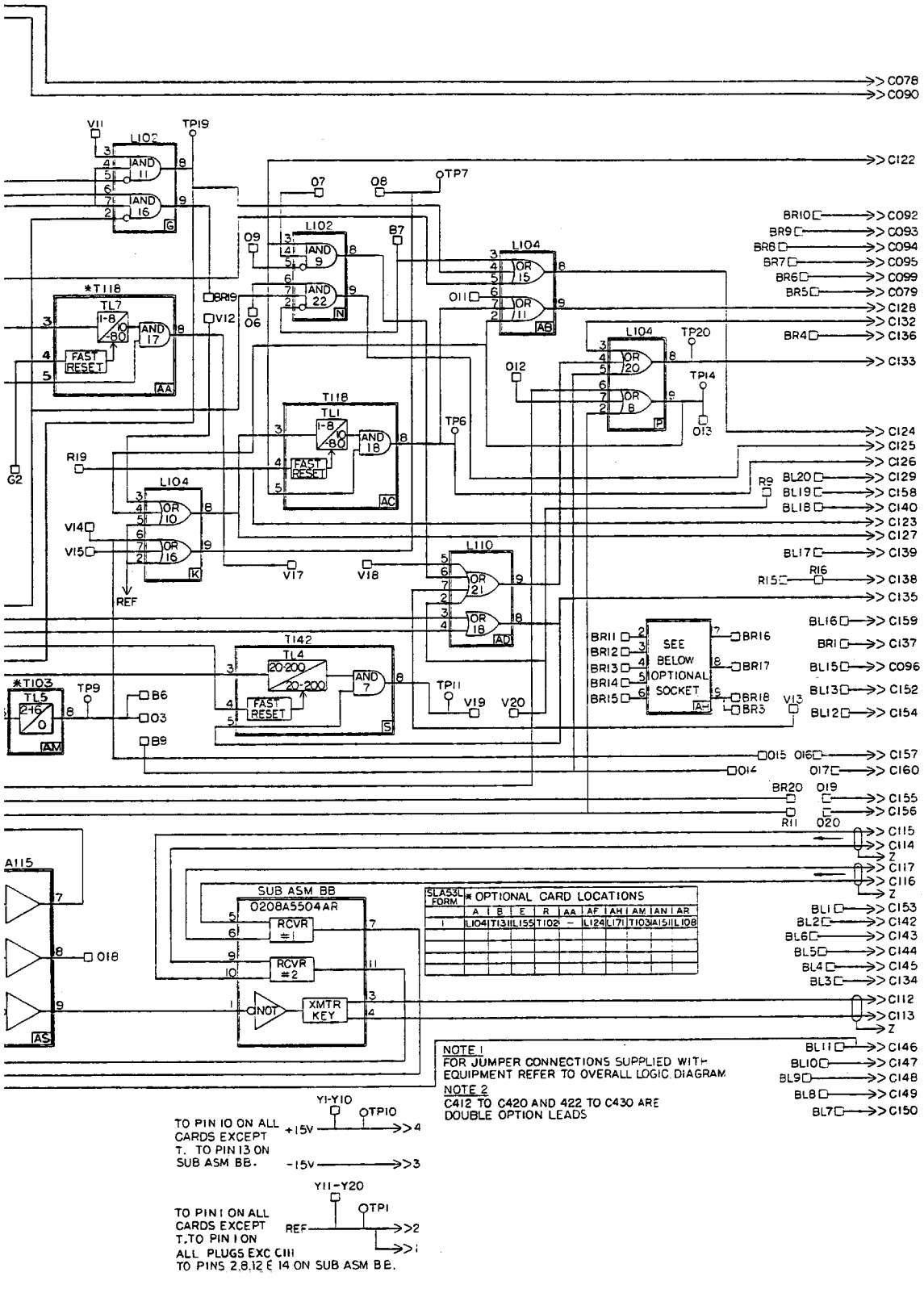
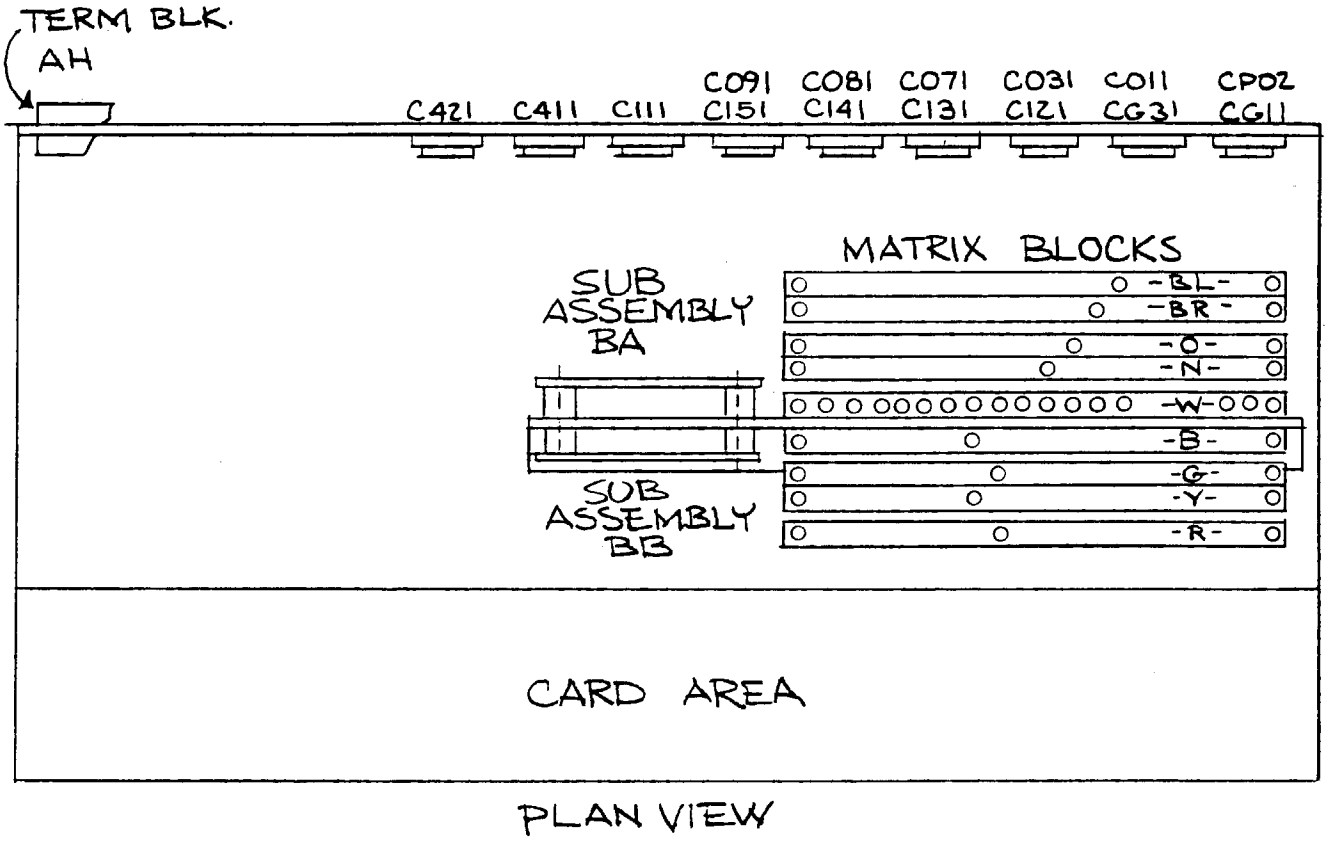
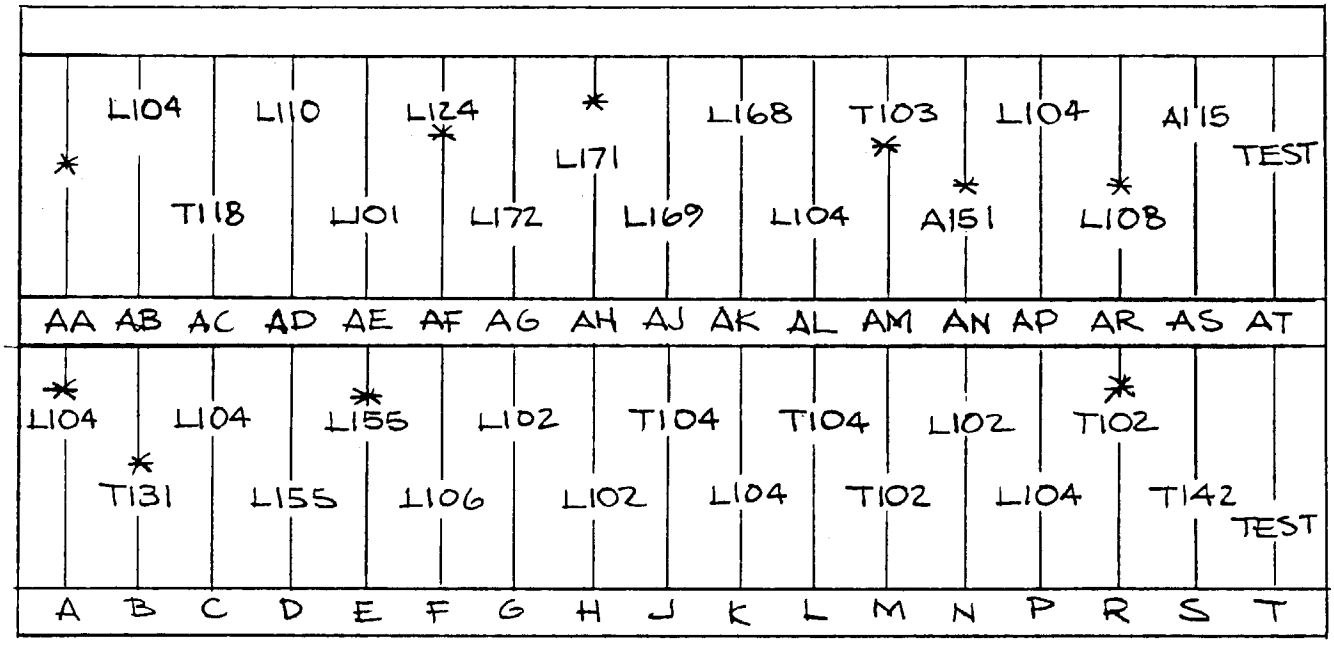


Figure 1B (0145D8959-0) Internal Connections for the Type SLA53L Relay



PLAN VIEW



*OPTIONAL CARDS

Figure 2 (0285A6766-0) Component Location Diagram for the Type SLA53L Relay

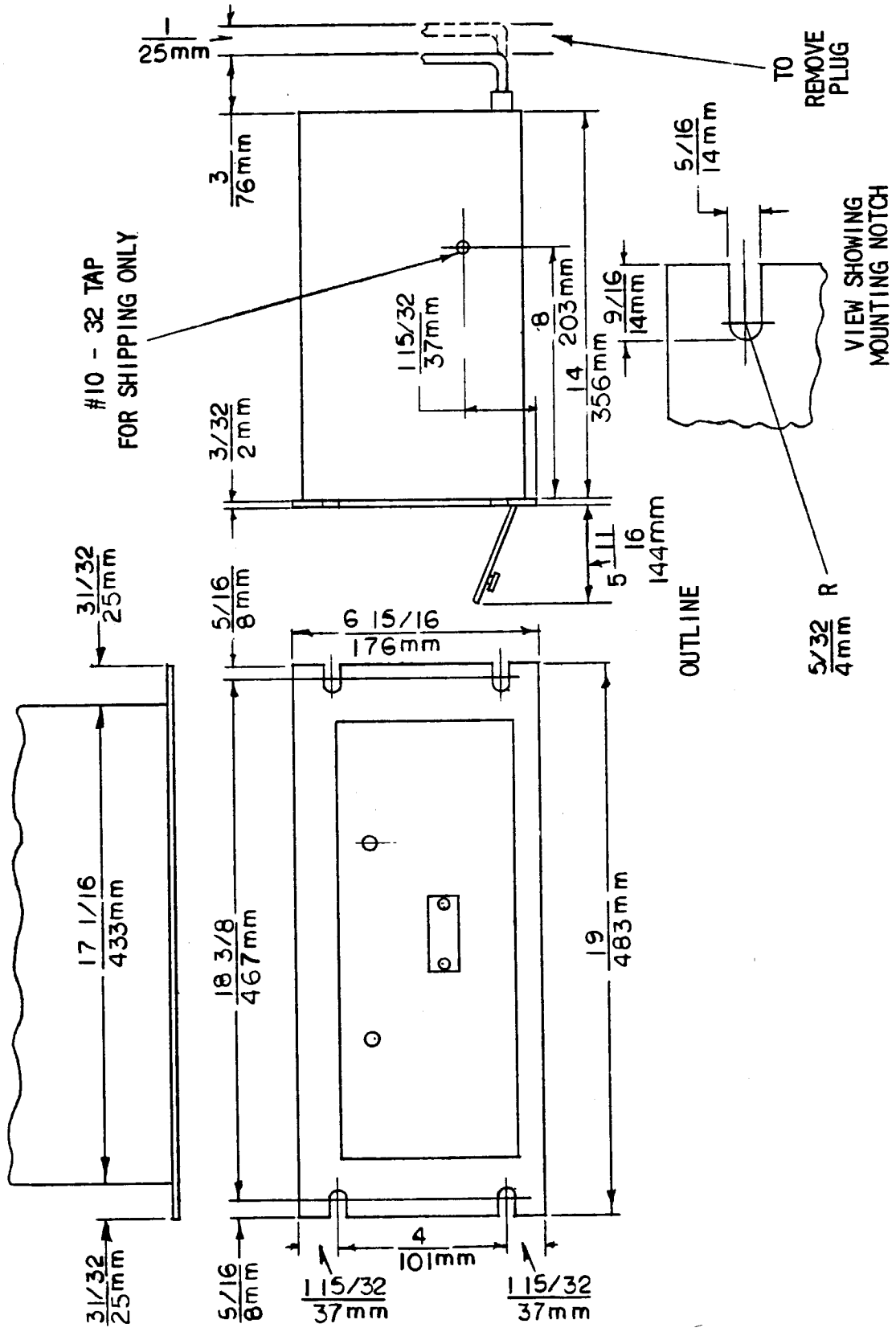


Figure 3 (0227A2037-0) Outline and Mounting Dimensions

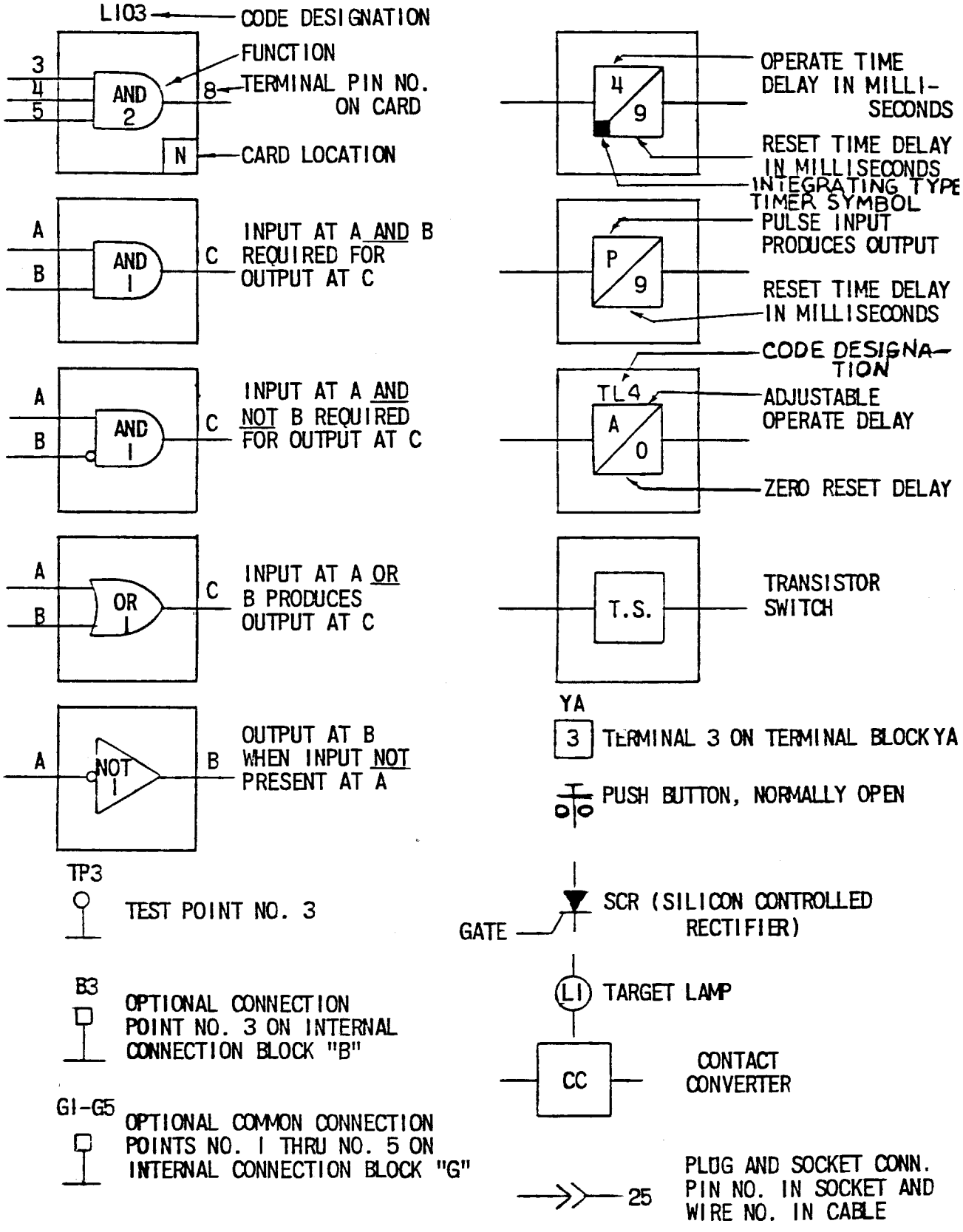


Figure 4 (0227A2047-1) Logic and Internal Connection Diagram Legend

THE FOLLOWING ARE FACTORY CONNECTIONS MADE AT THE MATRIX BLOCKS INSIDE OF THE SLA RELAY ASSOCIATED WITH THIS EQUIPMENT.

SYMBOLS LISTED: PL=RELAY INTERCONNECTING CABLE LEAD
(5)=LOGIC FUNCTION CARD PIN NUMBER
‡ =3-WAY CONNECTION
✕ = DLA MONITOR CONNECTION AVAILABLE BUT NOT USED
□ = 4-WAY CONNECTION

ALL DLA LEADS NOT USED, MUST BE INSULATED SEPARATELY (289)

MATRIX BLOCK JUMPERS		LOGIC FUNCTION		MATRIX BLOCK JUMPERS		LOGIC FUNCTION	
FROM	TO	FROM	TO	FROM	TO	FROM	TO
‡W17	G9	NOT1	OR6(4)	09	‡Y12	AND9(5)	REF
‡W17	G20	NOT1	PL77	011	Y13	OR11(6)	REF
W15	‡Y11	AND1(5)	REF	V18	Y14	OR21(5)	REF
V3	B10	TL9(8)	AND15(2)	V13	Y15	OR21(7)	REF
V5	BL6	TL9(8)	PL143	V20	Y16	OR21(2)	REF
‡V19	BL3	AND7(8)	PL134	B13	V12	AND15(9)	OR10(3)
‡V19	014	AND7(8)	OR20(5)	BR5	‡Y17	OR82(6)	REF
B9	BL19	AND7(8)	L7(4)	G17	G16	OR6(8)	D_2B(F.R.)
BR20	BL19	AND1(8)	L7(4)	BR7	W11	OR81	AND6(3)
BR20	V7	AND1(8)	TL2(3)	G14	R20	OR1(8)	AND8(4)
				‡V9	BR12	AND6(8)	OR27(3)
G1	B15	CC1(14)	OR17(2)	W4	‡Y19	AND4(2)	REF
R1	020	AND3(8)	L2(6)	BR2	‡Y19	OR4(9)	REF
R2	W8	AND3(8)	TL3(3)	BL15	BR15	TP18	AND27(6)
W6	01	OR17(9)	AND8(2)	G19	BR16	OR7(9)	AND27(7)
V6	019	AND1(8)	L1(4)	‡BR18	BR13	AND27(9)	OR27(4)
BL20	‡Y17	PL129	REF	G15	‡Y18	OR2(9)	REF
R5	V14	TL2(8)	OR16(6)	W16	Y3	AND2(2)	+15V
G10	‡Y18	OR7(6)	REF	R11	‡Y11	OR8(2)	REF
R7	V15	TL3(8)	OR16(7)	BL16	‡Y12	L9(3)	REF
‡08	016	OR16	L3(2)	B1	B7	CC2(11)	OR15(3)
‡08	07	OR16(9)	AND9(4)	W5	W1	OR14(8)	TL8(3)
BR17	012	OR27(8)	OR8(7)	W2	W9	TL8(8)	NOT1(5)
B17	B19	AND8(8)	TL5(3)	‡03	BL12	TL5(8)	LG(3)
B20	BL5	V1	PL144	‡03	BR14	TL5(8)	OR27(5)
W18	W19	OR5(8)	AND16(6)	R14	R4	PB1(8)	OR8(6)
‡BR19	B11	AND16(9)	AND15(7)	G4	W12	M1B	AND6(5)
‡BR19	BL9	AND16(9)	L1(5)	‡V9	BL13	AND6(8)	L4(4)
□BR4	BR1	AND31(6)	AND34(7)	G3	BR11	D_2B	AND27(2)
□BR4	R15	AND31(6)	OR31(8)	‡BR18	BL1	AND27(9)	L5(6)
□BR4	BL18	AND31(6)	TS37(3)				
R16	017	OR31(8)	L8(6)				
B12	Y1	AND15(6)	+15V				
W3	Y2	AND3(3)	+15V				
V11	Y4	AND11(3)	+15V				
06	Y5	AND22(6)	+15V				

Figure 5 (0227A2050-0, Sh. 289) Sample Option Chart

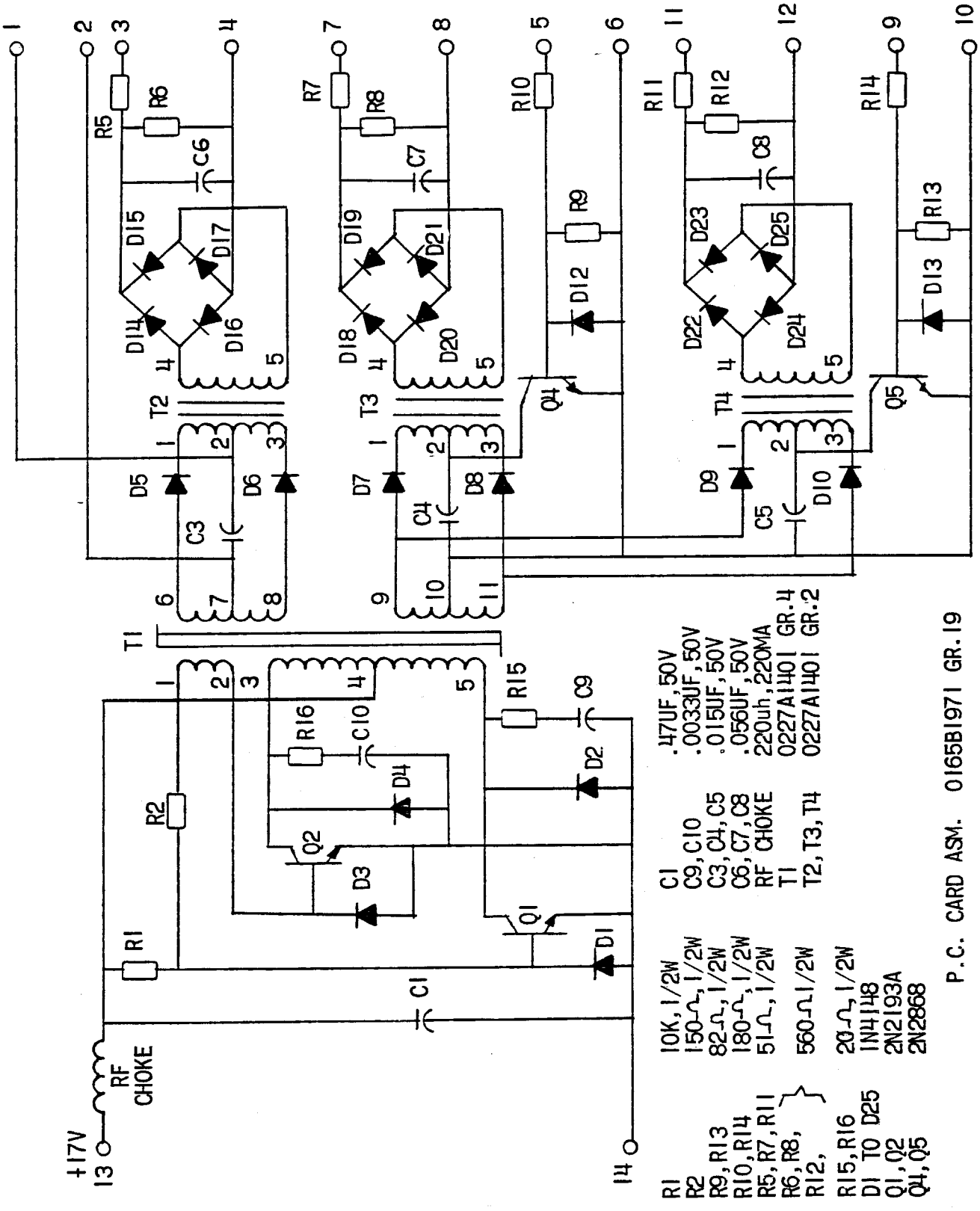
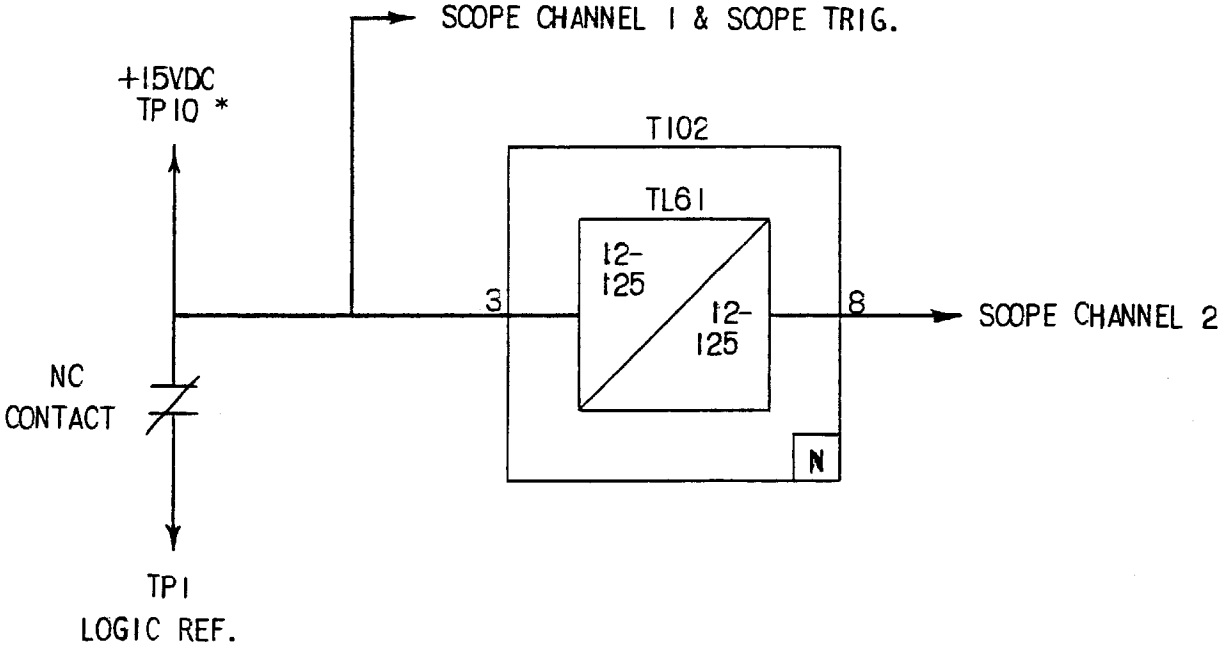


Figure 6 (0208A5504AR-0) Isolation Interface Internal Connection Diagram



* THE 15VDC SIGNAL AT PIN 10 HAS A CURRENT LIMITING RESISTOR MOUNTED ON THE TEST CARD.

Figure 7 (0246A7987-0) Logic Timer Test Circuit

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