



INSTRUCTIONS

GEK-86696

AUXILIARY LOGIC UNIT
TYPE SLA52V

GENERAL  **ELECTRIC**

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AUXILIARY LOGIC UNIT

TYPE SLA52V

DESCRIPTION

The SLA52V is an auxiliary logic relay for use in schemes using frequency shift channel equipment. It is usually used with a Type SLYP positive-sequence distance unit, a Type SLCN negative-sequence directional overcurrent unit, a Type SLAT output tripping unit, a Type SSA power supply, and a test panel.

The SLA52V has appropriate interconnections for use with a Type SLAT54 auxiliary and tripping unit when applied in single pole tripping and reclosing schemes.

The SLA52V is designed with considerable flexibility to accommodate various types of schemes such as blocking, unblocking, permissive transfer tripping, or combined schemes such as an unblocking scheme combined with a direct transfer trip scheme. Provision is made for various auxiliary tripping circuits which may be supplied initially or easily added later in the field. These optional circuits include direct tripping overcurrent and distance functions, line "pickup" circuitry, "weak infeed" trip circuitry, out-of-step tripping or blocking circuitry, and second zone back-up timing circuitry.

APPLICATION AND SETTINGS

Because of the flexibility of the Type SLA52V, the application and settings will vary with the particular type of scheme in which it is used. Refer to the overall logic diagram description for application and setting information for the particular scheme in which the SLA52V is used.

RATINGS

The Type SLA52V relay is designed for use in an environment where the ambient temperature outside the relay case is between -20°C and $+65^{\circ}\text{C}$.

The Type SLA52V relay requires a ± 15 volt DC power source which can be obtained from a Type SSA power supply.

Each contact converter in this relay has a link for selecting the proper voltage for the coil circuit of the contact converter. The three available voltage taps are for 48 VDC, 125 VDC or 250 VDC.

These instructions do not purport to cover all details or variations in equipment nor to provide for every possible contingency to be met in connection with installation, operation or maintenance. Should further information be desired or should particular problems arise which are not covered sufficiently for the purchaser's purposes, the matter should be referred to the General Electric Company.

To the extent required the products described herein meet applicable ANSI, IEEE and NEMA standards; but no such assurance is given with respect to local codes and ordinances because they vary greatly.

BURDENS

The SLA52V relay presents a burden of 350 mA to the +15 VDC supply of the Type SSA power supply.

Each contact converter, when energized, will draw approximately 10 mA from the station battery, regardless of the station battery voltage.

OPERATING PRINCIPLES

The functions included in the Type SLA52V relay involve basic logic operations (AND, OR, and NOT) where the presence or absence of signals, rather than their magnitude, controls the operation. Signals are measured with respect to a reference bus accessible at TP1. In general, a signal below one VDC represents an OFF or LOGIC ZERO condition; an ON or LOGIC ONE condition is represented by a signal of approximately +15 VDC.

The symbols used on the internal connection diagram (Fig. 1) are explained by the legend shown in Fig. 2.

The matrix blocks shown in the internal connections diagram of the SLA52V relay are connected by jumpers at the factory. These connections are used to implement the logic arrangement shown on the associated overall logic diagram. These matrix jumpers are listed on the associated option chart. A typical option chart for the Type SLA52V relay is shown in Fig. 3. Some of the matrix block connections may be customer options. These connections will then be shown as optional connections on the overall logic and must be selected by the user before the unit is placed in service.

The purpose of the contact converters (CC1, CC2, CC3, CC4, CC5, CC6) included in the Type SLA52V relay is to convert a contact operation into a signal that is compatible with the logic circuitry of the relay. When the external contact is closed, a plus 15 VDC signal is produced by the contact converter. The function of each contact converter depends upon the particular relaying scheme in which it is employed.

The Type SLA52V relay includes an isolation interface between the relaying equipment and the associated channel. When required, the internal connections of the interface card are shown in Fig. 4. The circuitry of the isolation interface provides a signal path but maintains metallic isolation. This feature makes it possible to maintain isolation between the DC power supply used for the relays and that employed by the channel.

CAUTION: Since this equipment uses sinking logic, namely the output stage of each printed circuit card is normally on, all externally supplied signals must be current limited. TP10 in each relay unit should be used exclusively for this purpose.

CONSTRUCTION

The SLA52V relay is packaged in an enclosed metal case with hinged front covers and removable top cover. The outline and mounting dimensions of the case and the physical location of the components are shown in Fig. 5 and 6, respectively.

The SLA52V relay contains printed circuit cards identified by a code number, such as A1110, T102, L104 where A designates auxiliary function, T designates time-delay function, and L designates logic function. The printed circuit cards plug in from the front of the unit. The sockets are marked with letter designations or "addresses" (D, E, F, etc.) which appear on the guide strips in front of each socket, on the component location drawing, on the internal connection diagram, and on the printed circuit card. The test points (TP1, TP2, etc.) shown in the internal connection diagram are connected to instrument jacks on a test card in position T or AT with TP1 at the top of the AT card. TP10 is tied to +15 VDC through a 2.2K resistor. This resistor limits the current when TP10 is used to supply a logic signal to a card.

Logic options in the SLA52S relay are selectable by means of jumper wires with taper tip pins on each end which are used to interconnect the matrix block points. These matrix blocks are located in the rear of the unit as shown in Fig. 6. The top cover of the relay must be removed to make the blocks accessible. The taper tip jumpers should be inserted and removed using the special tools which are supplied with each equipment. The green (G), black (B), white (W), violet (V), orange (O), blue (BL), natural (NA) and brown (BR) matrix blocks have 20 individual matrix points. The red (R) block has 20 points, which are grouped in ten pairs. The yellow (Y) block has 20 points which are grouped in two sets of ten common points; Y1 to Y10 are connected to plus 15 VDC, Y11 to Y20 are connected to reference.

RECEIVING, HANDLING AND STORAGE

These relays will normally be supplied as part of a static relay equipment, mounted in a rack or cabinet with other static relays and test equipment. Immediately upon receipt of a static relay equipment, it should be unpacked and examined for any damage sustained in transit. If injury or damage resulting from rough handling is evident, file a damage claim at once with the transportation company and promptly notify the nearest General Electric Sales Office.

Reasonable care should be exercised in unpacking the equipment. If the equipment is not to be installed immediately, it should be stored indoors in a location that is free from moisture, dust, metallic chips, and severe atmospheric contaminants.

Just prior to final installation the shipping support bolt should be removed from each side of all relay units to facilitate possible future unit removal for maintenance. These shipping support bolts are approximately eight inches back from the relay front panel.

STATIC RELAY EQUIPMENT, WHEN SUPPLIED IN SWING RACK CABINETS, SHOULD BE SECURELY ANCHORED TO THE FLOOR OR TO THE SHIPPING PALLET TO PREVENT THE EQUIPMENT FROM TIPPING OVER WHEN THE SWING RACK IS OPENED.

INSTALLATION TESTS

If the SLA52V relay that is to be tested is installed in an equipment which has already been connected to the power system, disconnect the outputs in the associated Type SLAT relay from the system.

CAUTION

THE LOGIC SYSTEM SIDE OF THE DC POWER SUPPLY USED WITH MOD III STATIC RELAY EQUIPMENT IS ISOLATED FROM GROUND. IT IS A DESIGN CHARACTERISTIC OF MOST ELECTRONIC INSTRUMENTS THAT ONE OF THE SIGNAL INPUT TERMINALS IS CONNECTED TO THE INSTRUMENT CHASSIS. IF THE INSTRUMENT USED TO TEST THE RELAY EQUIPMENT IS ISOLATED FROM GROUND, ITS CHASSIS MAY HAVE AN ELECTRICAL POTENTIAL WITH RESPECT TO GROUND. THE USE OF A TEST INSTRUMENT WITH A GROUNDED CHASSIS WILL NOT AFFECT THE TESTING OF THE EQUIPMENT. HOWEVER, A SECOND GROUND CONNECTION TO THE EQUIPMENT, SUCH AS A TEST LEAD INADVERTENTLY DROPPING AGAINST THE RELAY CASE, MAY CAUSE DAMAGE TO THE LOGIC CIRCUITRY. NO EXTERNAL TEST EQUIPMENT SHOULD BE LEFT CONNECTED TO THE STATIC RELAYS WHEN THEY ARE IN PROTECTIVE SERVICE, SINCE TEST EQUIPMENT GROUNDING REDUCES THE EFFECTIVENESS OF THE ISOLATION PROVIDED.

GENERAL

The SLA52V relay is supplied from the factory either mounted in a static relay equipment or as a separate unit associated with measuring relays, a Type SSA power supply, and some form of channel equipment. All relay units for a given terminal of static relaying equipment are tested together at the factory, and each unit will have the same summary number stamped on its nameplate.

Timers should be set for the operating or reset times indicated on the associated overall logic diagram. Where a time range is indicated on the overall logic diagram, the timer should be set for the value recommended for that function in the descriptive write-up accompanying the overall logic diagram. Where a setting depends upon conditions encountered on a specific application, this is so stated and the factors influencing the choice of setting are described. The procedure for checking and setting the timers is described in a later section.

OPERATIONAL CHECKS

Operation of the SLA52V unit can be checked by observing the signals at the twenty test points (TP1 to TP20) in the SLA52V, by observing the operation of the associated channel equipment, or by observing the output functions in the associated Type SLAT tripping relay. The test points are located on two test cards in positions T and AT and are numbered 1 to 20 from top to bottom. TP1 is the reference bus for the logic circuit; TP2 is at -15 VDC. The remaining points are located at various strategic points throughout the logic as shown on the internal connection diagram, Fig. 1. Test point voltages can be monitored with a portable high impedance voltmeter, the voltmeter on the test panel of the associated equipment, or an oscilloscope.

Operation of any logic function may be checked by supplying the correct inputs to the card. This is accomplished by placing the card under test in a card extender, removing the cards which normally supply the input signals, and then connecting the card inputs to either TP10 or TP1. An output should be produced when the proper combination of inputs is supplied.

TEST CARD ADAPTER

The test card adapter provides a convenient means of gaining access to any pin of a particular card. Detailed information on the use of the test card adapter is included in the card instruction book, GEK-34158.

TIMER ADJUSTMENTS AND TESTS

When the time-delay cards are to be adjusted or checked, an oscilloscope that can display two traces simultaneously and that has a calibrated horizontal sweep should be used.

In order to test the timer cards it is necessary to remove the card which supplies the input signal to the timer. If there are no test points at the input and output of the timer card under test, it is necessary to place it in a card adapter. This allows access to the inputs and outputs of the timer. A timer test card (catalog number 0172C5151G-1, see Fig. 8) can be used to supply an input signal to the timer, and at the same time trigger a scope or timing device. The timer card output is connected to stop the timing device, or display a step function on the scope. The pickup and drop-out times can be adjusted to the desired values. An alternative to the timer test card is the test circuit of Fig. 7. A bounce-free switch is recommended.

OVERALL EQUIPMENT TESTS

After the SLA52V relay and the associated static relay units have been individually calibrated and tested for the desired settings, a series of overall operating circuit checks is advisable.

The elementary, overall logic, and logic description for the specific job will be useful for determining the overall operation of the scheme.

Overall equipment tests can be performed by applying alternating current to the measuring units at the voltages specified in the instruction book for the measuring units, and checking that proper outputs are obtained from the associated SLAT when the measuring units operate.

MAINTENANCEPERIODIC TESTS

It should be sufficient to check the outputs produced at test points in the SLA52V when periodic calibration tests are made on the associated measuring units, for example, the phase and ground relay in the line relaying scheme. No separate periodic tests on the SLA52V itself should be required.

TROUBLESHOOTING

A dual trace oscilloscope is a valuable aid to detailed troubleshooting, since it can be used to determine phase shift, operate and reset times, as well as input and output levels. A portable dual-trace oscilloscope with a calibrated sweep and trigger facility is recommended.

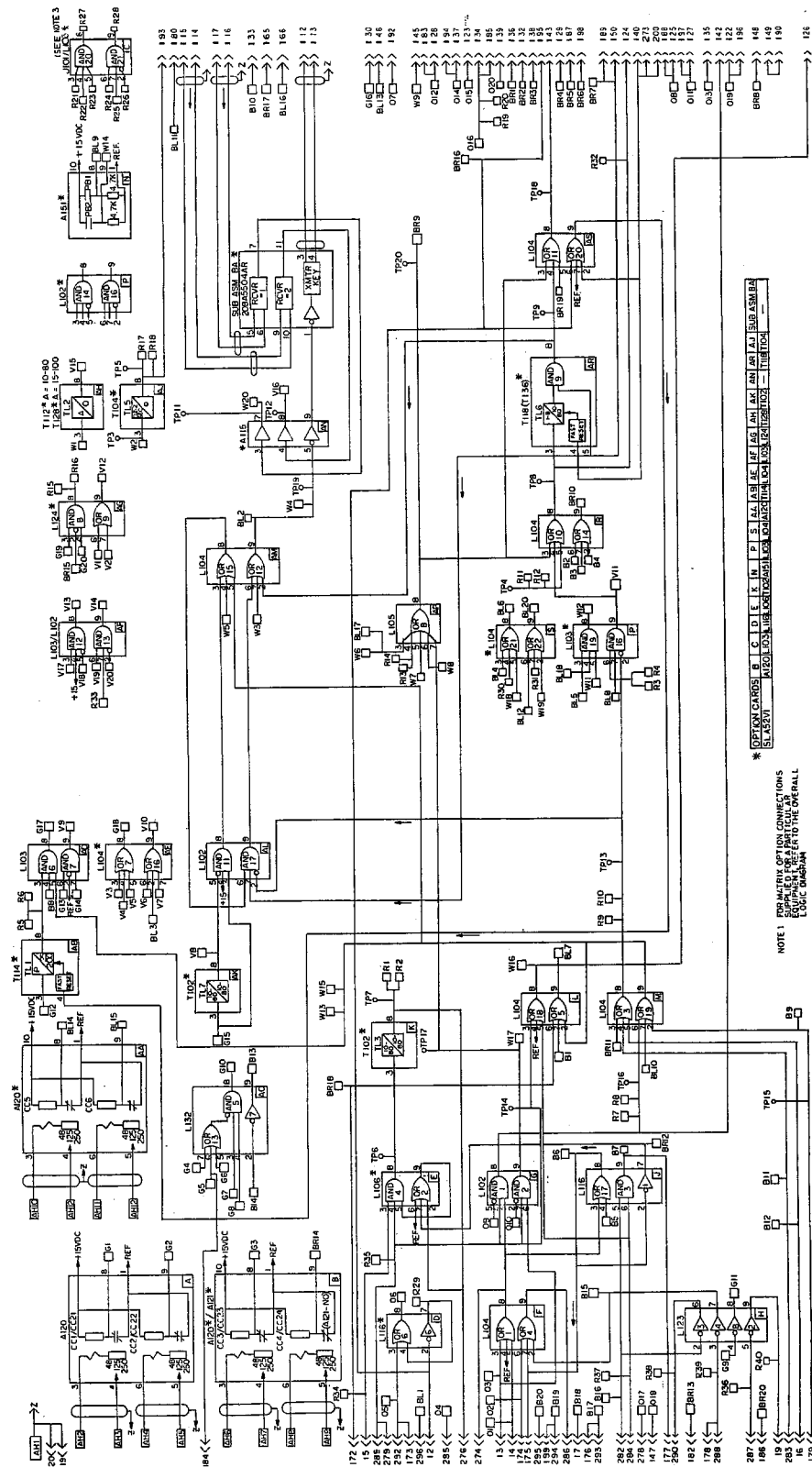
In any troubleshooting of equipment, it should first be established which unit is functioning incorrectly. The overall logic diagram supplied with the equipment shows the combined logic of the complete equipment and the various test points in

each unit. By signal tracing, using the overall logic diagram and the various test points, it should be possible to isolate the trouble quickly.

A test adapter card is supplied with each static relay equipment to supplement the prewired test points on the test cards. Use of the adapter card is described in the card instruction book, GEK-34158.

SPARE PARTS

To minimize possible outage time, it is recommended that a complete maintenance program should include the stocking of at least one spare card of each type. It is possible to replace damaged or defective components on the printed circuit cards, but great care should be taken in soldering so as not to damage or bridge-over the printed circuit buses, or overheat the semiconductor and other components. The repaired area should be re-covered with a suitable high-dielectric plastic coating to prevent possible breakdowns across the printed buses due to moisture and dust. The wiring diagrams for the cards in the SLA52V relay are included in the card book, GEK-34158.



* OPTION CARDS B C D I E K N P S T A L A B A C E F G H J M A N A R A S A T A U A V A W A X A Y A Z SUB ASM BA
 SLA52V MICRO LOGIC OPTION CARDS FOR CONTROLLER LOGIC CENTER LOGIC - TIME LOGIC

NOTE 1: RED MATRIX OPTION CONNECTIONS SHOWN FOR A PART CULMINATING EQUIPMENT REFER TO THE OVERALL LOGIC DIAGRAM

NOTE 2: J, K, L, M, N, P, S, T REPRESENTS RED MATRIX BLOCK
 A, B, C, D, E, F, G, H, I, J, K, L, M, N, O, P, Q, R, S, T, U, V, W, X, Y, Z

NOTES: W, X, Y, Z, A, B, C, D, E, F, G, H, I, J, K, L, M, N, O, P, Q, R, S, T, U, V, W, X, Y, Z
 PIN 3 TO PINS AND JUMPER PINS TO PINS
 PIN 3 TO PINS AND JUMPER PINS TO PINS

C412-C400 - TRIPLE OPTION LEADS SEE MATRIX BLOCK
 C402-C430 - DOUBLE OPTION LEADS CORN DUSHAM
 ** NOTE 4: THERE ARE TWO RED MATRIX BLOCKS

TO PIN 10 ALL CARDS EXCEPT I, TO PIN 13 ON SUB ASM BA
 TO PIN 10 ALL CARDS EXCEPT I, TO PIN 13 ON SUB ASM BA
 TO PIN 10 ALL CARDS EXCEPT I, TO PIN 13 ON SUB ASM BA
 TO PIN 10 ALL CARDS EXCEPT I, TO PIN 13 ON SUB ASM BA

Fig. 1 (0153D6933-0) Internal Connections Diagram for the Type SLA52V Relay

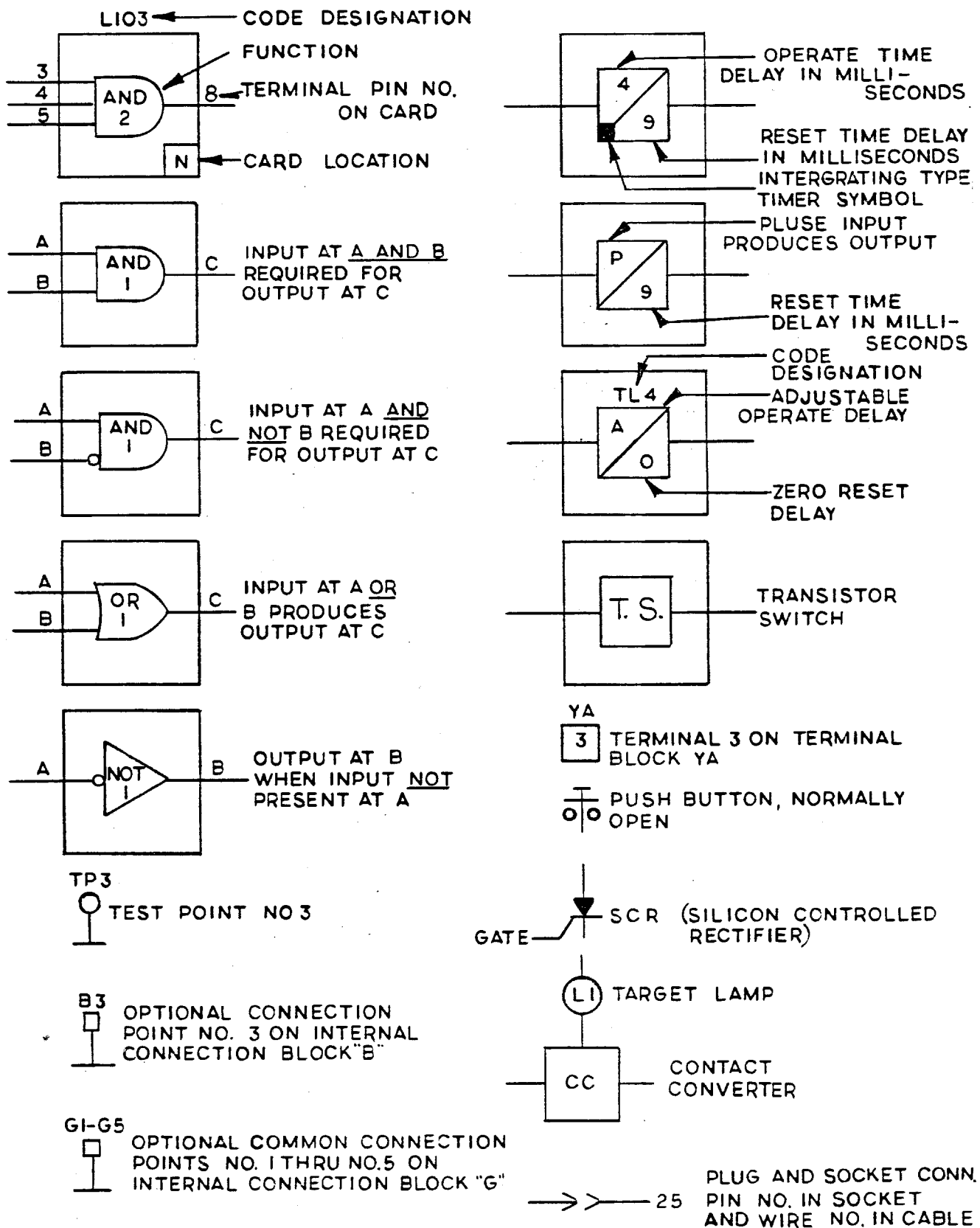


Fig. 2 (0227A2047-1) Internal Connection Diagram Legend

THE FOLLOWING ARE FACTORY CONNECTIONS MADE AT THE MATRIX BLOCKS INSIDE OF THE SLA RELAY ASSOCIATED WITH THIS EQUIPMENT.

SYMBOLS LISTED: PL=RELAY INTERCONNECTING CABLE LEAD

(5)=LOGIC FUNCTION CARD PIN NUMBER

±=3-WAY CONNECTION

*=DLA MONITOR CONNECTION AVAILABLE BUT NOT USED

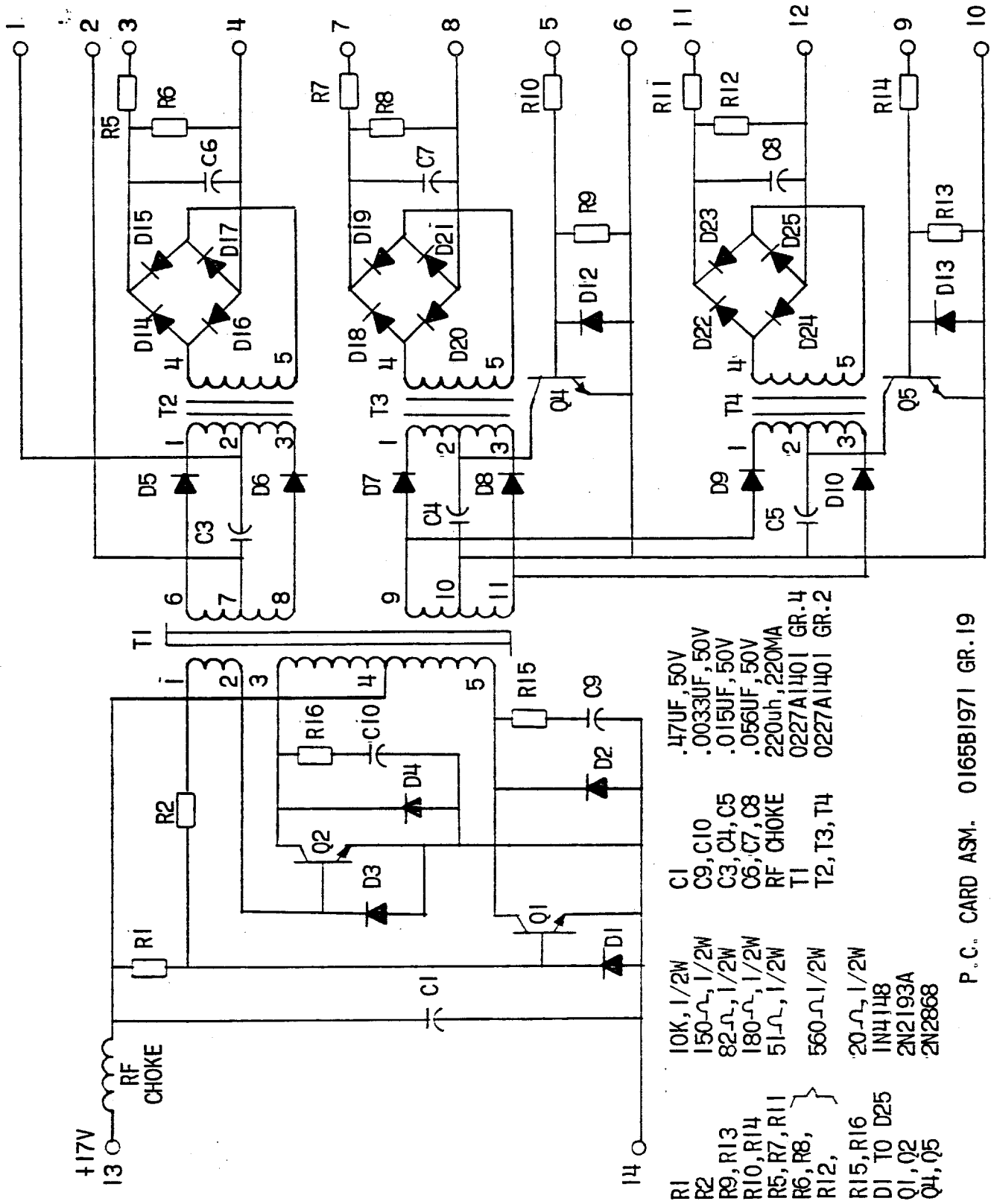
Δ=4 WAY CONNECTION

UNUSED DLA WIRE FROM PLUGS 411 & 412 MUST BE INDIVIDUALLY INSULATED & BOUND TOGETHER.

352A

MATRIX BLOCK JUMPERS		LOGIC FUNCTION		MATRIX BLOCK JUMPERS		LOGIC FUNCTION	
FROM	TO	FROM	TO	FROM	TO	FROM	TO
422 ±	V4	PL422	OR7 (AE4)	B18	BR12	PL17	NOT1 (J7)
422 ±	V15	PL422	TL2 (AH6)	413 Δ	R1	PL413	TL3 (K8)
R10	G6	OR3 (M8)	OR13 (AC5)	413 Δ	O9	PL413	AND1 (G5)
V10	O19	OR16 (AE9)	PL196	413 Δ	B2	PL413	OR14 (R6)
G18 Δ	V7	OR7 (AE8)	OR16 (AF7)	R4 ±	G15	AND16 (P6)	TL7 (AK3)
G18 Δ	W7	OR7 (AE8)	OR8 (AP5)	R4 ±	G16	AND16 (P6)	PL130
G18 Δ	BR6	OR7 (AE8)	PL196	V8	G4	TL7 (AK8)	OR13 (AC7)
V14 ±	G7	AND13 (AF9)	AND5 (AC3)	G2	W5	CC2 (A9)	OR15 (AM4)
V14 ±	R3	AND13 (AF9)	AND16 (P6)	418 ±	B12	PL418	PL16
G3	V20	CC3 (B8)	AND13 (AF2)	418 ±	B3	PL418	OR14 (R7)
V6	Y14	OR16 (AE6)	REF.	W3	Y11	OR12 (AM7)	REF.
O16	BR2	PL134	PL132	BR10	O10	OR14 (R9)	AND2 (G2)
R2	O13	TL3 (K8)	PL135	BL10	Y12	OR19 (M7)	REF.
R7	W2	AND1 (G8)	TL5 (AJ3)	G12	G1	TL1 (AB3)	CC1 (A8)
423 ±	R18	PL423	TL5 (AJ8)	R5	G13	TL1 (AB8)	AND7 (AD6)
423 ±	V3	PL423	OR7 (AE3)	R6	B5	TL1 (AB8)	OR17 (J4)
BR16	O15	PL195	PL123	415 ±	O4	PL415	PL285
BR20	B14	PL186	NOT7 (AC2)	415 ±	W6	PL415	OR8 (AP3)
G17	V1	AND6 (AD8)	OR9 (AG6)	W16	G14	OR18 (L8)	AND7 (AD7)
V9	V2	AND7 (AD9)	OR9 (AG7)	B9 ±	W10	PL179	PL144
419 Δ	V5	PL419	OR7 (AE5)	B8	Y1	AND6 (AD4)	+15VDC
419 Δ	V12	PL419	OR9 (AG9)	BL7	BL8	OR5 (L9)	AND16 (P7)
419 Δ	BL13	PL419	PL146	B1	Y13	OR5 (L7)	REF.
417 ±	V11	PL417	AND16 (P9)	R9 ±	BR15	OR3 (M8)	AND8 (AG2)
417 ±	BR1	PL417	PL136	R16	W1	AND8 (AG6)	TL2 (AH3)
O18	BR9	PL147	OR8 (AP8)	O6	G8	OR6 (D8)	AND5 (AC4)
414 Δ	G10	PL414	AND5 (AC8)	B13	G20	NOT7 (AC9)	AND8 (AG4)
414 Δ	R12	PL414	OR10 (R5)	416	B11	PL416	PL283
414 Δ	W9	PL414	PL145	BL3	Y15	OR16 (AE2)	REF.
412 ±	BL1	PL412	PL296	BL2	R24	OR12 (AM9)	AND21 (C6)
B19	G19	PL294	AND8 (AG3)	W4	R21	OPI2 (AM9)	AND20 (C3)
				412 ±	R31	PL412	OR22 (57)
				W19	Y16	OR22 (52)	REF.

Fig. 3 (0227A2050 Sh. 352A) Typical Option Chart for the Type SLA52V Relay



- R1 10K, 1/2W
- R2 150Ω, 1/2W
- R9, R13 82Ω, 1/2W
- R10, R14 180Ω, 1/2W
- R5, R7, R11 51Ω, 1/2W
- R6, R8, R12, R15, R16 20Ω, 1/2W
- D1 TO D25 1N4148
- Q1, Q2 2N2193A
- Q4, Q5 2N2868
- C1 .47UF, 50V
- C9, C10 .0033UF, 50V
- C3, C4, C5 .015UF, 50V
- C6, C7, C8 .056UF, 50V
- RF CHOKE 220uh, 220MA
- T1 0227A1401 GR.4
- T2, T3, T4 0227A1401 GR.2

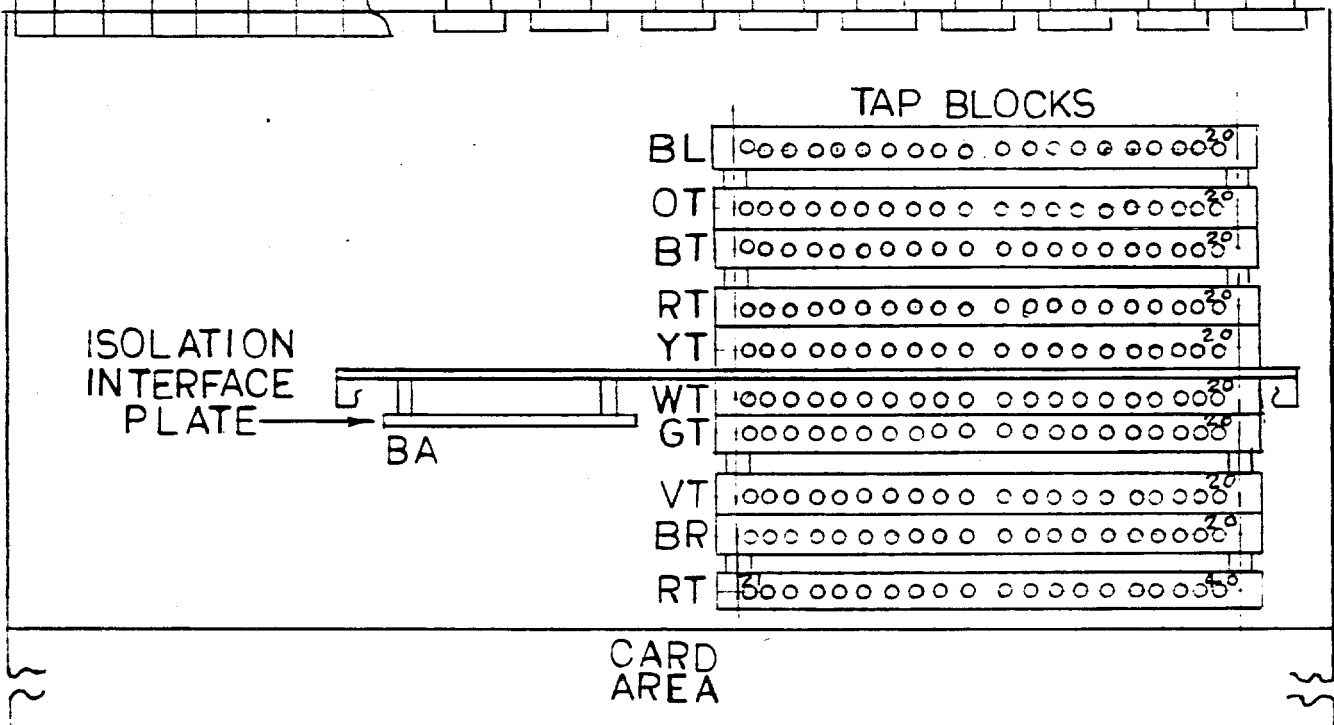
P.C. CARD ASM. 0165B1971 GR.19

Fig. 4 (0208A5504AR-0) Isolation Interface Circuit Internal

TERMINAL BLOCKS

(TOP)
(BOT)

C161 C421 C411 C141 C131 C121 C111 C011 CPO2
C291 C281 C271 C191 C181 C171



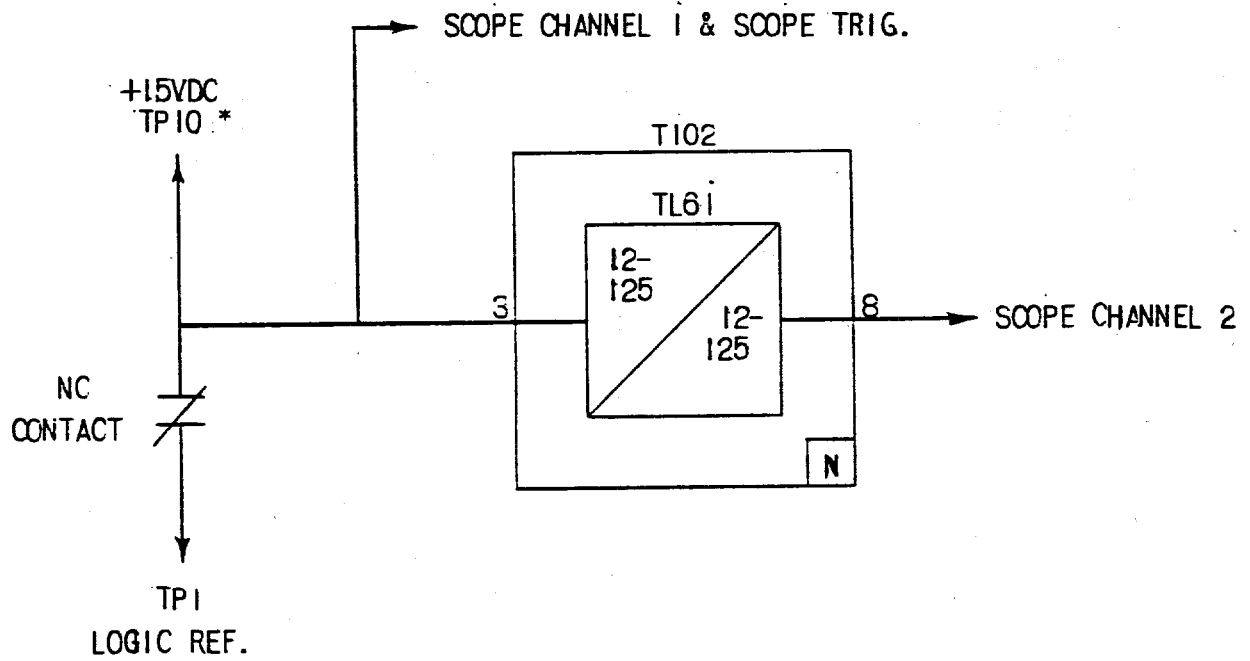
* OPTIONAL
P.C.CAPDS

PLAN VIEW

* AI20	* T114	LI03	* LI03	* T128	* T102	LI04	LI05	LI04							
	LI32	* LI04	* LI24	* T104	LI02	*	* T118	TEST							
AA	AB	AC	AD	AE	AF	AG	AHA	AJ	AK	AL	AMAN	AP	AR	AS	AT
* AI20		* LI16	LI04	LI23	* T102	LI04	* LI03	* LI04							
AI20		LI03	* LI06	LI02	LI16	LI04	* AI51	LI04	TEST						
A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T

FRONT VIEW

Fig. 6 (0285A9252-0) Component and Printed Circuit Card Location Diagram for the Type SLA52V Relay



* THE 15VDC SIGNAL AT PIN 10 HAS A CURRENT LIMITING RESISTOR MOUNTED ON THE TEST CARD.

Fig. 7 (0246A7987-0) Logic Timer Test Circuit

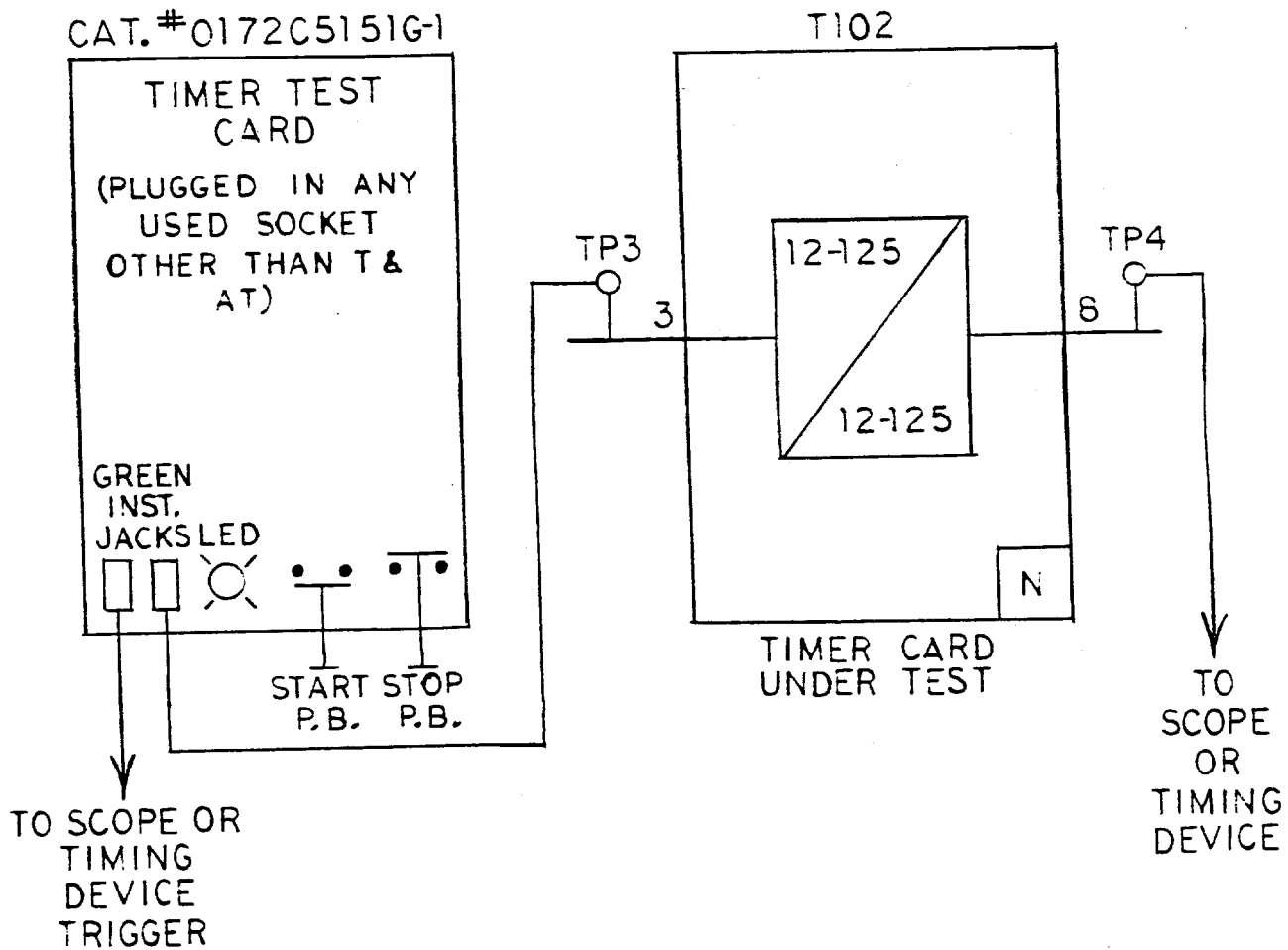


Fig. 8 (0285A6135-0) Timer Test Card Test Circuit

