



INSTRUCTIONS

GEK-45425

STATIC OUTPUT AND TRIPPING UNIT

TYPE SLAT51F

POWER SYSTEMS MANAGEMENT DEPARTMENT

GENERAL  ELECTRIC

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STATIC OUTPUT AND TRIPPING UNIT

TYPE SLAT51F

DESCRIPTION

The Type SLAT51F relay is a static output and tripping unit. This relay is not intended to be used by itself, but rather as part of a complement of equipment that forms a protective relaying scheme. For a complete description of the overall scheme in which this relay is employed, refer to the overall logic diagram and its associated logic description that is supplied with each terminal.

The Type SLAT51F relay is packaged in a two rack unit (1 R.U. = 1 3/4") enclosed metal case suitable for mounting on a 19 inch rack. The outline and mounting dimensions are shown in Figure 1. The internal connections for the SLAT51F relay are shown in Figure 2. The component and card locations are shown in Figure 3.

APPLICATION

The Type SLAT51F relay is a static output and tripping relay designed for use in various types of static relaying schemes. For example, the SLAT51F relay can be used in conjunction with types SLY, SLYG, SLC, SSA and SLA relays to make up a directional comparison pilot relaying scheme. Other schemes are also available in which the SLAT51F relay can be used. For a complete description of the particular scheme in which the SLAT51F relay is employed, refer to the overall logic diagram and description supplied with the scheme. The following is a listing of the various output functions included in the SLAT51F together with a general description of their intended uses.

SCR - Two silicon controlled rectifier trip circuits are provided to permit tripping of associated circuit breakers.

RI - The reclose initiation outputs are provided to initiate automatic reclosing after a high speed trip.

BFI - The breaker failure initiation outputs are provided for breaker failure protection.

RR1,RR2,RR3 - Optional reed relay contact outputs, the driving function of which may be selected from any of the number of logic points available in the associated SLA relay. The reed relay outputs are typically used for oscillograph start, data logging or other miscellaneous operations.

In addition to the above output functions, three target lamps are provided with each SLAT51F, and three more lamps can be provided as an option.

An adjustable timer, TL-32, can be provided as an option and it may be used to restrict target lamp indication to the function(s) that first operated. See the section under CALCULATION OF SETTINGS for further details and instructions for setting this timer.

RATINGS

The Type SLAT51F relay is designed for use in an environment where the air temperature outside the relay case does not exceed -20°C and $+65^{\circ}\text{C}$.

The Type SLAT51F relay requires a ± 15 volt d-c power source which can be obtained from a Type SSA power supply.

The SCR tripping circuits are rated for 48/125 or 250 volt d-c. Each has a 1.0 ampere series target. The tripping circuits are designed to carry 30 amperes for one second.

The contacts of the telephone type relays that are used for RI and BFI will make and carry 3 amperes continuously, and will interrupt up to 0.5 amperes (inductive) at 125 volt d-c or 0.25 ampere (inductive) at 250 volt d-c.

The contacts of the reed relays that are used for options A and B are rated for 100 watts d-c. They will carry 3 amperes continuously and have a one second rating of 20 amperes.

Refer to the unit nameplate for the ratings of a particular relay.

These instructions do not purport to cover all details or variations in equipment nor to provide for every possible contingency to be met in connection with installation, operation or maintenance. Should further information be desired or should particular problems arise which are not covered sufficiently for the purchaser's purposes, the matter should be referred to the General Electric Company.

To the extent required the products described herein meet applicable ANSI, IEEE and NEMA standards; but no such assurance is given with respect to local codes and ordinances because they vary greatly.

BURDENS

The SLAT51F relay presents a maximum burden to the Type SSA power supply of:

370 ma from the +15 volt d-c supply
120 ma from the -15 volt d-c supply

In addition, each target lamp draws 80 ma from the -15 volt d-c supply.

A. SCR TRIP CIRCUIT

Two electrically separate, isolated SCR trip circuits are provided to trip two breakers. Each circuit is capable of carrying 30 amperes for one second.

The internal connections for the SCR trip and isolator subassemblies are shown in Figure 4. The isolator card, by means of a DC to DC converter, provides a signal path but maintains metallic isolation. This feature makes it possible to isolate the relay power supply from the trip circuit power supply.

B. RI RECLOSE INITIATE CIRCUIT

Two electrically separate normally open contacts are provided. These contacts close within 17 milliseconds from the time the associated coil is energized by the logic. The contacts open within 170 milliseconds from the time the coil is deenergized. The RI function uses a telephone type relay with contact ratings stated under RATINGS.

C. BFI BREAKER FAILURE INITIATE CIRCUIT

Two electrically separate normally open contacts are provided. These contacts close within 17 milliseconds from the time the associated coil is energized by the logic. These contacts open within 170 milliseconds from the time the coil is deenergized. The BFI function uses a telephone type relay with contact ratings stated under RATINGS.

D. OPTIONAL OUTPUTS

Four optional reed relay contact outputs can be provided in either normally open or normally closed configuration. The contacts operate within 2 milliseconds from the time logic signals change state. These are selected from the matrix points in the SLA.

TARGETS

Two electromechanical target coils are included, one in series with each SCR. These targets operate on one ampere of trip current when the associated SCR passes current. The trip circuit resistance in the relay is 0.40 ohm. Three target lamps are included and three additional lamps are available as options in the Type SLAT51F as shown on the internal connections diagram, Figure 2. Refer to the overall logic diagram for the scheme for the target lamps provided. When TL32 is provided, its output will prevent the target lamps from turning on. A long pickup setting on this timer will permit all functions that operate to light their associated lamps. A short time setting will allow only those functions that operate initially to be indicated.

LOGIC CIRCUITS

The functions of the Type SLAT51F involve basic logic (AND, OR, AND NOT) where the presence or absence of signals, rather than their magnitude, controls the operation. Signals are measured with respect to a reference bus accessible at TP1. In general a signal below 1 volt d-c represents an OFF or LOGIC ZERO condition, an ON or LOGIC ONE is represented by a signal of approximately +15 volt d-c.

The symbols used on the internal connection diagram (Figure 2) are explained by the legend shown in Figure 5.

CALCULATION OF SETTINGS

There is one optional timer function in the SLAT51F that requires field adjustment.

- 1) The 5-30/0 timer TL32 enables the user to control the number of lamps that will light under certain fault conditions. With a short pickup setting (5-10 milliseconds) only lamp(s) associated with those units which first sensed the fault will light. Increased pickup settings will cause the lamps associated with all units that operate to light. The timer setting should not exceed the minimum

breaker clearing time in order to avoid targets which may result from breaker unequal pole opening times.

CONSTRUCTION

The SLAT51F relay is packaged in an enclosed metal case with hinged front cover and removable top cover. The outline and mounting dimensions of the case and the physical location of the components are shown in Figures 1 and 3 respectively.

The SLAT51F relay contains printed circuit cards identified by a code number such as: A104, T106, L109 where A designated an auxiliary function, T designated a time-delay function, and L designated a logical function. The printed circuit cards plug in from the front of the unit. The sockets are marked with letter designations or "addresses" (D,E,F, etc.) which appear on the guide strips in front of each socket, on the component location drawing, on the unit internal connection diagram, and on the printed circuit card. The test points (TP1, TP2, etc.) shown on the internal connection diagram are connected to instrument jacks on a test card in position T with TP1 at the top of the T card. TP1 is tied to reference; TP10 is tied to +15 volt d-c through a 1.5K resistor. This resistor limits the current when TP10 is used to supply a logic signal to a card.

The SLAT51F relay receives its inputs from the associated Type SLA relay. These units are interconnected by ten conductor shielded cables. The sockets for these cables are located on the rear panel of the unit. The SLAT51F output functions are connected to 12-point terminal strips, which are also located on the rear of the unit.

A window is provided in the hinged cover of the relay to allow target lamps and the mechanical targets to be seen. Push buttons are also provided to reset the targets and lamps without opening the cover.

RECEIVING, HANDLING AND STORAGE

These relays will normally be supplied as a part of a static relay equipment, mounted in a rack or cabinet with other static relays and test equipment. Immediately upon receipt of a static relay equipment, it should be unpacked and examined for any damage sustained in transit. If injury or damage resulting from rough handling is evident, file a damage claim at once with the transportation company and promptly notify the nearest General Electric Sales Office.

Reasonable care should be exercised in unpacking the equipment. If the equipment is not to be installed immediately, it should be stored indoors in a location that is free from moisture, dust, metallic chips, and severe atmospheric contaminants.

Just prior to final installation the shipping support bolt should be removed from each side of all relay units, to facilitate possible future unit removal for maintenance. These shipping support bolts are approximately eight inches back from the relay front panel. Static relay equipment, when supplied in swing rack cabinets, should be securely anchored to the floor or to the shipping pallet to prevent the equipment from tipping over when the swing rack is opened.

TEST INSTRUCTIONS

CAUTION

THE LOGIC SYSTEM SIDE OF THE D-C POWER SUPPLY USED WITH MOD III STATIC RELAY EQUIPMENT IS ISOLATED FROM GROUND. IT IS A DESIGN CHARACTERISTIC OF MOST ELECTRONIC INSTRUMENTS THAT ONE OF THE SIGNAL INPUT TERMINALS IS CONNECTED TO THE INSTRUMENT CHASSIS. IF THE INSTRUMENT USED TO TEST THE RELAY EQUIPMENT IS ISOLATED FROM GROUND, ITS CHASSIS MAY HAVE AN ELECTRICAL POTENTIAL WITH RESPECT TO GROUND. THE USE OF A TEST INSTRUMENT WITH A GROUNDED CHASSIS WILL NOT AFFECT THE TESTING OF THE EQUIPMENT. HOWEVER, A SECOND GROUND CONNECTION TO THE EQUIPMENT, SUCH AS A TEST LEAD INADVERTENTLY DROPPING AGAINST THE RELAY CASE, MAY CAUSE DAMAGE TO THE LOGIC CIRCUITRY. NO EXTERNAL TEST EQUIPMENT SHOULD BE LEFT CONNECTED TO THE STATIC RELAYS WHEN THEY ARE IN PROTECTIVE SERVICE, SINCE TEST EQUIPMENT GROUNDING REDUCES THE EFFECTIVENESS OF THE ISOLATION PROVIDED.

If the SLAT51F relay that is to be tested is installed in an equipment which has already been connected to the power system, disconnect the outputs to the system.

A. GENERAL

The SLAT51F relay is supplied from the factory either mounted in a static relay equipment or as a separate unit associated with measuring relays, a Type SSA power supply, and some form of channel equipment. All relay units for a given terminal of static relaying equipment are tested together at the factory, and each unit will have the same summary number stamped on its nameplate.

In general, when a time range is indicated on the internal connections diagram, the timer has been factory set at a mid-range value. Timers should be set for the operating or reset times indicated on the associated overall logic diagram. Where a time range is indicated on the overall logic diagram, the timer should be set for the value recommended for that function in the descriptive writeup accompanying the overall logic diagram. Where a setting depends upon conditions encountered on a specific application, this is so stated and the factors influencing the choice of setting are described. The procedure for checking and setting the timers is described in a later section.

B. OPERATIONAL CHECKS

Operation of the SLAT51F unit can be checked by observing the signals at the twenty test points (TP1 to TP20) in the SLAT51F by observing the operation of the associated channel equipment, or by observing the output functions. The test points are located on two test cards in positions T and AT, and are numbered 1 to 20 from top to bottom. TP1 is the reference bus for the logic circuit, TP10 is at +15 volt d-c. The remaining points are located at various strategic points throughout the logic as shown in the internal connection diagram (Figure 2). Test point voltages can be monitored with a portable high impedance voltmeter, the voltmeter on the test panel of the associated equipment, or an oscilloscope.

C. TEST CARD ADAPTER

The test card adapter provides a convenient means of gaining access to any pin of a particular card. Detailed information on the use of the test adapter card is included in the card instruction book GEK-34158.

D. TIMER ADJUSTMENTS AND TESTS

When the time-delay cards are to be adjusted or checked, an oscilloscope that can display two traces simultaneously and that has a calibrated horizontal sweep should be used.

In order to test the timer cards it is necessary to remove the card previous to the timer (see Table I) and to place the timer card in a card adapter. The card adapter allows access to the input and output of the timer if they are not brought out on test points. The timer test circuit is shown on Figure 6. Opening the normally closed contact causes the output to step up to +15 volt d-c after the pickup delay of the timer. To increase the pickup time, turn the upper potentiometer on the timer card clockwise; to decrease the time turn it counterclockwise. Closing the contact causes the timer output to drop out after the reset time-delay setting of the card. If the timer card is provided with a variable reset delay, it can be adjusted by the lower potentiometer on the timer card (clockwise increases reset time).

TABLE I

TIME UNDER TEST	POSITION	REMOVE CARD IN POSITION
TL31	F	NONE*
TL32	H	G **

* Turn power supply switch on and off.

** Refer to overall logic diagram for functions in associated units which should be removed.

E. TRIP CIRCUIT TESTS

The SCR trip circuits and series mechanical targets may be checked by connecting an auxiliary lock-out relay, such as the Type HEA relay, in series with the SCR circuit. A typical circuit is shown in Figure 7. The HEA relay should have the same d-c rating as the SCR trip circuit of the SLAT51F. If an auxiliary lock-out relay is not available, it can be replaced by a resistive load which limits the trip circuit current to three amperes. In most equipments, the SCR can be gated by operating a test push button in the associated units.

Prior to final installation, a check of the overall trip circuit should be made with the SCR outputs connected to trip the circuit breakers.

F. OVERALL EQUIPMENT TESTS

After the SLAT51F relay and the associated static relay units have been individually calibrated and tested for the desired settings, a series of overall operating circuit checks is advisable.

The elementary, overall logic, and logic description for the specific job will be useful for determining the overall operation of the scheme.

Overall equipment test can be performed by applying alternating current and voltages to the measuring units as specified in the instruction book for the measuring units and checking that proper outputs are obtained when the measuring units operate.

MAINTENANCE

A. PERIODIC TESTS

It should be sufficient to check the outputs produced at test points in the SLAT51F when periodic calibration tests are made on the associated measuring units, for example, the phase and ground relays in line-relaying scheme. No separate periodic tests in the SLAT51F itself should be required.

B. TROUBLE SHOOTING

In any trouble shooting of equipment, it should first be established which unit is functioning incorrectly. The overall logic diagram supplied with the equipment shows the combined logic of the complete equipment and the various test points in each unit. By signal tracing, using the overall logic diagram and the various test points, it should be possible to quickly isolate the trouble.

A test adapter card is supplied with each static relay equipment to supplement the prewired test points on the test cards. Use of the adapter card is described in the card instruction book GEK-34158.

A dual trace oscilloscope is a valuable aid to detailed trouble shooting, since it can be used to determine phase shift, operate and reset times as well as input and output levels. A portable dual-trace oscilloscope with a calibrated sweep and trigger facility is recommended.

C. SPARE PARTS

To minimize possible outage time, it is recommended that a complete maintenance program should include the stocking of at least one spare card of each type. It is possible to replace damaged or defective components on the printed circuit cards, but great care should be taken in soldering so as not to damage or bridge-over the printed circuit busses, or overheat the semi-conductor components. The repaired area should be recovered with a suitable high-dielectric plastic coating to prevent possible breakdowns across the printed busses due to moisture and dust. The wiring diagrams for the cards in the SLAT51F relay are included in the card book GEK-34158.

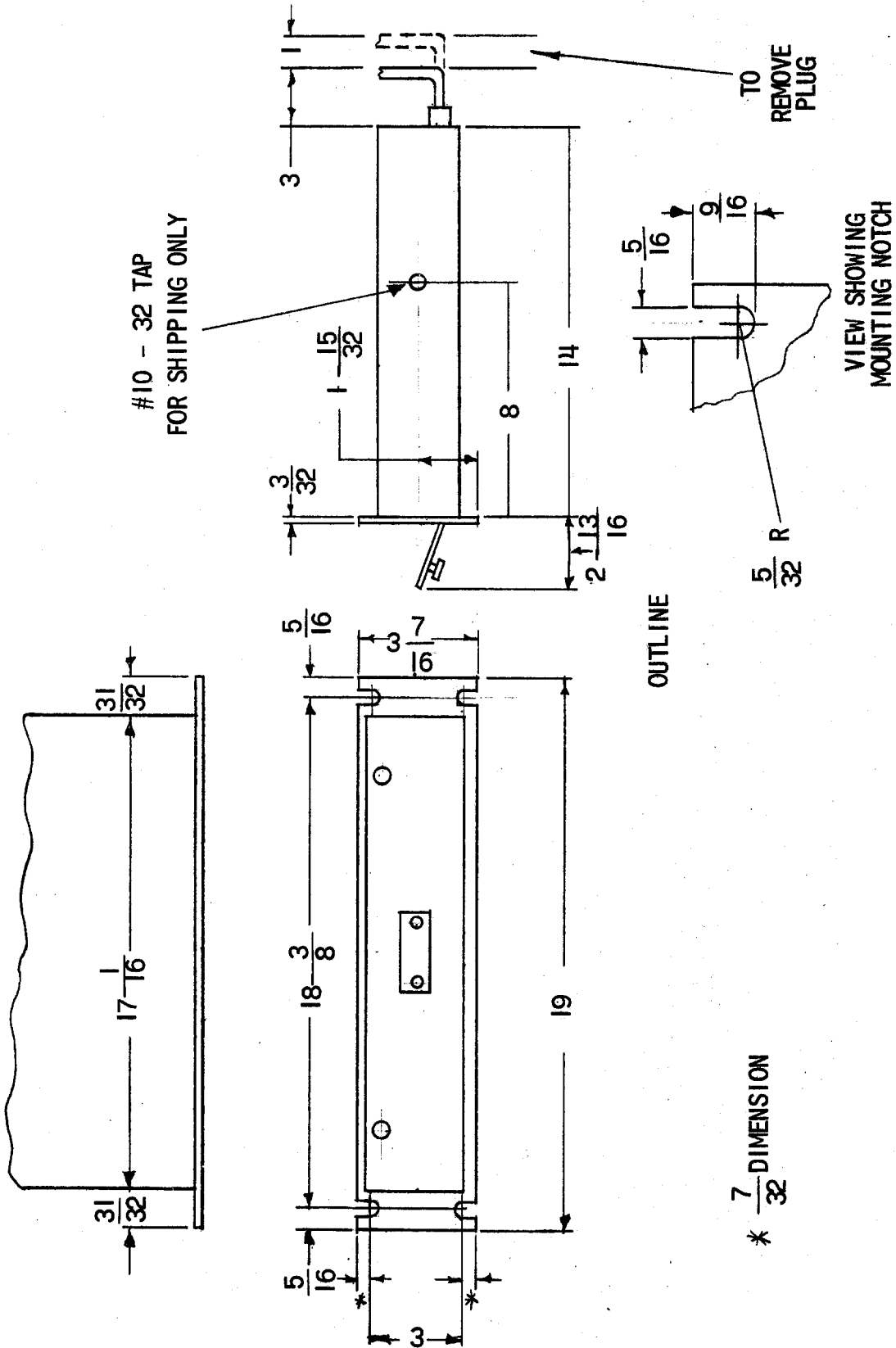


FIG. 1 (0227A2036-0) Outline and Mounting Dimensions for the Type SLAT51F

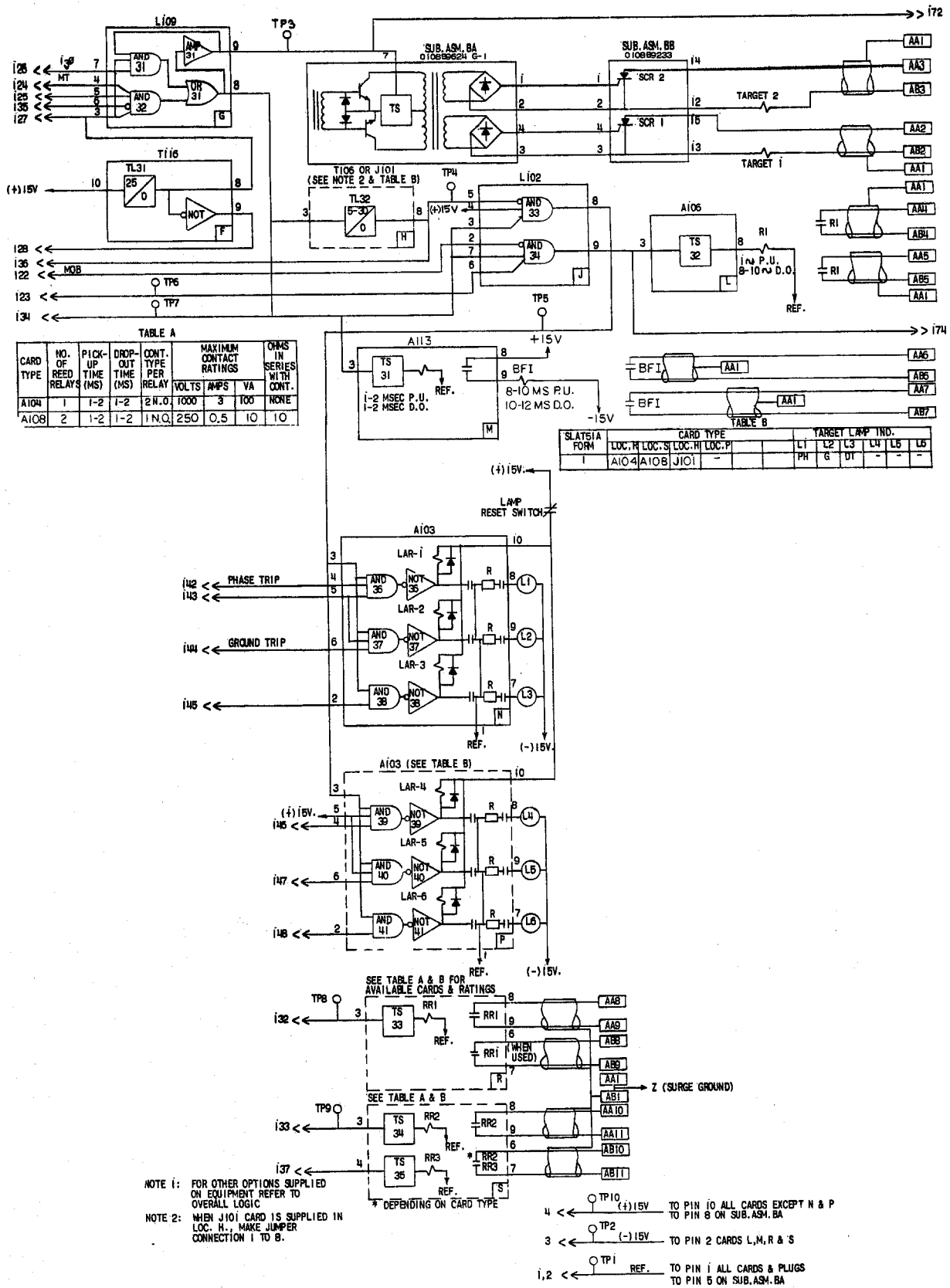
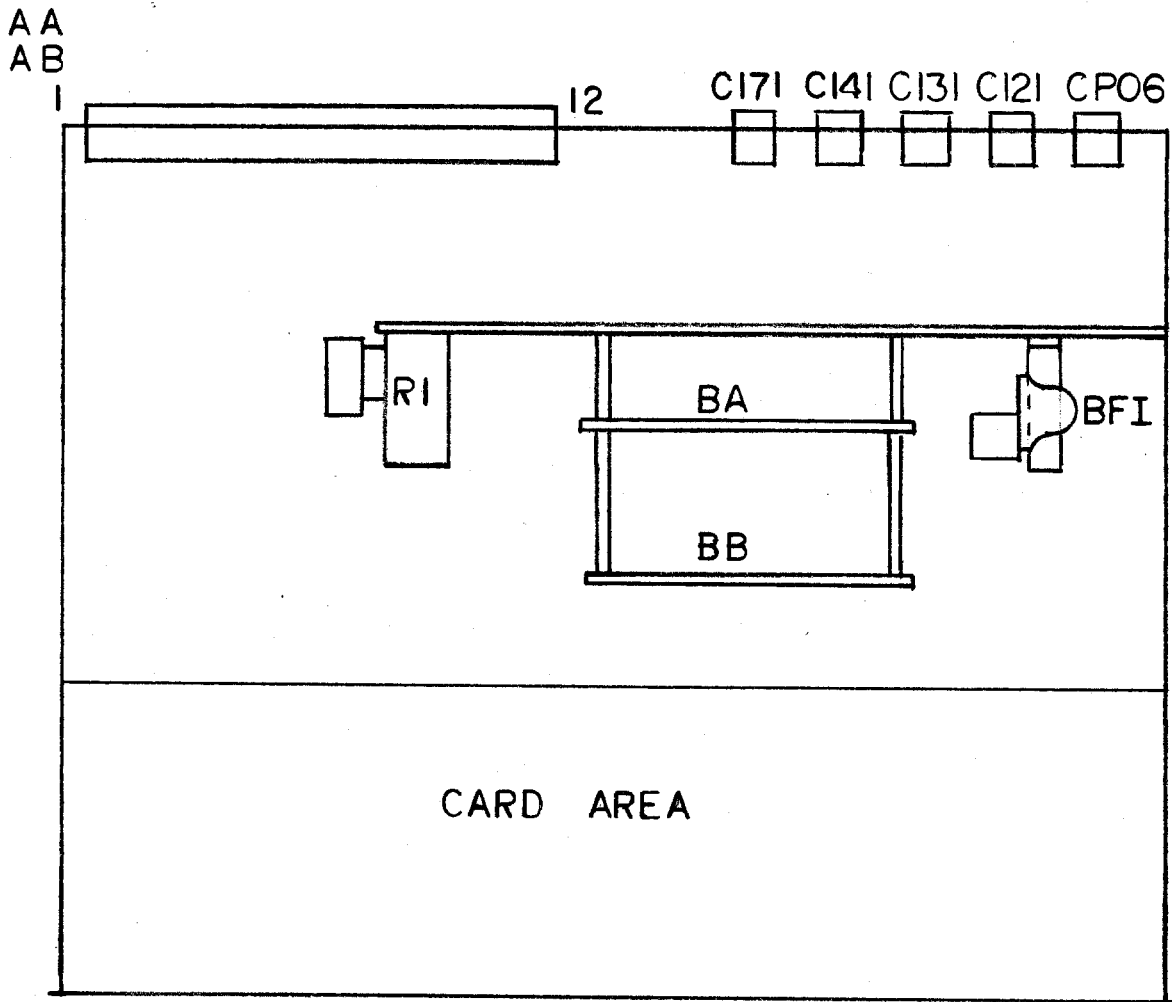
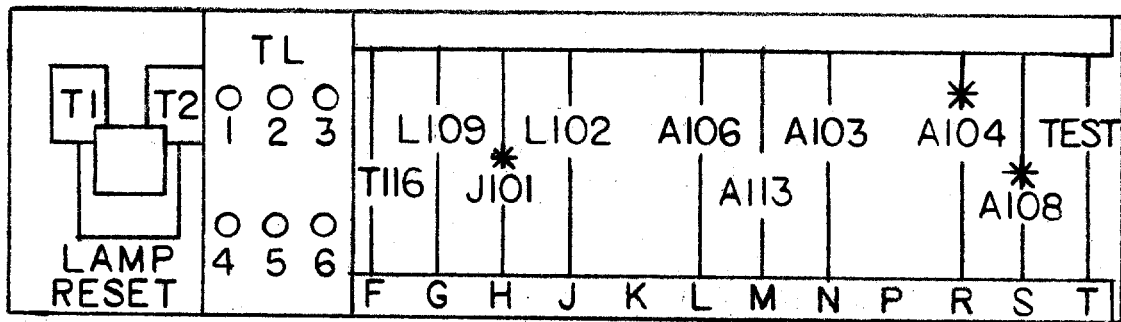


FIG. 2 (171C7879-0) Internal Connections for the Type SLAT51F Relay



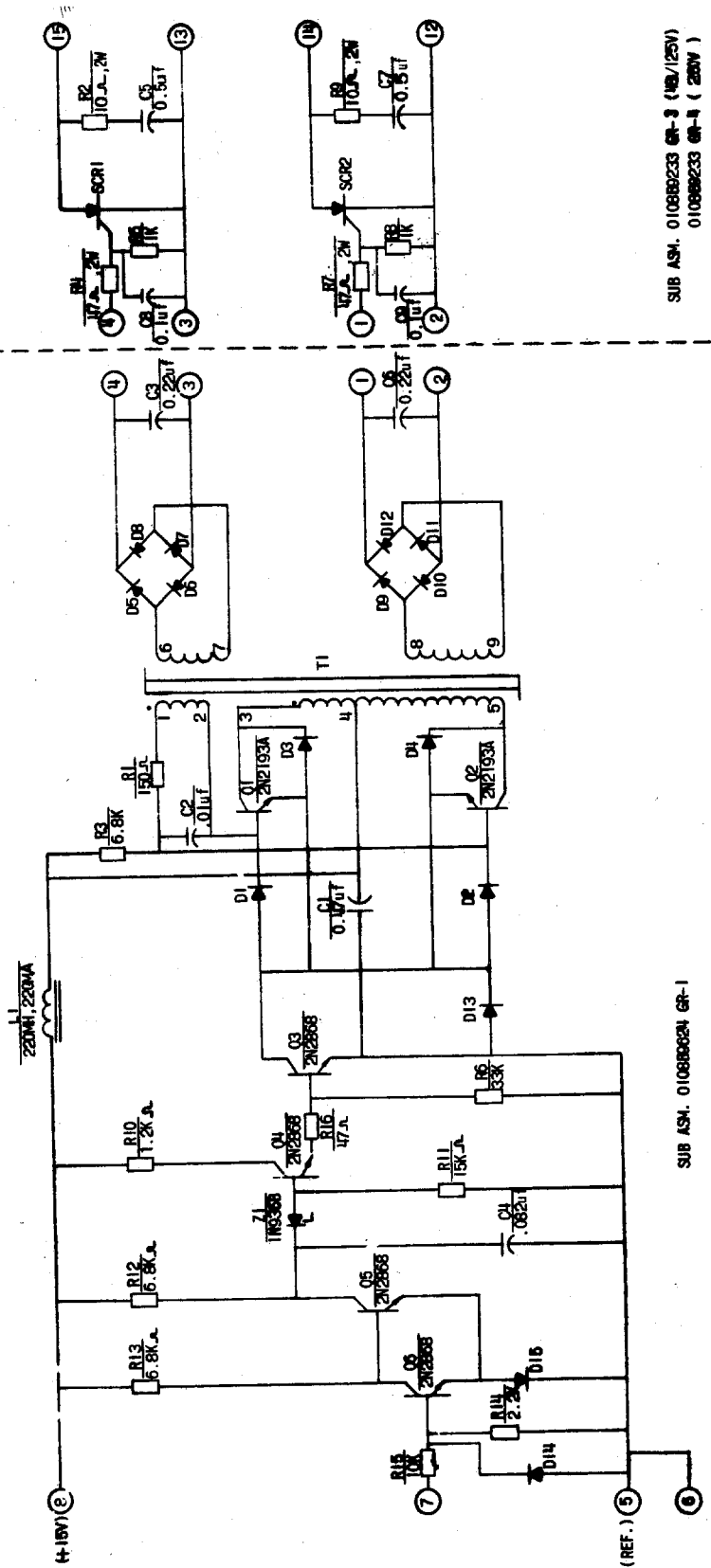
PLAN VIEW



FRONT VIEW

*OPTIONAL REFER TO UNIT INTERNAL CONNECTIONS

FIG. 3 (257A8781-0) Component Locations for the Type SLAT51F Relay



SUB ASM. 0108B9233 GR-3 (100/125V)
 0108B9233 GR-4 (200V)

SUB ASM. 0108B9624 GR-1

ALL DIODES 1N4148 UNLESS NOTED
 ALL RES. 1/2 WATT ± 5% UNLESS NOTED
 (2) = TERM. POST ON BOARD ASM
 1N6358 = 9.1V ± 5%

FIG. 4 (108B9610-0) Internal Connections for the SCR Trip and Isolator Subassemblies

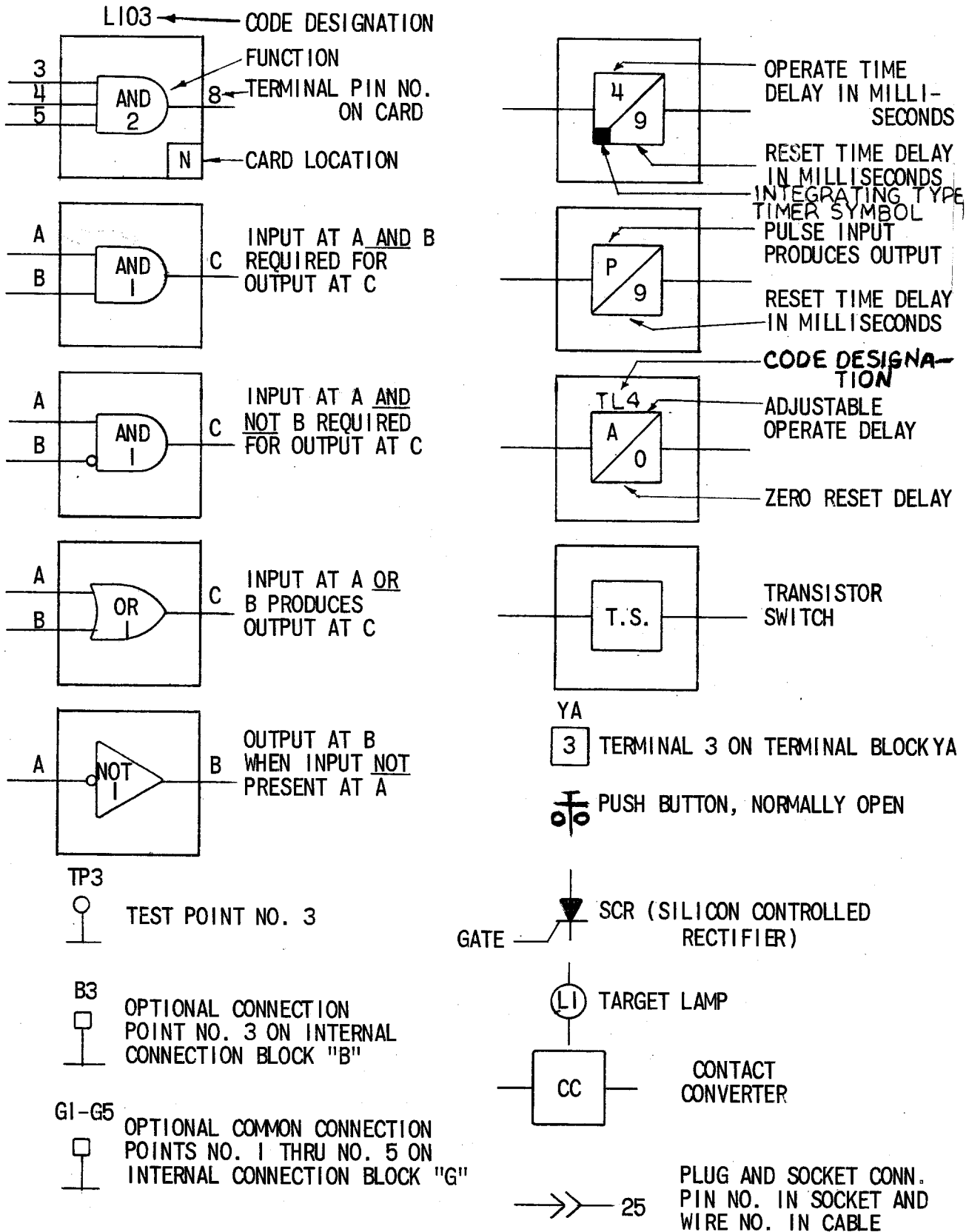
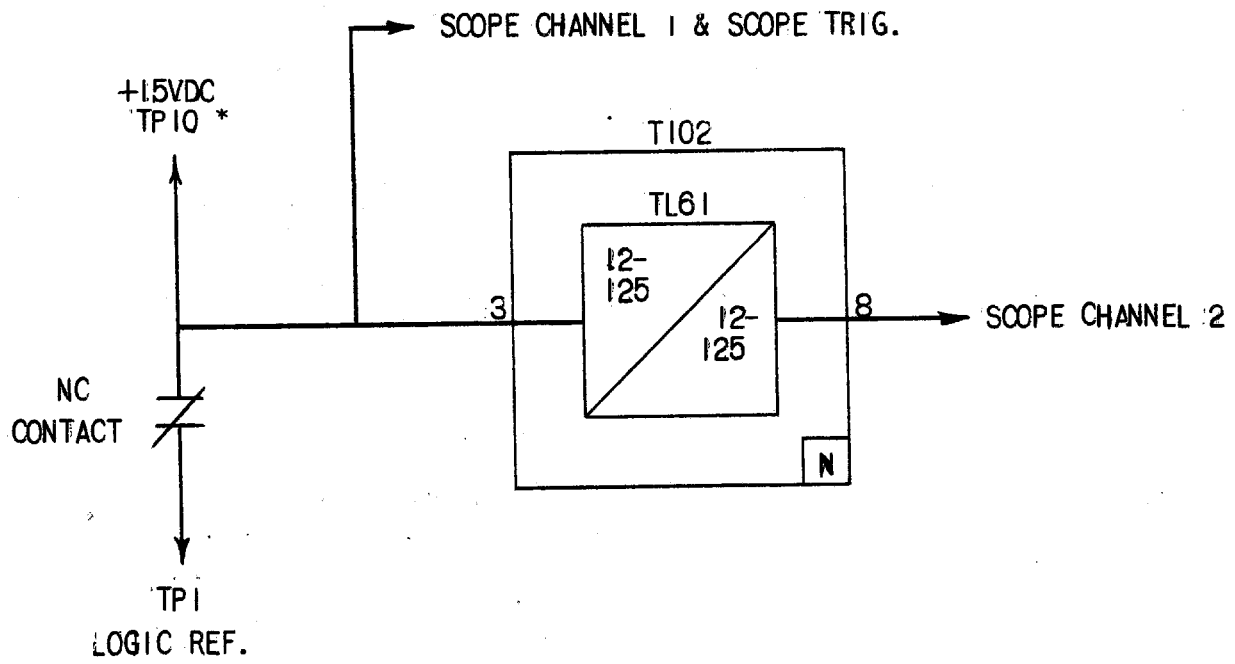


FIG. 5 (0227A2047-0) Logic and Internal Connection Diagram Legend



* THE 15VDC SIGNAL AT PIN 10 HAS A CURRENT LIMITING RESISTOR MOUNTED ON THE TEST CARD.

FIG. 6 (0246A7987-0) Logic Timer Test Circuit

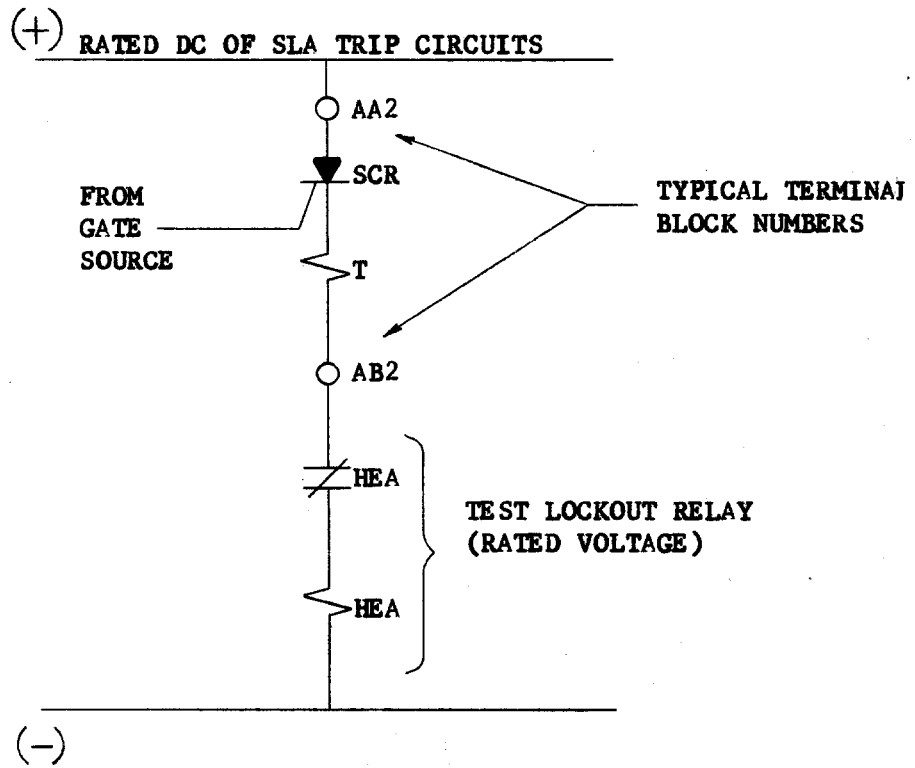


FIG. 7

TYPICAL SCR TEST CIRCUIT FOR TYPE SLA RELAYS

FIG. 7 (0208A2365-0) Typical SCR Trip Circuit Test Connections