INSTRUCTIONS

GEK-45493A

SUPERSEDES GEK-45493

AUXILIARY LOGIC AND TRIPPING UNIT

TYPE SLAT61B

POWER SYSTEMS MANAGEMENT DEPARTMENT

GENERAL ELECTRIC

PHILADELPHIA, PA.

CONTENTS

* Denotes change since superseded issue.

AUXILIARY LOGIC AND TRIPPING UNIT

TYPE SLAT61B

DESCRIPTION

* The SLAT61B relay is a static logic, output and tripping relay intended for application in phase comparison schemes operating via a frequency shift tone channel. In addition to the SLAT61B relay, the complete relay scheme would also include an SLD phase comparison measuring unit, a power supply and the appropriate frequency shift channel equipment.

The outputs of the SLAT61B relay include four SCR trip circuits, each with an electromechanical target; two electrically separate breaker failure timer initiating contacts (BFI); one reclose cancellation contact (RC); and two electrically separate channel status alarm contacts (TX). The inputs to the SLAT61B are from the associated SLD relay, from the channel equipment and from switch contacts which provide means for changing the channel status for test purposes, or for checking the tripping logic.

The relay is packaged in a four rack unit enclosed metal case suitable for mounting on a 19 inch rack. The outline and mounting dimensions are shown in Figure 1, the internal connections in Figure 2, and the card and component locations in Figure 3.

There are eight points in the logic which can be monitored from data monitoring points on the rear of the relay, as indicated in Figure 2. If these points are to be monitored, a separate data logging amplifier (DLA) is required.

There are two d-c voltage ratings available, one for 250 volts and the other for 48/125 volts.

APPLICATION

The SLAT61B relay is designed for application with the appropriate SLD phase comparison relay and frequency shift tone channel in a permissive phase comparison scheme.

* There are no measuring functions in the SLAT61B, but there are three timers which require adjustment in the field. These are the symmetry adjustment (TL42), the phase-delay timer (TL41) and back-up timer (TL48). Refer to the section on CALCULATION OF SETTINGS for a discussion of these required settings.

Note that the RC and TX units are reed relays the contacts of which are not suitable for use in trip circuits. Refer to the section on RATINGS for the contact duty capability of these units.

For a complete description of the overall scheme in which the relay is to be used, refer to the overall logic diagram and its associated logic description for the specific scheme.

RATINGS

The Type SLAT61B relay is designed for use in an environment where the air temperature outside the relay case does not exceed -20°C and +65°C.

The Type SLAT61B relay requires a ± 15 VDC power source which can be obtained from a Type SSA power supply.

The SCR tripping circuits are rated for 48/125 or 250 VDC. Each has a 1.0 ampere series target. The tripping circuits are designed to carry 30 amperes for one second.

The contacts of the telephone-type relay that is used for BFI will make and carry three amperes continuously and will interrupt up to 0.5 ampere (inductive) at 125 VDC or 0.25 ampere (inductive) at 250 VDC.

The contacts of the reed relays that are used for TX and RC are rated for 100 watts direct current. They will make and carry three amperes continuously.

Refer to the unit nameplate for the ratings of a particular relay.

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BURDENS

The SLAT61B relay presents a maximum burden to the Type SSA power supply of:

260 ma from the +15 VDC supply.

135 ma from the -15 VDC supply.

Each contact converter, when energized, will draw approximately 10 milliamperes from the station battery, regardless of tap setting.

FUNCTIONS

SCR TRIP CIRCUIT

* Four electrically separate, isolated SCR trip circuits are provided to trip four breakers. Each circuit is capable of carrying 30 amperes for one second.

The internal connections for the SCR trip and isolator subassemblies are shown in Figure 4. The isolator card, by means of a DC-to-DC converter, provides a signal path but maintains metallic isolation. This feature makes it possible to isolate the relay power supply from the trip circuit power supply.

TX CHANNEL STATUS ALARM CIRCUIT

The TX unit has two electrically separate normally open contacts which close within 1-2 milliseconds from the time the TX coil is energized by an output from the logic circuit. The contacts will open in about 15 milliseconds after the associated TL46 timer is de-energized. The TX function is provided by a reed relay, with contact capability listed in the section on RATINGS.

BFI BREAKER FAILURE INITIATE CIRCUIT

Two electrically separate normally open contacts are provided. These contacts close within 4 milliseconds from the time the associated coil is energized by the logic. These contacts open within 16 milliseconds from the time the coil is de-energized. The BFI function uses a telephone-type relay with contact ratings stated under RATINGS.

RC RECLOSE CANCELLATION

One normally open contact is provided. This contact closes within 1-2 milliseconds from the time the associated coil is energized by the logic. The contacts open within 1-2 milliseconds from the time the coil is de-energized. The RC function uses a reed relay with contact ratings stated under RATINGS.

CONTACT CONVERTERS

The purpose of this function is to convert a contact operation into a signal that is compatible with the logic circuit of the Type SLAT61B relay. The contact converters are labeled CC1, CC2 and CC3. These contact converters have a non-adjustable 4 millisecond pickup delay.

CC1

Contact converter CC1 permits an external contact to maintain the channel in the low-shift or permissive mode. The external contact is typically associated with a breaker failure back-up scheme.

CC2

Contact converter CC2 permits an external contact to block pilot tripping at the comparer (AND45).

CC3

Contact converter CC3 permits an external contact to shift the channel transmitter to the high-shift frequency.

CHANNEL INTERFACE

The logic of the Type SLAT61B relay includes an isolation interface (Figure 6) between the relays in the scheme and the associated channel. The circuitry of the isolation interface provides a signal path but maintains metallic isolation. This feature makes it possible to maintain isolation between the d-c supply used for the relays and that employed by the channel.

* Denotes change since superseded issue.

When pins 9 and 10 are both connected to relay reference, a metallically separate positive logic signal appears at pin 11 with respect to 12. The output from the isolation interface is a 5 VDC, 20 milliampere signal.

DATA MONITORING POINTS

Data monitoring points are brought out of a plug at the rear of the SLAT61B relay. The plug contains eight monitoring points and reference as shown on the overall logic diagram for the scheme. To monitor these points an additional piece of equipment termed a Data Logging Amplifier is required.

CALCULATIONS OF SETTINGS

The SLAT61B contains seven timers. Four of the timers are factory set and do not generally need field adjustment. The three timers that require field adjustment are the symmetry, phase-delay and back-up timers. The symmetry adjustment should be set before the phase-delay, however before either setting is made the communication equipment should be completely tested and have its final settings made.

SYMMETRY ADJUSTMENT

This 0-3/0-3 timer (TL42) is included to compensate for any asymmetry that may exist in the pickup and drop-out of the channel equipment. The purpose of this setting is to assure that the near end comparer receives equal on-and-off half cycles when the transmitter at the remote end is keyed for equal on-and-off half cycles. See the section titled SYMMETRY AND PHASE-DELAY TIMER ADJUSTMENTS for instructions for making this setting in the field.

PHASE-DELAY ADJUSTMENT

This 1-8/1-8 timer (TL41) is intended to delay the local input to the comparer by exactly the same amount of time that it takes for the remote signal to arrive. This time is equal to the channel delay in the communication equipment plus the propagation time of the signal. This setting should be made after the symmetry adjustment setting discussed above.

Because both of the above timer settings are affected by service conditions, the settings cannot be made at the factory. For instructions relating to the method of adjustment, see the SYMMETRY AND PHASE-DELAY TIMER ADJUSTMENTS section of this book.

BACK-UP TIMER

The back-up tripping timer (TL48) is identified as the 0.1-2 sec/0 timer and is located in printed circuit card position "AM". This timer is initiated by the output of the high-set level detector FDH in the associated SLD relay, and its output provides delayed tripping via the SCR trip circuits. Since this timer will operate for faults in either direction for faults of sufficient magnitude to operate FDH, it must be set to coordinate with relaying on other transmission lines terminating at the local bus and the bus at the remote end of the protected line.

The output of the back-up timer also energizes the RC unit. Contacts of this unit can be used to cancel reclosing following a delayed trip.

TARGETS

Four electromechanical target coils are included, one in series with each SCR. These targets operate on one ampere of trip current when the associated SCR passes current. The trip circuit resistance in the relay is 0.40 ohm.

LOGIC CIRCUITS

The functions of the Type SLAT61B involves basic logic (AND, OR, AND NOT) where the presence or absence of signals, rather than their magnitude, controls the operation. Signals are measured with respect to a reference bus accessible at TP1. In general a signal below one VDC represents an OFF or LOGIC ZERO condition, an ON or LOGIC ONE is represented by a signal of approximately +15 VDC.

The symbols used on the internal connection diagram (Figure 2) are explained by the legend shown in Figure 5.

CONSTRUCTION

The SLAT61B relay is packaged in an enclosed metal case with hinged front cover and removable top cover. The outline and mounting dimensions of the case and the physical location of the components are shown in Figures 1 and 3 respectively.

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The SLAT61B relay contains printed circuit cards identified by a code number such as: A104, T116, L106 where A designated an auxiliary function, T designated a time-delay function, and L designated a logical function. The printed circuit cards plug in from the front of the unit. The sockets are marked with letter designations or "addresses" (D, E, F, etc.) which appear on the guide strips in front of each socket, on the component location drawing, on the unit internal connection diagram, and on the printed circuit card. The test points (TP1, TP2, etc.) shown on the internal connection diagram are connected to instrument jacks on a test card in position T with TP1 at the top of the T card. TP1 is tied to reference; TP10 is tied to +15 VDC through a 1.5K resistor. This resistor limits the current when TP10 is used to supply a logic signal to a card.

The SLAT61B relay receives its inputs from the associated Type SLD relay. These units are interconnected by ten-conductor-shielded cables. The sockets for these cables are located on the rear panel of the unit. The SLAT61B output functions are connected to 12 point terminal strips, which are also located on the rear of the unit.

A window is provided in the hinged cover of the relay to allow the mechanical targets to be seen. Push buttons are also provided to reset the targets without opening the cover.

RECEIVING, HANDLING AND STORAGE

These relays will normally be supplied as a part of a static relay equipment, mounted in a rack or cabinet with other static relays and test equipment. Immediately upon receipt of a static relay equipment, it should be unpacked and examined for any damage sustained in transit. If injury or damage resulting from rough handling is evident, file a damage claim at once with the transportation company and promptly notify the nearest General Electric Sales Office.

Reasonable care should be exercised in unpacking the equipment. If the equipment is not to be installed immediately, it should be stored indoors in a location that is free from moisture, dust, metallic chips, and severe atmospheric contaminants.

Just prior to final installation the shipping support bolt should be removed from each side of all relay units, to facilitate possible future unit removal for maintenance. These shipping support bolts are approximately eight inches back from the relay front panel. Static relay equipment, when supplied in swing rack cabinets, should be securely anchored to the floor or to the shipping pallet to prevent the equipment from tripping over when the swing rack is opened.

TEST INSTRUCTIONS

CAUTION

IF THE SLAT61B RELAY THAT IS TO BE TESTED IS INSTALLED IN AN EQUIPMENT WHICH HAS ALREADY BEEN CONNECTED TO THE POWER SYSTEM, DISCONNECT THE OUTPUTS TO THE SYSTEM.

A. GENERAL

The SLAT61B relay is supplied from the factory either mounted in a static relay equipment or as a separate unit associated with measuring relays, a Type SSA power supply, and some form of channel equipment. All relay units for a given terminal of static relaying equipment are tested together at the factory, and each will have the same summary number stamped on its nameplate.

In general, when a time range is indicated on the internal connections diagram, the timer has been factory set at a mid-range value. Timers should be set for the operating or reset times indicated on the associated overall logic diagram. Where a time range is indicated on the overall logic diagram, the timer should be set for the value recommended for that function in the descriptive write-up accompanying the overall logic diagram. Where a setting depends upon conditions encountered on a specific application, this is so stated and the factors influencing the choice of setting are described. The procedure for checking and setting the timers is described in a later section.

B. OPERATIONAL CHECKS

Operation of the SLAT61B unit can be checked by observing the signals at the ten test points (TP1 to TP10) in the SLAT61B by observing the operation of the associated channel equipment, or by observing the output functions. The test points are located on a test card in position T, and are numbered 1 to 10 from top to bottom. TP1 is the reference bus for the logic circuit, TP10 is at +15 VDC. The remaining points are located at various strategic points throughout the logic as shown in the internal connection diagram (Figure 2). Test point voltages can be monitored with a portable high impedance voltmeter, the voltmeter on the test panel of the associated equipment, or an oscilloscope.

C. TEST CARD ADAPTER

The test card adapter provides a convenient means of gaining access to any pin of a particular card. Detailed information on the use of the test adapter card is included in the card instruction book GEK-34158.

D. TIMER ADJUSTMENTS AND TESTS

When the time-delay cards are to be adjusted or checked, an oscilloscope that can display two traces simultaneously and that has a calibrated horizontal sweep should be used.

In order to test the timer cards it is necessary to remove the card previous to the timer (see Table I) and to place the timer card in a card adapter. The card adapter allows access to the input and output of the timer if they are not brought out on test points. The timer test circuit is shown in Figure 7. Opening the normally closed contact causes the output to step up to +15 VDC after the pickup delay of the timer. To increase the pickup time, turn the upper potentiometer on the timer card clockwise; to decrease the time turn it counterclockwise. Closing the contact causes the timer output to drop out after the reset time-delay setting of the card. If the timer card is provided with a variable reset delay, it can be adjusted by the lower potentiometer on the timer card (clockwise increases reset time).

TABLE I

TIME UNDER TEST	POSITION	REMOVE CARD IN POSITION
TL41	J	AK
TL42	H	G
TL43	N	AL
TL44	M	NONE*
TL45	L	K
TL46	S	G
TL48	AM	AL

*Turn power supply switch on and off.

E. TRIP CIRCUIT TESTS

The SCR trip circuits and the series mechanical targets may be checked by connecting an auxiliary lock-out relay, such as the Type HEA relay, in series with the SCR circuit. A typical circuit is shown in Figure 8. The HEA relay should have the same d-c rating as the SCR trip circuit of the SLAT61. If an auxiliary lock-out relay is not available, it can be replaced by a resistive load which limits the trip circuit current to three amperes. In most equipments, the SCR can be gated by operating a test push button in the associated units.

Prior to final installation, a check of the overall trip circuit should be made with the SCR outputs connected to trip the circuit breakers.

F. OVERALL EQUIPMENT TESTS

After the SLAT61B relay and the associated static relay units have been individually calibrated and tested for the desired settings and ranges, a series of overall operating circuit checks is advisable. The elementary, overall logic and logic description for the specific job will be useful for determining the overall operation of the scheme.

Overall equipment tests can be performed by applying alternating current and voltages to the measuring units as specified in the instruction book for the measuring units and checking that proper outputs are obtained when the measuring units operate.

G. SYMMETRY AND PHASE-DELAY TIMER ADJUSTMENTS

The symmetry timer (TL42, "H" position) and phase-delay timer (TL41, "J" position) final settings must be made in the field after the transmitters, receivers and coupling equipment have been tuned and adjusted for proper sensitivity per the channel instructions. Operation of the squaring amplifier and fault detectors, FDL and FDH, are required for accomplishment of the final symmetry and phase-delay adjustments; refer to the measuring unit instruction book for the recommended procedure.

The symmetry adjustment must be accomplished prior to phase-delay adjustments as described in the measuring unit instructions. The transient blocking timer (TL43, "N" position) should be removed to prevent continuous channel keying when the logic trip bus is energized. Clockwise adjustment of P1 and P2 on TL42, "H" position card, increases the pickup delay or drop-out delay respectively. Conversely, counterclockwise adjustment reduces the respective operate times. The minimum delay on pickup which allows equal half cycle block and trip output as measured at TP8 is the recommended final setting.

After the symmetry adjustment has been accomplished, the phase-delay adjustment is made to obtain the proper alignment of the local signal with the received signal; refer to the measuring unit instructions. Clockwise adjustment of P1 or P2 on TL41, "J" position card, increases the pickup or drop-out delay respectively. The final setting is the alignment of the trip attempt signal monitored at TP4 compared to the trip or block signal monitored at TP8 which is dependent upon internal or external fault simulation during the adjustment.

* H. BACK-UP TIMER ADJUSTMENTS

The back-up tripping timer (TL48) in position AM is initiated by the output of the high-set level detector FDH in the associated SLD relay, and provides delayed tripping via the SCR trip circuits. Since this timer will be energized for faults in either direction of sufficient magnitude to operate FDH, at the time of installation it must be set to coordinate with the relaying on other transmission lines terminating at the local bus and the bus at the remote end of the protected line.

This timer should be adjusted following the procedures noted in Section D above, using Table I and Figure 7.

MAINTENANCE

A. PERIODIC TESTS

It should be sufficient to check the outputs produced at test points in the SLAT61B when periodic calibration tests are made on the associated measuring units, for example, the phase and ground relays in line relaying scheme. No separate periodic tests on the SLAT61B itself should be required.

B. TROUBLESHOOTING

In any troubleshooting of equipment, it should first be established which unit is functioning incorrectly. The overall logic diagram supplies with the equipment shows the combined logic of the complete equipment and the various test points in each unit. By signal tracing, using the overall logic diagram and the various test points, it should be possible to quickly isolate the trouble.

A test adapter card is supplied with each static relay equipment to supplement the prewired test points on the test cards. Use of the adapter card is described in the card instruction book GEK-34158.

A dual-trace oscilloscope is a valuable aid to detailed troubleshooting, since it can be used to determine phase shift, operate and reset times as well as input and output levels. A portable dual-trace oscilloscope with a calibrated sweep and trigger facility is recommended.

C. SPARE PARTS

To minimize possible outage time, it is recommended that a complete maintenance program should include the stocking of at least one spare card of each type. It is possible to replace damaged or defective components on the printed circuit cards, but great care should be taken in soldering so as not to damage or bridge-over the printed circuit busses, or overheat the semi-conductor components. The repaired area should be recovered with a suitable high-dielectric plastic coating to prevent possible breakdowns across the printed busses due to moisture and dust. The wiring diagrams for the cards in the SLAT61B relay are included in the card book GEK-34158.

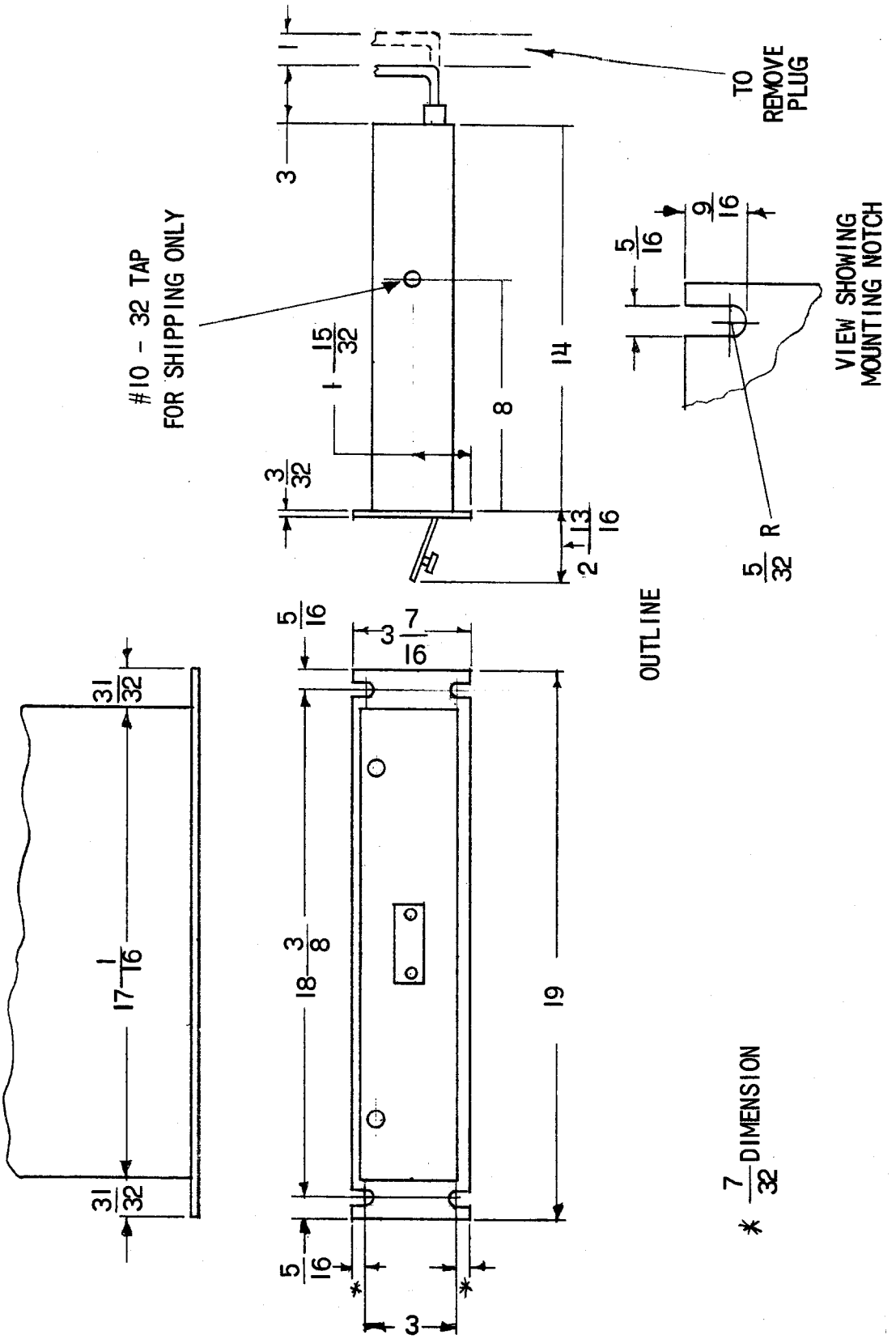
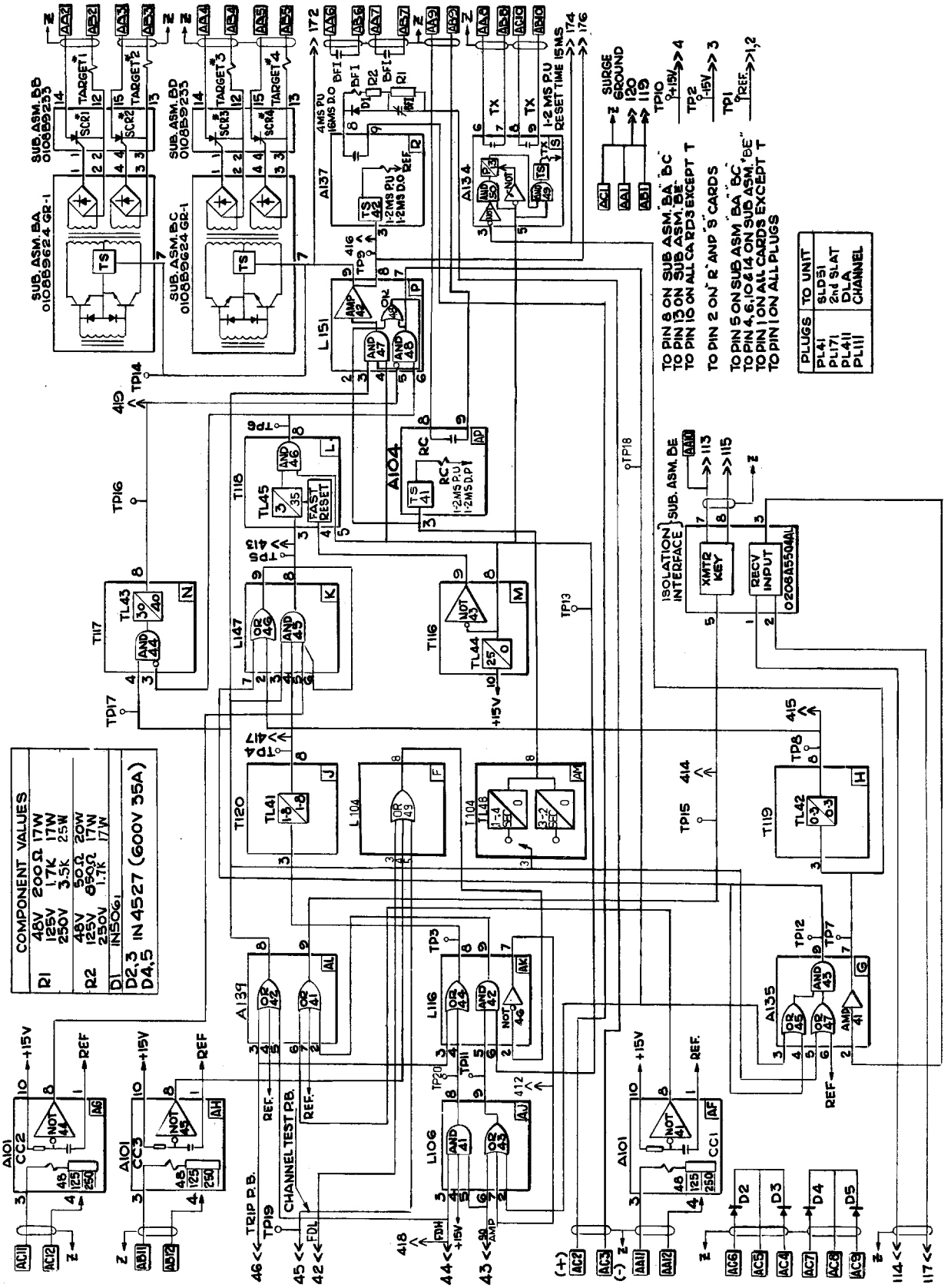
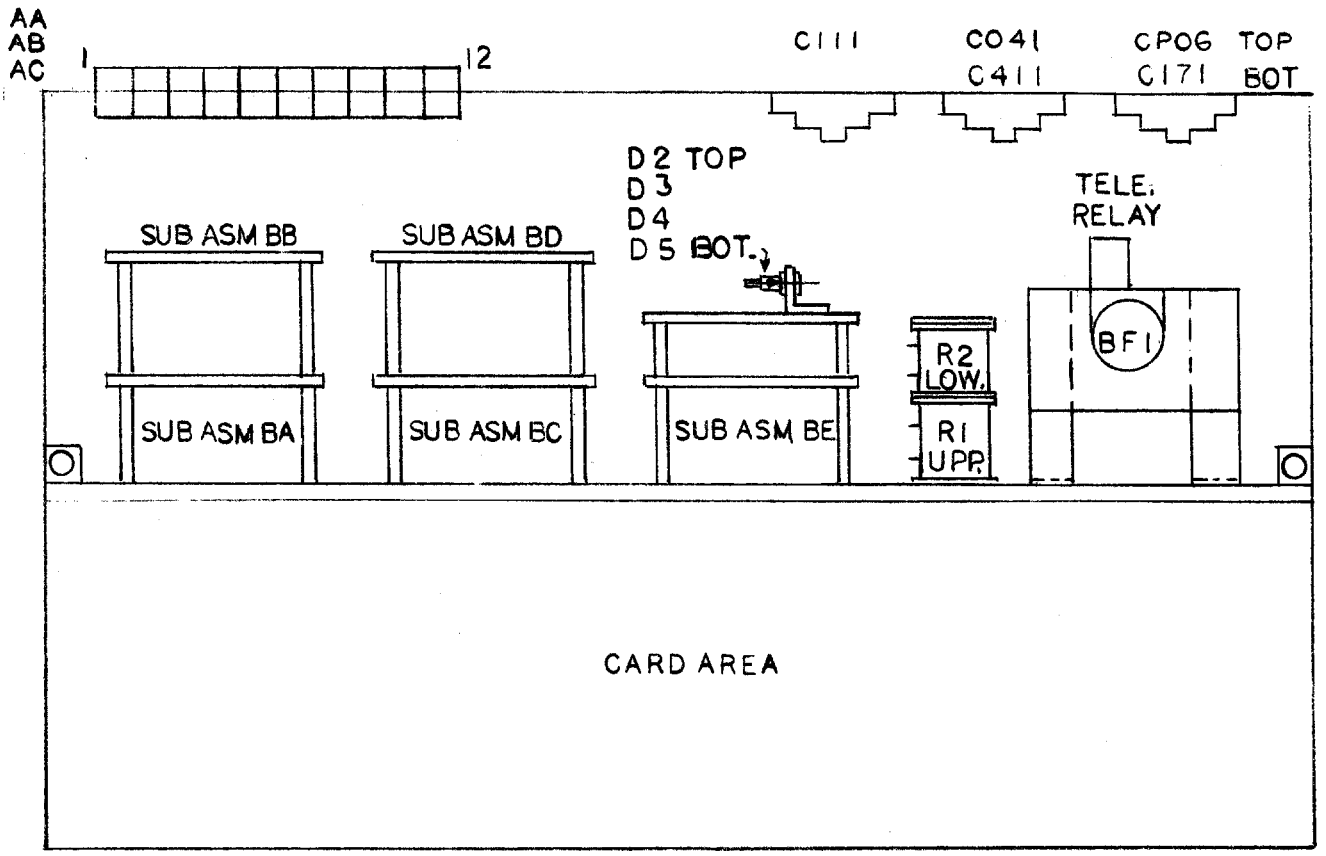


Fig. 1 (0227A2036-0) Outline and Mounting Dimensions for the Type SLT61B Relay



* Fig. 2 (0171C7875-3) Internal Connections for Type SLAT61B Relay

* Denotes change since superseded issue.



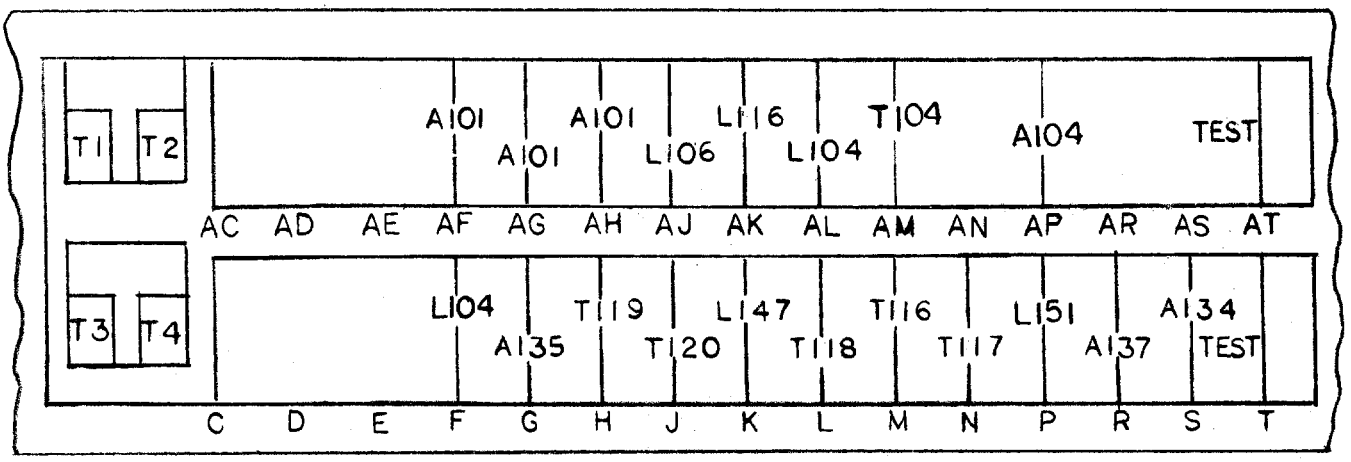


Fig. 3 (0257A8772-2) Component Locations for the Type SLAT61B Relay

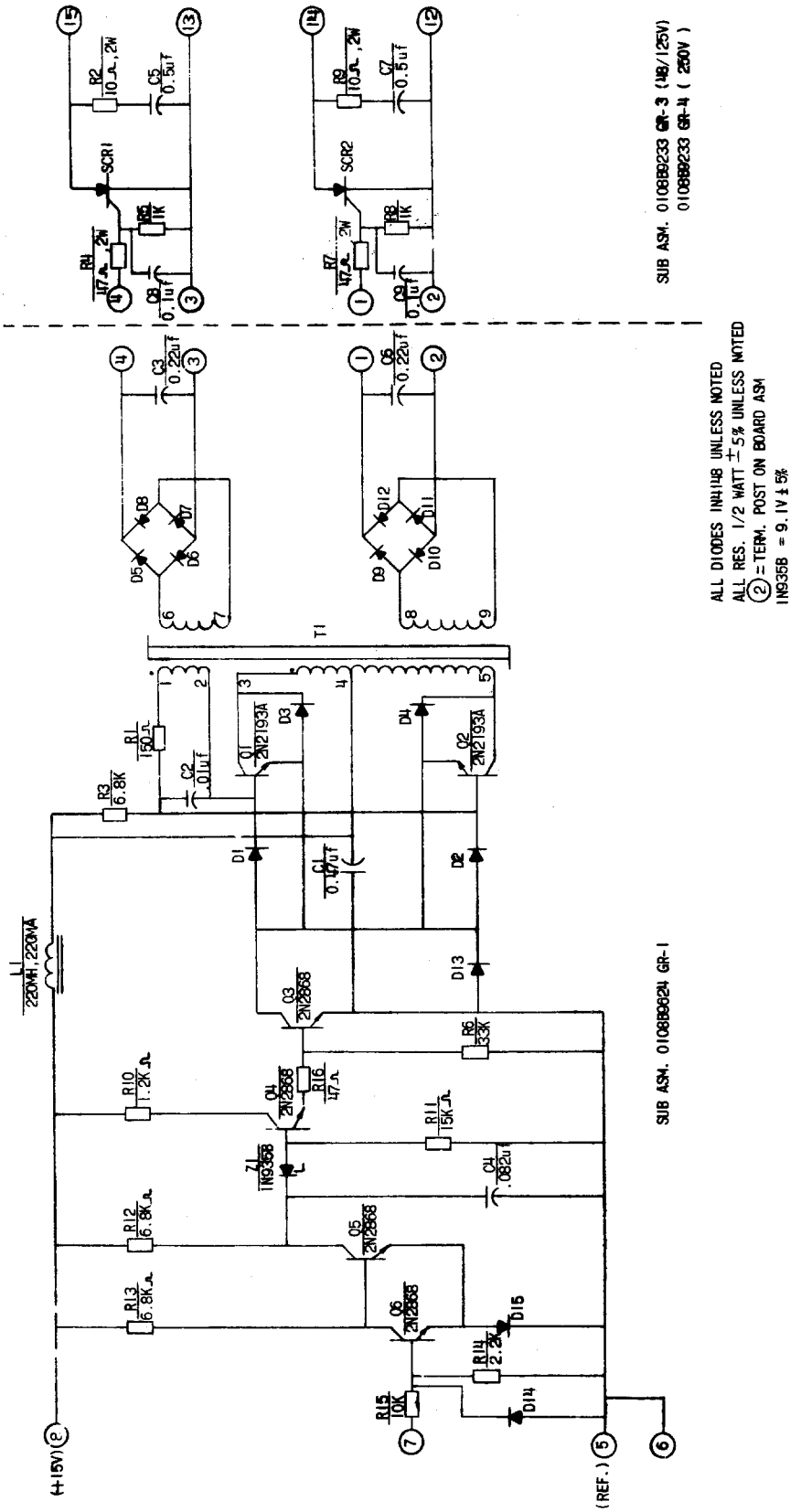


Fig. 4 (0108B9610-0) Internal Connections for the SCR Trip and Isolation Subassemblies

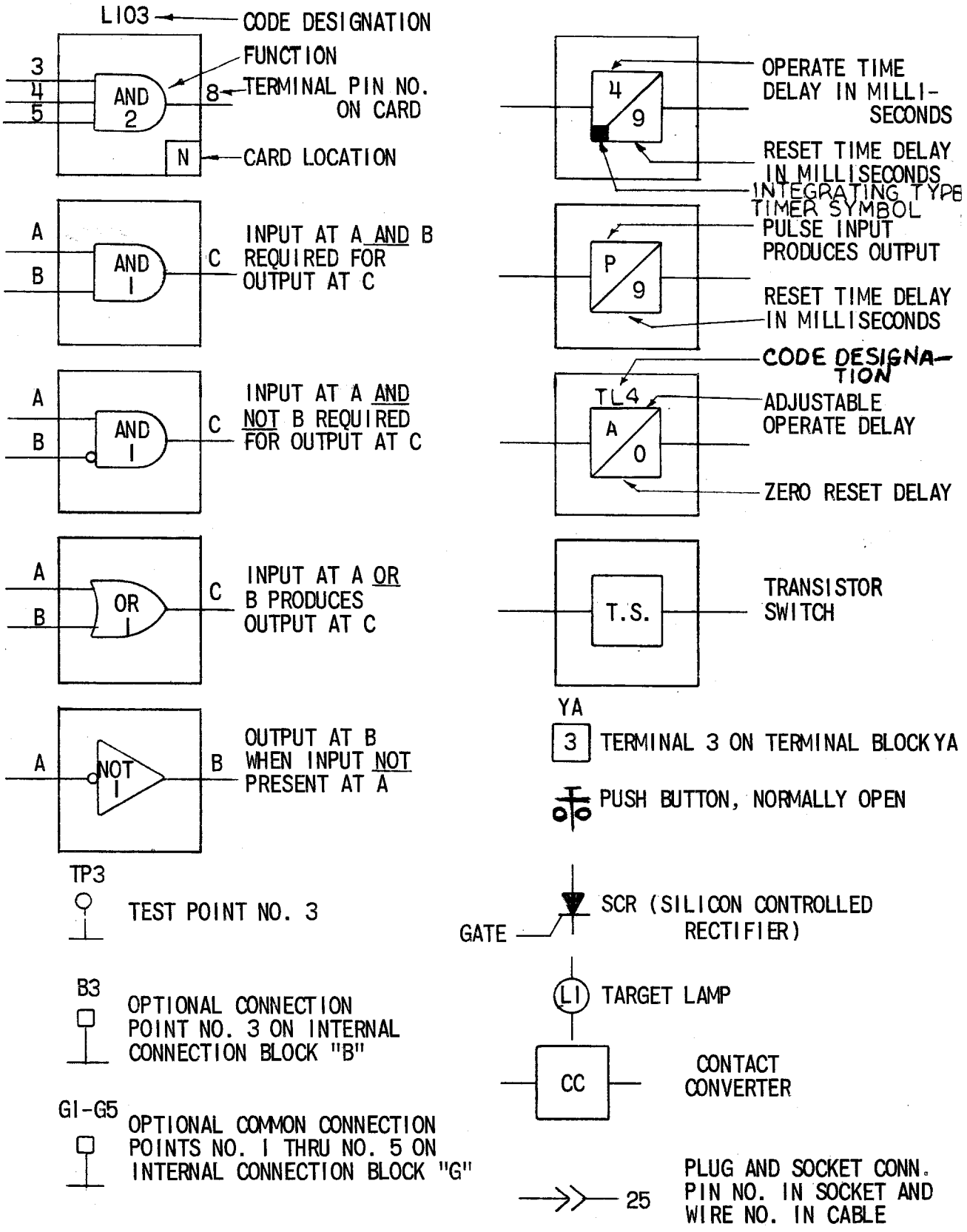
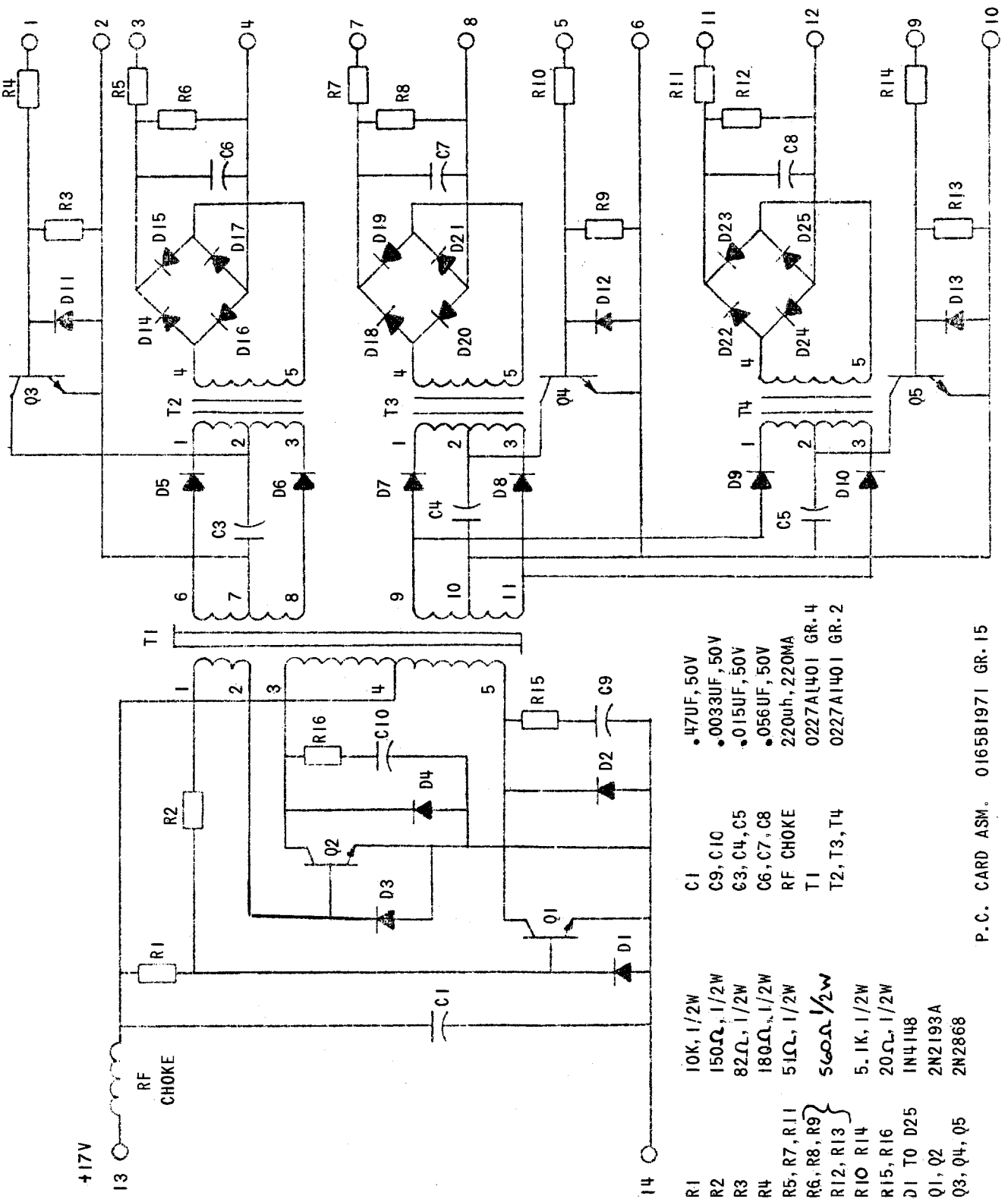
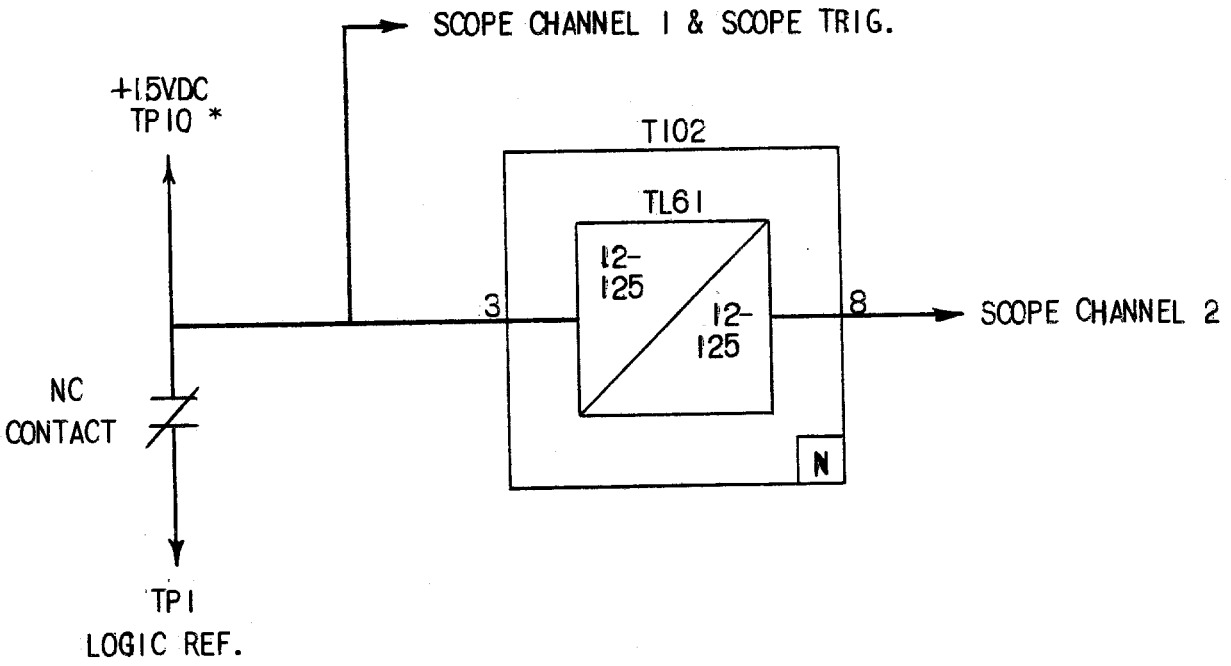


Fig. 5 (0227A2047-1) Logic and Internal Connection Diagram Legend



* Fig. 6 (0208A5504AL-1) Isolation interface Circuit

* Denotes change since superseded issue.



* THE 15VDC SIGNAL AT PIN 10 HAS A CURRENT LIMITING RESISTOR MOUNTED ON THE TEST CARD.

Fig. 7 (0246A7987-0) Logic Timer Test Circuit

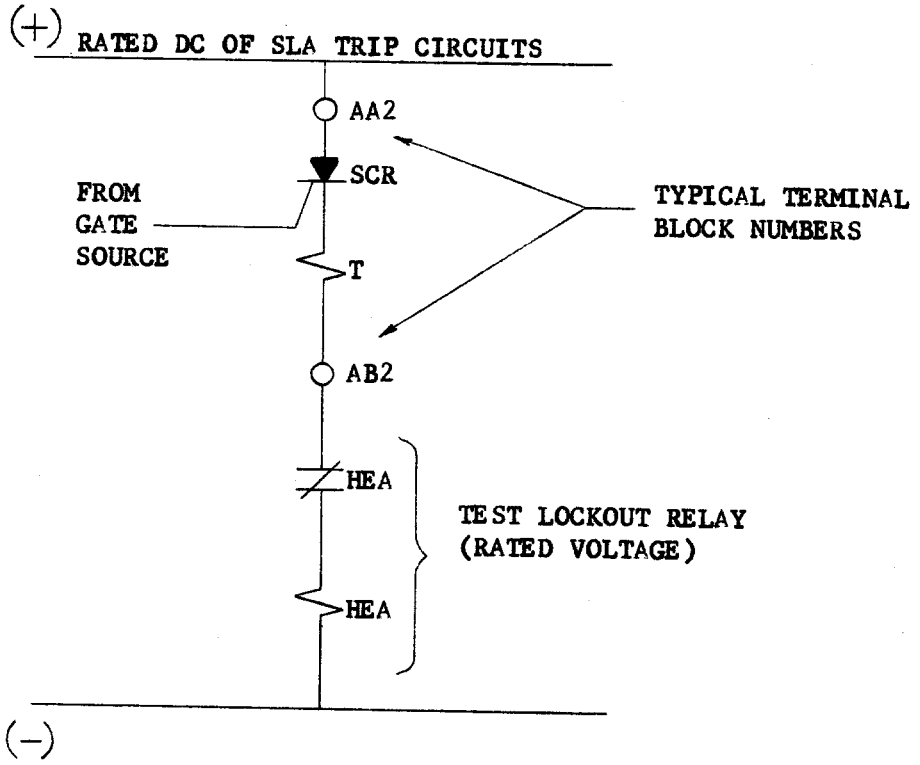


Fig. 8 (0208A2365-0) Typical SCR Trip Circuit Test Connections