INSTRUCTIONS

GEK-49776

AUXILIARY LOGIC AND TRIPPING UNIT

TYPE SLAT51H

POWER SYSTEMS MANAGEMENT DEPARTMENT

GENERAL ELECTRIC

PHILADELPHIA, PA.

CONTENTS

AUXILIARY LOGIC AND TRIPPING UNIT

TYPE SLAT51H

DESCRIPTION

The SLAT51H relay is a static logic, output and tripping unit for use in phase comparison schemes with two zone phase distance back-up. In addition to the SLAT51H relay, the appropriate SLD, SLY, SLA logic unit, power supply and frequency shift channel equipment are required to complete a particular relaying scheme.

The outputs of the SLAT51H include one trip output with four electrically separate output contacts (TR) and four electromechanical targets; two electrically separate reclose initiating contacts (RI); two electrically separate breaker failure timer initiating contacts; and four electrically separate channel status contacts (TX). The inputs to the SLAT51H are logic signals from the associated logic unit.

The SLAT51H relay is packaged in a two rack unit enclosed metal case suitable for mounting on a 19 inch rack. The outline and mounting dimensions are shown in Figure 1. The internal connections for the SLAT51H relay are shown in Figure 2. The component and card locations are shown in Figure 3.

APPLICATION

The SLAT51H relay is designed to operate in conjunction with appropriate phase comparison measuring units, SLA logic unit, SLY phase distance units, and a frequency shift channel equipment. The following is a listing of the various output functions included in the SLAT51H together with a general description of their intended uses.

TR - Four trip circuit contacts are provided to permit tripping of associated circuit breakers.

RI - The reclose initiation outputs are provided to initiate automatic reclosing after a high speed trip.

BFI - The breaker failure initiation outputs are provided to initiate breaker failure protection.

TX - The channel status contacts are provided to monitor the output of the receiver in the associated frequency shift channel equipment.

In addition to the above output functions, five target lamps are provided. An adjustable timer, TL-31 is provided which may be used to restrict target lamp indication to the function(s) that first operated. See the section under CALCULATION OF SETTINGS for further details and instructions for setting this timer.

For the complete description of the overall scheme in which the relay is employed, refer to the overall logic diagram and its associated logic description that is supplied with each terminal equipment.

RATINGS

The Type SLAT51H relay is designed for use in an environment where the air temperature outside the relay base does not exceed -20°C and +65°C.

The Type SLAT51H relay requires a ±15 VDC power source which can be obtained rrom a Type SSA power supply.

The contacts of the telephone-type relays that are used for the tripping circuits will carry three amperes; they have a maximum intermittent rating of 30 amperes and they will interrupt 60 volt amperes (inductive). These tripping circuits are rated for 48 or 125 VDC. Each circuit has a 1.0 ampere series target.

The contacts of the telephone-type relays that are used for RI and TX will make and carry three amperes continuously and will interrupt up to 0.5 amperes (inductive) at 125 VDC or at 0.25 ampere (inductive) at 250 VDC.

The contacts of the reed relays that are used for BFI are rated for 100 watts direct current. They will make and carry three amperes continuously.

Refer to the unit nameplate for the ratings of a particular relay.

BURDENS

The SLAT51H relay presents a maximum burden to the Type SSA power supply of:

255 ma from +15 VDC supply
210 ma from -15 VDC supply

In addition, each target lamp draws 80 milliamperes from the -15 VDC supply.

FUNCTIONS

TR TRIP CIRCUIT

Four electrically separate normally open contacts are provided to trip four breakers. The contacts close within four milliseconds from the time the associated coil is energized by the logic. The TR function uses a telephone-type relay with contact ratings stated under RATINGS.

TX CHANNEL STATUS CIRCUIT

A normally open and a "C" transfer contact are provided on the TX relay. These contacts close within 17 milliseconds from the time the associated coil is energized by the logic. The contacts open within 170 milliseconds from the time the coil is deenergized. The TX function uses a telephone-type relay with contact ratings stated under RATINGS.

RI RECLOSE INITIATE CIRCUIT

Two electrically separate normally open contacts are provided. These contacts close within 17 milliseconds from the time the associated coil is energized by the logic. The contacts open within 170 milliseconds from the time the coil is deenergized. The RI function uses a telephone-type relay with contact ratings stated under RATINGS.

BFI BREAKER FAILURE INITIATE CIRCUIT

Two electrically separate normally open contacts are provided. These contacts close within 2 milliseconds from the time the associated coil is energized by the logic. These contacts open within 2 milliseconds from the time the coil is deenergized. The BFI function uses a reed relay with contact ratings stated under RATINGS.

CALCULATIONS OF SETTINGS

The SLAT51H contains one timer that requires field adjustment.

The 5-30/0 timer TL31 enables the user to control the number of lamps that will light under certain fault conditions. With a short pickup setting (5-10 milliseconds) only lamp(s) associated with those units which first sensed the fault will light. Increased pickup settings will cause the lamps associated with all units that operate to light. The timer setting should not exceed the minimum breaker clearing time in order to avoid targets which may result from breaker unequal pole opening times.

TARGETS

Four electromechanical target coils are included, one in series with each TR contact. These targets operate on one ampere of trip current when the associated circuit passes current. The trip circuit resistance in the relay is 0.40 ohm.

LOGIC CIRCUITS

The functions of the Type SLAT51H involves basic logic (AND, OR, AND NOT) where the presence or absence of signals, rather than their magnitude, controls the operation. Signals are measured with respect to a reference bus accessible at TP1. In general a signal below one VDC represents an OFF or LOGIC ZERO condition, an ON or LOGIC ONE is represented by a signal of approximately +15 VDC.

The symbols used on the internal connection diagram (Fig. 2) are explained by the legend shown in Figure 4.

CONSTRUCTION

The SLAT51H relay is packaged in an enclosed metal case with hinged front cover and removable top cover. The outline and mounting dimensions of the case and the physical location of the components are shown in Figures 1 and 3 respectively.

The SLAT51H relay contains printed circuit cards identified by a code number such as: A104, T106, L109 where A designated an auxiliary function, T designated a time-delay function, and L designated a logical function. The printed circuit cards plug in from the front of the unit. The sockets are marked with letter designations or "addresses" (D, E, F, etc.) which appear on the guide strips in front of each socket, on the component location drawing, on the unit internal connection diagram, and on the printed circuit card. The test points (TP1, TP2, etc.) shown on the internal connection diagram are connected to instrument jacks on a test card in position T with TP1 at the top of the T card. TP1 is tied to reference; TP10 is tied to +15 VDC through a 1.5K resistor. This resistor limits the current when TP10 is used to supply a logic signal to a card.

The SLAT51H relay receives its inputs from the associated Type SLA relay. These units are interconnected by ten conductor shielded cables. The sockets for these cables are located on the rear panel of the unit. The SLAT51H output functions are connected to 12-point terminal strips, which are also located on the rear of the unit.

A window is provided in the hinged cover of the relay to allow the mechanical targets to be seen. Push buttons are also provided to reset the targets without opening the cover.

RECEIVING, HANDLING AND STORAGE

These relays will normally be supplied as a part of a static relay equipment, mounted in a rack or cabinet with other static relays and test equipment. Immediately upon receipt of a static relay equipment, it should be unpacked and examined for any damage sustained in transit. If injury or damage resulting from rough handling is evident, file a damage claim at once with the transportation company and promptly notify the nearest General Electric Sales Office.

Reasonable care should be exercised in unpacking the equipment. If the equipment is not to be installed immediately, it should be stored indoors in a location that is free from moisture, dust, metallic chips, and severe atmospheric contaminants.

Just prior to final installation the shipping support bolt should be removed from each side of all relay units, to facilitate possible future unit removal for maintenance. These shipping support bolts are approximately eight inches back from the relay front panel. Static relay equipment, when supplied in swing rack cabinets, should be securely anchored to the floor or to the shipping pallet to prevent the equipment from tipping over when the swing rack is opened.

TEST INSTRUCTIONS

CAUTION

IF THE SLAT51H RELAY THAT IS TO BE TESTED IS INSTALLED IN AN EQUIPMENT WHICH HAS ALREADY BEEN CONNECTED TO THE POWER SYSTEM, DISCONNECT THE OUTPUTS TO THE SYSTEM.

A. GENERAL

The SLAT51H relay is supplied from the factory either mounted in a static relay equipment or as a separate unit associated with measuring relays, a Type SSA power supply, and some form of channel equipment. All relay units for a given terminal of static relaying equipment are tested together at the factory, and each will have the same summary number stamped on its nameplate.

In general, when a time range is indicated on the internal connections diagram, the timer has been factory set at a mid-range value. Timers should be set for the operating or reset times indicated on the associated overall logic diagram. Where a time range is indicated on the overall logic diagram, the timer should be set for the value recommended for that function in the descriptive write-up accompanying the overall logic diagram. Where a setting depends upon conditions encountered on a specific application, this is so stated and the factors influencing the choice of setting are described. The procedure for checking and setting the timers is described in a later section.

B. OPERATIONAL CHECKS

Operation of the SLAT51H unit can be checked by observing the signals at the ten test points (TP1 to TP10) in the SLAT51H by observing the operation of the associated channel equipment, or by observing the output functions. The test points are located on a test card in position T, and are numbered 1 to 10 from top to bottom. TP1 is the reference bus for the logic circuit, TP10 is at +15 VDC. The remaining points are located at various strategic points throughout the logic as shown in the internal connection diagram (Figure 2). Test point voltages can be monitored with a portable high impedance voltmeter, the voltmeter on the test panel of the associated equipment, or an oscilloscope.

C. TEST CARD ADAPTER

The test card adapter provides a convenient means of gaining access to any pin of a particular card. Detailed information on the use of the test adapter card is included in the card instruction book GEK-34158.

D. TIMER ADJUSTMENTS AND TESTS

When the time-delay cards are to be adjusted or checked, an oscilloscope that can display two traces simultaneously and that has a calibrated horizontal sweep should be used.

In order to test the timer cards it is necessary to remove the card previous to the timer (see Table I) and to place the timer card in a card adapter. The card adapter allows access to the input and output of the timer if they are not brought out on test points. The timer test circuit is shown in Figure 5. Opening the normally closed contact causes the output to step up to +15 VDC after the pickup delay of the timer. To increase the pickup time, turn the upper potentiometer on the timer card clockwise; to decrease the time turn it counterclockwise. Closing the contact causes the timer output to drop out after the reset time-delay setting of the card. If the timer card is provided with a variable reset delay, it can be adjusted by the lower potentiometer on the timer card (clockwise increases reset time).

TABLE I

TIME UNDER TEST	POSITION	REMOVE CARD IN POSITION
TL32	K	F
TL31	E	NONE*

*Turn power supply switch on and off.

E. TRIP CIRCUIT TESTS

The TR trip circuits and the series mechanical targets may be checked by connecting an auxiliary lock-out relay, such as the Type HEA relay, in series with the TR circuit. A typical circuit is shown in Figure 6. The HEA relay should have the same d-c rating as the trip circuit of the SLAT51H. If an auxiliary lock-out relay is not available, it can be replaced by a resistive load which limits the trip circuit current to three amperes In most equipments, the TR circuits can be activated by operating a test push button in associated units.

Prior to final installation, a check of the overall trip circuit should be made with the TR outputs connected to trip the circuit breakers.

F. OVERALL EQUIPMENT TESTS

After the SLAT51H relay and the associated static relay units have been individually calibrated and tested for the desired settings and ranges, a series of overall operating circuit checks is advisable. The elementary, overall logic and logic description for the specific job will be useful for determining the overall operation of the scheme.

Overall equipment tests can be performed by applying alternating current and voltages to the measuring units as specified in the instruction book for the measuring units and checking that proper outputs are obtained when the measuring units operate.

MAINTENANCE

A. PERIODIC TESTS

It should be sufficient to check the outputs produced at test points in the SLAT51H when periodic calibration tests are made on the associated measuring units, for example, the phase and ground relays in line relaying scheme. No separate periodic tests on the SLAT51H itself should be required.

B. TROUBLESHOOTING

In any troubleshooting of equipment, it should first be established which unit is functioning incorrectly. The overall logic diagram supplied with the equipment shows the combined logic of the complete equipment and the various test points in each unit. By signal tracing, using the overall logic diagram and the various test points, it should be possible to quickly isolate the trouble.

A test adapter card is supplied with each static relay equipment to supplement the prewired test points on the test cards. Use of the adapter card is described in the card instruction book GEK-34258.

A dual trace oscilloscope is a valuable aid to detailed troubleshooting, since it can be used to determine phase shift, operate and reset times as well as input and output levels. A portable dual-trace oscilloscope with a calibrated sweep and trigger facility is recommended.

C. SPARE PARTS

To minimize possible outage time, it is recommended that a complete maintenance program should include the stocking of at least one spare card of each type. It is possible to replace damaged or defective components on the printed circuit cards, but great care should be taken in soldering so as not to damage or bridge-over the printed circuit busses, or overheat the semiconductor components. The repaired area should be recovered with a suitable high-dielectric plastic coating to prevent possible breakdowns across the printed busses due to moisture and dust. The wiring diagrams for the cards in the SLAT51H relay are included in the card book GEK-34158.

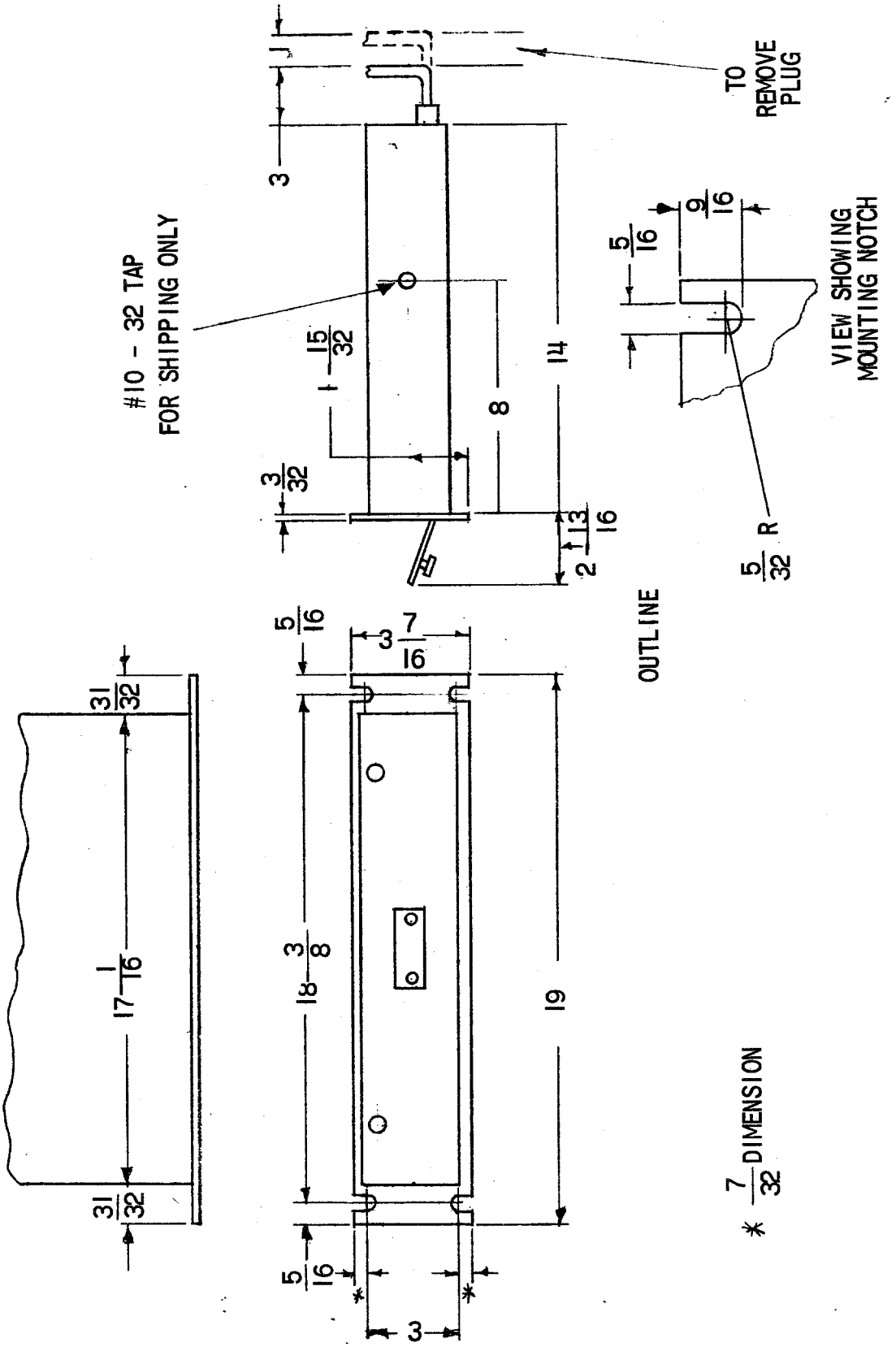


Fig. 1 (0227A2036-0) OUTLINE AND MOUNTING DIMENSIONS FOR THE TYPE SLAT51H RELAY

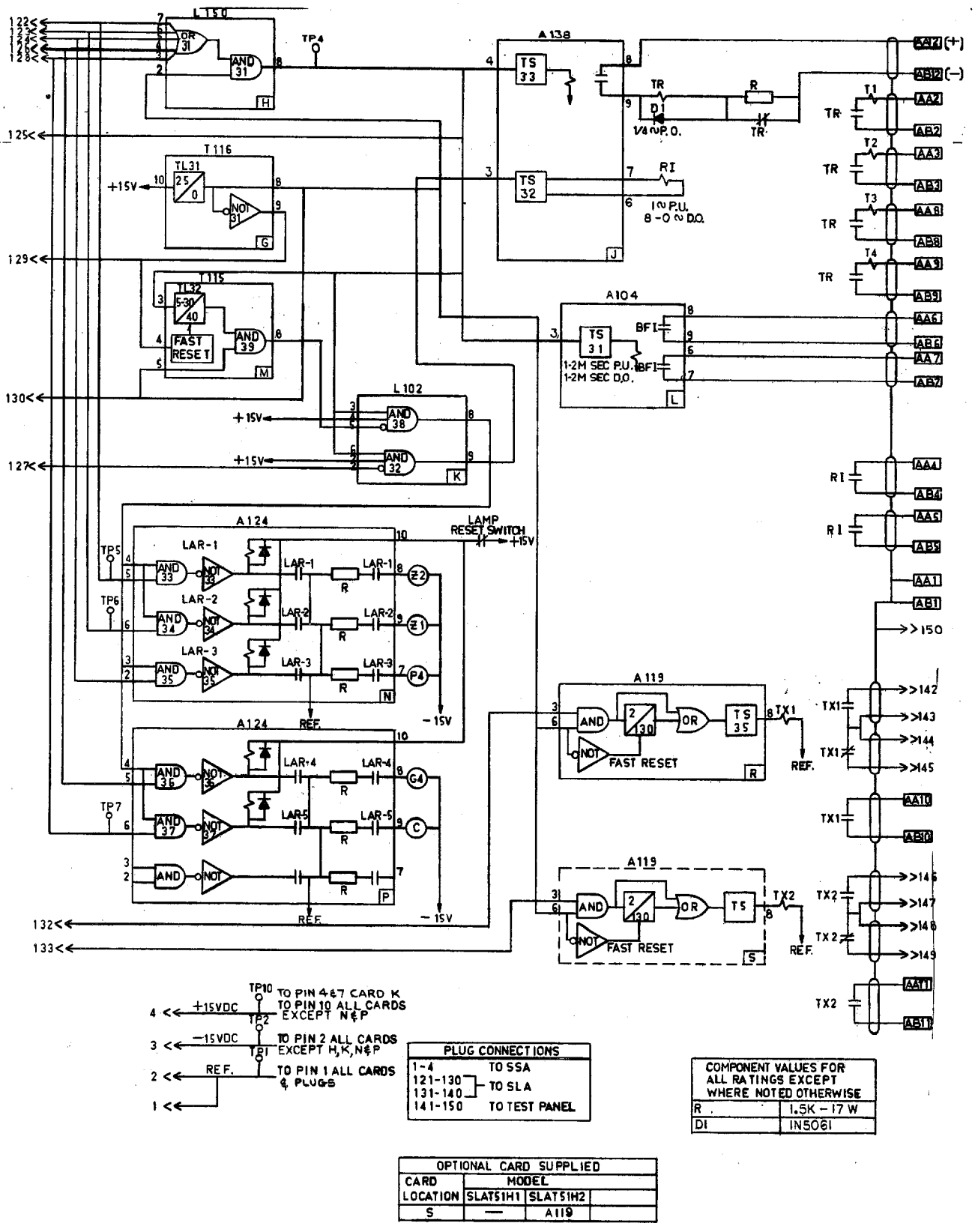


Fig. 2 (0171C7876-0) INTERNAL CONNECTIONS FOR THE TYPE SLAT51H RELAY

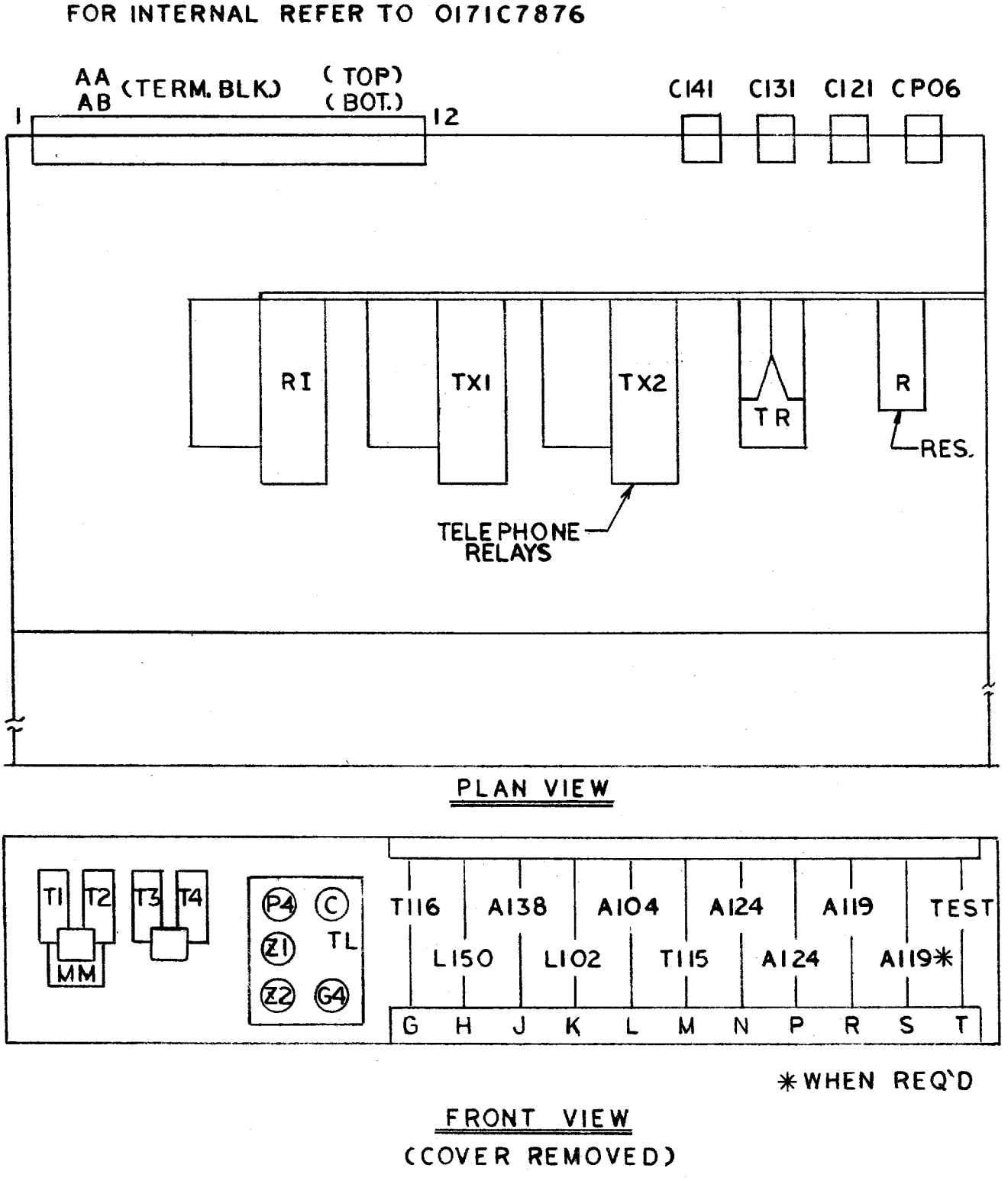


Fig. 3 (0269A3103-0) COMPONENT LOCATIONS FOR THE TYPE SLAT51H RELAY

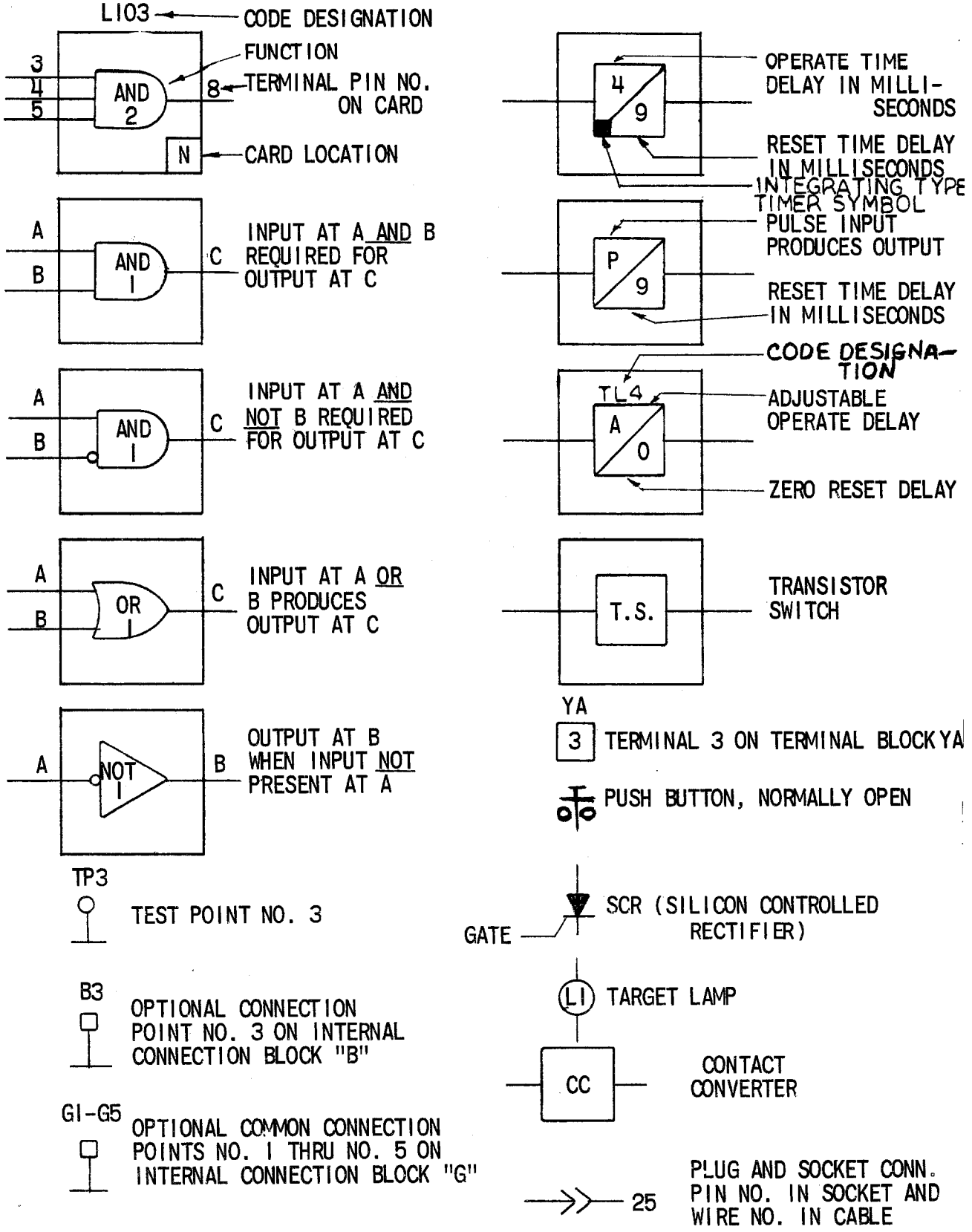
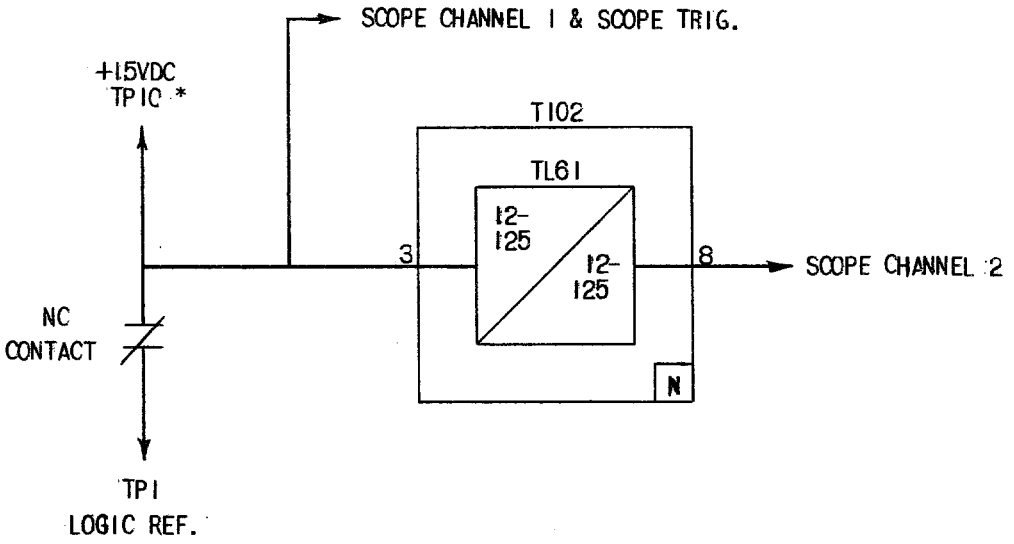


Fig. 4 (0227A2047-1) LOGIC AND INTERNAL CONNECTION DIAGRAM LEGEND



* THE 15VDC SIGNAL AT PIN 10 HAS A CURRENT LIMITING RESISTOR MOUNTED ON THE TEST CARD.

Fig. 5 (0246A7987-0) LOGIC TIMER TEST CIRCUIT

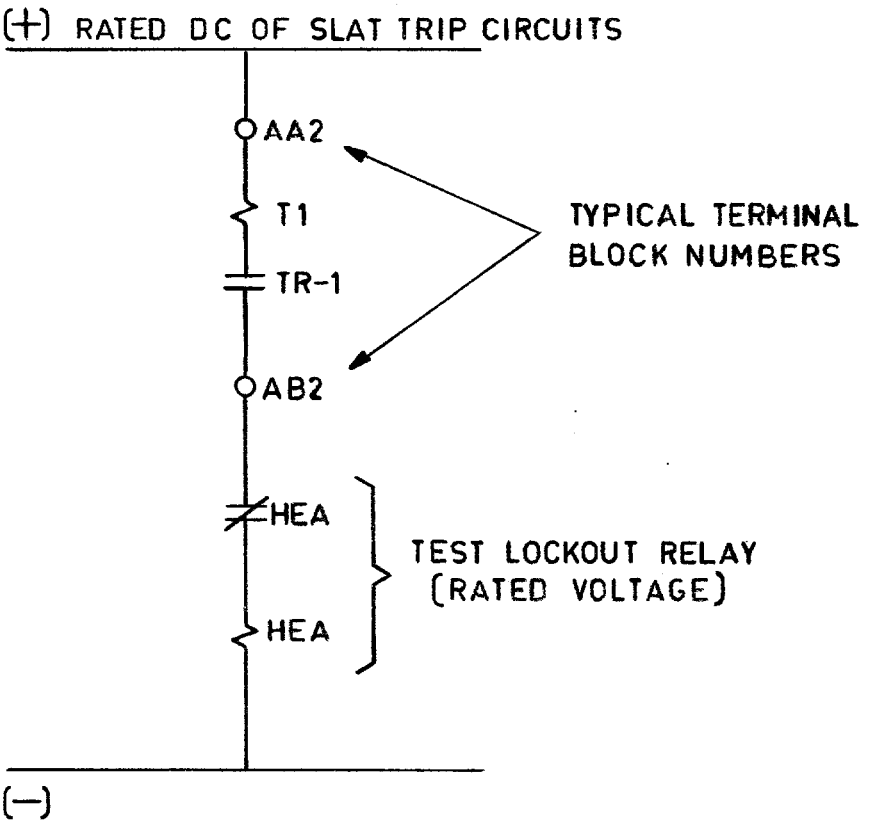


Fig. 6 (0257A8788-0) TYPICAL TR TRIP CIRCUIT TEST CONNECTIONS