

# STATIC OUTPUT AND TRIPPING UNIT TYPE SLAT54P

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#### DESCRIPTION

The Type SLAT54P relay is a static output and tripping unit. The relay is not intended to be used by itself, but rather as part of a complement of equipment that forms a protective relaying scheme. For a complete description of the overall scheme in which this relay is employed, refer to the overall logic diagram and its associated logic description that is supplied with each terminal of equipment.

The SLAT54P relay is packaged in a four rack unit (one rack unit equals 1-3/4 inches) enclosed metal case suitable for mounting in a 19-inch rack. The outline and mounting dimensions are shown in Fig. 1. The internal connections for the relay are shown in Fig. 2. The component and card locations are shown in Fig. 3.

#### APPLICATION

The SLAT54P relay is a static output and tripping relay that was designed for use in a variety of schemes. For example, the SLAT54P can be used with Types SLYP, SLCN, SLS, SLAT, SSA and SLA relays to make up a single pole tripping and reclosing directional comparison scheme. For a complete description of the application of this relay in a particular scheme, refer to the logic description and diagram supplied with the scheme. The following is a list of the various functions included in the relay.

- TR The tripping circuit includes a single relay with two separate normally open contacts which are in series with mechanical target coils.
- RI-10 The reclose initiation outputs are provided to initiate automatic reclosing after a high speed single pole trip.
- BFI-ØA, ØB, ØC The breaker failure initiation outputs are provided for breaker failure protection.
- T3, T4, T5, T6 Electromechanical targets that give an indication when the associated contact passes trip current.
- OPTIONAL Four optional outputs, each having one normally open or normally closed contact, are available.
  - One optional output (Z2) having two separate normally open or normally closed contact is available.
- CONTACT CONVERTERS Three contact converters are supplied to allow remote inputs into the SLAT54P logic circuits.

These instructions do not purport to cover all details or variations in equipment nor to provide for every possible contingency to be met in connection with installation, operation or maintenance. Should further information be desired or should particular problems arise which are not covered sufficiently for the purchaser's purposes, the matter should be referred to the General Electric Company.

To the extent required the products described herein meet applicable ANSI, IEEE and NEMA standards; but no such assurance is given with respect to local codes and ordinances because they vary greatly.

#### RATINGS

The Type SLAT54P relay is designed for use in an environment where the air temperature outside the relay case does not exceed minus  $20^{\circ}\text{C}$  and plus  $65^{\circ}\text{C}$ .

The Type SLAT54P relay requires a plus or minus 15 VDC power source which can be obtained from a Type SSA power supply.

The tripping circuits are available in ratings for 48, 125 or 250 VDC.

The contacts of the telephone-type relays that are used for TR will make and carry three amperes continuously, and will interrupt up to 0.5 ampere (inductive) at 125 VDC.

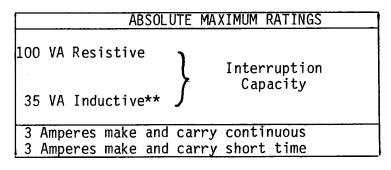
The ratings for the RI-10 relay are listed in Table I, the ratings of the (Z2) optional output, BFI-0A, 0B, 0C are listed in Table II, and the ratings of the optional outputs (single contact) are listed in Table III.

Refer to unit nameplate for the ratings of a particular relay.

# TABLE I

	ABSOLUTE MAXIMUM RATINGS
180	VA Resistive Interruption
60	VA Inductive** Capacity
3	Amperes make and carry continuous
30	Amperes make and carry short time

#### TABLE II



#### TABLE III

# ABSOLUTE MAXIMUM RATINGS 10 VA Resistive Interruption Capacity 3 VA Inductive\*\* 0.5 Ampere make and carry continuous 0.5 Ampere make and carry short time

\*\*The inductive rating is based on the inductance of a coil having a XL/R ratio of three-to-one.

#### BURDENS

The SLAT54P relay presents a maximum burden to the Type SSA power supply of:

200 milliamperes from the +15 VDC supply 130 milliamperes from the -15 VDC supply

#### TRIP CIRCUIT

There are four electrically separate, normally open trip circuits. In addition there is an electromechanical target which indicates trip current was passed by the associated trip contact. The contact outputs permit isolating the relay power supply from the trip circuit power supply.

#### RI-10 RECLOSE INITIATE CIRCUIT

Two electrically separate normally open contacts are provided. These contacts close within 16 milliseconds from the time the associated coil is energized by the logic. The contacts open within 160 milliseconds from the time the coil is deenergized. The RI function uses a telephone-type relay with contact ratings stated under RATINGS.

# BFI-ØA, ØB, ØC - BREAKER FAILURE INITIATE CIRCUITS AND (Z2) OPTIONAL OUTPUT CIRCUITS

Eight electrically separate normally open contacts are provided. These contacts close within two milliseconds from the time the associated coil is energized by the logic. These contacts open within three milliseconds from the time the coil is deenergized. These functions use reed relays with contact ratings stated under RATINGS.

#### OPTIONAL OUTPUTS

Four optional reed relay contact outputs can be provided in either normally open or normally closed configuration. The contacts operate within 0.5 millisecond from the time logic signals, available from the selected matrix points in the SLAT54P or associated SLA, change state.

#### CONTACT CONVERTERS

Three contact converters are included, each of which can be picked up from 48, 125 or 250 VDC sources. Taps for selecting input voltage to contact converter are located on the associated CC card.

#### **TARGETS**

Four electromechanical target coils are included; one in series with each output contact. These contacts operate on one ampere of trip current. The trip circuit resistance in the relay is 0.35 ohm.

#### LOGIC CIRCUITS

The functions of the Type SLAT54P involve basic logic (AND, OR, and NOT) where the presence or absence of signals, rather than their magnitude, controls the operation. Signals are measured with respect to a reference bus accessible at TP1. In general, a signal below one VDC represents an OFF or LOGIC ZERO condition; an ON or LOGIC ONE is represented by a signal of approximately plus 15 VDC.

The symbols used on the internal connection diagram (Fig. 2) are explained by the legend shown in Fig. 5.

The SLAT54P also contains matrix blocks which allow for the interconnection of different logic functions both within and outside the SLAT54P relay. The matrix block points shown on the internal connection diagram for the SLAT54P are connected by jumpers at the factory. These connections are used to implement the logic arrangement shown on the associated logic diagram. These connections are listed on the associated option chart. A typical option chart for the SLAT54P relay is shown in Fig. 7. Some matrix block connections may be customer options. These connections will be shown as optional connections on the overall logic and must be selected by the user before the unit is placed in service.

#### CALCULATION OF SETTINGS

The SLAT54P is an integral part of an overall scheme, and reference should be made to the overall logic diagram description for both application and setting information.

#### CONSTRUCTION

The SLAT54P relay is packaged in an enclosed metal case with hinged front cover and removable top cover. The outline and mounting dimensions of the case and the physical location of the components are shown in Fig. 1 and 3, respectively.

The SLAT54P relay contains printed circuit cards identified by a code number such as: A104, T115, L109 where A designates an auxiliary function, T designates a time-delay function, and L designates a logic function. The printed circuit cards plug in

from the front of the unit. The sockets are marked with letter designations or "addresses" (D, E, F, etc.), which appear on the guide strips in front of each socket, on the component location drawings, on the unit internal connection diagram, and on the printed circuit card. The test points (TP1, TP2, etc.) shown on the internal connections diagram are connected to instrument jacks on the test card in position T with TP1 at the top of the AT card. TP1 is tied to reference; TP10 is tied to plus 15 VDC through a 2.2K resistor. The resistor limits the current when TP10 is used to supply a logic signal to a card.

The SLAT54P relay receives its inputs from and sends outputs to the associated Type SLA relay. These units are interconnected by ten conductor shielded cables. The sockets for these cables are located on the rear panel of the unit. The SLAT54P output functions are connected to 12-point terminal strips, which are also located on the rear of the unit.

A window is provided in the hinged cover of the relay to allow the mechanical targets to be seen. Push buttons are also provided to reset the targets without opening the cover.

# RECEIVING, HANDLING AND STORAGE

The SLAT54P relay will normally be supplied as part of a static relay equipment, mounted in a rack or cabinet with other static relays and test equipment. Immediately upon receipt of a static relay equipment, it should be unpacked and examined for any damage sustained in transit. If injury or damage resulting from rough handling is evident, file a damage claim at once with the transportation company and promptly notify the nearest General Electric Sales Office.

Reasonable care should be exercised in unpacking the equipment. If the equipment is not to be installed immediately, it should be stored indoors in a location that is free from moisture, dust, metallic chips, and severe atmospheric contaminants.

Just prior to final installation, the shipping support bolt should be removed from each side of all relay units, to facilitate possible future unit removal for maintenance. These shipping support bolts are approximately eight inches back from the relay front panel. STATIC RELAY EQUIPMENT, WHEN SUPPLIED IN SWING RACK CABINETS, SHOULD BE SECURELY ANCHORED TO THE FLOOR OR TO THE SHIPPING PALLET TO PREVENT THE EQUIPMENT FROM TIPPING OVER WHEN THE SWING RACK IS OPENED.

#### TEST INSTRUCTIONS

## CAUTION:

THE LOGIC SYSTEM SIDE OF THE DC POWER SUPPLY USED WITH MOD III STATIC RELAY EQUIPMENT IS ISOLATED FROM GROUND. IT IS A DESIGN CHARACTERISTIC OF MOST ELECTRONIC INSTRUMENTS THAT ONE OF THE SIGNAL INPUT TERMINALS IS CONNECTED TO THE INSTRUMENT CHASSIS. IF THE INSTRUMENT USED TO TEST THE RELAY EQUIPMENT IS ISOLATED FROM GROUND, ITS CHASSIS MAY HAVE AN ELECTRICAL POTENTIAL WITH RESPECT TO GROUND. THE USE OF A TEST INSTRUMENT WITH A GROUNDED CHASSIS WILL NOT AFFECT THE TESTING OF THE EQUIPMENT.

HOWEVER, A SECOND GROUND CONNECTION TO THE EQUIPMENT, SUCH AS A TEST LEAD INADVERTENTLY DROPPING AGAINST THE RELAY CASE, MAY CAUSE DAMAGE TO THE LOGIC CIRCUITRY. NO EXTERNAL TEST EQUIPMENT SHOULD BE LEFT CONNECTED TO THE STATIC RELAYS WHEN THEY ARE IN PROTECTIVE SERVICE, SINCE TEST EQUIPMENT GROUNDING REDUCES THE EFFECTIVENESS OF THE ISOLATION PROVIDED.

IF THE SLAT54P RELAY THAT IS TO BE TESTED IS INSTALLED IN AN EQUIPMENT WHICH HAS ALREADY BEEN CONNECTED TO THE POWER SYSTEM, DISCONNECT THE OUTPUTS TO THE SYSTEM DURING TEST.

## GENERAL

The SLAT54P relay is supplied from the factory either as a separate unit, or mounted in a static relay equipment associated with measuring relays, a Type SSA power supply, and some form of channel equipment. All relay units for a given terminal of static relaying equipment are tested together at the factory, and each unit will have the same summary number stamped on its nameplate.

In general, when a time range is indicated on the internal connections diagram, the timer has been factory set at a mid-range value. Timers should be set for the operating or reset times indicated on the associated overall logic diagram. Where a time range is indicated on the overall logic diagram, the timer should be set for the value recommended for that function in the descriptive writeup accompanying the overall logic diagram. Where a setting depends upon conditions encountered on a specific application, this is so stated and the factors influencing the choice of setting are described. The procedure for checking and setting the timers is described in a later section.

# OPERATIONAL CHECKS

Operation of the SLAT54P unit can be checked by observing the signals at the twenty test points (TP1 to TP20) in the SLAT54P by observing the operation of the associated channel equipment, or by observing the output functions. The test points are located on the test cards in positions T and AT and are numbered 1 to 20 from top to bottom. TP1 is the reference bus for the logic circuit, TP10 is at plus 15 VDC. The remaining points are located at various strategic points throughout the logic as shown in the internal connection diagram (Fig. 2). Test point voltages can be monitored with a portable high impedance voltmeter, the voltmeter on the test panel of the associated equipment, or an oscilloscope.

### TEST CARD ADAPTER

The test card adapter provides a convenient means of gaining access to any pin of a particular card. Detailed information on the use of the test adapter card is included in the card instruction book GEK-34158.

# TIMER ADJUSTMENTS AND TESTS

When the time-delay cards are to be adjusted or checked, an oscilloscope that can display two traces simultaneously, and that has a calibrated horizontal sweep, should be used.

In order to test the timer cards, it is necessary to remove the card previous to the timer and to place the timer card in a card adapter. The card adapter allows access to the input and output of the timer if they are not brought out on test points. The timer test circuit is shown on Fig. 6. Opening the normally closed contact causes the output to step up to plus 15 VDC after the pickup delay of the timer. To increase the pickup time, turn the upper potentiometer on the timer card clockwise; to decrease the time, turn it counterclockwise. Closing the contact causes the timer output to drop out after the reset time-delay setting of the card. If the timer card is provided with a variable reset delay, it can be adjusted by the lower potentiometer on the timer card (clockwise increases reset time).

# TRIP CIRCUIT TESTS

The trip circuits and series mechanical targets may be checked by connecting an auxiliary lock-out relay, such as the Type HEA relay, in series with the trip circuit. A typical circuit is shown in Fig. 4. The HEA relay should have the same DC rating as the trip circuit of the relay. If an auxiliary lock-out relay is not available, it can be replaced by a resistive load which limits the trip circuit current to three amperes. In most equipments, the trip circuit can be energized by operating a test push button.

# OVERALL EQUIPMENT TESTS

After the SLAT54P relay and the associated static relay units have been individually calibrated and tested for the desired settings, a series of overall operating circuit checks is advisable.

The elementary, overall logic, and logic description for the specific job will be useful for determining the overall operation of the scheme.

An overall equipment test can be performed by applying the AC current and voltages to the measuring units as specified in the instruction book for the measuring units and checking that proper outputs are obtained when the measuring units operate.

#### MAINTENANCE

# PERIODIC TESTS

It should be sufficient to check the outputs produced at test points in the SLAT54P when periodic calibration tests are made on the associated measuring units, for example, the phase and ground relays in line relaying scheme. No separate periodic tests on the SLAT54P itself should be required.

# TROUBLESHOOT ING

In any troubleshooting of equipment, it should first be established which unit is functioning incorrectly. The overall logic diagram supplied with the equipment shows the combined logic of the complete equipment and the various test points in each unit. By signal tracing, using the overall logic diagram and the various test points, it should be possible to quickly isolate the trouble.

#### **GEK-65592**

A test adapter card is supplied with each static relay equipment to supplement the prewired test points on the test cards. Use of the adapter card is described in the card instruction book GEK-34158.

A dual trace oscilloscope is a valuable aid to detailed troubleshooting, since it can be used to determine phase shift, operate and reset times as well as input and output levels. A portable dual-trace oscilloscope with a calibrated sweep and trigger facility is recommended.

#### SPARE PARTS

To minimize possible outage time, it is recommended that a complete maintenance program should include the stocking of at least one spare card of each type. It is possible to replace damaged or defective components on the printed circuit cards, but great care should be taken in soldering, so as not to damage or bridge-over the printed circuit buses, or overheat the semiconductor components. The repaired areas should be recovered with a suitable hi-dielectric plastic coating to prevent possible breakdowns across the printed buses due to moisture and dust. The wiring diagrams for the cards in the SLAT54P relay are included in the card book GEK-34158.

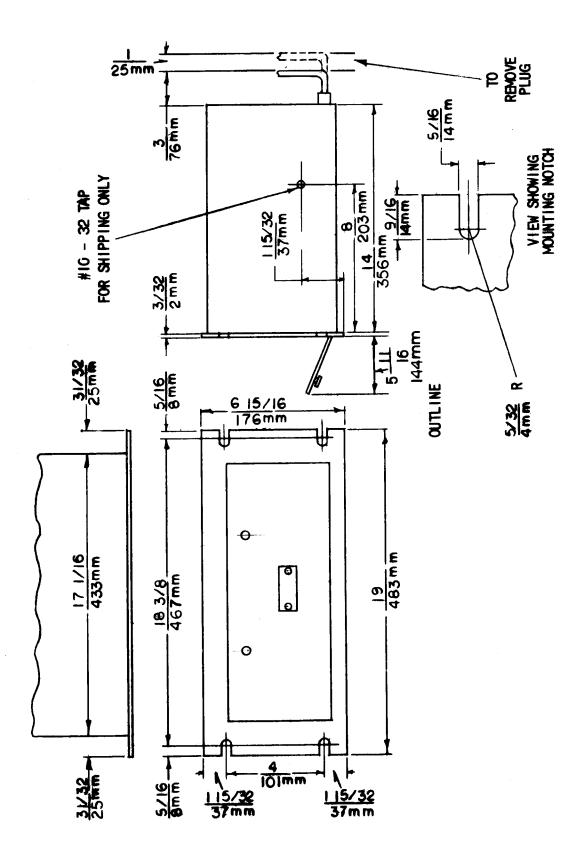


Fig. 1 (0227A2037-0) Outline and Mounting Dimensions

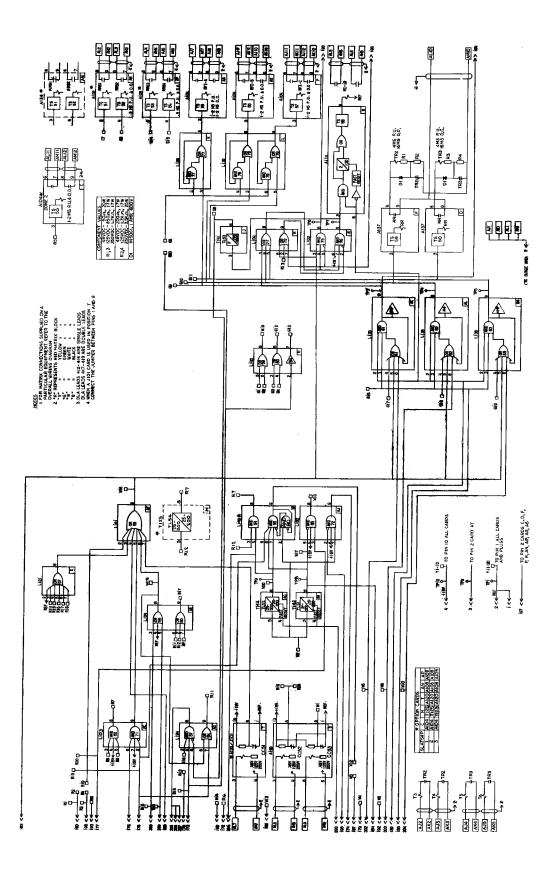


Fig. 2 (0145D7161-1) Internal Connections for the Type SLAT54P Relay

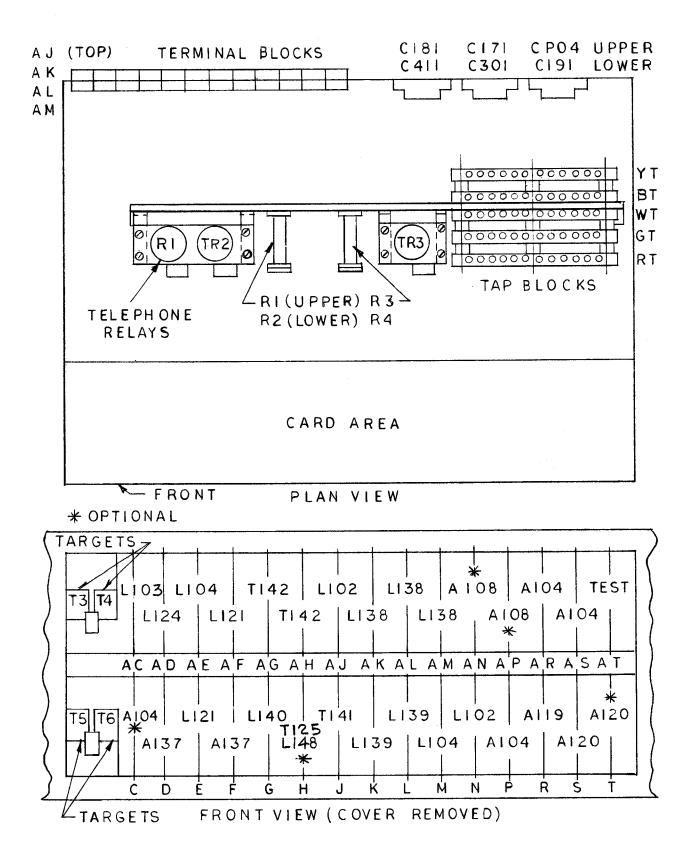


Fig. 3 (0275A4589-1) Component Location Diagram

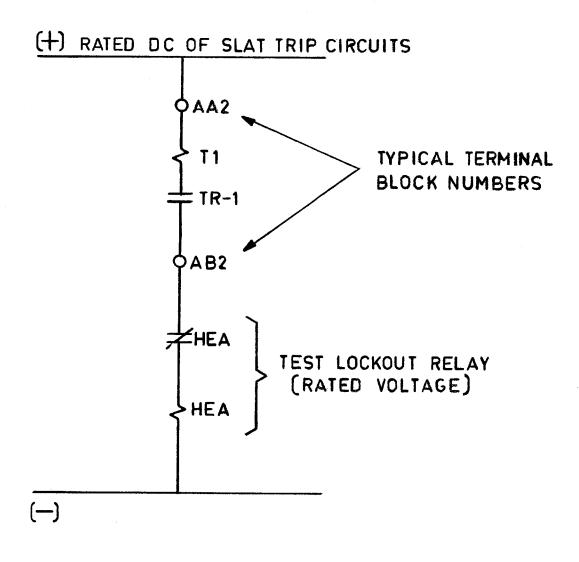


Fig. 4 (0257A8788-0) Typical Trip Circuit Test Connections for Relays with Trip Contacts

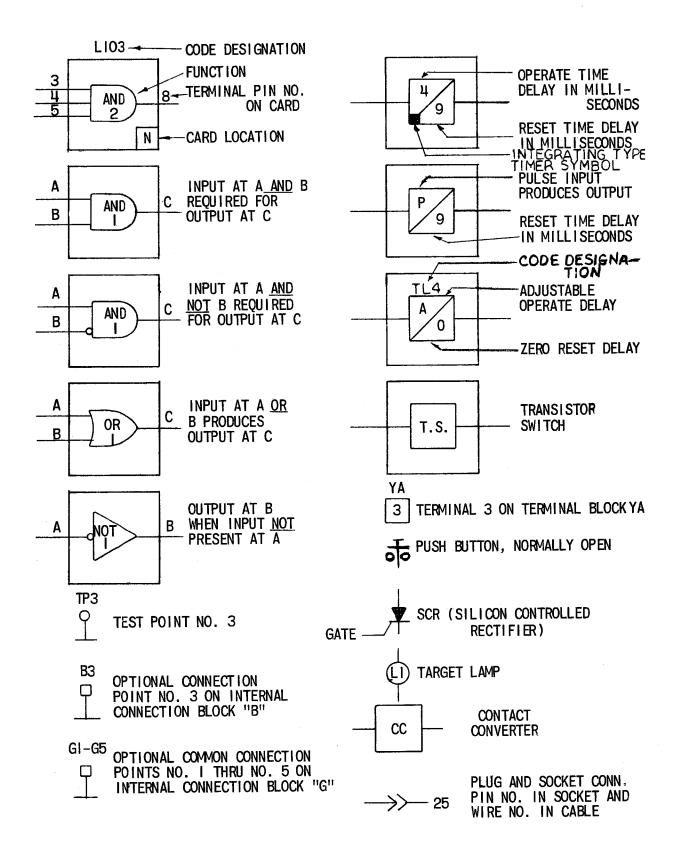
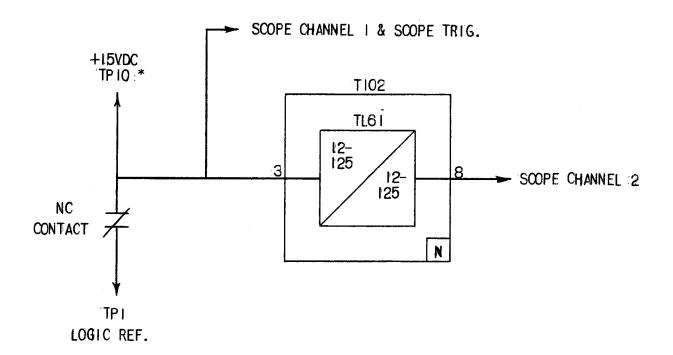


Fig. 5 (0227A2047-1) Logic and Internal Connection Diagram Legend



\* THE 15VDC SIGNAL AT PIN 10 HAS A CURRENT LIMITING RESISTOR MOUNTED ON THE TEST CARD.

Fig. 6 (0246A7987-0) Logic Timer Test Circuit

THE FOLLOWING ARE FACTORY CONNECTIONS MADE AT THE MATRIX BLOCKS INSIDE OF THE SLA RELAY ASSOCIATED WITH THIS EQUIPMENT.

SYMBOLS LISTED: PL=RELAY INTERCONNECTING CABLE LEAD

(5)=LOGIC FUNCTION CARD PIN NUMBER

=3-WAY CONNECTION

- DLA MONITOR CONNECTION AVAILABLE BUT NOT USED

MATRIX BLOCK LOGIC FUNCTION			MATRIX BLOCK		LOGIC FUNCTION		
JUMPERS				JUMPERS		FROM TO	
FROM	ТО	FROM	ТО	FROM	TO		
R13	Y//	OR 72	REF	G9	<u>57</u>	AND51	TS51
<i>Ģ5</i>	GI	TL 53	OR59	<u>G10</u>	<u>68</u>	AND52	T552
B19	G2	CC 52	OR 59	G11	914	AND 53	TS53
B20	W14	CC 52	PL 199				
G20	G6	PL 173	AND 77				
B/3	B18	PL 178	AND 57				
G17	Y12	OR 51	REF	ļ			
G18	Y13	OR52	REF				
619	Y14	OR53	REF				
	<u> </u>	<u> </u>					
±W15	G15	0R55	TS54				
<b>B17</b>	R18	OR80	OR57(5W)				
R14	Y/5	OR 57	REF				
R 15	Y/6	OR 57	REF				
R16	Y/7	OR57	REF				
R17	YIB	OR57	REF				
R4	R19	PL198	OR56				
R5	85	PL 193	TS50				
W/3	BII	PL182	0R80				
WI	B/2	CC53	ORBO				
#W 20	R8	TL 52	OR 80				
W/9	WZ	OR 59	7452				
W18	W4	AND56	P4179				
\$ W15	64	OR55(8)	0R60(4)				
B10	63	PL176	0860(3)				
G12	39		AND60(5)				
# W20	B8		AND60(3)				
B7	RI2		TL54(3)				
R7	RI	TL54(8)					
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Fig. 7 (0227A2050-1, Sh. 220) Typical Option Chart for Type SLAT54P Relay

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