INSTRUCTIONS

GEK-65684

STATIC OUTPUT AND TRIPPING UNIT

TYPE SLAT61K

GENERAL ELECTRIC

CONTENTS

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DESCRIPTION

The SLAT61K relay is a static logic, output, and tripping relay intended for application in dual phase comparison schemes operating via a frequency shift channel. In addition to the SLAT61K relay, the complete relay scheme would also include an SLD phase comparison measuring unit, a power supply and the appropriate frequency-shift channel equipment.

The outputs of the SLAT61K include two trip contact circuits, each with an electromechanical target; two electrically separate breaker failure timer initiating contacts (BFI); two electrically separate reclose initiating contacts (RI); two electrically separate receive-high-frequency contacts (RH); and two electrically separate receive-low-frequency contacts (RL). The inputs to the SLAT61K are from the associated SLD relay, from the channel equipment, and from switch contacts which provide means for changing the channel status for test purposes, or for checking the tripping logic. Additional inputs from an SLA logic unit may be used in three-terminal-line applications.

APPLICATION

The SLAT61K logic and tripping unit is specifically designed for use with the SLD51 relay in a dual phase comparison relay scheme utilizing a frequency shift tone channel. Dual phase comparison means that the comparison of the phase angles of the currnts at the two ends of the protected transmission line are made on both the positive and negative half cycles of the current sine wave. This provides a faster response in the overall scheme for tripping on internal line faults.

To accomplish the dual phase comparison function, the SLD51 relay supplies squaring amplifier inputs from both the positive and negative half cycles of current. The SLAT has two parallel paths of logic for both the local attempt to trip and the tone signals received from the remote line terminal via the frequency shift channel. The parallel logic paths for the local attempt to trip are composed of AND41/AND51, the phase delay timers TL1/TL2, the comparers AND45/AND55 and the trip coordination timers TL3/TL4. The parallel logic paths for the tone signals received from the remote line terminal via the tone receivers are composed of symmetry adjustment timers TL7/TL8, AND47/AND57, AND42/AND52 and to the comparers AND45/AND55. Interconnections are provided so that the frequency shift tone transmitter can be keyed either to the high or low frequency via the SLAT logic.

There are eight points in the logic which may be monitored via a connection plug on the rear of the unit. These points are indicated on the unit internal connection diagram, Fig. 2, and are numbered 412 through 419 with 411 on reference. If these points are to be monitored, a separate data logging amplifier (DLA) is required.

There are no measuring functions to be set in this unit, but there are several timers which require field adjustment. Refer to the section entitled **TIMER SETTINGS** for a discussion of the considerations involved in making these settings.

For a complete description of the scheme in which the relay is to be used, refer to the overall logic diagram and its associated logic description that is supplied with each terminal of equipment.

RATINGS

The Type SLAT61K relay is designed for use in an environment where the air temperature outside the relay case does not exceed minus 20°C and plus 65°C.

The Type SLAT61K relay requires a plus or minus 15 VDC power source which can be obtained from a Type SSA power supply.

The contacts of the telephone-type relay (TR) used for the trip circuit, will make and carry three amperes continuously. Each has a 1.0 ampere series target. The tripping circuits are designed to carry 30 amperes for one second.

The contacts of the telephone-type relays that are used for RI will make and carry three amperes continuously and will interrupt up to 0.5 ampere (inductive) at 125 VDC or up to 0.25 ampere (inductive) at 250 VDC.

The contacts of the reed relays that are used for BFI, RH and RL are rated for 100 watts direct current. They will make and carry three amperes continuously.

Refer to the unit nameplate for the ratings of a particular relay.

BURDENS

The SLAT61K relay presents a maximum burden to the Type SSA power supply of:

250 milliamperes from the +15 VDC supply
200 milliamperes from the -15 VDC supply

Each contact converter, when energized, will draw approximately ten milliamperes from the station battery, regardless of tap setting.

FUNCTIONS

RELAY CONTACT TRIP CIRCUITS

Two electrically separate, isolated relay contact trip circuits are provided to trip two breakers. Each circuit is capable of carrying 30 amperes for one second.

RI RECLOSE INITIATE CIRCUIT

Two electrically separate normally open contacts are provided. These contacts close within 17 milliseconds from the time the associated coil is energized by the logic. The contacts open within 170 milliseconds from the time the coil is de-energized. The RI function uses a telephone-type relay with contact ratings stated under **RATINGS.**

BFI BREAKER FAILURE INITIATE CIRCUIT

Two electrically separate normally open contacts are provided. These contacts close within two milliseconds from the time the associated coil is energized by the logic. These contacts open within two milliseconds from the time the coil is de-energized. The BFI function uses a reed relay with contact ratings stated under **RATINGS.**

RH RECEIVE HIGH CIRCUIT

Two electrically separate normally open contacts are provided. These contacts close within two milliseconds from the time the associated coil is energized by the logic. The contacts open within two milliseconds from the time the coil is de-energized. The RH function uses a reed relay with contact ratings stated under **RATINGS.**

RL RECEIVE LOW CIRCUIT

Two electrically separate normally open contacts are provided. These contacts close within two milliseconds from the time the associated coil is energized by the logic. These contacts open within two milliseconds from the time the coil is de-energized. The RL function uses a reed relay with contact ratings stated under **RATINGS.**

CONTACT CONVERTERS

The purpose of this function is to convert a contact operation into a signal that is compatible with the logic circuit of the Type SLAT61K relay. The contact converters are labeled CC1, CC2 and CC3.

CC1

Contact converter CC1 permits an external contact to shift the channel transmitter to the low-shift frequency.

CC2

Contact converter CC2 permits an external contact to block pilot tripping at the comparer (AND45 or AND55).

CC3

Contact converter CC3 permits an external contact to shift the channel transmitter to the high-shift frequency.

CHANNEL INTERFACE

The logic of the Type SLAT61K relay includes two isolation interfaces (Fig. 6) between the relays in the scheme and the associated channel. The circuitry of the isolation provides signal paths, but maintains metallic isolation. This feature makes it possible to maintain isolation between the DC supply used for the relays and that employed by the channel.

When pins 9 and 10 are both connected to relay reference, a metallically separate positive logic signal appears at pin 11 with respect to pin 12. The output from the isolation interface is a five VDC, 20 milliampere signal.

DATA MONITORING POINTS

Data monitoring points are brought out of a plug at the rear of the SLAT61K relay. The plug contains eight monitoring points and reference as shown on the overall logic diagram for the scheme. To monitor these points, and additional piece of equipment termed a data logging amplifier (DLA) is required.

TIMER SETTINGS

This SLAT unit contains ten timers, six of which are factory set and do not generally need field adjustment. These timers are:

(a) TL3 and TL4 trip coordination delay timers
(b) TL5 transient blocking timer
(c) TL6 DC timer which prevents incorrect relay operation resulting from turning on the DC supply
(d) TL9 and TL10 pulse stretcher timers for the RH and RL received trip auxiliary units.

The remaining four timers should only be set after the equipment is completely installed, adjusted and tested. These timers and their functions are as follows:

(a) The TL7 and TL8 symmetry adjustment timers are adjusted so that a full half-cycle input is provided to AND47/AND57 eliminating as much as possible the non-symmetrical effects of the tone receivers that may be present.

(b) The TL1 and TL2 phase-delay adjustment timers are to be adjusted so that the half-cycle blocks of signal for the local trip attempt from AND41/AND51 are properly aligned with the half-cycle received trip tone signals at the comparers AND45/AND46. For a simulated internal fault condition these two signals should be exactly in phase. For an external fault condition, the two signals should be 180 degrees out of phase.

The proper adjustment of the above timers is described in detail in the section entitled TEST INSTRUCTIONS - SYMMETRY AND PHASE-DELAY TIMER ADJUSTMENTS.

TARGETS

Two electromechanical target coils are included, one in series with each trip contact. These targets operate on one ampere of trip current when the associated contact closes. The trip circuit resistance in the relay is 0.40 ohm.

LOGIC CIRCUITS

The functions of the Type SLAT61K involve basic logic (AND, OR and NOT) where the presence or absence of signals, rather than their magnitude, controls the operation. Signals are measured with respect to a reference bus accessible at TP1. In general, a signal below one VDC represents an OFF or LOGIC ZERO condition, an ON or LOGIC ONE is represented by a signal of approximately plus 15 VDC.

The symbols used on the internal connection diagram (Fig. 2) are explained by the legend shown in Fig. 5.

CONSTRUCTION

The SLAT61K relay is packaged in an enclosed metal case with hinged front cover and removable top cover. The outline and mounting dimensions of the case and the physical location of the components are shown in Fig. 1 and 3, respectively.

The SLAT61K relay contains printed circuit cards identified by a code number, such as: A104, T116, L106 where A designates an auxiliary function, T designates a time-delay function, and L designates a logic function. The printed circuit cards plug in from the front of the unit. The sockets are marked with letter designations or "addresses" (D, E, F, etc.) which appear on the guide strips in front of each socket, on the component location drawing, on the unit internal connection diagram, and on the printed circuit card. The test points (TP1, TP2, etc.) shown on the internal connection diagram are connected to instrument jacks on a test card in position T with TP1 at the top of the T card. TP1 is tied to reference; TP10 is tied to plus 15 VDC through a 1.5K resistor. This resistor limits the current when TP10 is used to supply a logic signal to a card.

The SLAT61K relay receives its inputs from the associated Type SLD relay. These units are interconnected by ten-conductor-shielded cables. The sockets for these cables are located on the rear panel of the unit. The SLAT61K output functions are connected to 12-point terminal strips, which are also located on the rear of the unit.

A window is provided in the hinged cover of the relay to allow the mechanical targets to be seen. Push buttons are also provided to reset the targets without opening the cover.

RECEIVING, HANDLING AND STORAGE

These relays will normally be supplied as part of a static relay equipment, mounted in a rack or cabinet with other static relays and test equipment. Immediately upon receipt of a static relay equipment, it should be unpacked and examined for any damage sustained in transit. If injury or damage resulting from rough handling is evident, file a damage claim at once with the transportation company and promptly notify the nearest General Electric Sales Office.

Reasonable care should be exercised in unpacking the equipment. If the equipment is not to be installed immediately, it should be stored indoors in a location that is free from moisture, dust, metallic chips, and severe atmospheric contaminants.

Just prior to final installation the shipping support bolt should be removed from each side of all relay units, to facilitate possible future unit removal for maintenance. These shipping support bolts are approximately eight inches back from the relay front panel. Static relay equipment, when supplied in swing rack cabinets, should be securely anchored to the floor or to the shipping pallet to prevent the equipment from tipping over when the swing rack is opened.

TEST INSTRUCTIONS

CAUTION

IF THE SLAT61K RELAY THAT IS TO BE TESTED IS INSTALLED IN AN EQUIPMENT WHICH HAS ALREADY BEEN CONNECTED TO THE POWER SYSTEM, DISCONNECT THE OUTPUTS FROM THE SYSTEM BEFORE TESTING.

GENERAL

The SLAT61K relay is supplied from the factory either mounted in a static relay equipment or as a separate unit associated with measuring relays, a Type SSA power supply, and some form of channel equipment. All relay units for a given terminal of static relaying equipment are tested together at the factory, and each unit will have the same summary number stamped on its nameplate.

In general, when a time range is indicated on the internal connection diagram, the timer has been factory set at a mid-range value. Timers should be set for the operating or reset times indicated on the associated overall logic diagram. When a time range is indicated on the overall logic diagram, the timer should be set at the value recommended for that function in the descriptive writeup accompanying the overall logic diagram. Where a setting depends upon conditions encountered on a specific application, this is so stated and the factors influencing the choice of setting are described. The procedure for checking and setting the timers is described in a later section.

OPERATIONAL CHECKS

Operation of the SLAT61K unit can be checked by observing the signals at the twenty test points (TP1 to TP20) in the SLAT61K, by observing the operation of the associated channel equipment, or by observing the output functions. The test points are located on the test card in position T, and are numbered 1 to 10 from top to bottom.

TP1 is the reference bus for the logic circuit; TP10 is at plus 15 VDC. The remaining points are located at various strategic points throughout the logic as shown on the internal connection diagram (Fig. 2). Test point voltages can be monitored with a portable high impedance voltmeter, the voltmeter on the test panel of the associated equipment, or an oscilloscope.

TEST CARD ADAPTER

The test card adapter provides a convenient means of gaining access to any pin of a particular card. Detailed information on the use of the test adapter card is included in the card instruction book, GEK-34158.

TIMER ADJUSTMENTS AND TESTS

When the time-delay cards are to be adjusted or checked, an oscilloscope that can display two traces simultaneously, and that has a calibrated horizontal sweep, should be used.

In order to test the timer cards it is necessary to remove the card previous to the timer (see Table I) and to place the timer card in a card adapter. The card adapter allows access to the input and output of the timer if they are not brought out on test points. The timer test circuit is shown in Fig. 6. Opening the normally closed contact causes the output to step up to plus 15 VDC after the pickup delay of the timer. To increase the pickup time, turn the upper potentiometer on the timer card clockwise; to decrease the time, turn it counterclockwise. Closing the contact causes the timer output to drop out after the reset time-delay setting of the card. If the timer card is provided with a variable reset delay, it can be adjusted by the lower potentiometer on the timer card (clockwise increases reset time).

A timer tester card (0172C5151G-1) can be obtained to replace the test circuit of Fig. 6. This card is equipped with an "ON" and "OFF" push button, a test light and two parallelled test jacks. This test card can be plugged into any printed circuit card socket in the unit (except the "T" location). One of the test jacks should be connected, via a jumper lead, to the input of the timer under test. The other test jack connects to trigger the timing device. This timer test card provides ease of operation and due to its bounceless contact action, it gives consistent results.

TABLE I

TIMER UNDER TEST	POSITION	REMOVE CARD IN POSITION
TL1	E	D
TL2	F	D
TL3	J	G
TL4	K	H
TL5	N	R (IN SLD)
TL6	K	NONE**
TL7	AH	AP
TL8	AJ	AR

**Turn power supply switch on and off

TRIP CIRCUIT TESTS

The trip contact circuits and the series mechanical targets may be checked by connecting an auxiliary lock-out relay, such as the Type HEA relay, in series with the trip circuit. If an auxiliary lock-out relay is not available, it can be replaced by a resistive load which limits the trip circuit current to three amperes. In most equipments, trip circuit can be triggered by operating a test push button in the associated units.

Prior to final installation, a check of the overall trip circuit should be made with the trip circuit outputs connected to trip the circuit breakers.

OVERALL EQUIPMENT TESTS

After the SLAT61K relay and the associated static relay units have been individually calibrated and tested for the desired settings and ranges, a series of overall operating circuit checks is advisable. The elementary, overall logic and logic description for the specific job will be useful for determining the overall operation of the scheme.

Overall equipment tests can be performed by applying alternating current and voltages to the measuring units as specified in the instruction book for the measuring units and checking that proper outputs are obtained when the measuring units operate.

SYMMETRY AND PHASE-DELAY TIMER ADJUSTMENTS

The symmetry timer (TL7 and TL8, AH and AJ positions) and phase-delay timers (TL1 and TL2, "E" and "F" positions) final settings must be made in the field after the transmitters, receivers and coupling equipment have been tuned and adjusted for proper sensitivity per the channel instructions. Operation of the squaring amplifier and fault detectors, FDL and FDH, are required for accomplishment of the final symmetry and phase-delay adjustments; refer to the measuring unit instruction book for the recommended procedure.

The symmetry adjustment must be accomplished prior to phase-delay adjustments as described in the measuring unit instructions. The transient blocking timer (TL5, "N" position) should be removed to prevent continuous channel keying when the logic trip bus is energized. Clockwise adjustment of P1 and P2 on TL7, AH position card, increases the pickup delay or drop-out delay, respectively. Conversely, counter-clockwise adjustment reduces the respective operate times. The minimum delay on pickup which allows equal half-cycle block and trip output as measured at TP13 is the recommended final setting. The TL8, AJ position card, is adjusted in the same manner; its output is measured at TP15.

After the symmetry adjustment has been accomplished, the phase-delay adjustment is made to obtain the proper alignment of the local signal with the received signal; refer to the measuring unit instructions. Clockwise adjustment of P1 or P2 on TL1, "E" position card, increases the pickup or drop-out delay, respectively. The final setting is the alignment of the trip attempt signal monitored at TP4 compared to the trip or block signal monitored at TP13, which is dependent upon internal or external fault simulation during the adjustment. The TL2, "F" position card, is adjusted in the same manner; the trip attempt signal should be monitored at TP6 and the trip or block signal monitored at TP15.

MAINTENANCE

PERIODIC TESTS

It should be sufficient to check the outputs produced at test points in the SLAT61K when periodic calibration tests are made on the associated measuring unit. No separate periodic tests on the SLAT61K itself should be required.

TROUBLESHOOTING

In any troubleshooting of equipment, it should first be established which unit is functioning incorrectly. The overall logic diagram supplied with the equipment shows the combined logic of the complete equipment and the various test points in each unit. By signal tracing, using the overall logic diagram and the various test points, it should be possible to quickly isolate the trouble.

A test adapter card is supplied with each static relay equipment to supplement the prewired test points on the test cards. Use of the adapter card is described in the card instruction book, GEK-34158.

A dual-trace oscilloscope is a valuable aid to detailed troubleshooting, since it can be used to determine phase shift, operate and reset times, as well as input and output levels. A portable dual-trace oscilloscope with a calibrated sweep and trigger facility is recommended.

SPARE PARTS

To minimize possible outage time, it is recommended that a complete maintenance program should include the stocking of a least one spare card of each type. It is possible to replace damaged or defective components on the printed circuit cards, but great care should be taken in soldering so as not to damage or bridge-over the printed circuit buses, or overheat the semiconductor components. The repaired area should be recovered with a suitable high-dielectric plastic coating to prevent possible breakdowns across the printed buses due to moisture and dust. The wiring diagrams for the cards in the SLAT61K relay are included in the card book, GEK-34158.

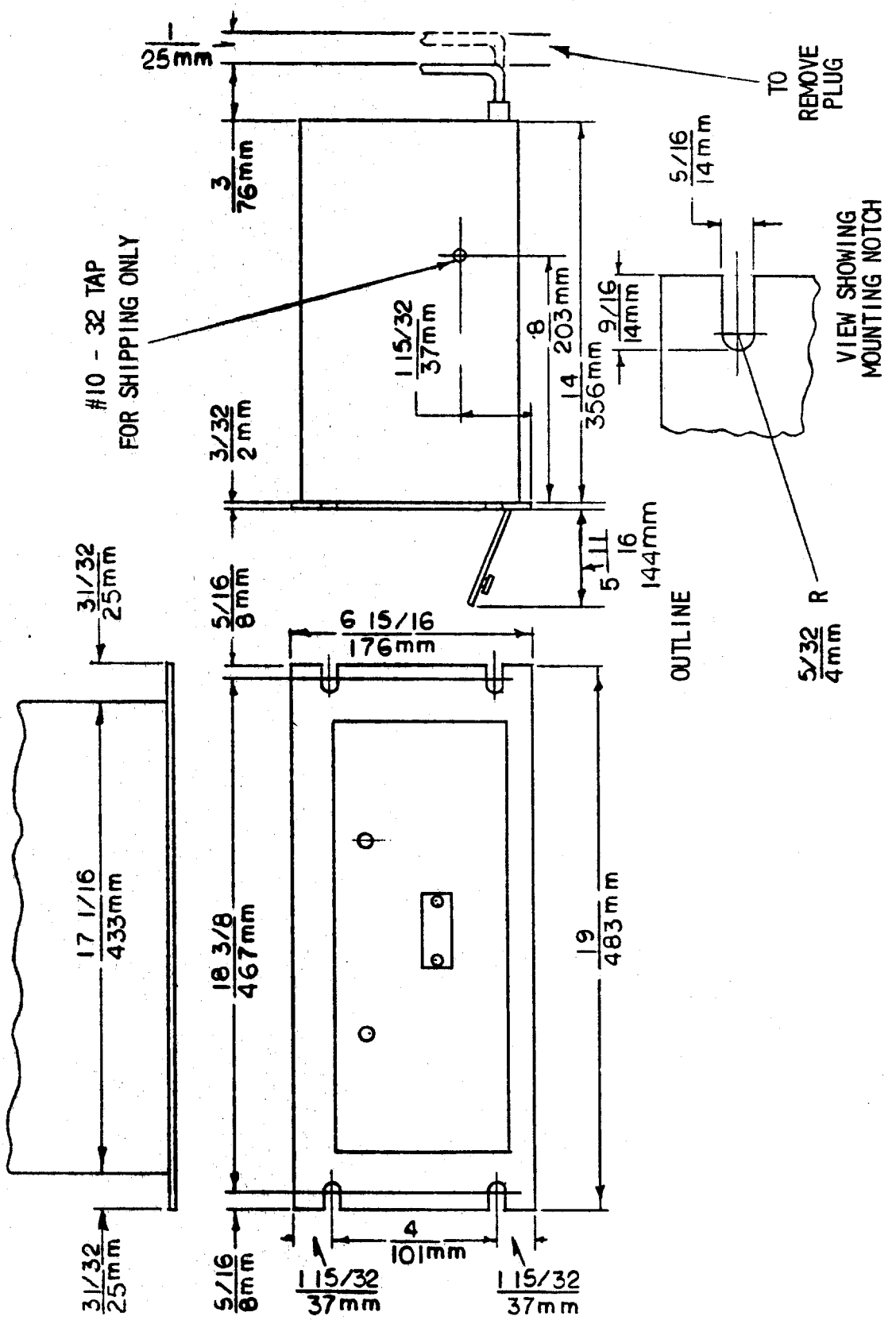


Fig. 1 (0227A2037-1) Outline and Mounting Dimensions for the Type SLAT61K Relay

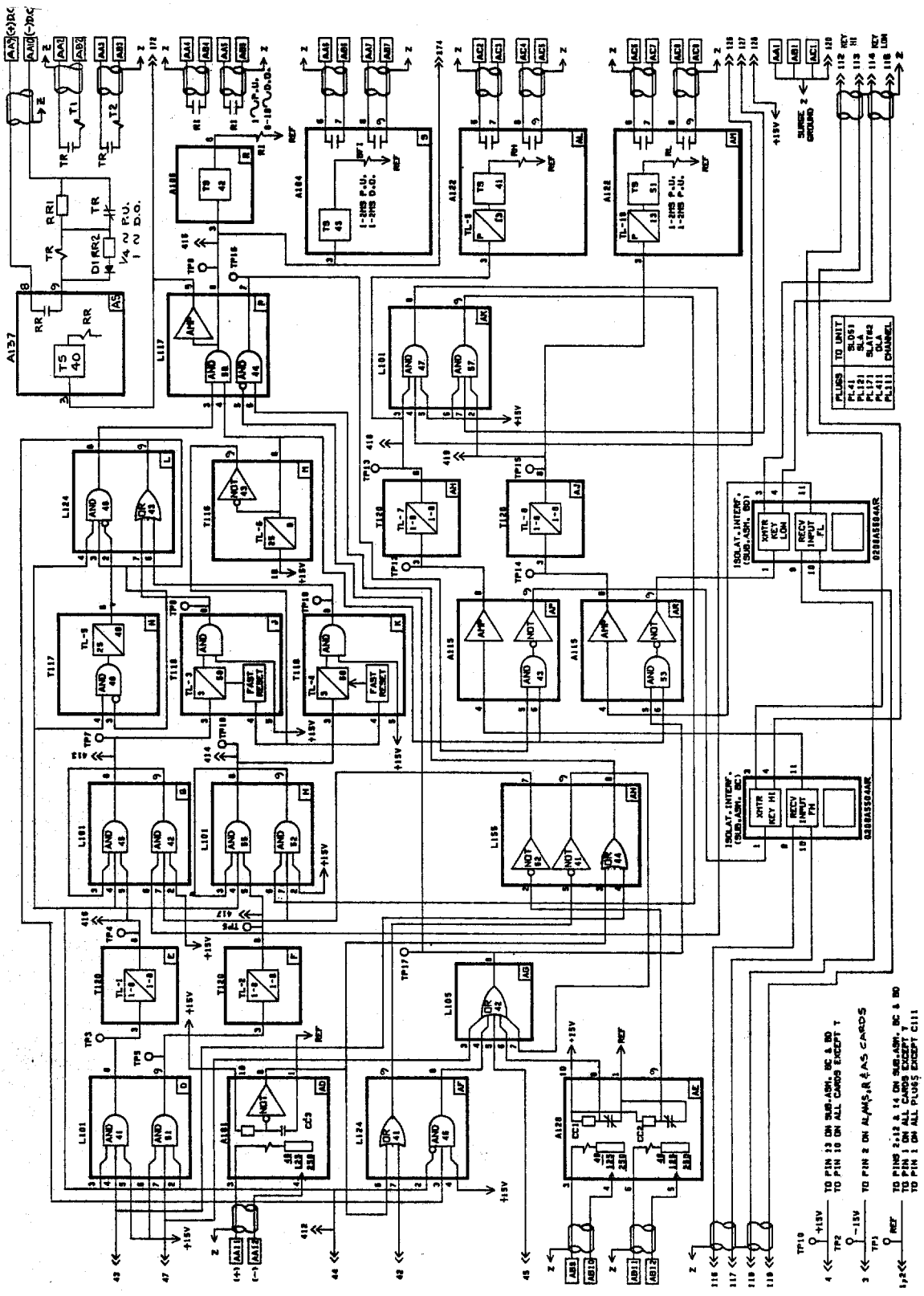


Fig. 2 (0179C6166-0) Internal Connection Diagram for the Type SLAT61K Relay

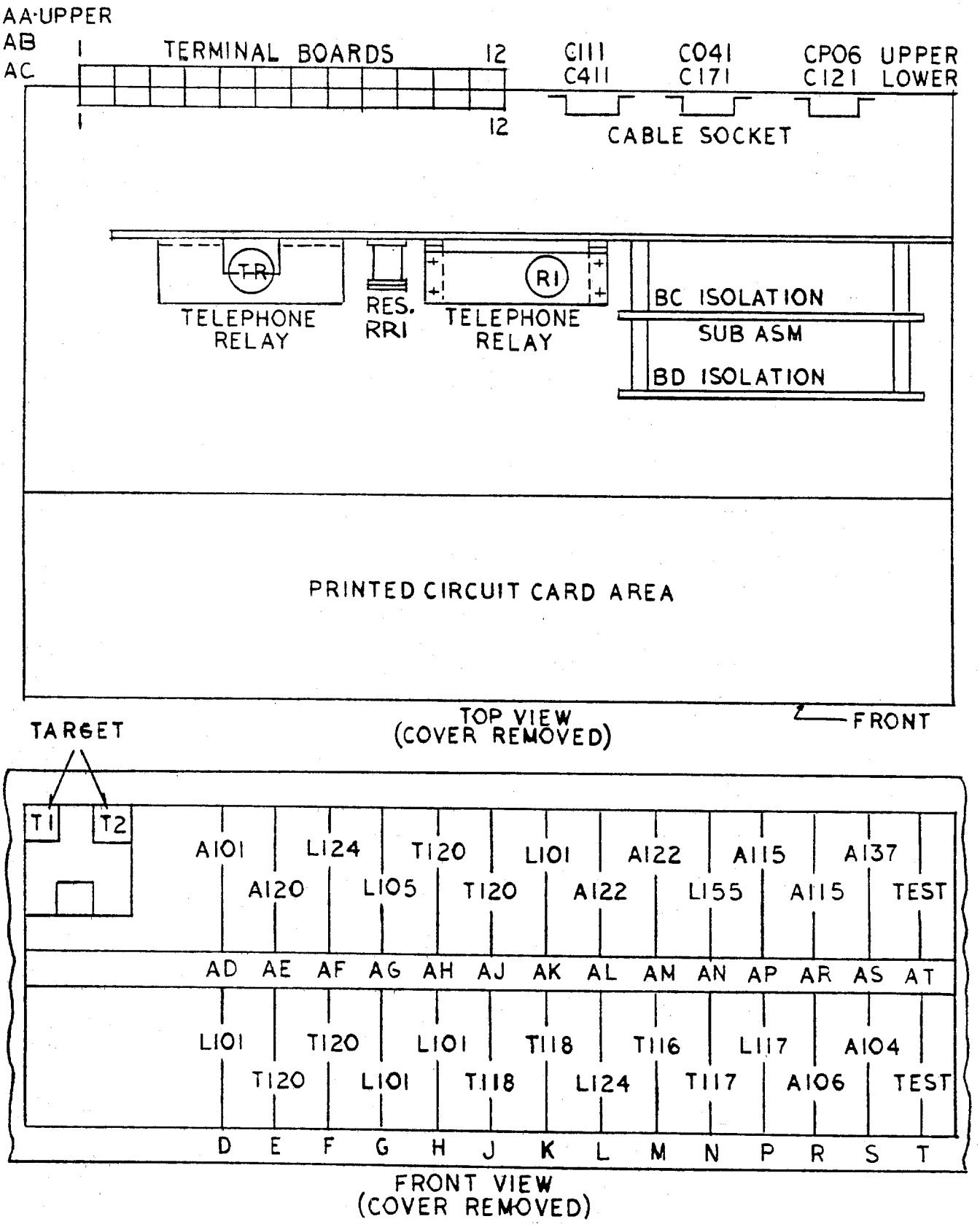


Fig. 3 (0285A5853-0) Component Location Diagram for the Type SLAT61K Relay

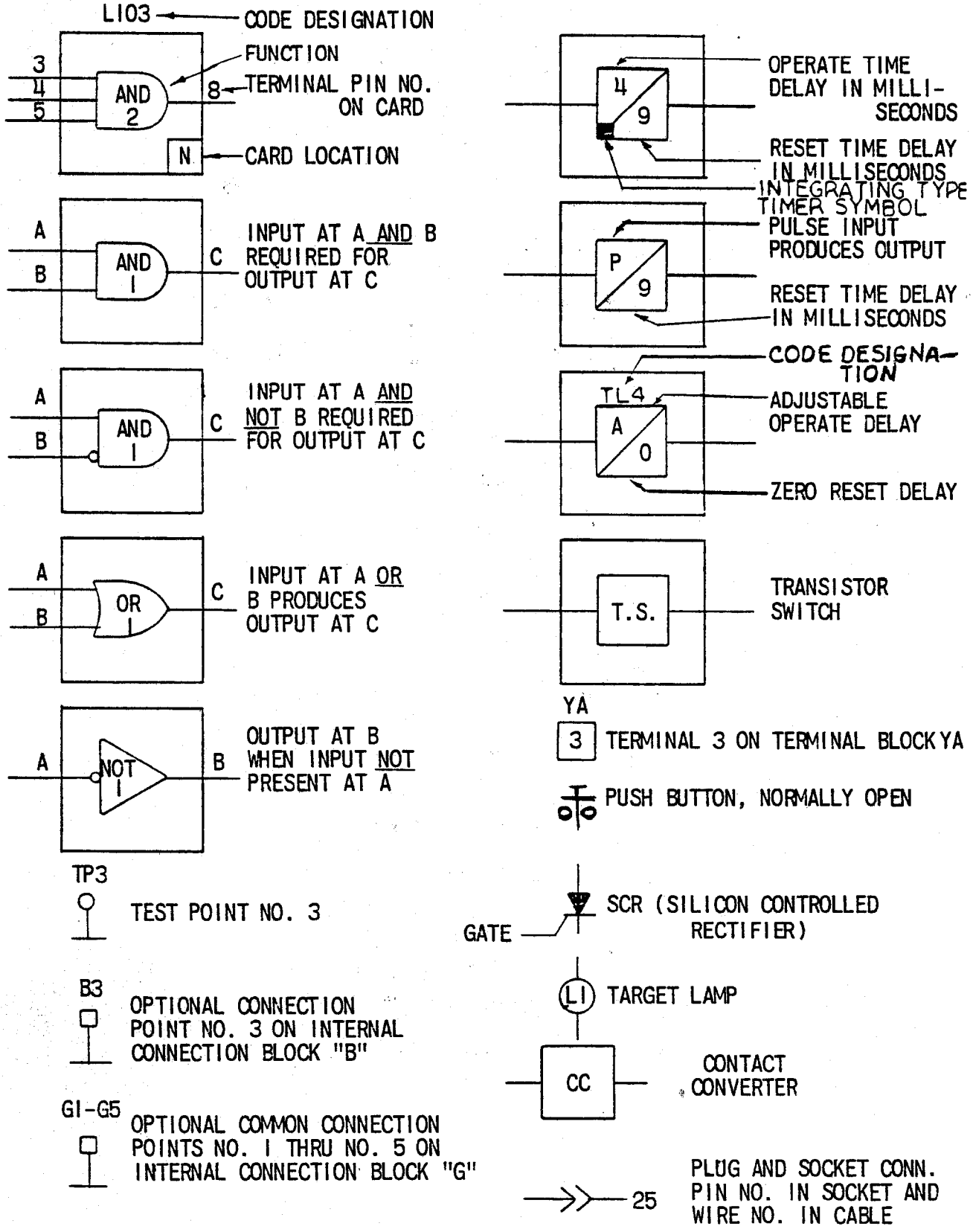


Fig. 4 (0227A2047-1) Logic and Internal Connection Diagram Legend

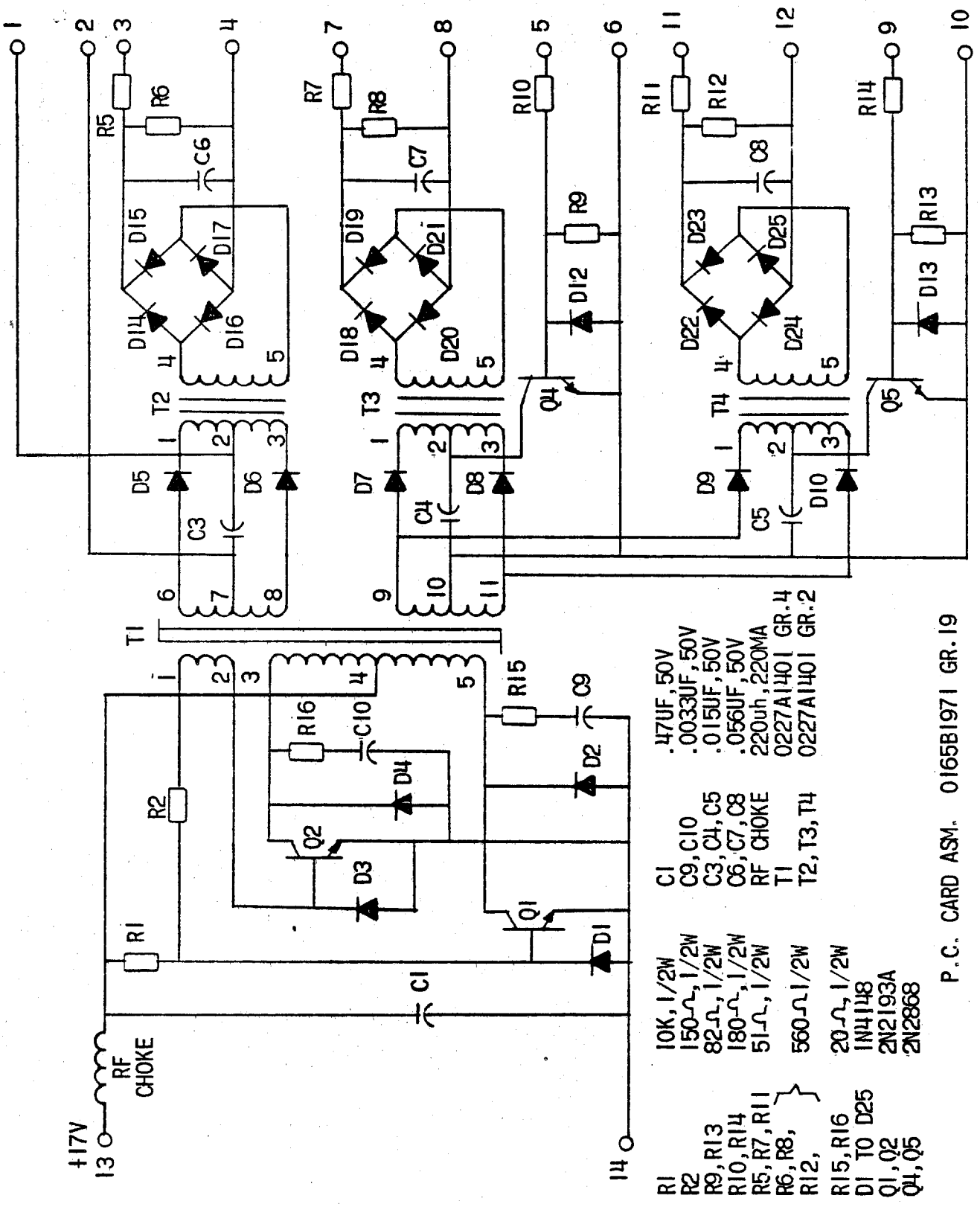
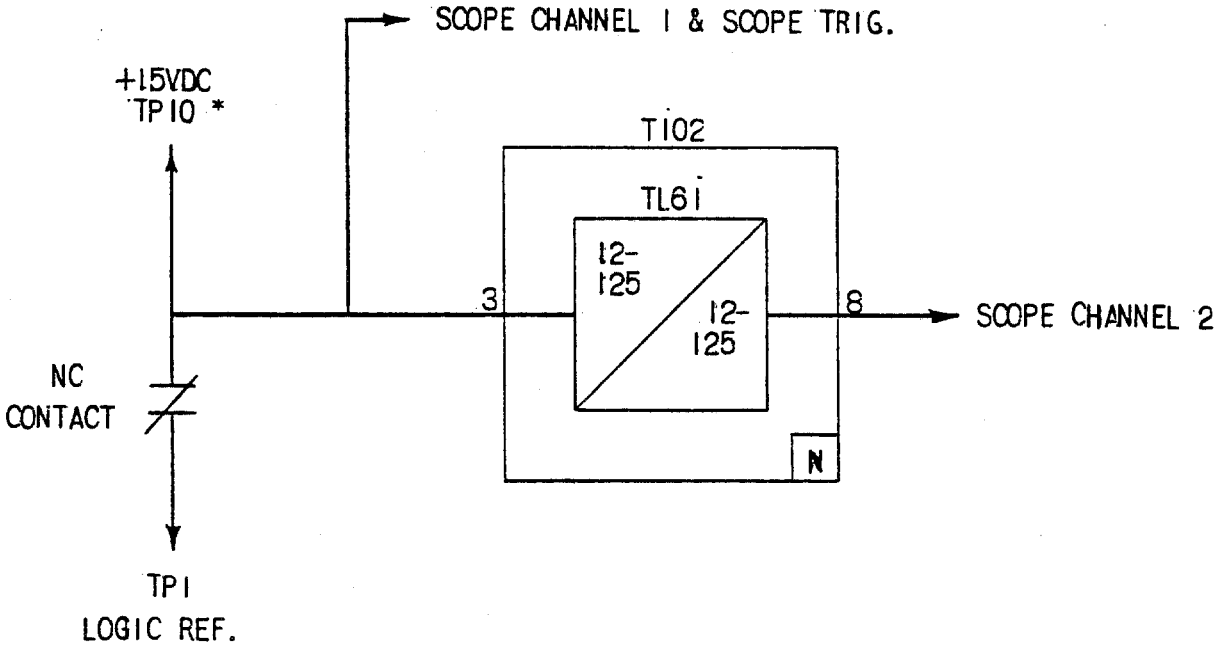


Fig. 5 (0208A5504AR-0) Isolation Interface Circuit Internal



* THE 15VDC SIGNAL AT PIN 10 HAS A CURRENT LIMITING RESISTOR MOUNTED ON THE TEST CARD.

Fig. 6 (0246A7987-0) Logic Timer Test Circuit

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