



INSTRUCTIONS

GEK-65688

STATIC OUTPUT AND TRIPPING UNIT

TYPE SLAT53J

GENERAL  **ELECTRIC**

CONTENTS

	<u>PAGE</u>
DESCRIPTION	3
APPLICATION	3
RATINGS	4
BURDENS	4
FUNCTIONS	4
SCR TRIP CIRCUIT	4
RI RECLOSE INITIATE CIRCUIT	5
BFI BREAKER FAILURE INITIATE CIRCUIT	5
OPTIONAL OUTPUTS	5
TARGETS	5
LOGIC CIRCUITS	5
CALCULATION OF SETTINGS	6
CONSTRUCTION	6
RECEIVING, HANDLING AND STORAGE	7
TEST INSTRUCTIONS	7
CAUTION	7
GENERAL	7
OPERATIONAL CHECKS	8
TEST CARD ADAPTER	8
TIMER ADJUSTMENTS AND TESTS	8
TRIP CIRCUIT TESTS	8
OVERALL EQUIPMENT TESTS	9
MAINTENANCE	9
PERIODIC TESTS	9
TROUBLESHOOTING	9
SPARE PARTS	10

STATIC OUTPUT AND TRIPPING UNIT

TYPE SLAT53J

DESCRIPTION

The Type SLAT53J relay is a static output and tripping unit. The relay is not intended to be used by itself, but rather as part of a complement of equipment that forms a protective relaying scheme. For a complete description of the overall scheme in which this relay is employed, refer to the overall logic diagram and the associated logic description that is supplied with each terminal of equipment.

The Type SLAT53J relay is packaged in a four-rack unit (one rack unit equals 1-3/4 inches) enclosed metal case suitable for mounting on a 19-inch rack. The outline and mounting dimensions are shown in Fig. 1. The internal connections for the relay are shown in Fig. 2. The component and card locations are shown in Fig. 3.

APPLICATION

The Type SLAT53J relay was originally designed to operate in a directional comparison scheme with a pilot channel. The following is a list of the various output functions included in the relay, together with a general description of their intended use.

- SCR - Two silicon controlled rectifier trip circuits are provided to permit tripping of associated circuit breakers.
- TR1, TR2 - Two normally open contacts are provided for TR1 and TR2. They are furnished to initiate automatic reclosing after a high speed trip-out.
- RR36, RR38 - Two normally open contacts are provided for TS36 and TS38. They are primarily intended for keying transistors.
- RR37, RR39 - Two normally open contacts are provided for TS37 and TS39. They are furnished for breaker failure protection.
- RR40 - Two normally closed contacts are provided for RR40.

If any of these functions are not required, the outputs may be used for whatever purposes their characteristics are suited. All of these functions may not be included in all applications. Refer to the overall logic diagram supplied with each terminal to determine which functions have been included.

These instructions do not purport to cover all details or variations in equipment nor to provide for every possible contingency to be met in connection with installation, operation or maintenance. Should further information be desired or should particular problems arise which are not covered sufficiently for the purchaser's purposes, the matter should be referred to the General Electric Company.

To the extent required the products described herein meet applicable ANSI, IEEE and NEMA standards; but no such assurance is given with respect to local codes and ordinances because they vary greatly.

RATINGS

The Type SLAT53J relay is designed for use in an environment where the air temperature outside the relay case does not exceed minus 20°C and plus 65°C.

The Type SLAT53J relay requires a plus or minus 15 volt DC power source which can be obtained from a Type SSA power supply.

The SCR tripping circuits are rated for 48/125 or 250 volts DC. Each has a 1.0 ampere series target. The tripping circuits are designed to carry 30 amperes for one second.

The contacts of the telephone-type relays that are used for TR1 and TR2 will make and carry three amperes continuously, and will interrupt up to 0.5 ampere (inductive) at 125 volts DC, or 0.25 ampere (inductive) at 250 volts DC.

The contacts of the reed relays designated RR37 and RR39 are rated for 100 watts direct current. They will make and carry 3.0 amperes continuously.

The contacts of the reed relays that are designated RR36, RR38 and RR40 are rated for ten volt-amperes. They will carry 0.5 ampere (resistive) continuously.

Refer to the unit nameplate for the ratings of a particular relay.

BURDENS

The SLAT53J relay presents a maximum burden to the Type SSA power supply of:

450 milliamperes from the plus 15 volt DC supply
720 milliamperes from the minus 15 volt DC supply

In addition, each target lamp draws 80 milliamperes from the minus 15 volt DC power supply.

FUNCTIONS

SCR TRIP CIRCUIT

Two electrically separate, isolated SCR trip circuits are provided to trip two breakers. Each circuit is capable of carrying 30 amperes for one second.

The internal connections for the SCR trip and isolation subassemblies are shown in Fig. 4. The isolation card, by means of a DC-to-DC converter, provides a signal path but maintains metallic isolation. This feature makes it possible to isolate the relay power supply from the trip circuit power supply.

RI RECLOSE INITIATE CIRCUIT

Two electrically separate, normally open contacts are provided. These contacts close within 17 milliseconds from the time the associated coil is energized by the logic. These contacts open within 170 milliseconds from the time the coil is de-energized. The RI function uses a telephone-type relay with contact ratings stated under **RATINGS**.

BFI BREAKER FAILURE INITIATE CIRCUIT

Two electrically separate, normally open contacts are provided. These contacts close within two milliseconds from the time the associated coil is energized by the logic. These contacts open within two milliseconds from the time the coil is de-energized. The BFI function uses a reed relay with contact ratings stated under **RATINGS**.

OPTIONAL OUTPUTS

Additional outputs are furnished and may be used for any purpose required. Refer to the logic diagram for the specific purpose that the output function may be used.

TARGETS

Two electromechanical target coils are included, one in series with each output contact. These targets operate on one ampere of trip current. The trip circuit resistance in the relay is 0.35 ohm.

Nine target lamps are included in the SLAT53J. These are designated as indicated on the internal connection diagram of Fig. 2. An output from TL31 will prevent the target lamps from turning on. A long pickup setting on this timer will permit all functions that operate to light their associated lamps. A short time setting will allow only those functions that operate initially to be indicated.

LOGIC CIRCUITS

The functions of the Type SLAT53J involve basic logic (AND, OR, and NOT) where the presence or absence of signals, rather than their magnitude, controls the operation. Signals are measured with respect to a reference bus accessible at TP1. In general, a signal below one volt DC represents an OFF or LOGIC ZERO condition; an ON or LOGIC ONE state is represented by a signal of approximately plus 15 volts DC.

The symbols used on the internal connection diagram (Fig. 2) are explained by the legend shown in Fig. 5.

The matrix block options shown in the internal connections of the SLAT53J relay are provided at the factory. The connections are shown on the associated overall logic and are listed on the associated option chart. A sample option chart for the Type SLAT53J relay is shown in Fig. 6.

CALCULATION OF SETTINGS

There are two timer functions in the SLAT53J that require field adjustment.

The 5-30/40 timer enables the user to control the number of lamps that will light under certain fault conditions. With a short pickup setting (5-10 milliseconds) only lamp(s) associated with those units which first sensed the fault will light. Increased pickup settings will cause the lamps associated with all units that operate to light. The timer setting should not exceed the minimum breaker clearing time in order to avoid targets which may result from breaker unequal pole opening times.

The P/25-200 timer insures an adequate duration of the transfer trip signal for dependable tripping at the remote terminal. A setting of six cycles is suggested. This allows a total duration of approximately eight cycles, if two-cycle breakers are used. However, if the channel is also used for direct transfer trip protection of shunt reactors and the line is equipped with reclosing, the lock-out of the remote terminal should be delayed until the line protection transfer trip has reset. In this case, the reset delay on P/25-200 should be set to coordinate with the timer, which delays lock-out of the remote terminal on shunt reactor faults.

CONSTRUCTION

The SLAT53J relay is packaged in an enclosed metal case with hinged front cover and removable top cover. The outline and mounting dimensions of the case and the physical location of the components are shown in Fig. 1 and 3, respectively.

The SLAT53J relay contains printed circuit cards identified by a code number, such as A110, T114, L102; where A designates an auxiliary function, T designates a time-delay function, and L designates a logic function. The printed circuit cards plug in from the front of the unit. The sockets are marked with letter designations or "addresses" (D, E, F, etc.) which appear on the guide strips in front of each socket, on the component location drawing, on the unit internal connection diagram, and on the printed circuit card. The test points (TP1, TP2, etc.) shown on the internal connection diagram are connected to instrument jacks on a test card in position T or AT with TP1 at the top of the AT card. TP1 and TP11 are tied to reference; TP10 and TP20 are tied to plus 15 volts DC through a 1.5K resistor. This resistor limits the current when TP10 or TP20 is used to supply a logic signal to a card.

The SLAT53J relay receives its inputs from the associated Type SLA relay. These units are interconnected by ten conductor shielded cables. The sockets for these cables are located on the rear panel of the unit. The SLAT53J output functions are connected to 12-point terminal strips, which are also located on the rear of the unit.

A window is provided in the hinged cover of the relay to allow target lamps and the mechanical targets to be seen. Push buttons are also provided to reset the targets and lamps without opening the cover.

RECEIVING, HANDLING AND STORAGE

The SLAT53J relay will normally be supplied as part of a static relay equipment, mounted in a rack or cabinet with other static relays and test equipment. Immediately upon receipt of a static relay equipment, it should be unpacked and examined for any damage sustained in transit. If injury or damage resulting from rough handling is evident, file a damage claim at once with the transportation company and promptly notify the nearest General Electric Sales Office.

Reasonable care should be exercised in unpacking the equipment. If the equipment is not to be installed immediately, it should be stored indoors in a location that is free from moisture, dust, metallic chips, and severe atmospheric contaminants.

Just prior to final installation the shipping support bolt should be removed from each side of all relay units, to facilitate possible future unit removal for maintenance. These shipping support bolts are approximately eight inches back from the relay front panel. STATIC RELAY EQUIPMENT, WHEN SUPPLIED IN SWING RACK CABINETS, SHOULD BE SECURELY ANCHORED TO THE FLOOR OR TO THE SHIPPING PALLET TO PREVENT THE EQUIPMENT FROM TIPPING OVER WHEN THE SWING RACK IS OPENED.

TEST INSTRUCTIONS

CAUTION

If the SLAT53J relay that is to be tested is installed in an equipment which has already been connected to the power system, disconnect the outputs to the system during test.

THE LOGIC SYSTEM SIDE OF THE DC POWER SUPPLY USED WITH MOD III STATIC RELAY EQUIPMENT IS ISOLATED FROM GROUND. IT IS A DESIGN CHARACTERISTIC OF MOST ELECTRONIC INSTRUMENTS THAT ONE OF THE SIGNAL INPUT TERMINALS IS CONNECTED TO THE INSTRUMENT CHASSIS. IF THE INSTRUMENT USED TO TEST THE RELAY EQUIPMENT IS ISOLATED FROM GROUND, ITS CHASSIS MAY HAVE AN ELECTRICAL POTENTIAL WITH RESPECT TO GROUND. THE USE OF A TEST INSTRUMENT WITH A GROUNDED CHASSIS WILL NOT AFFECT THE TESTING OF THE EQUIPMENT. HOWEVER, A SECOND GROUND CONNECTION TO THE EQUIPMENT, SUCH AS A TEST LEAD INADVERTENTLY DROPPING AGAINST THE RELAY CASE, MAY CAUSE DAMAGE TO THE LOGIC CIRCUITRY. NO EXTERNAL TEST EQUIPMENT SHOULD BE LEFT CONNECTED TO THE STATIC RELAYS WHEN THEY ARE IN PROTECTIVE SERVICE, SINCE TEST EQUIPMENT GROUNDING REDUCES THE EFFECTIVENESS OF THE ISOLATION PROVIDED.

GENERAL

The SLAT53J relay is supplied from the factory either mounted in a static relay equipment or as a separate unit associated with measuring relays, a Type SSA power supply, and some form of channel equipment. All relay units for a given terminal of static relaying equipment are tested together at the factory, and each unit will have the same summary number stamped on its nameplate.

Timers should be set for the operating or reset times indicated on the associated overall logic diagram. Where a time range is indicated on the overall logic diagram, the timer should be set for the value recommended for that function in the descriptive write-up accompanying the overall logic diagram. Where a setting depends upon conditions encountered on a specific application, this is so stated and the factors influencing the choice of setting are described. The procedure for checking and setting the timers is described in a later section.

OPERATIONAL CHECKS

Operation of the SLAT53J unit can be checked by observing the signals at the twenty test points (TP1 to TP20) in the SLAT53J, by observing the operation of the associated channel equipment; or by observing the output functions. The test points are located on the test card in positions T and AT, and are numbered 1 to 20 from top to bottom. TP1 is the reference bus for the logic circuit; TP10 is at plus 15 volts DC. The remaining points are located at various strategic points throughout the logic as shown on the internal connection diagram (Fig. 2). Test point voltages can be monitored with a portable high impedance voltmeter, the voltmeter on the test panel of the associated equipment, or an oscilloscope.

TEST CARD ADAPTER

The test card adapter provides a convenient means of gaining access to any pin of a particular card. Detailed information on the use of the test adapter card is included in the card instruction book, GEK-34158.

TIMER ADJUSTMENTS AND TESTS

When the time-delay cards are to be adjusted or checked, an oscilloscope that can display two traces simultaneously, and that has a calibrated horizontal sweep, should be used.

In order to test the timer cards it is necessary to remove the card which supplied the input to the timer, and to place the timer card in a card adapter. The card adapter allows access to the input and output of the timer if they are not brought out on test points. The timer test circuit is shown in Fig. 7. Opening the normally closed contact causes the output to step up to plus 15 volts DC after the pickup delay of the timer. To increase the pickup time, turn the upper potentiometer on the timer card clockwise; to decrease the time, turn it counterclockwise. Closing the contact causes the timer output to drop out after the reset time-delay setting of the card. If the timer card is provided with a variable reset delay, it can be adjusted by the lower potentiometer on the timer card (clockwise increases reset time).

TRIP CIRCUIT TESTS

The SCR trip circuits and series mechanical targets may be checked by connecting an auxiliary lock-out relay, such as the Type HEA relay, in series with the SCR circuit. A typical circuit is shown in Fig. 8. The HEA relay should have the same DC rating as the SCR trip circuit of the SLAT53J. If an auxiliary lock-out relay is not

available, it can be replaced by a resistive load which limits the trip circuit current to three amperes. In most equipments, the SCR circuit can be gated by operating a test push button in the associated units.

Prior to final installation, a check of the overall trip circuit should be made with the SCR outputs connected to trip the circuit breakers.

OVERALL EQUIPMENT TESTS

After the SLAT53J relay and the associated static relay units have been individually calibrated and tested for the desired settings, a series of overall operating circuit checks is advisable.

The elementary, overall logic and logic description for the specific terminal will be useful for determining the overall operation of the scheme.

Overall equipment tests can be performed by applying alternating current and voltages to the measuring units as specified in the instruction book for the measuring units and checking that proper outputs are obtained when the measuring units operate.

MAINTENANCE

PERIODIC TESTS

It should be sufficient to check the outputs produced at test points in the SLAT53J when periodic calibration tests are made on the associated measuring units, for example, the phase and ground relays in a line relaying scheme. No separate periodic tests on the SLAT53J itself should be required.

TROUBLESHOOTING

In any troubleshooting of equipment, it should first be established which unit is functioning incorrectly. The overall logic diagram supplied with the equipment shows the combined logic of the complete equipment and the various test points in each unit. By signal tracing, using the overall logic diagram and the various test points, it should be possible to quickly isolate the trouble.

A test adapter card is supplied with each static relay equipment to supplement the prewired test points on the test cards. Use of the adapter card is described in the card instruction book, GEK-34158.

A dual-trace oscilloscope is a valuable aid to detailed troubleshooting, since it can be used to determine phase shift, operate and reset times, as well as input and output levels. A portable dual-trace oscilloscope with a calibrated sweep and trigger facility is recommended.

SPARE PARTS

To minimize possible outage time, it is recommended that a complete maintenance program should include the stocking of a least one spare card of each type. It is possible to replace damaged or defective components on the printed circuit cards, but great care should be taken in soldering so as not to damage or bridge-over the printed circuit buses, or overheat the semiconductor components. The repaired area should be recovered with a suitable high-dielectric plastic coating to prevent possible breakdowns across the printed buses due to moisture and dust. The wiring diagrams for the cards in the SLAT53J relay are included in the card instruction book, GEK-34158.

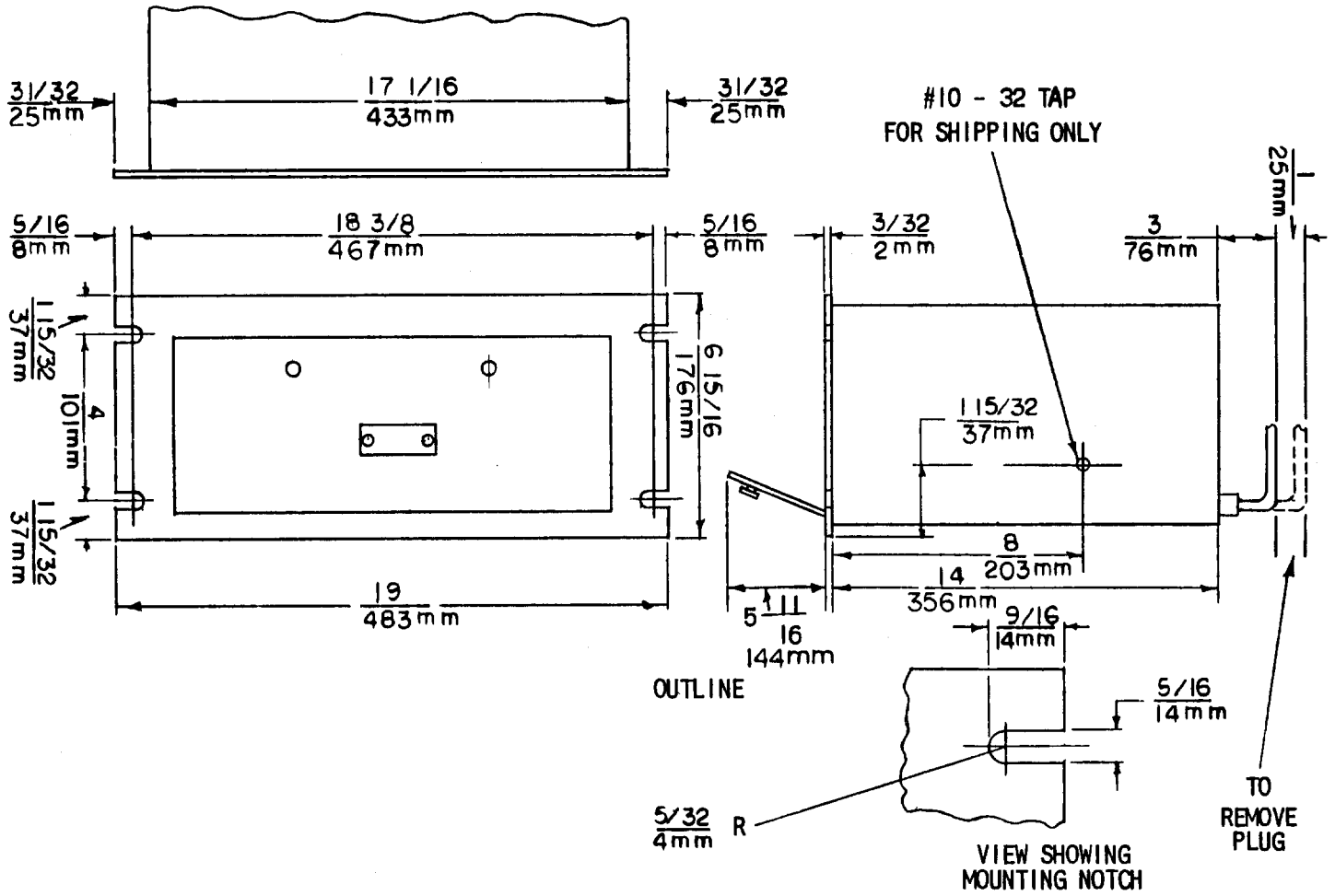


Fig. 1 (0227A2037-0) Outline and Mounting Dimensions for the Type SLAT53J Relay

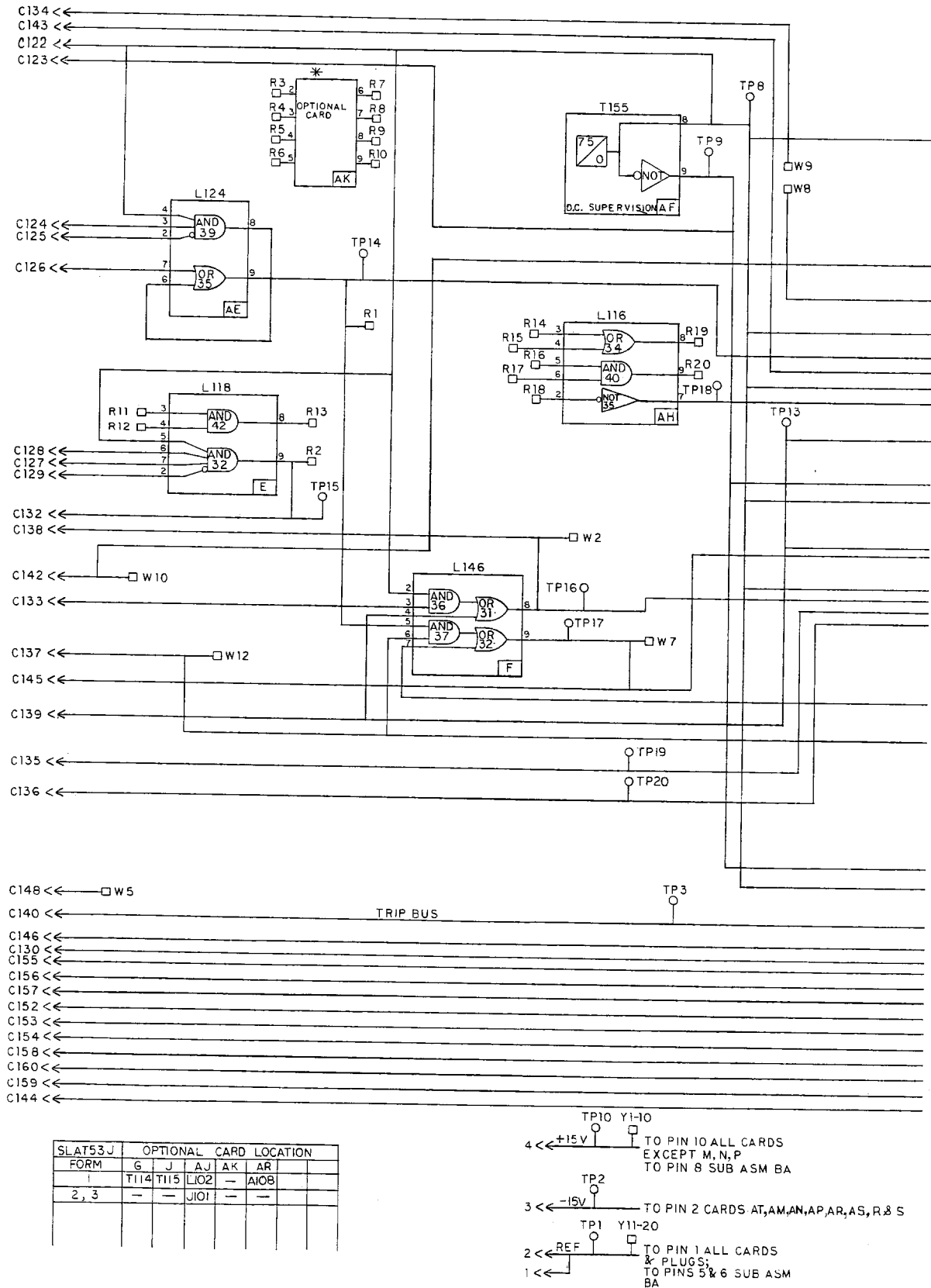
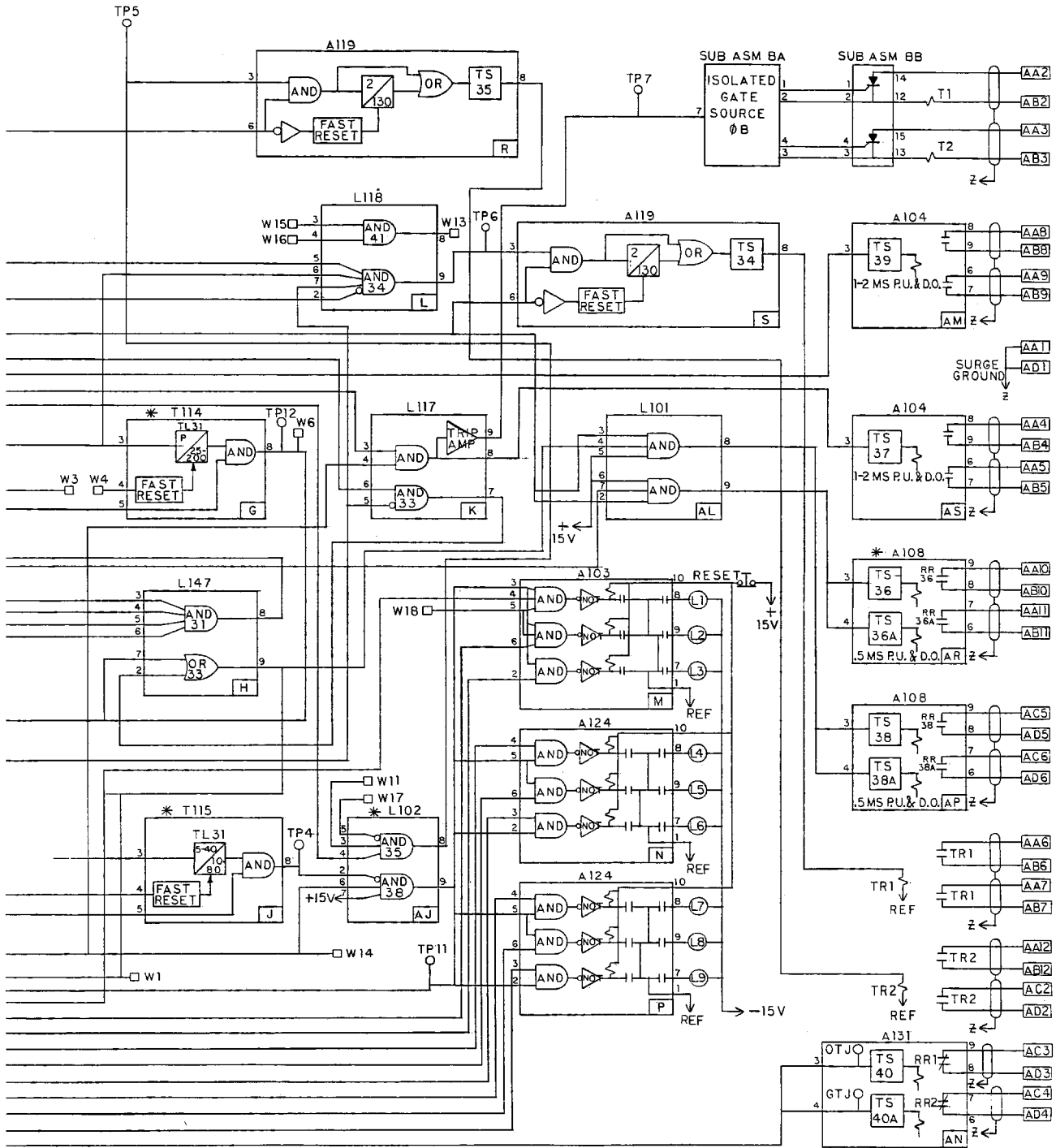


Fig. 2A (0145D8630-0) Internal Connection Diagram for the Type SLAT53J Relay

GEK-65688



- NOTES:
1. FOR MATRIX CONNECTIONS SUPPLIED ON A PARTICULAR EQUIPMENT REFER TO THE OVERALL LOGIC DIAGRAM AND OPTION CHART
 2. "R" REPRESENTS RED MATRIX BLOCK
 "Y" " " " YELLOW " " "
 "W" " " " WHITE " " "
 3. WHEN J101 CARD IS USED IN POSITION AJ JUMPER PIN 5 TO 8 AND PIN 6 TO 9

Fig. 2B (0145D8630-0) Internal Connection Diagram for the Type SLAT53J Relay

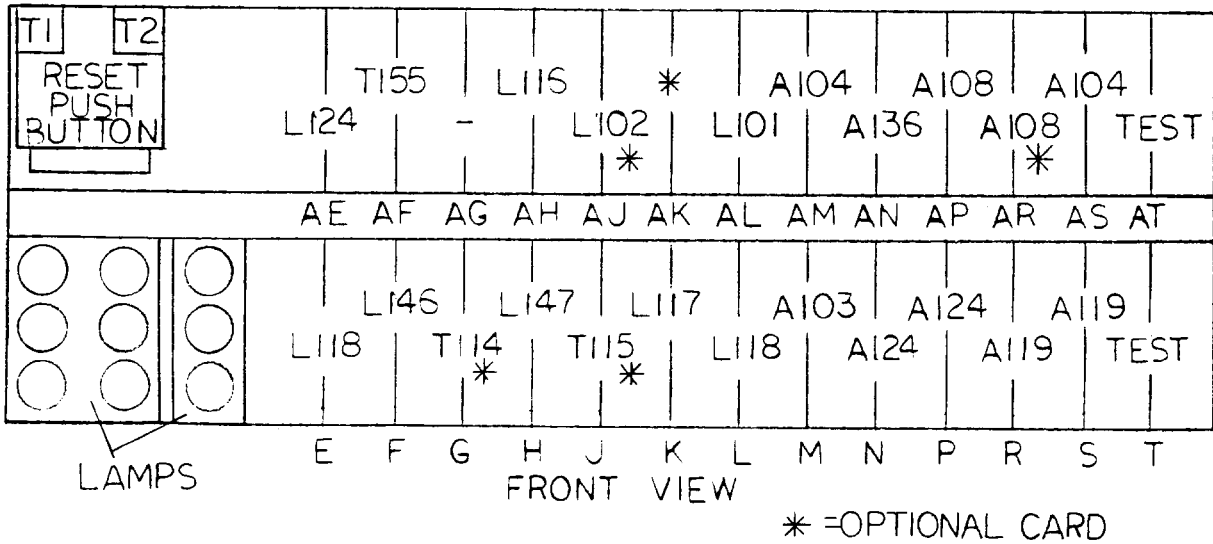
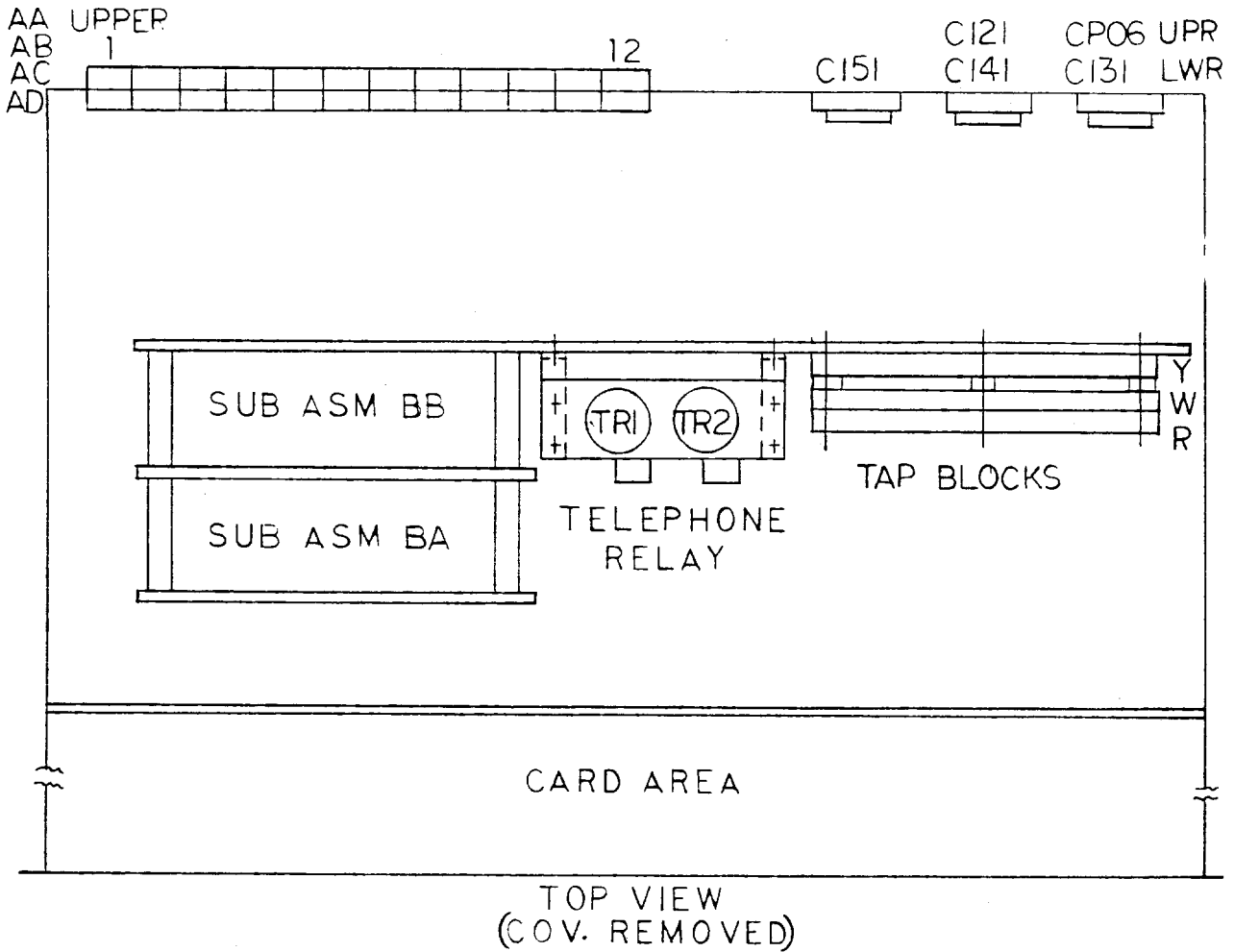


Fig. 3 (0285A6106-0) Component Location Diagram for the Type SLAT53J Relay

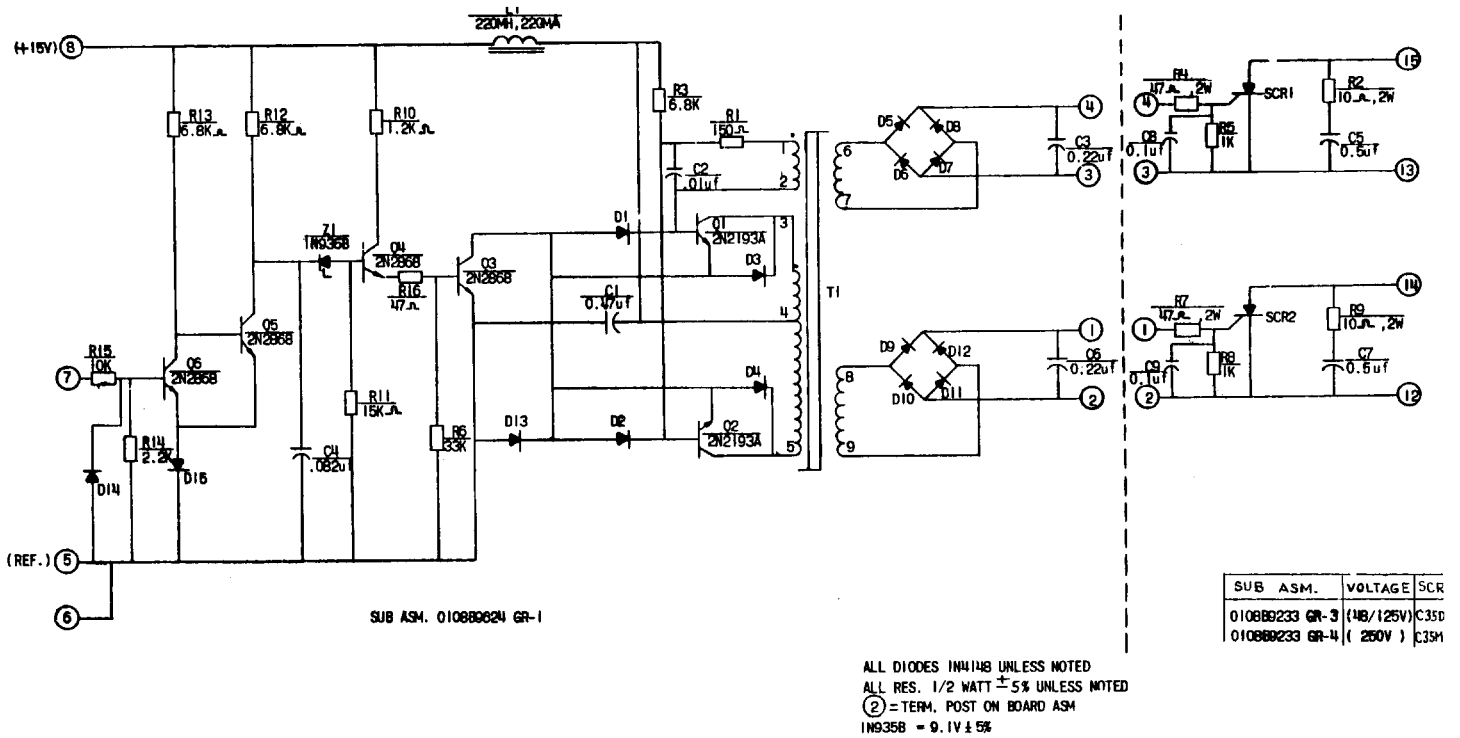


Fig. 4 (0108B9610-0) Internal Connections for SCR Trip and Isolation Subassemblies

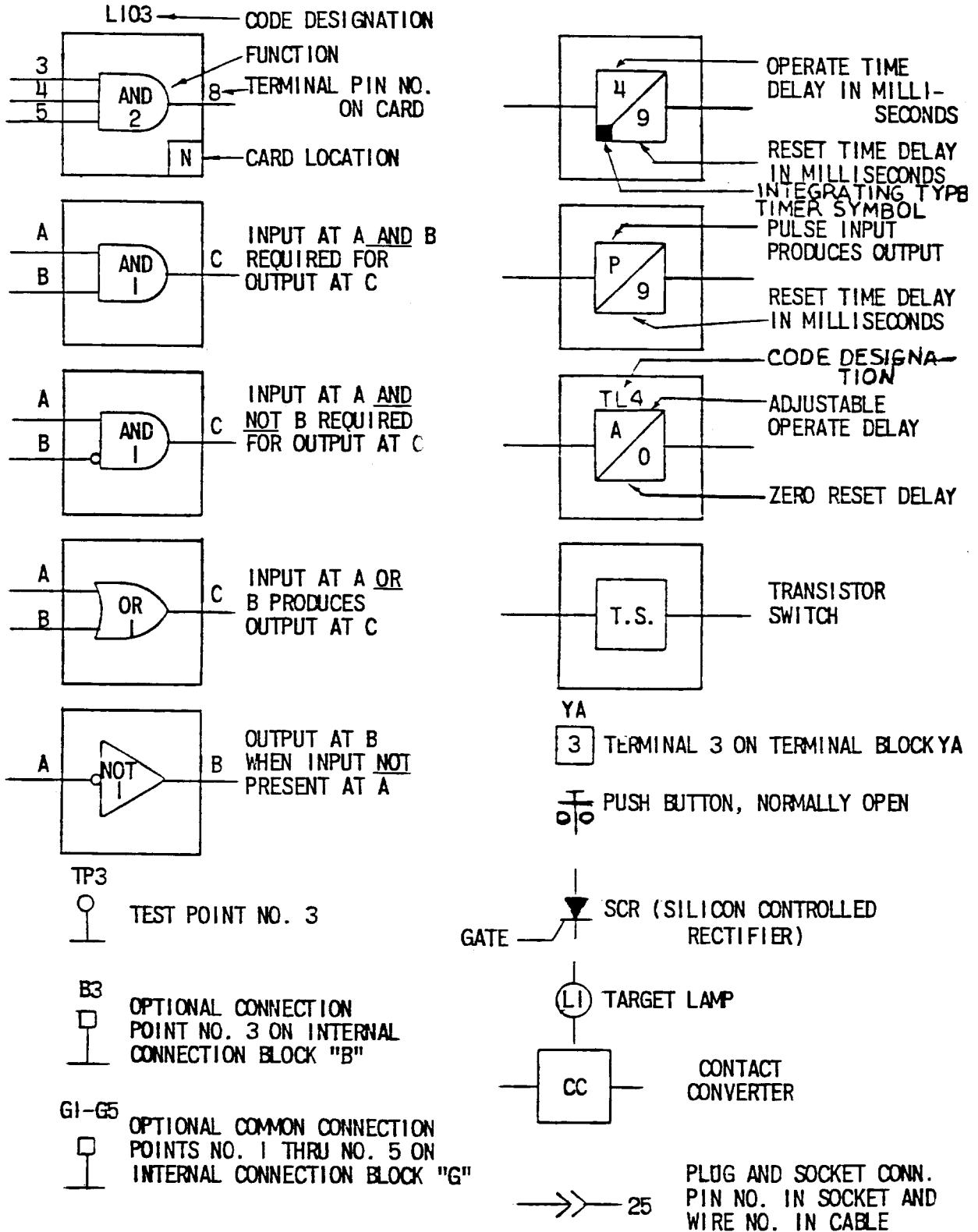


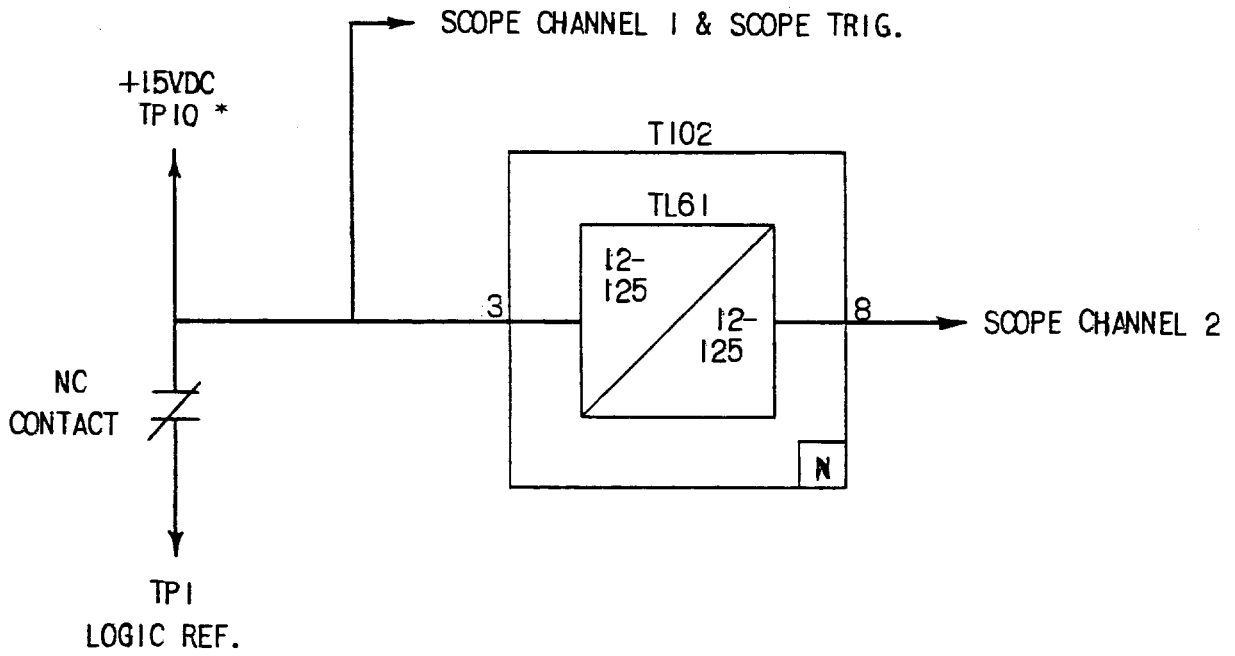
Fig. 5 (0227A2047-1) Internal Connection Diagram Legend

THE FOLLOWING ARE FACTORY CONNECTIONS MADE AT THE MATRIX BLOCKS
 INSIDE OF THE SLA RELAY ASSOCIATED WITH THIS EQUIPMENT.
 SYMBOLS LISTED: PL=RELAY INTERCONNECTING CABLE LEAD
 (5)=LOGIC FUNCTION CARD PIN NUMBER
 ‡=3-WAY CONNECTION
 *X=DLA MONITOR CONNECTION AVAILABLE BUT NOT USED

255

MATRIX BLOCK JUMPERS		LOGIC FUNCTION		MATRIX BLOCK JUMPERS		LOGIC FUNCTION	
FROM	TO	FROM	TO	FROM	TO	FROM	TO
R1	W1	OR35(9)	TS38(3)				
#R2	W17	AND37(9)	TS35(3)				
#R2	R14	AND32(9)	OR32(3)				
W10	Y1	AND34(5)	+15V				
W9	R15	AND7(8)	OR34(4)				
R19	W8	OR34(8)	AND34(2)				
W5	W18	AND16(9)	L1(5)				

Fig. 6 (0227A2050-1, Sh. 255) Sample Option Chart for Type SLAT53J Relay



* THE 15VDC SIGNAL AT PIN 10 HAS A CURRENT LIMITING RESISTOR MOUNTED ON THE TEST CARD.

Fig. 7 (0246A7987-0) Logic Timer Test Circuit

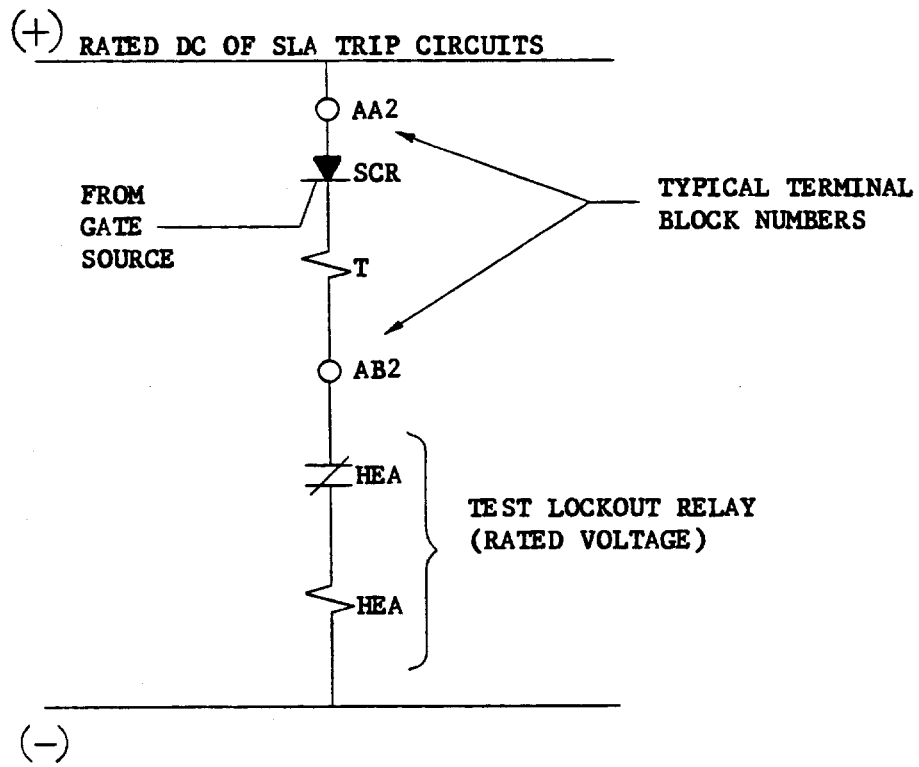


Fig. 8 (0208A2365-0) Typical SCR Trip Circuit Test Connections

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