INSTRUCTIONS

GEK-86045

AUXILIARY LOGIC AND TRIPPING UNIT

TYPE SLAT61L

GENERAL ELECTRIC

CONTENTS

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DESCRIPTION

The SLAT61L relay is a static logic, output and tripping unit intended for application in phase comparison schemes utilizing an ON-OFF blocking carrier channel. In addition to the SLAT61L relay, the appropriate phase comparison measuring unit, a power supply and the appropriate ON-OFF channel equipment are required to complete a particular relaying scheme.

The outputs of the SLAT61L include two electrically separate tripping contacts, each with an electromechanical target; two electrically separate reclose initiating contacts (RI); and two electrically separate breaker failure timer initiating contacts (BFI). The inputs to the SLAT61L are from the associated relays and channel equipment, and two contact converters that may be energized by external contacts, one to stop all carrier transmission, and one to start carrier.

The relay is packaged in a two-rack unit enclosed metal case suitable for mounting on a 19-inch rack. The outline and mounting dimensions are shown in Fig. 1, the internal connections in Fig. 2, and the card and component locations in Fig. 3.

APPLICATION

The SLAT61L relay is designed to operate in conjunction with appropriate phase comparison measuring units and an ON-OFF carrier equipment in a phase comparison blocking scheme.

There are nine points which may be monitored from a data monitoring plug on the rear of the SLAT61L relay. These points are indicated in Fig. 2. If these points are to be monitored, a separate data logging amplifier (DLA) is required.

There are no measuring functions to be set in the SLAT61L, but two timers are included that require field adjustment. These are the symmetry adjustment and the phase-delay adjustment. Refer to the section on **CALCULATION OF SETTINGS** for a discussion of the required settings.

The BFI contacts are reed relay contacts and are not suitable for use in trip circuits. Refer to the section on **RATINGS** for contact duty capability.

For a complete description of the overall scheme in which the relay is to be used, refer to the overall logic diagram and its associated logic description, which is supplied with each terminal of equipment.

RATINGS

The Type SLAT61L relay is designed for use in an environment where the air temperature outside the relay case does not exceed minus 20°C and plus 65°C.

The Type SLAT61L relay requires a plus or minus 15 volt DC power source which can be obtained from a Type SSA power supply.

Each trip circuit consists of a dry contact and a 1.0 ampere series target. The tripping circuits are designed to carry 30 amperes for one second.

The contacts of the telephone type relays that are used for RI will make and carry three amperes continuously and will interrupt up to 0.5 ampere (inductive) at 125 volts DC or up to 0.25 ampere (inductive) at 250 volts DC.

The contacts of the reed relays that are used for BFI are rated for 100 watts DC. They will make and carry three amperes continuously.

Refer to the unit nameplate for the ratings of a particular relay.

BURDENS

The SLAT61L relay presents a maximum burden to the Type SSA power supply of:

200 milliamperes (standby), 280 milliamperes (operated)
from the plus 15 volt DC supply
10 milliamperes (standby), 125 milliamperes (operated)
from the minus 15 volt DC supply

Each contact converter, when energized, will draw approximately ten milliamperes from the station battery, regardless of tap setting.

FUNCTIONS

TRIP CIRCUIT

Two electrically separate, isolated tripping contacts are provided to trip two breakers. Each circuit is capable of carrying 30 amperes for one second.

RI RECLOSE INITIATE CIRCUIT

Two electrically separate, normally open contacts are provided. These contacts close within 17 milliseconds from the time the associated coil is energized by the logic. The contacts open within 170 milliseconds from the time the coil is de-energized. The RI function uses a telephone-type relay with contact ratings stated under **RATINGS.**

3FI BREAKER FAILURE INITIATE CIRCUIT

Two electrically separate, normally open contacts are provided. These contacts close within two milliseconds from the time the associated coil is energized by the logic. These contacts open within two milliseconds from the time the coil is de-energized. The BFI function uses a reed relay with contact ratings stated under **RATINGS.**

CONTACT CONVERTERS

The purpose of this function is to convert a contact operation into a signal that is compatible with the logic circuit of the Type SLAT61L relay. The contact converters are labeled CC41 and CC42. They have a non-adjustable, four millisecond pickup delay.

CC41

Contact converter CC41 is energized by an external contact to stop carrier transmission.

CC42

Contact converter CC42 is energized by an external contact to start carrier.

CHANNEL INTERFACE

The logic of the Type SLAT61L relay includes an isolation interface (Fig. 5) between the relays in the scheme and the associated channel. The circuitry of the isolation interface provides a signal path, but maintains metallic isolation. This feature makes it possible to maintain isolation between the DC supply used for the relays and that employed by the channel.

When pins 9 and 10 are both connected to relay reference, a metallically separate positive logic signal appears at pin 11 with respect to pin 12. The output from the isolation interface is a five volt DC, 20 milliampere signal.

CALCULATION OF SETTINGS

The SLAT61L contains five timers. Three of the timers are factory set and do not generally need field adjustment. The two timers that require field adjustment are the symmetry and phase-delay timers. The symmetry adjustment should be set first. However, before either setting is made, the communication equipment should be completely tested and have its final settings made.

SYMMETRY ADJUSTMENT

This 0-3/0 timer is included to compensate for any asymmetry that may exist in the pickup and drop-out of the channel equipment. The purpose of this setting is to assure that the near-end comparer receives equal on-and-off half cycles when the transmitter at the remote end is keyed for equal on-and-off half cycles. See the section titled, SYMMETRY AND PHASE-DELAY TIMER ADJUSTMENTS, for instructions for making this setting in the field.

PHASE DELAY ADJUSTMENT

This 1-8/1-8 timer is intended to delay the local input to the comparer by exactly the same amount of time that it takes for the remote signal to arrive. This time is equal to the channel delay in the communication equipment plus the propagation time of the signal. This setting should be made after the symmetry adjustment setting discussed above.

Because both the above timer settings are affected by service conditions, the settings cannot be made at the factory. For instructions relating to the method of adjustment, see the SYMMETRY AND PHASE-DELAY TIMER ADJUSTMENTS section of this book.

DATA MONITORING POINTS

Data monitoring points are brought out on a plug at the rear of the SLAT61L relay. The plug contains nine monitoring points and reference as shown on the overall logic diagram for the scheme. To monitor these points an additional piece of equipment, termed a data logging amplifier (DLA), is required.

TARGETS

Two electromechanical target coils are included, one in series with each tripping contact. The target operates on one ampere of trip current when the associated contact closes. Each trip circuit resistance in the relay is 0.40 ohm.

LOGIC CIRCUITS

The functions of the Type SLAT61L involve basic logic (AND, OR, NOT) where the presence or absence of signals, rather than their magnitude, controls the operation. Signals are measured with respect to a reference bus accessible at TP1. In general, a signal below one volt DC represents an OFF or LOGIC ZERO condition, an ON or LOGIC ONE is represented by a signal of approximately plus 15 volts DC.

The symbols used on the internal connection diagram (Fig. 2) are explained by the legend shown in Fig. 4.

CONSTRUCTION

The SLAT61L relay is packaged in an enclosed metal case with hinged front cover and removable top cover. The outline and mounting dimensions of the case and the physical location of the components are shown in Fig. 1 and 3, respectively.

The SLAT61L relay contains printed circuit cards identified by a code number, such as A104, T106, L109; where A designates an auxiliary function, T designates a time-delay function, and L designates a logic function. The printed circuit cards plug in from the front of the unit. The sockets are marked with letter designations or "addresses" (D, E, F, etc.) which appear on the guide strips in front of each socket, on

the component location drawing, on the unit internal connection diagram, and on the printed circuit card. The test points (TP1, TP2, etc.) shown on the internal connection diagram are connected to instrument jacks on a test card in position T with TP1 at the top of the T card. TP1 is tied to reference; TP10 is tied to plus 15 volts DC through a 1.5K resistor. This resistor limits the current when TP10 is used to supply a logic signal to a card. Only TP10 should be used to supply logic signals to any card.

The SLAT61L relay receives its inputs from the associated Type SLD relay. These units are interconnected by ten-conductor shielded cables. The sockets for these cables are located on the rear panel of the unit. The SLAT61L output functions are connected to 12-point terminal strips, which are also located on the rear of the unit.

A window is provided in the hinged cover of the relay to allow the mechanical targets to be seen. Push buttons are also provided to reset the targets without opening the cover.

RECEIVING, HANDLING AND STORAGE

These relays will normally be supplied as part of a static relay equipment, mounted in a rack or cabinet with other static relays and test equipment. Immediately upon receipt of a static relay equipment, it should be unpacked and examined for any damage sustained in transit. If injury or damage resulting from rough handling is evident, file a damage claim at once with the transportation company and promptly notify the nearest General Electric Sales Office.

Reasonable care should be exercised in unpacking the equipment. If the equipment is not to be installed immediately, it should be stored indoors in a location that is free from moisture, dust, metallic chips, and severe atmospheric contaminants.

Just prior to final installation the shipping support bolt should be removed from each side of all relay units, to facilitate possible future unit removal for maintenance. These shipping support bolts are approximately eight inches back from the relay front panel. STATIC RELAY EQUIPMENT, WHEN SUPPLIED IN SWING RACK CABINETS, SHOULD BE SECURELY ANCHORED TO THE FLOOR OR TO THE SHIPPING PALLET TO PREVENT THE EQUIPMENT FROM TIPPING OVER WHEN THE SWING RACK IS OPENED.

INSTALLATION TESTS

CAUTION

THE LOGIC SYSTEM SIDE OF THE DC POWER SUPPLY USED WITH MOD III STATIC RELAY EQUIPMENT IS ISOLATED FROM GROUND. IT IS A DESIGN CHARACTERISTIC OF MOST ELECTRONIC INSTRUMENTS THAT ONE OF THE SIGNAL INPUT TERMINALS IS CONNECTED TO THE INSTRUMENT CHASSIS. IF THE INSTRUMENT USED TO TEST THE RELAY EQUIPMENT IS ISOLATED FROM GROUND, ITS CHASSIS MAY HAVE AN ELECTRICAL POTENTIAL WITH RESPECT TO GROUND. THE USE OF A TEST INSTRUMENT WITH A GROUNDED CHASSIS WILL NOT AFFECT THE TESTING OF THE EQUIPMENT. HOWEVER, A SECOND GROUND CONNECTION TO THE EQUIPMENT, SUCH AS A TEST LEAD INADVERTENTLY DROPPING AGAINST THE RELAY CASE, MAY CAUSE DAMAGE TO THE LOGIC CIRCUITRY. NO EXTERNAL TEST EQUIPMENT SHOULD BE LEFT CONNECTED TO THE STATIC RELAYS WHEN THEY ARE IN PROTECTIVE SERVICE, SINCE TEST EQUIPMENT GROUNDING REDUCES THE EFFECTIVENESS OF THE ISOLATION PROVIDED.

GENERAL

If the SLAT61L relay that is to be tested is installed in an equipment which has already been connected to the power system, disconnect the outputs from the system before testing.

The SLAT61L relay is supplied from the factory either mounted in a static relay equipment or as a separate unit associated with measuring relays, a Type SSA power supply, and some form of channel equipment. All relay units for a given terminal of static relaying equipment are tested together at the factory, and each unit will have the same summary number stamped on its nameplate.

In general, when a time range is indicated on the internal connections diagram, the timer has been factory set at a mid-range value. Timers should be set for the operating or reset times indicated on the associated overall logic diagram. Where a time range is indicated on the overall logic diagram, the timer should be set for the value recommended for that function in the descriptive write-up accompanying the overall logic diagram. Where a setting depends upon conditions encountered on a specific application, this is so stated and the factors influencing the choice of setting are described. The procedure for checking and setting the timers is described in a later section.

OPERATIONAL CHECKS

Operation of the SLAT61L unit can be checked by observing the signals at the ten test points (TP1 to TP10) in the SLAT61L, by observing the operation of the associated channel equipment, or by observing the output functions. The test points are located on the test card in position T, and are numbered 1 to 10 from top to bottom. TP1 is the reference bus for the logic circuit; TP10 is plus 15 volts DC. The remaining points are located at various strategic points throughout the logic as shown on the internal connection diagram (Fig. 2). Test point voltages can be monitored with a portable high impedance voltmeter, the voltmeter on the test panel of the associated equipment, or an oscilloscope.

TEST CARD ADAPTER

The test card adapter provides a convenient means of gaining access to any pin of a particular card. Detailed information on the use of the test adapter card is included in the card instruction book, GEK-34158.

TIMER ADJUSTMENTS AND TESTS

When the time-delay cards are to be adjusted or checked, an oscilloscope that can display two traces simultaneously, and that has a calibrated horizontal sweep, should be used.

In order to test the timer cards it is necessary to remove the card previous to the timer (see Table I) and to place the timer card in a card adapter. The card adapter allows access to the input and output of the timer if they are not brought out on test points. The timer test circuit is shown in Fig. 6. Opening the normally closed contact causes the output to step up to plus 15 volts DC after the pickup delay of the timer.

To increase the pickup time, turn the upper potentiometer on the timer card clockwise; to decrease the time, turn it counterclockwise. Closing the contact causes the timer output to drop out after the reset time-delay setting of the card. If the timer card is provided with a variable reset delay, it can be adjusted by the lower potentiometer on the timer card (clockwise increases reset time).

TABLE I

TIMER UNDER TEST	POSITION	REMOVE CARD IN POSITION
TL41	J	E
TL42	H	G
TL43	N	C
TL44	M	NONE**
TL45	L	K

**Turn power supply switch on and off

TRIP CIRCUIT TESTS

The trip circuits with the series mechanical targets may be checked by connecting an auxiliary lock-out relay, such as the Type HEA relay, in series with the trip circuit. A typical circuit is shown in Fig. 7. The HEA relay should have the same DC rating as the trip circuit of the SLAT61L. If an auxiliary lock-out relay is not available, it can be replaced by a resistive load which limits the trip circuit current to three amperes. In most equipments, a trip output can be produced bt pushing a push button in the associated units.

Prior to final installation, a check of the overall trip circuit should be made with the tripping contacts connected to trip the circuit breakers.

OVERALL EQUIPMENT TESTS

After the SLAT61L relay and the associated static relay units have been individually calibrated and tested for the desired settings and ranges, a series of overall operating circuit checks is advisable. The elementary, overall logic and logic description for the specific job will be useful for determining the overall operation of the scheme.

Overall equipment tests can be performed by applying alternating current and voltages to the measuring units as specified in the instruction book for the measuring units and checking that proper outputs are obtained when the measuring units operate.

SYMMETRY AND PHASE-DELAY TIMER ADJUSTMENTS

The symmetry timer (TL42, "H" position) and phase-delay timer (TL41, "J" position) final settings must be made in the field after the transmitters, receivers and coupling equipment have been tuned and adjusted for proper sensitivity per the channel

instructions. Operation of the squaring amplifier and fault detectors, FDL and FDH, are required for accomplishment of the final symmetry and phase-delay adjustments; refer to the measuring unit instruction book for the recommended procedure.

The symmetry adjustment must be accomplished prior to phase-delay adjustments as described in the measuring unit instructions. The transient blocking timer (TL43, "N" position) should be removed to prevent continuous channel keying when the logic trip bus is energized. Clockwise adjustment of P1 and P2 on TL42 "H" position card, increases the pickup delay or drop-out delay, respectively. Conversely, counterclockwise adjustment reduces the respective operate times. The minimum delay on pickup which allows equal half-cycle block and trip output, as measured at TP8, is the recommended final setting.

After the symmetry adjustment has been accomplished, the phase-delay adjustment is made to obtain the proper alignment of the local signal with the received signal; refer to the measuring unit instructions. Clockwise adjustment of P1 or P2 on TL41, "S" position card, increases the pickup or drop-out delay, respectively. The final setting is the alignment of the trip attempt signal monitored at TP4 compared to the trip or block signal monitored at TP8, which is dependent upon internal or external fault simulation during the adjustment.

MAINTENANCE

PERIODIC TESTS

It should be sufficient to check the outputs produced at test points in the SLAT61L when periodic calibration tests are made on the associated measuring units, for example, the phase and ground relays in line-relaying scheme. No separate periodic tests on the SLAT61L itself should be required.

TROUBLESHOOTING

In any troubleshooting of equipment, it should first be established which unit is functioning incorrectly. The overall logic diagram supplied with the equipment shows the combined logic of the complete equipment and the various test points in each unit. By signal tracing, using the overall logic diagram and the various test points, it should be possible to quickly isolate the trouble.

A test adapter card is supplied with each static relay equipment to supplement the prewired test points on the test cards. Use of the adapter card is described in the card instruction book GEK-34158.

A dual-trace oscilloscope is a valuable aid to detailed troubleshooting, since it can be used to determine phase shift, operate and reset times, as well as input and output levels. A portable dual-trace oscilloscope with a calibrated sweep and trigger facility is recommended.

SPARE PARTS

To minimize possible outage time, it is recommended that a complete maintenance program should include the stocking of a least one spare card of each type. It is possible to replace damaged or defective components on the printed circuit cards, but great care should be taken in soldering so as not to damage or bridge-over the printed circuit buses, or overheat the semiconductor components. The repaired area should be recovered with a suitable high-dielectric plastic coating to prevent possible breakdowns across the printed buses due to moisture and dust. The wiring diagrams for the cards in the SLAT61L relay are included in the card instruction book GEK-34158.

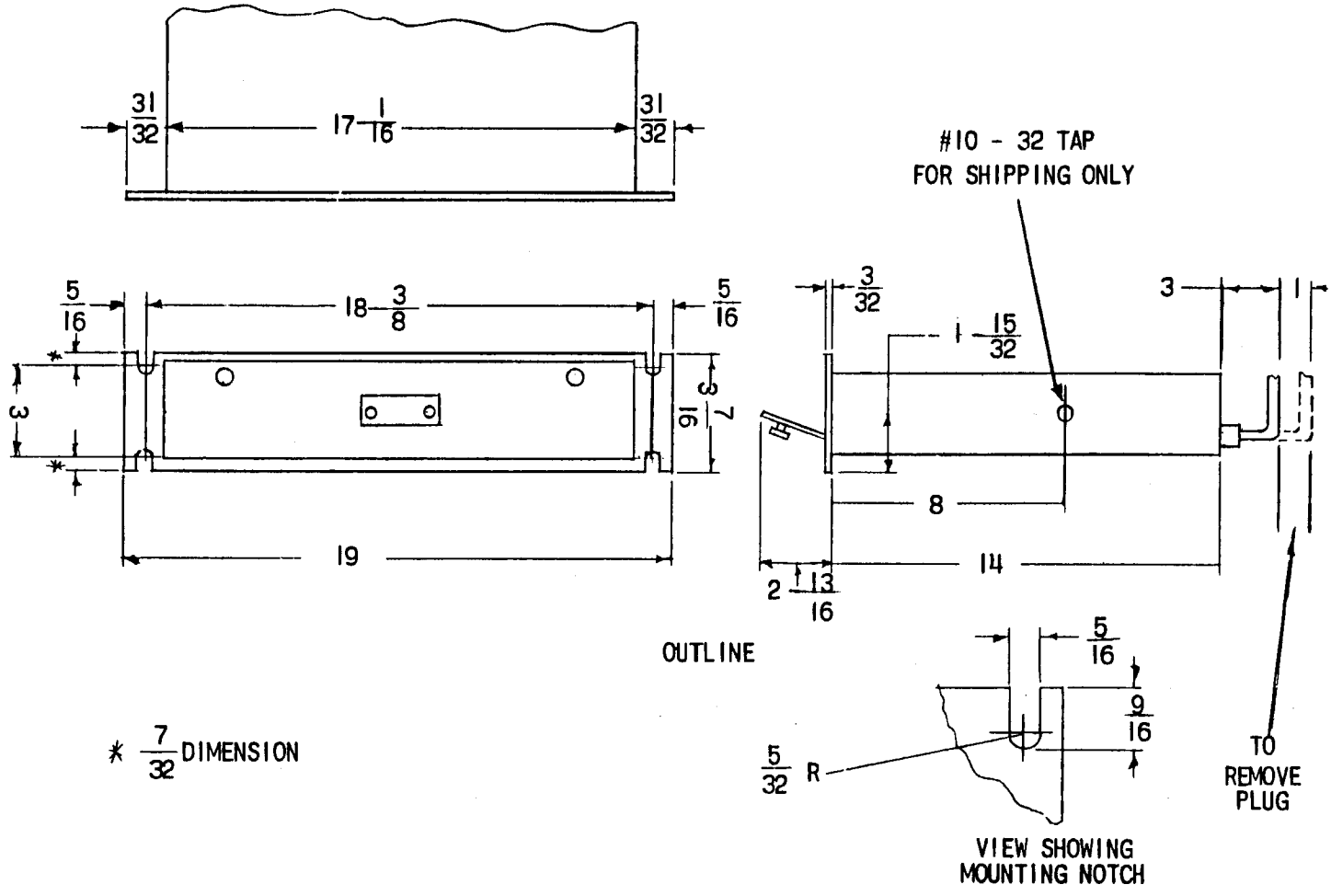


Fig. 1 (0227A2036-0) Outline and Mounting Dimensions for the Type SLAT61L Relay

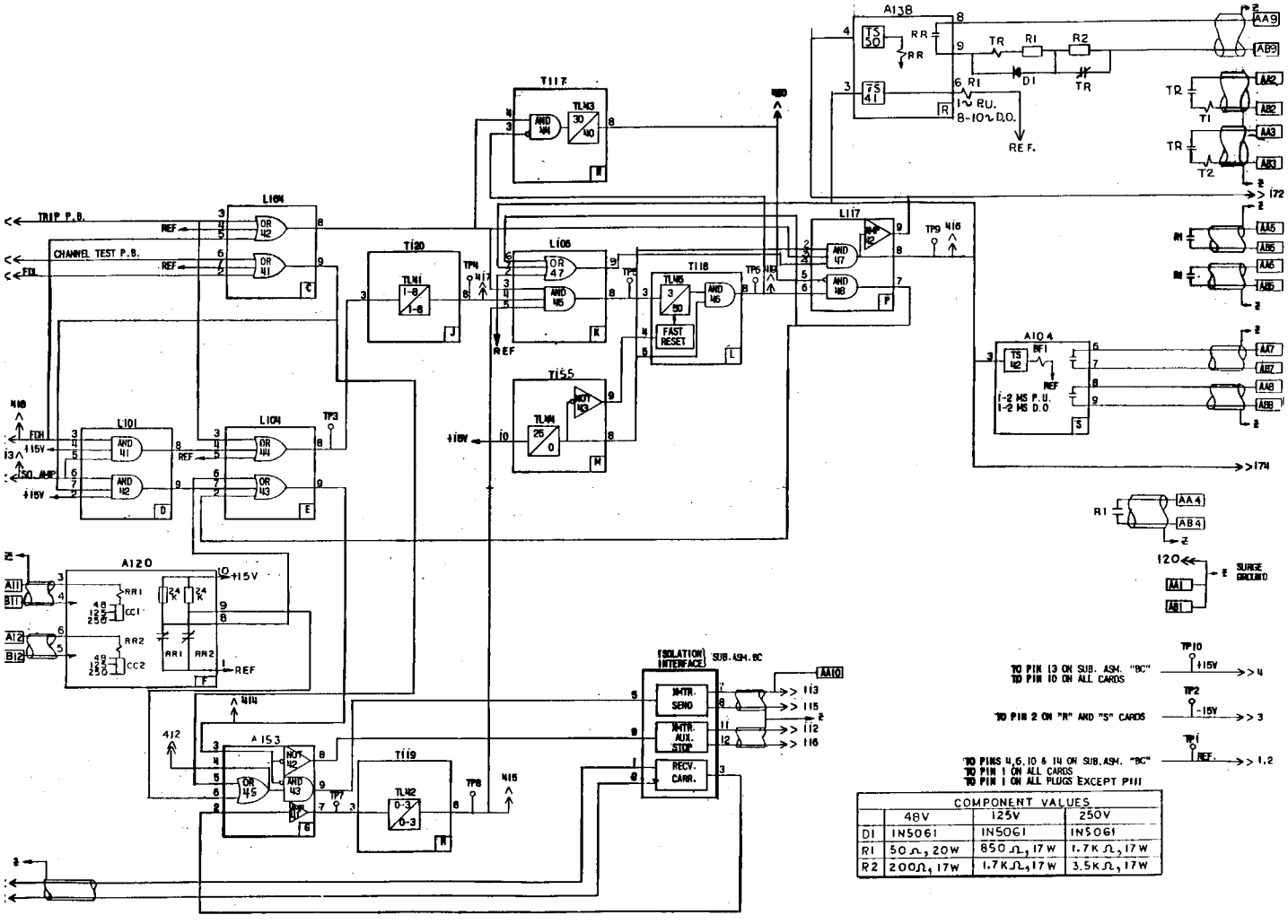
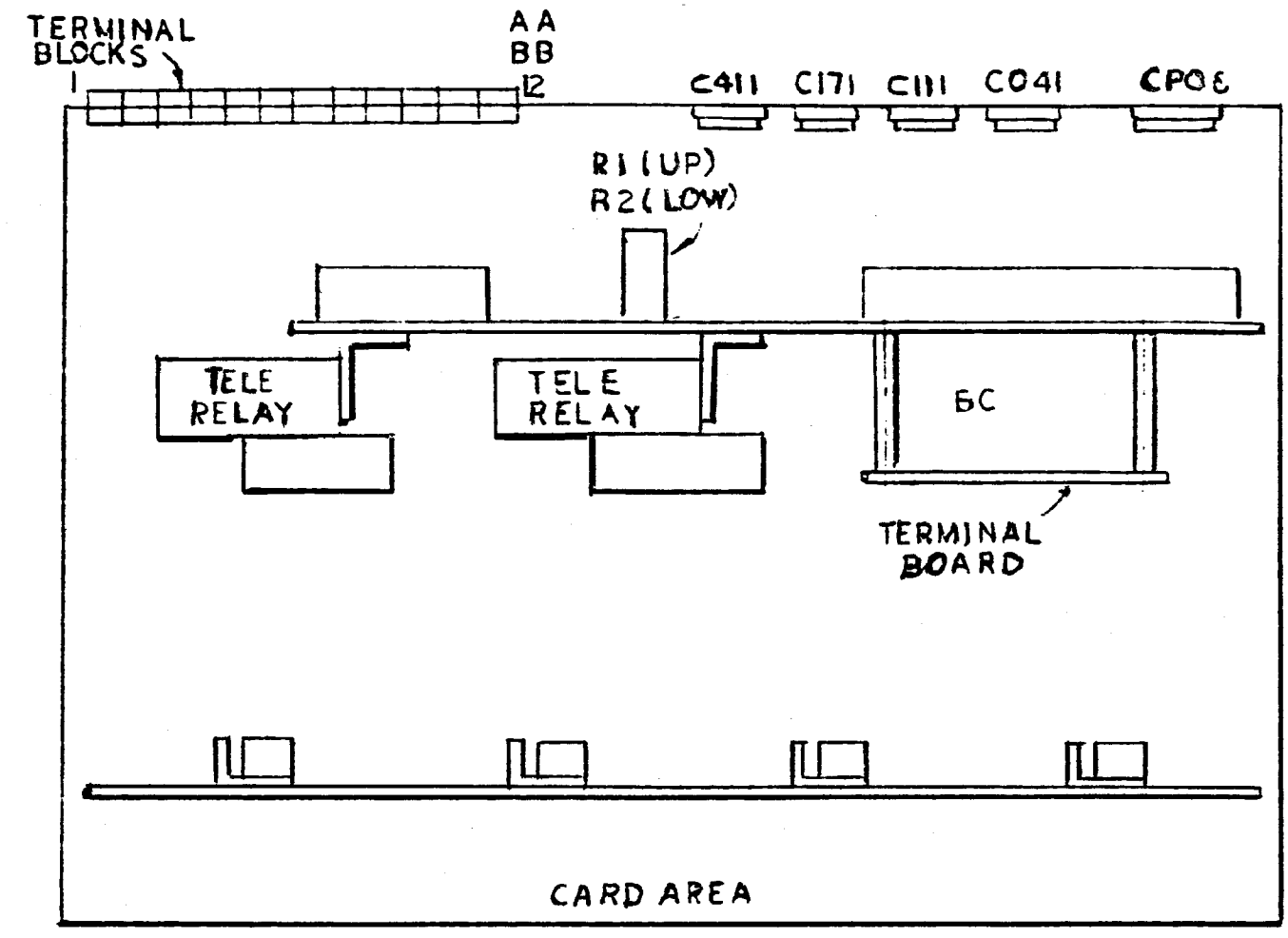


Fig. 2 (0179C6263-0) Internal Connections for the Type SLAT61L Relay



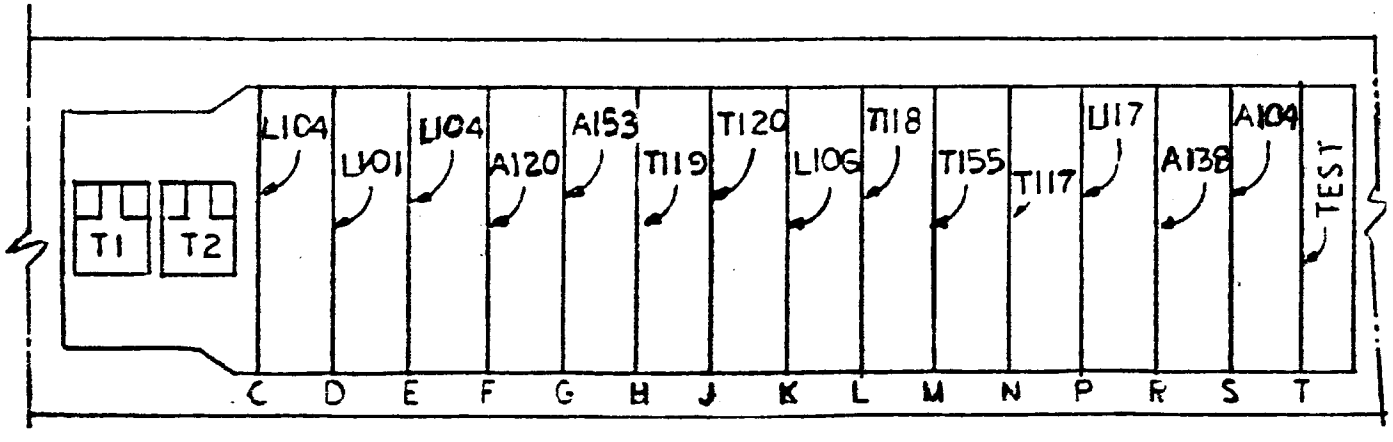


Fig. 3 (0285A6231-0) Component Location Diagram for the Type SLAT61L Relay

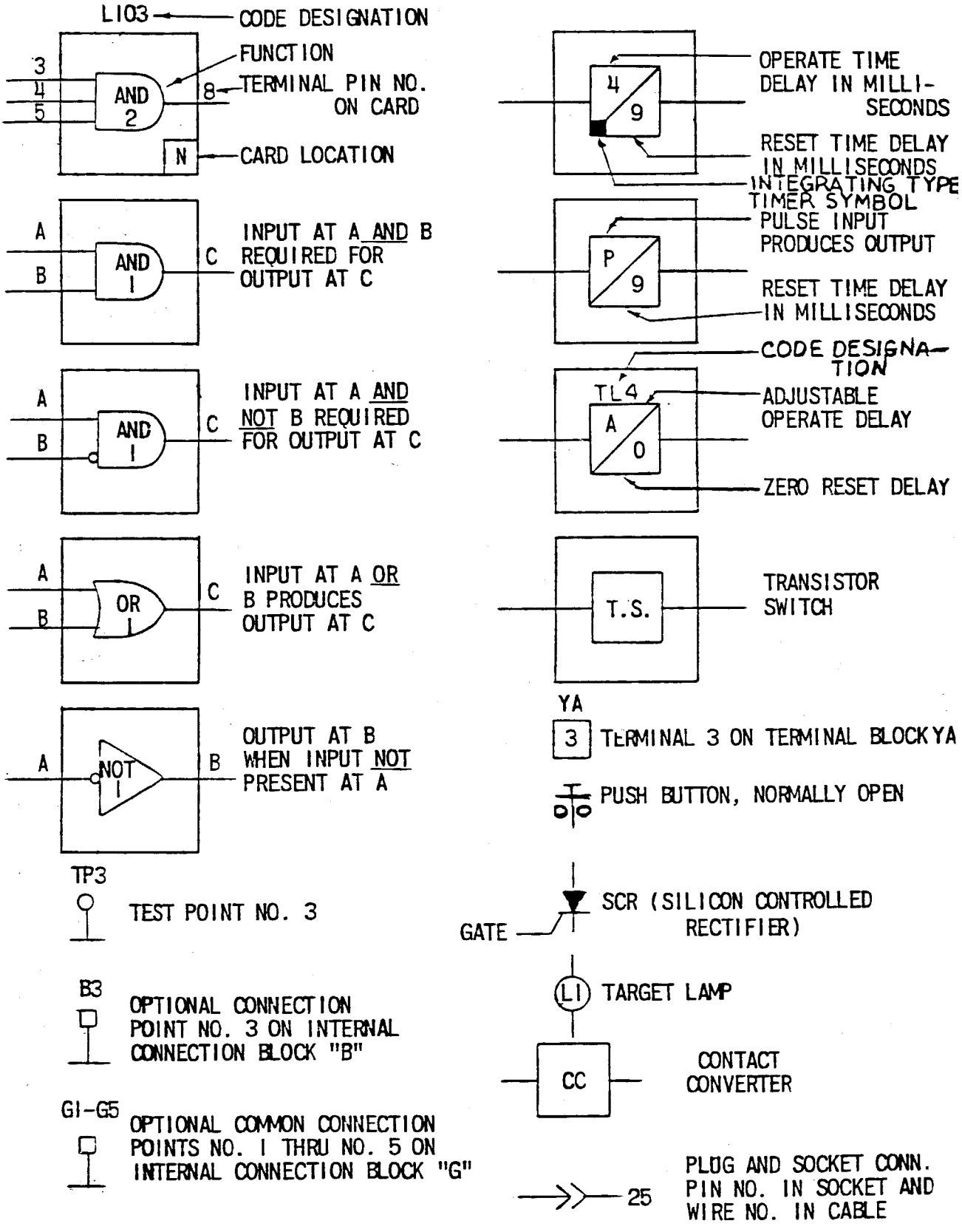
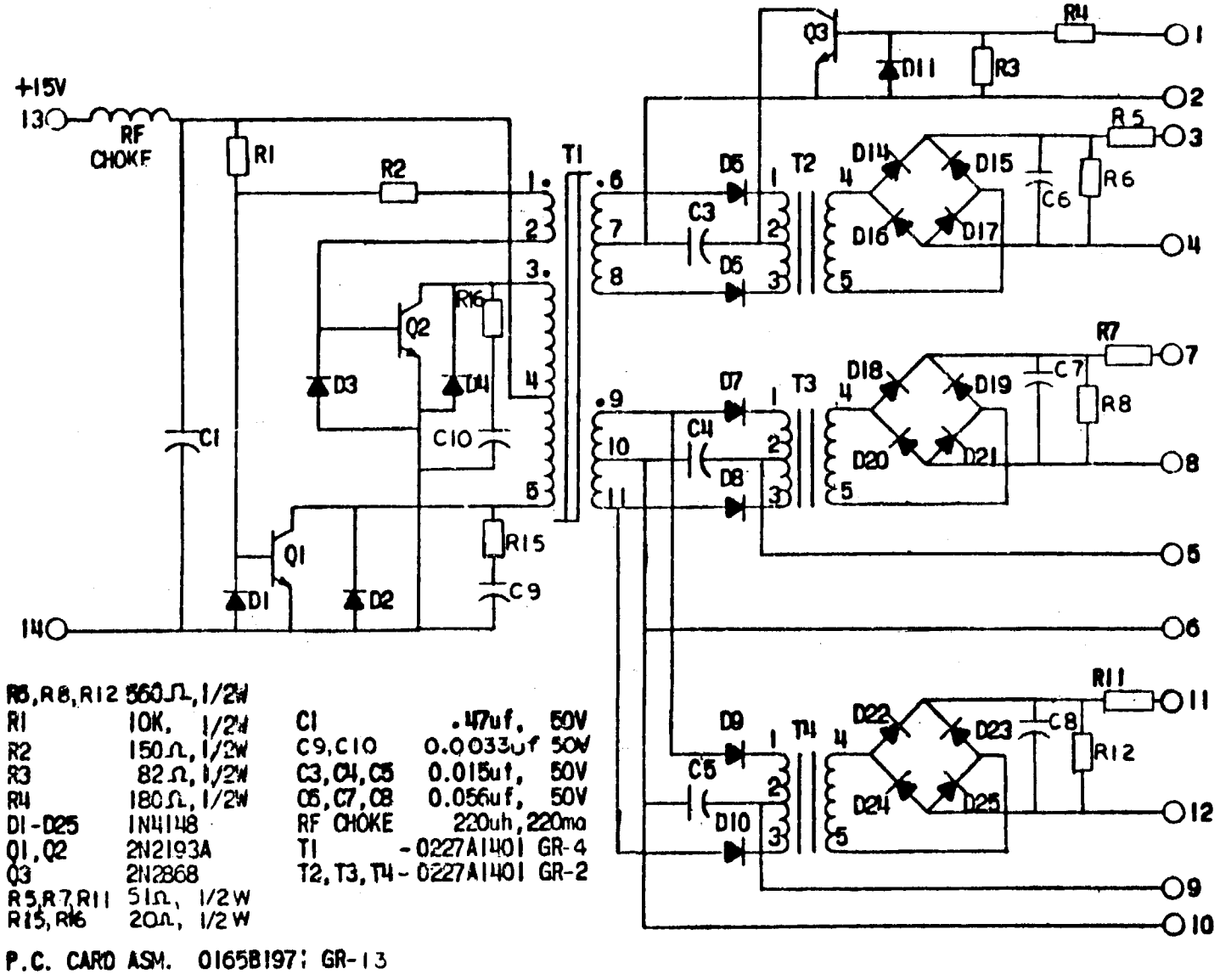


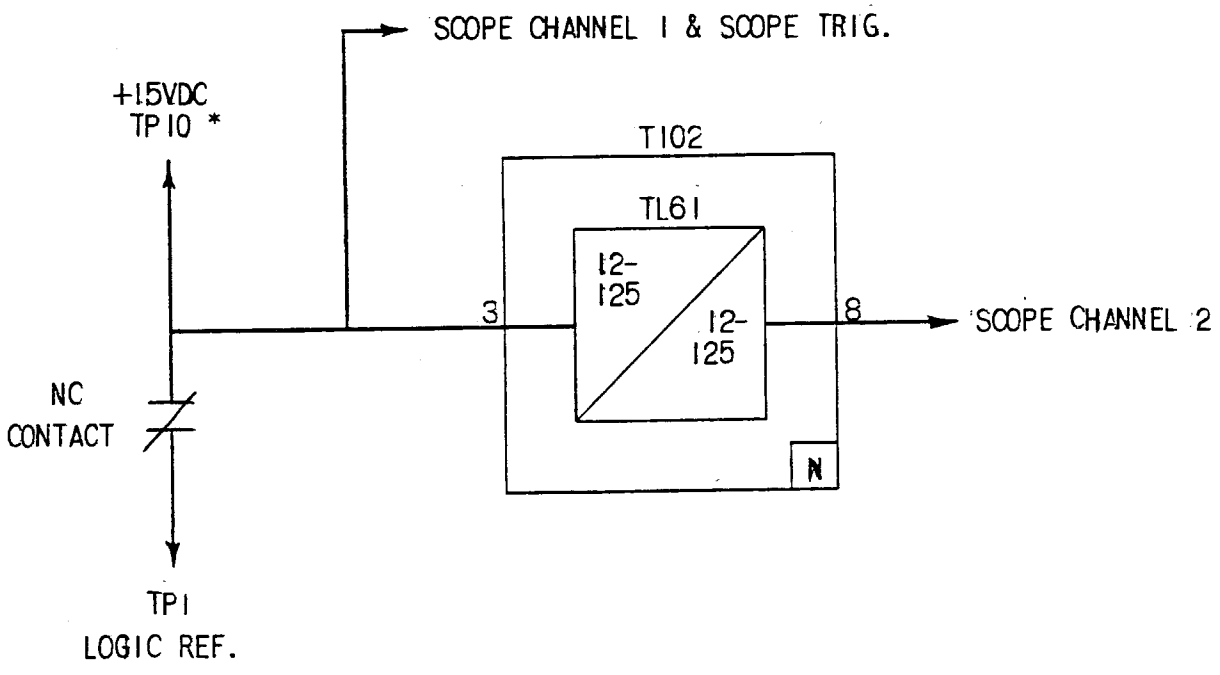
Fig. 4 (0227A2047-1) Logic and Internal Connection Diagram Legend



R6,R8,R12	560Ω, 1/2W	C1	.47uf, 50V
R1	10K, 1/2W	C9,C10	0.0033uf 50V
R2	150Ω, 1/2W	C3,C4,C5	0.015uf, 50V
R3	82Ω, 1/2W	C6,C7,C8	0.056uf, 50V
R4	180Ω, 1/2W	RF CHOKE	220uh, 220ma
D1-D25	1N4148	T1	-0227A1401 GR-4
Q1,Q2	2N2193A	T2,T3,T4	-0227A1401 GR-2
Q3	2N2868		
R5,R7,R11	51Ω, 1/2W		
R15,R16	20Ω, 1/2W		

P.C. CARD ASM. 0165B197; GR-13

Fig. 5 (0208A5504AJ-1) Isolation Interface Circuit Connection Diagram



* THE 15VDC SIGNAL AT PIN 10 HAS A CURRENT LIMITING RESISTOR MOUNTED ON THE TEST CARD.

Fig. 6 (0246A7987-0) Logic Timer Test Circuit

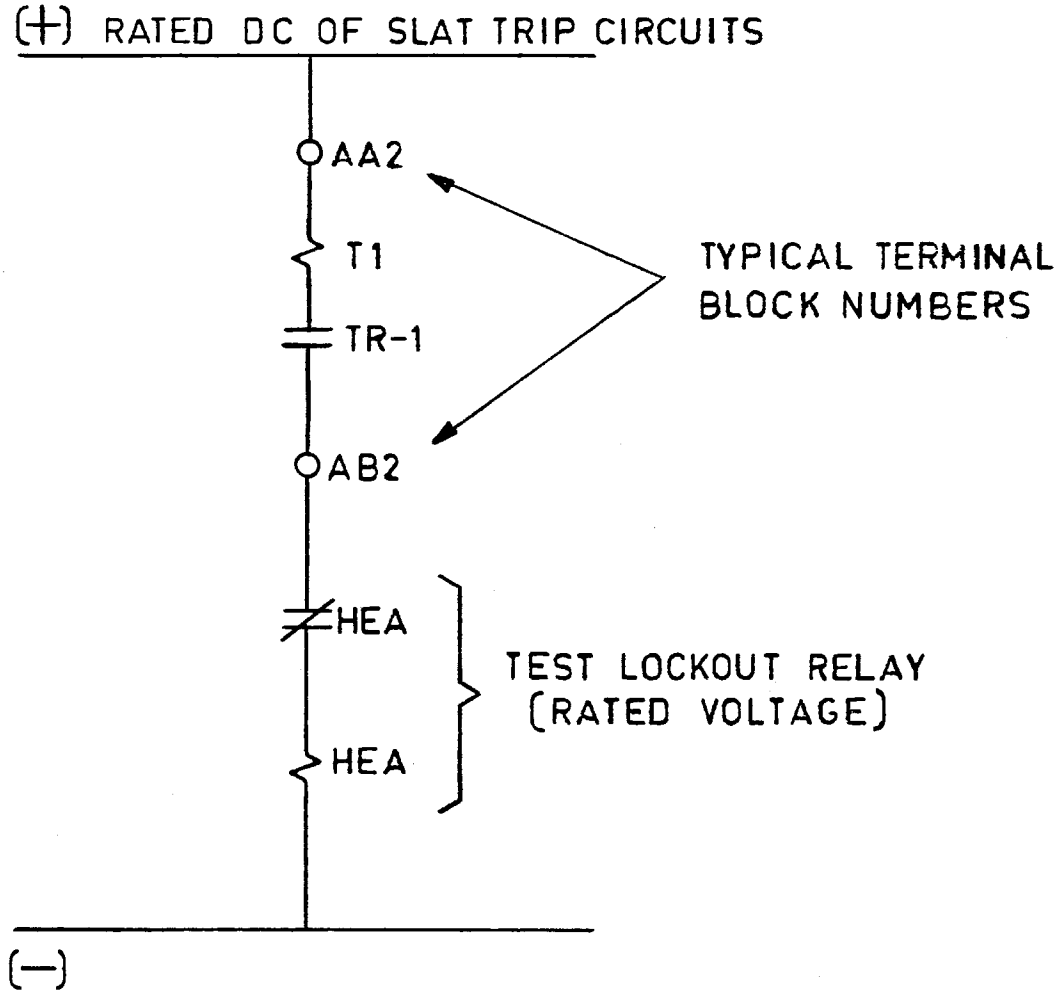


Fig. 7 (0257A8788-0) Typical Trip Circuit Test Connections for Relays with Trip Contacts

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