INSTRUCTIONS

GEK-86725

STATIC OUTPUT AND TRIPPING UNIT

TYPE SLAT61N

GENERAL ELECTRIC

CONTENTS

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DESCRIPTION

The Type SLAT61N relay is a static logic, output and tripping relay intended for application in phase comparison schemes operating via a frequency shift tone channel. In addition to the SLAT 61N relay, the complete relay scheme would also include an SLD phase comparison measuring unit, a power supply and the appropriate frequency-shift channel equipment.

The outputs of the SLAT61N include two electrically separate SCR trip circuits, each with an electromechanical target; two electrically separate reclose initiating contacts (RI); and two electrically separate breaker failure timer initiating contacts (BFI).

The inputs to the SLAT61N are from the associated SLD relay, from the channel equipment, and from external contacts.

The relay is packaged in a two-rack-unit enclosed metal case suitable for mounting on a 19-inch rack. The outline and mounting dimensions are shown in Figure 1, the internal connections in Figure 2, and the card and component locations in Figure 3.

APPLICATION

The SLAT61N relay is designed for use with a Type SLD51 phase comparison relay and an appropriate frequency-shift-type communications channel. Depending on the specific matrix connections made in the SLAT61N, the resulting relaying scheme can be applied in a permissive mode, or in a blocking mode of operation. Please refer to the overall logic description supplied with the scheme for a discussion of the mode of operation.

RATINGS

The Type SLAT61N relay is designed for use in an environment where the ambient temperature around the relay case is between -20°C and +65°C.

The Type SLAT61N relay requires a $\pm$ 15 VDC power source which can be obtained from a Type SSA power supply.

The SCR tripping circuits are rated for 48, 125 or 250 VDC. Each has a 1.0 ampere series target. The tripping circuits are designed to carry 30 amperes for one second.

The contacts of the telephone-type relays that are used for RI will make and carry 3 amperes continuously, and will interrupt up to 0.5 amperes (inductive) at 125 VDC or up to 0.25 ampere (inductive) at 250 VDC.

The contacts of the reed relay that is used for the BFI function have a 100 volt-ampere rating. The contacts of the other reed relays may be rated at 100 volt amperes or 10 volt amperes. See the specific application for the type supplied. The contact current-carrying and interrupting ratings are listed below.

RELAY RATING		MAXIMUM						
		VOLTS	CURRENT					
			MAKE AND CARRY	INTERRUPT				
				RESISTIVE			INDUCTIVE	
RES	IND			@ 48V	@ 125V	@ 250V	@ 48V	@ 125V	@ 250V
100 VA	35 VA	1000	3A	2A	0.8A	0.4A	0.72A	0.28A	0.14A
50 VA	15 VA	1000	3A	1A	0.4A	0.2A	0.3 A	0.12A	0.06A
10 VA	3 VA	250	0.5A	0.2A	0.08A	0.04A	0.06A	0.02A	0.01A

Refer to the unit nameplate and the unit connection diagram for the ratings of the particular functions supplied.

BURDENS

The SLAT61N relay presents a maximum burden to the Type SSA power supply of:

210 milliamperes from the +15 VDC supply
125 milliamperes from the -15 VDC supply

Each contact converter, when energized, would draw approximately 10 milliamperes from the station battery, regardless of tap setting.

FUNCTIONS

LOGIC CIRCUIT

The functions of the Type SLAT61N relay involve basic logic (AND, OR, and NOT) where the presence or absence of signals, rather than their magnitude, controls the operation. Signals are measured with respect to a reference bus acessible at TP1. In general, a signal below 1 VDC represents an OFF or LOGIC ZERO condition; an ON or LOGIC ONE condition is represented by a signal of approximately +15 VDC.

The symbols used on the internal connection diagram, Figure 2, are explained by the legend shown in Figure 5.

SCR TRIP CIRCUIT

Two electrically separate, isolated SCR trip circuits are provided to trip two breakers. Each circuit is capable of carrying 30 amperes for one second.

The internal connections for the SCR trip and isolator subassemblies aare shown in Figure 4. The isolator card, by means of a DC-to-DC converter, provides a signal path but maintains metallic isolation. This feature makes it possible to isolate the relay power supply from the trip circuit power supply.

RI RECLOSE INITIATE CIRCUIT

Two electrically separate normally-open contacts are provided. These contacts close within 17 milliseconds from the time the associated coil is energized by the logic. The contacts open within 170 milliseconds from the time the coil is deenergized. The RI function uses a telephone-type relay with contact ratings stated under **RATINGS.**

BFI BREAKER FAILURE INITIATE CIRCUIT

Two electrically separate normally-open contacts are provided. These contacts close within 2 milliseconds from the time the associated coil is energized by the logic. These contacts open within 2 milliseconds from the time the coil is deenergized. The BFI function uses a reed relay with contact ratings stated under **RATINGS.**

CONTACT CONVERTERS

The purpose of these functions is to convert a contact operation into a signal that is compatible with the logic circuit of the Type SLAT61N relay.

Refer to the specific equipment elementary diagram for the use of these converters.

CHANNEL INTERFACE

The logic of the Type SLAT61N relay includes an isolation interface (Figure 6) between the relays in the scheme and the associated channel. The circuitry of the isolation interface provides a signal path but maintains metallic isolation. This feature makes it possible to maintain isolation between the DC supply used for the relays and that employed by the channel.

When pins 9 and 10 are both connected to relay reference, a metallically separate positive logic signal appears at pin 11 with respect to 12. The output from the isolation interface is a 5 VDC, 20 milliampere signal.

TARGETS

Two electromechanical target coils are included, one in series with each SCR. These targets operate on 1 ampere of trip current when the associated SCR passes current. The trip circuit resistance in the relay is 0.40 ohm.

CONSTRUCTION

The SLAT 61N relay is packaged in an enclosed metal case with hinged front cover and removable top cover. The outline and mounting dimensions of the case and the physical location of the components are shown in Figures 1 and 3 respectively.

The SLAT61N relay contains printed circuit cards identified by a code number such as: A104, T116, L106 where A designates an auxiliary function, T designates a time-delay function, and L designates a logic function. The printed circuit cards plug in from the front of the unit. The sockets are marked with letter designations or "addresses" (D, E, F, etc.), which appear on the guide strips in front of each socket, on the component location drawing, on the unit internal connection diagram, and on the printed circuit card. The test points (TP1, TP2, etc.) shown on the internal connection diagram are connected to instrument jacks on the test card in position T with TP1 at the top of the AT card. TP1 is tied to reference; TP10 is tied to + 15 VDC through a 2.2K resistor. The resistor limits the current when TP10 is used to supply a logic signal to a card.

The SLAT61N relay receives its inputs from the associated Type SLD relay. These units are interconnected by 10-conductor shielded cables. The sockets for these input cables are located on the rear panel of the unit. The SLAT61N output functions are connected to 12-point terminal strips, which are also located on the rear of the unit.

A window is provided in the hinged cover of the relay to allow the mechanical targets to be seen. Push buttons are also provided to reset the targets without opening the cover.

RECEIVING, HANDLING AND STORAGE

The SLAT61N relay will normally be supplied as part of a static relay equipment, mounted in a rack or cabinet with other static relays and test equipment. Immediately upon receipt of a static relay equipment, it should be unpacked and examined for any damage sustained in transit. If injury or damage resulting from rough handling is evident, file a damage claim at once with the transportation company and promptly notify the nearest General Electric Utility Sales Office.

Reasonable care should be exercised in unpacking the equipment. If the equipment is not to be installed immediately, it should be stored indoors in a location that is free from moisture, dust, metallic chips, and severe atmospheric contaminants.

Just prior to final installation, the shipping support bolt should be removed from each side of all relay units, to facilitate possible future unit removal for maintenance. These shipping support bolts are approximately eight inches back from the relay front panel.

STATIC RELAY EQUIPMENT, WHEN SUPPLIED IN SWING RACK CABINETS, SHOULD BE SECURELY ANCHORED TO THE FLOOR OR TO THE SHIPPING PALLET TO PREVENT THE EQUIPMENT FROM TIPPING OVER WHEN THE SWING RACK IS OPENED.

TEST INSTRUCTIONS

CAUTION:

THE LOGIC SYSTEM SIDE OF THE DC POWER SUPPLY USED WITH MOD III STATIC RELAY EQUIPMENT IS ISOLATED FROM GROUND. IT IS A DESIGN CHARACTERISTIC OF MOST ELECTRONIC INSTRUMENTS THAT ONE OF THE SIGNAL INPUT TERMINALS IS CONNECTED TO THE INSTRUMENT CHASSIS. IF THE INSTRUMENT USED TO TEST THE RELAY EQUIPMENT IS ISOLATED FROM GROUND, ITS CHASSIS MAY HAVE AN ELECTRICAL POTENTIAL WITH RESPECT TO GROUND. THE USE OF A TEST INSTRUMENT WITH A GROUNDED CHASSIS WILL NOT AFFECT THE TESTING OF THE EQUIPMENT. HOWEVER, A SECOND GROUND CONNECTION TO THE EQUIPMENT, SUCH AS A TEST LEAD INADVERTENTLY DROPPING AGAINST THE RELAY CASE, MAY CAUSE DAMAGE TO THE LOGIC CIRCUITRY. NO EXTERNAL TEST EQUIPMENT SHOULD BE LEFT CONNECTED TO THE STATIC RELAYS WHEN THEY ARE IN PROTECTIVE SERVICE, SINCE TEST EQUIPMENT GROUNDING REDUCES THE EFFECTIVENESS OF THE ISOLATION PROVIDED.

IF THE SLAT61N RELAY THAT IS TO BE TESTED IS INSTALLED IN AN EQUIPMENT WHICH HAS ALREADY BEEN CONNECTED TO THE POWER SYSTEM, DISCONNECT THE OUTPUTS TO THE SYSTEM DURING TEST.

GENERAL

The SLAT61N relay is supplied from the factory either as a separate unit, or mounted in a static relay equipment associated with measuring relays, a Type SSA power supply, and some form of channel equipment. All relay units for a given terminal of static relaying equipment are tested together at the factory, and each unit will have the same summary number stamped on its nameplate.

In general, when a time range is indicated on the internal connections diagram, the timer has been factory set at a mid-range value. Timers should be set for the operating or reset times indicated on the associated overall logic diagram. Where a time range is indicated on the overall logic diagram, the timer should be set for the value recommended for that function in the descriptive write-up accompanying the overall logic diagram. Where a setting depends upon conditions encountered on a specific application, this is so stated and the factors influencing the choice of setting are described. The procedure for checking and setting the timers is described in the Timer Adjustments & Tests section of printed circuit card book GEK-34158.

OPERATIONAL CHECKS

Operation of the SLAT61N unit can be checked by observing the signals at the ten test points (TP1 to TP10) in the SLAT61N, by observing the operation of the associated channel equipment, or by observing the output functions. The test points are located on a test card in position AT, and are numbered 1 to 10 from top to bottom. TP1 is the reference bus for the logic circuit, TP10 is at + 15 VDC. The remaining points are located at various strategic points throughout the logic as shown in the internal connection diagram (Figure 2). Test point voltages can be monitored with a portable high impedance voltmeter, the voltmeter on the test panel of the associated equipment, or an oscilloscope. Test points 11 to 20 are located on the test card, in position T.

TEST CARD ADAPTER

The test card adapter provides a convenient means of gaining access to any pin of a particular card. Detailed information on the use of the test card adapter is included in the card instruction book GEK-34158.

TIMER ADJUSTMENTS AND TESTS

When the time-delay cards are to be adjusted or checked, an oscilloscope that can display two traces simultaneously, and that has a calibrated horizontal sweep, should be used.

In order to test the timer cards, it is necessary to remove the printed circuit card before the timer (See Table I) and to place the timer card in a card adapter. The card adapter allows access to the input and output of the timer if they are not brought out on test points. The timer test circuit is shown on Figure 6. Opening the normally-closed contact causes the output to step up to + 15 VDC after the pickup delay of the timer. To increase the pickup time, turn the upper potentiometer on the timer card clockwise; to decrease the time, turn it counterclockwise. Closing the contact causes the timer output to drop out after the reset time-delay setting of the card. If the timer card is provided with a variable reset delay, it can be adjusted by the lower potentiometer on the timer card (clockwise increases reset time).

TABLE I

TIMER UNDER TEST	POSITION	REMOVE CARD IN POSITION
TL41	M	N
TL42	P	E
TL43	K	L
TL44	SS	NONE**
TL45	J	L

**Turn power supply switch on and off.

TRIP CIRCUIT TESTS

The SCR trip circuits and series mechanical targets may be checked by connecting an auxiliary lock-out relay, such as the Type HEA relay, in series with the SCR trip circuit. A typical circuit is shown in Figure 8. The HEA relay should have the same DC rating as the SCR trip circuit of the SLAT61N relay. If an auxiliary lock-out relay is not available, it can be replaced by a resistive load which limits the trip circuit current to 3 amperes. In most equipments, the trip circuit can be energized by operating a test push button in the associated units.

Prior to final installation, a check of the overall trip circuit should be made with the SCR outputs connected to trip the circuit breakers.

OVERALL EQUIPMENT TESTS

After the SLAT61N relay and the associated static relay units have been individually calibrated and tested for the desired settings and ranges, a series of overall operating circuit checks is advisable. The elementary, overall logic, and logic description for the specific job will be useful for determining the overall operation of the scheme.

Overall equipment tests can be performed by applying the alternating current and voltages to the measuring units, as specified in the instruction book for the measuring units, and checking that proper outputs are obtained when the measuring units operate.

SYMMETRY AND PHASE-DELAY TIMER ADJUSTMENTS

The symmetry timer (TL42, "P" position) and phase-delay timer (TL41, "M" position) final settings must be made in the field after the transmitters, receivers, and coupling equipment have been tuned and adjusted for proper sensitivity per the channel instructions. Operation of the squaring amplifier and fault detectors, FDL and FDH, are required for accomplishment of the final symmetry and phase-delay adjustments; refer to the measuring unit instruction book for the recommended procedure.

The symmetry adjustment must be accomplished prior to phase delay adjustments, as described in the measuring unit instructions. Clockwise adjustment of P1 and P2 on TL42, "P" position card, increases the pickup delay or dropout delay respectively. Conversely, counterclockwise adjustment reduces the respective operate times. The minimum delay on pickup which allows equal half-cycle block and trip output as measured at TP8 is the recommended final setting.

After the symmetry adjustment has been accomplished, the phase-delay adjustment is made to obtain the proper alignment of the local signal with the received signal; refer to the measuring unit instructions. Clockwise adjustment of P1 or P2 on TL41, "M" position card, increases the pickup or dropout delay respectively. The final setting is the alignment of the trip attempt signal monitored at TP4, compared to the trip of block signal monitored at TP8, which is dependent upon internal or external fault simulation during the adjustment.

MAINTENANCE

PERIODIC TESTS

It should be sufficient to check the outputs produced at test points in the SLAT61N when periodic calibration tests are made on the associated measuring units, for example the phase and ground relays in a line relaying scheme. No separate periodic tests on the SLAT61N itself should be required.

TROUBLESHOOTING

In any troubleshooting of equipment, it should first be established which unit is functioning incorrectly. The overall logic diagram supplied with the equipment shows the combined logic of the complete equipment and the various test points in

each unit. By signal tracing, using the overall logic diagram and the various test points, it should be possible to isolate the trouble quickly.

A test adapter card is supplied with each static relay equipment to supplement the prewired test points on the test cards. Use of the adapter card is described in the card instruction book GEK-34158.

A dual-trace oscilloscope is a valuable aid to detailed troubleshooting, since it can be used to determine phase shift, operate and reset times, as well as input and output levels. A portable dual-trace oscilloscope with a calibrated sweep and trigger facility is recommended.

SPARE PARTS

To minimize possible outage time, it is recommended that a complete maintenance program should include the stocking of at least one spare card of each type. It is possible to replace damaged or defective components on the printed circuit cards, but great care should be taken in soldering, so as not to damage or bridge-over the printed circuit buses, or overheat the semiconductor components. The repaired areas should be re-covered with a suitable hi-dielectric plastic coating to prevent possible breakdowns across the printed buses due to moisture and dust. The wiring diagrams for the cards in the SLAT61N relay are included in the card book GEK-34158.

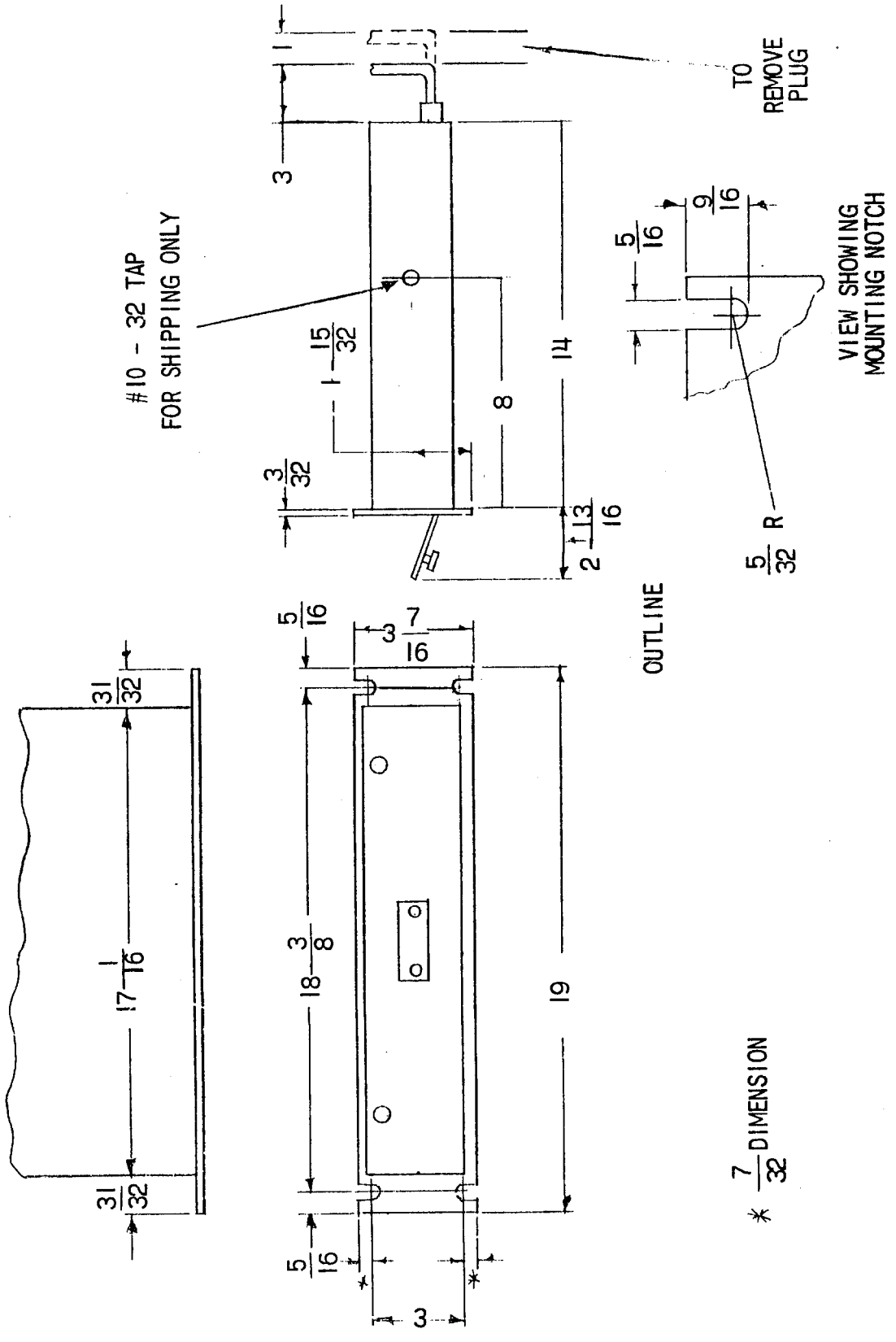


Figure 1 (0227A2036) Outline and Mounting Dimensions for the Type SLAT61N Relay

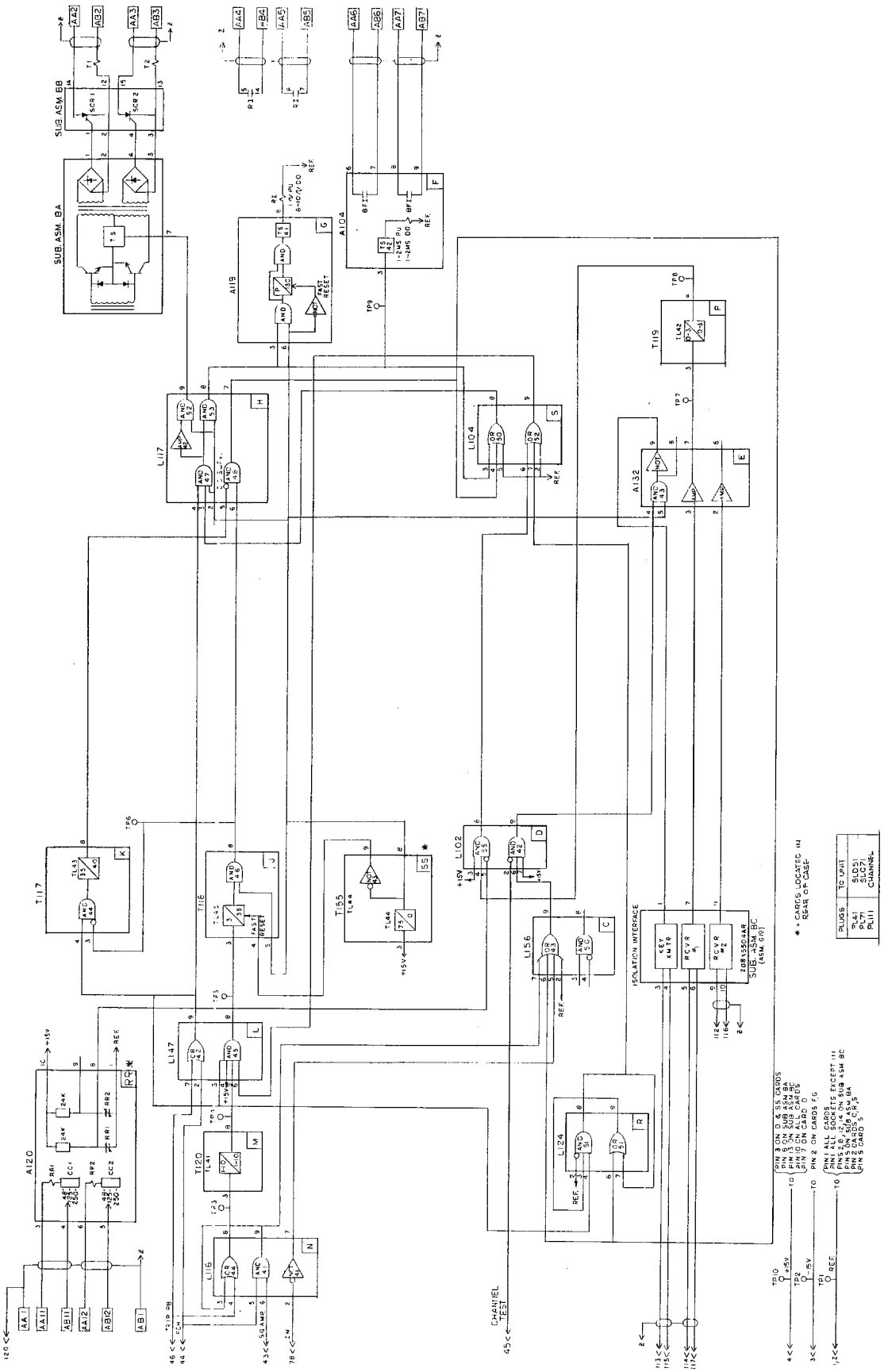
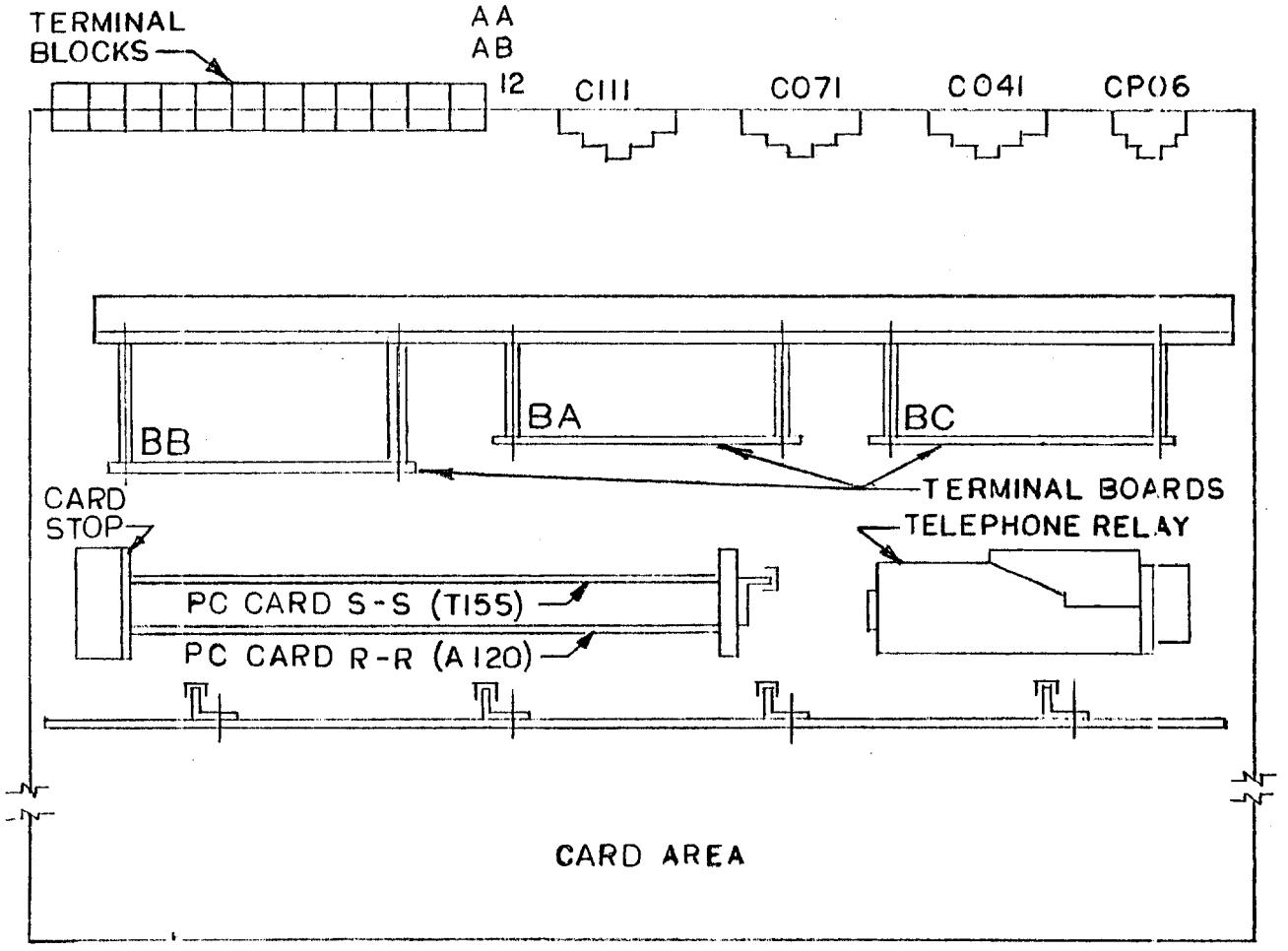


Figure 2 (0153D7218) Internal Connections for the Type SLAT61N Relay



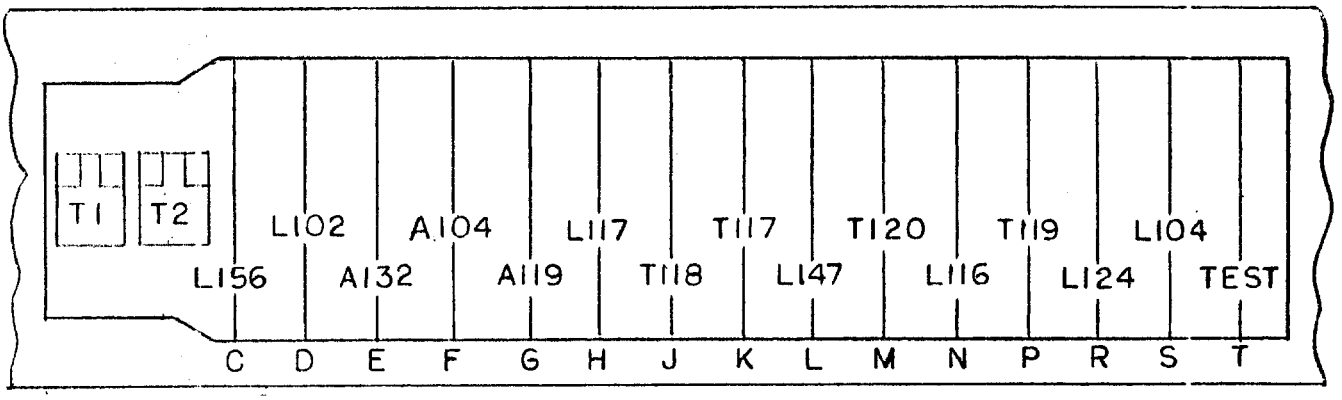


Figure 3 (0285A9298) Component Locations for the Type SLAT61N Relay

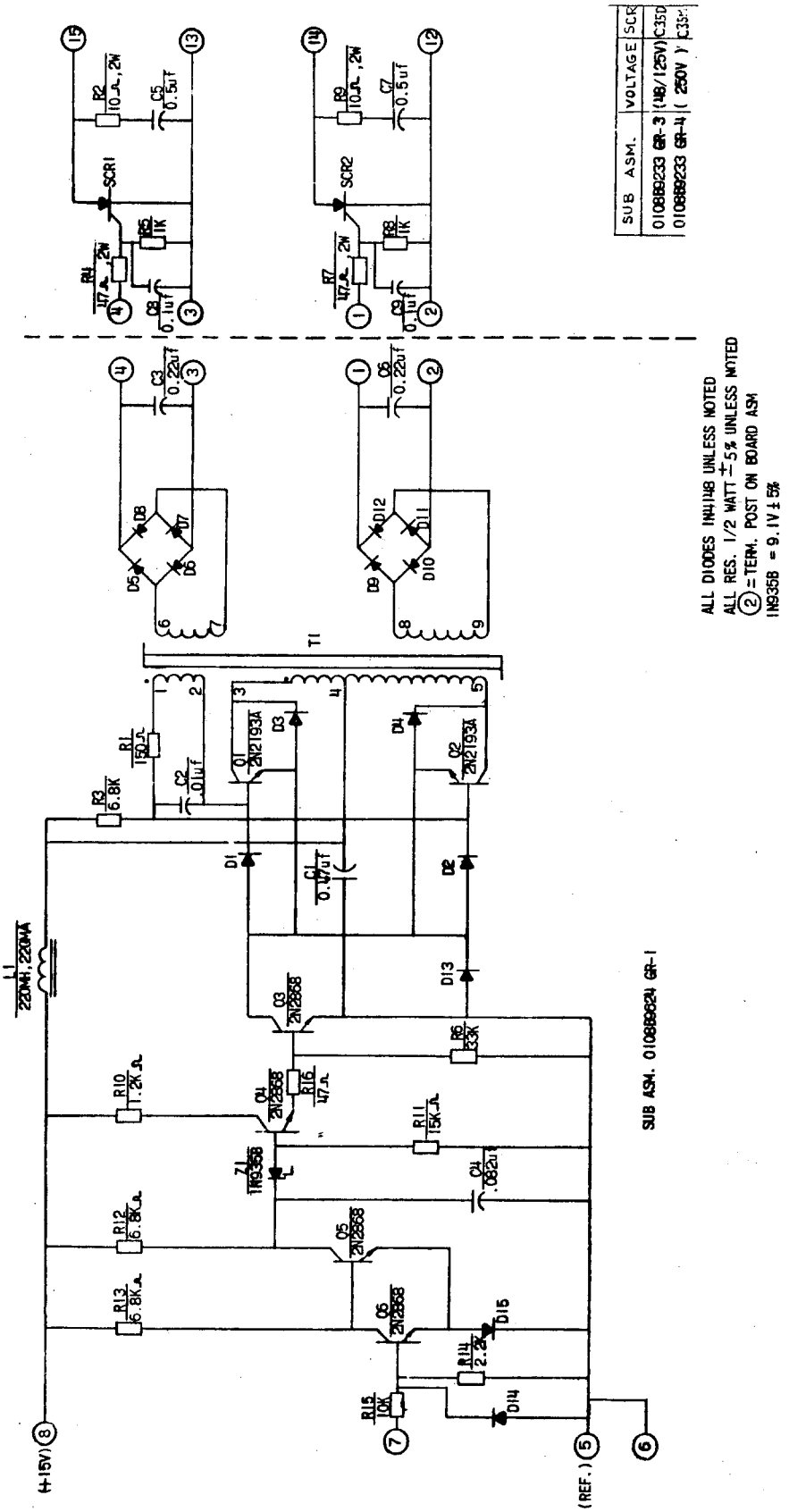


Figure 4 (0108B9610) Internal Connections for the SCR Trip and Isolator Subassemblies

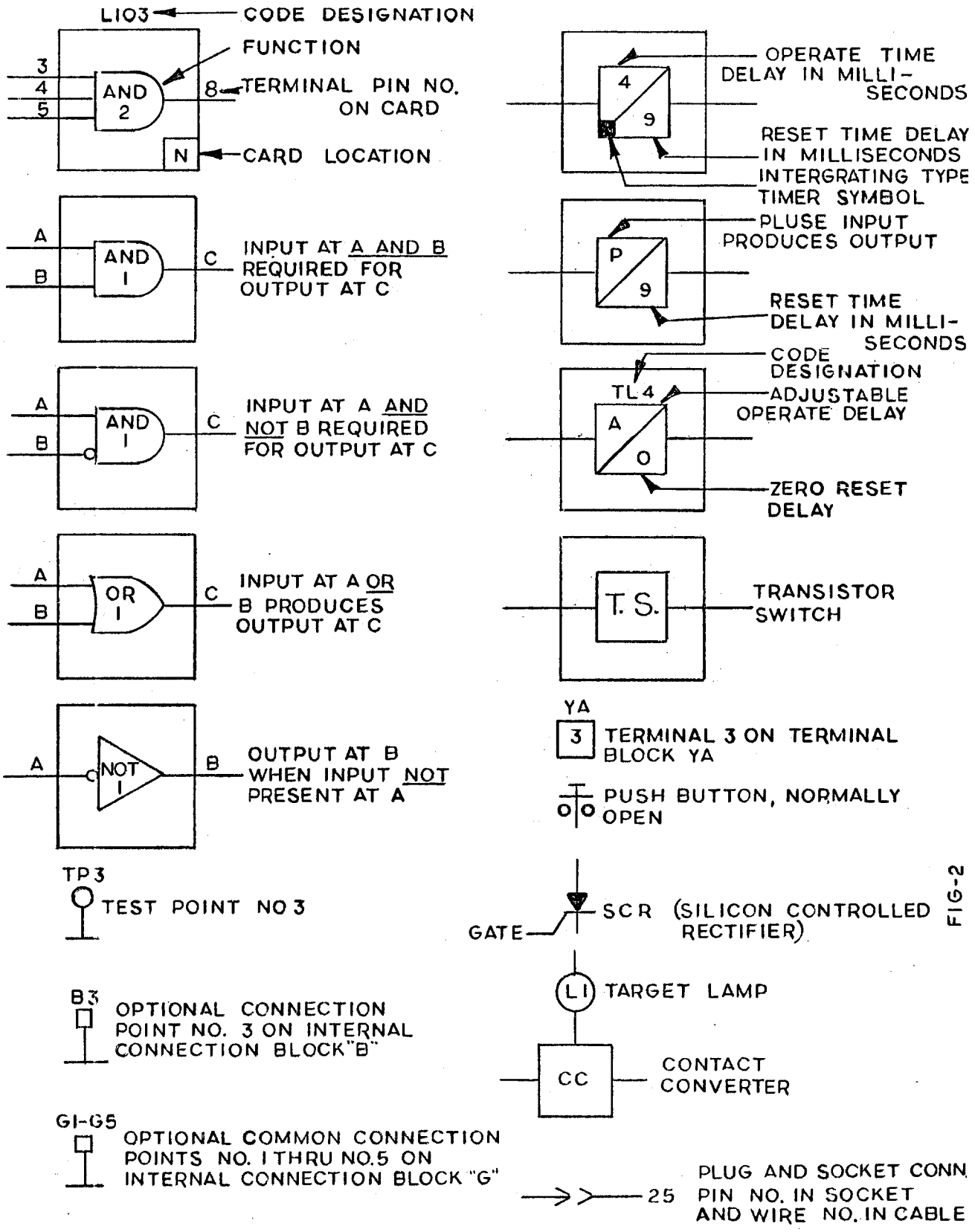


FIG-2

Figure 5 (0227A2047) Logic and Internal Connection Diagram Legend

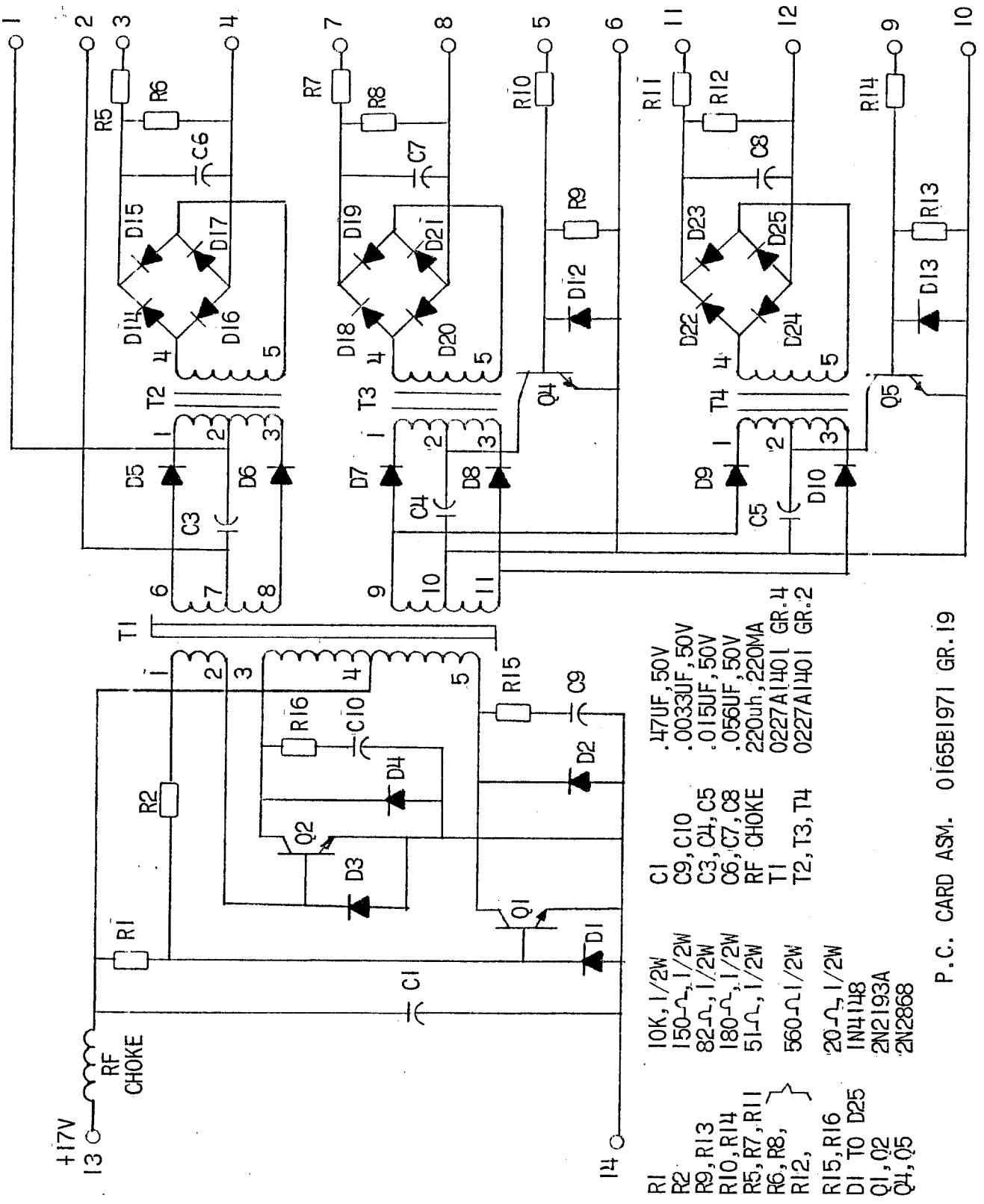
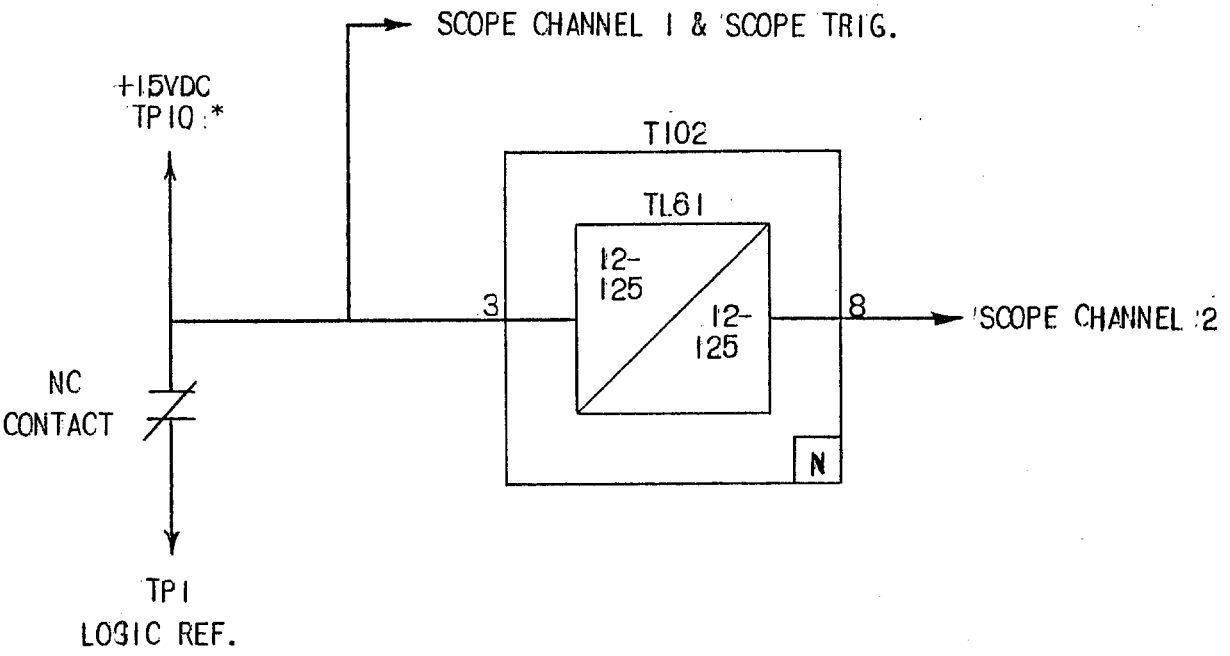


Figure 6 (0208A5504 AR) Isolation Interface Connection Diagram



* THE 15VDC SIGNAL AT PIN 10 HAS A CURRENT LIMITING RESISTOR MOUNTED ON THE TEST CARD.

Figure 7 (0246A7987) Logic Timer Test Circuit

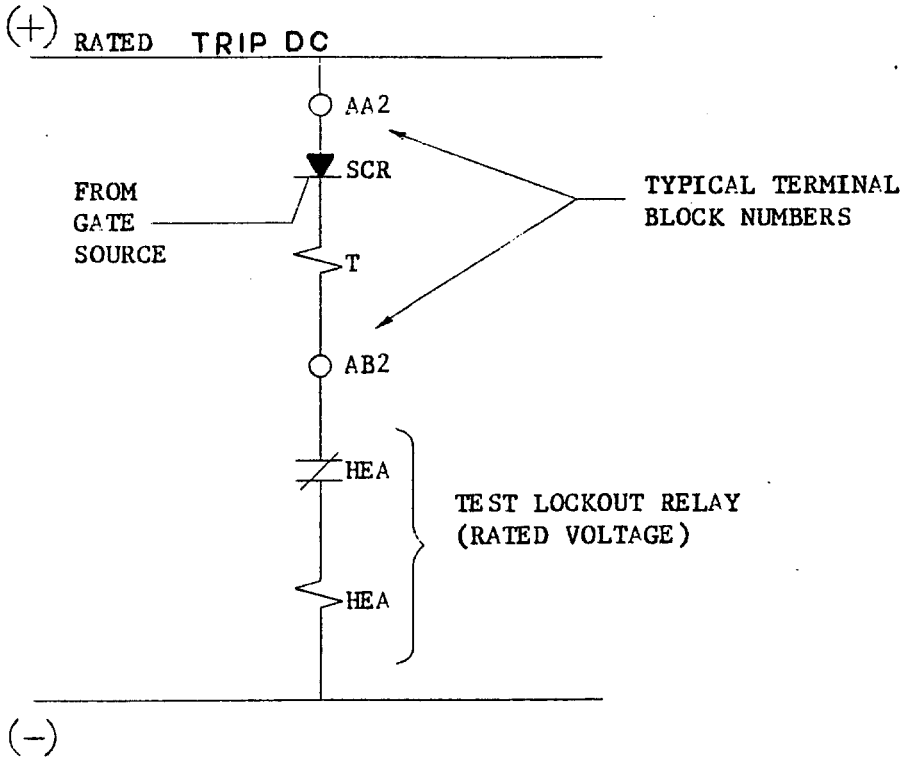


Figure 8 (0208A2365) Typical SCR Trip Circuit Test Connections

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