INSTRUCTIONS

GEK- 34080A

STATIC SEQUENCE OVERCURRENT RELAY

TYPE SLC52A

POWER SYSTEMS MANAGEMENT DEPARTMENT

GENERAL ELECTRIC

CONTENTS

DESCRIPTION

The Type SLC52A relay is a static sequence overcurrent relay designed to provide overcurrent blocking and tripping functions. The SLC52A is packaged in one 4 rack unit case for which the outline and mounting dimensions are shown in Figure 1. Component and card locations are shown in Figure 2. The internal connections for the SLC52A are shown in Figure 3.

The SLC52A is not designed to be used by itself, but rather as a part of a complement of relays that forms a protective relaying scheme. A Type SLYP relay must be present to provide the positive sequence current input quantity; a Type SLYN relay provides the negative sequence quantity. A Type SSA power supply must also be present to provide the ±15 VDC required by the static logic circuits. The SLC52A relay outputs are DC logic signals that feed into a Type SLA logic relay whose circuitry depends upon the overall protection scheme. For a complete description of the overall scheme in which the relay is employed, refer to the overall logic diagram and its associated logic description which is supplied with each terminal of equipment.

APPLICATION

The SLC52A static sequence overcurrent relay, in conjunction with the SLYP and SLYN relays, is intended primarily for protection of series compensated lines in a combined blocking and direct underreaching transfer trip scheme, with the potential source located on the line side of the series capacitors.

The I_1T and I_1B positive sequence overcurrent functions are used for current supervision of the positive sequence trip and blocking distance functions, respectively, in the SLYP relay. The overcurrent supervision is primarily intended to prevent outputs of the positive sequence distance functions during the de-energizing transients on lines with shunt reactors. However, the I_1T function may provide security for potential failure if the application permits settings above load current.

The I_1T_D function is designed for direct tripping of the circuit breakers to provide very fast tripping on very heavy three phase fault currents. For those applications where the terminal under consideration is considered a "weak infeed", the I_1T_D may have to be set below the maximum through fault current for a fault behind the relay in order to provide protection for a bolted three phase fault in front of the relay terminal when energizing the line. For the latter application, the I_1T_D function can be supervised by the "line pickup" circuitry in the SLA by appropriate matrix point connections. If the minimum infeed current is below the maximum load current and high speed reclosure is employed at both terminals, the supervised I_1T_D trip circuit should incorporate a time delay to provide co-ordination between the operate time of the I_1T_D function on load current and the operate time of V_1 on the unfaulted system positive sequence voltage.

The I_2T function provides co-ordination with the negative sequence directional function, D_2R, at the remote terminal on the basis of negative sequence current, and hence is used to supervise the negative sequence distance trip function, L_2T, and the zero sequence overcurrent trip function, $(I_0\text{-}KI_1)T$.

The I_2T_D is intended to provide high speed direct tripping of the circuit breakers on heavy phase to phase fault currents.

$(I_0\text{-}KI_1)_B$, the zero sequence blocking function, and $(I_0\text{-}KI_1)_T$, the zero sequence trip function, utilize positive sequence current restraint to minimize operation on current transformer error currents or on the zero sequence currents that may result from unsymmetrical gap flashing on series compensated lines.

$(I_0\text{-}KI_1)_D$, the zero sequence direct trip function, provides high speed tripping on heavy single and double line to ground fault currents. The use of positive sequence restraint tends to provide a larger margin between the net operating quantities on internal and external faults. The larger margin results from the normally higher ratio of the zero sequence line impedance to the positive sequence line impedance, when compared to the ratio of the zero sequence to positive sequence "source" impedances at each end of

the line. The positive sequence restraint tends to be more effective on long, series compensated lines.

On lines where the through fault current is much larger in one direction than the other, the $(I_0-KI_1)_D$ function may be supervised by the negative sequence directional function in the associated SLYN. However, it is suggested directional supervision only be used where it serves a useful purpose.

The zero sequence directional functions, D_{0F} and D_{0R}, are used to provide maximum protection for "broken conductor" faults, i.e. when a conductor breaks and is grounded on only one side of the break. In general, the D_{2F} and D_{2R} directional functions will work for the large majority of "broken conductor" faults.

CALCULATION OF SETTINGS

I_1T FUNCTION

I_1T should be set for 2/3 of the minimum fault current for which the positive sequence distance functions must operate.

I_1B FUNCTION

I_1B should be set for 50% of the I_1T setting.

I_1T_D FUNCTION

I_1T_D should be set for at least 125% of the maximum through positive sequence fault current or load current on a line where there are no series capacitors in the line or the source impedances. If there are series capacitors in the line or source impedances, the low frequency transients in the fault current require a minimum setting of 150% of the maximum steady state value of the positive sequence through fault or load current.

If there are series capacitors in the line under consideration, or adjacent to the bus at either end, the maximum through fault current may be limited by flashing of the series capacitor gaps. For the case where the fault current is limited by the capacitor gaps I_1T_D should be set for at least 125% of the steady state current that will flash the gaps. After the gaps are flashed, the fault current should be recalculated with the capacitors out of service, and the I_1T_D should be set for at least 150% of this latter current. The I_1T_D should be set at the higher of the two calculated settings.

If the I_1T_D is used with line pickup supervision, it should be set above 150% of the maximum through load current, (if high speed reclosing at both ends is employed) and equal or below 2/3 of the minimum fault current for a bolted 3 phase fault in front of the relay terminal. If these two settings are incompatible, then the I_1T_D can be set below the load current with an appropriate time delay to allow the V_1 function to reset the line pickup supervision for non fault conditions.

I_2T FUNCTION

I_2T should be set for 2/3 of the minimum negative sequence fault current for which the negative sequence trip function and the zero sequence trip function are intended to operate. I_2T must also be set to co-ordinate with D_2R at the remote terminal, the sensitivity of D_{2R} being 0.2^A negative sequence current; i.e. 4/3 (.2) + $I_{2\ SHUNT\ Z}$; where $I_{2\ SHUNT\ Z}$ is the negative sequence current in the line shunt impedance for an external fault. The shunt impedance is the parallel impedance of the shunt capacitance and the shunt reactors if they are electrically within the protected zone. It is often difficult to establish the magnitude of $I_{2\ SHUNT\ Z}$, and a conservative estimate is the use 1/2 the net positive sequence charging current of the unfaulted line.

I_2T_D FUNCTION

I_2T_D can be set for 125% of the maximum through negative sequence fault current on lines without series capacitors either in the line or the source impedances.

For series compensated lines or sources the same calculations made for I_1T_D can be used to obtain settings for the I_2T_D. For co-ordination with the series capacitor gaps, I_2T_D should be set for 75% of the steady state gap flashover, and for co-ordination on through fault currents with low frequency transients after the gaps flash, 75% of the calculated through three phase fault current.

$(I_o\text{-}KI_1)_T$ FUNCTION

$(I_o\text{-}KI_1)_T$ should be set for 2/3 of the minimum fault current at the remote end of the line with the remote breaker open when used in the combined blocking and direct transfer trip scheme. It is proposed that the restraint factor (K) will provide a good balance between dependability and security when set for 0.15.

It is possible that some confusion may arise from the terminology of the $(I_o\text{-}KI_1)$ functions. The formula is given in terms of the sequence quantities since fault study data is usually in this form. However, the range of the functions are given in terms of 3 $(I_o\text{-}KI_1)$ since $3I_o$ would normally be used in calibrating and testing the function.

$(I_o\text{-}KI_1)_B$ FUNCTION

$(I_o\text{-}KI_1)_B$ should be set to co-ordinate with $(I_o\text{-}KI_1)_T$ on through fault currents, i.e. the setting of $(I_o\text{-}KI_1)_B$ should be no larger than 3/4 of the setting of $(I_o\text{-}KI_1)_T$ minus the zero sequence current in the shunt impedance for an external fault. The zero sequence current in the shunt impedance can be ignored if the shunt impedance is inductive. For uncompensated lines, a zero sequence voltage of 0.6 per unit would provide a conservative basis for calculating I_o is the shunt impedance. For compensated lines, the zero sequence voltage may be higher, particularly for a fault near a switching station with only series compensated lines connected to it. For this case, it is suggested that the zero sequence voltage be obtained from fault studies.

The suggested restraint factor (K) setting is 2/3 of the restraint factor setting for $(I_o\text{-}KI_1)_T$, or K = .1 for $(I_o\text{-}KI_1)_B$.

$(I_o\text{-}KI_1)_D$ FUNCTION

In setting $(I_o\text{-}KI_1)_D$ on uncompensated lines, the setting should be based on the maximum through fault current, with a safety margin based on 25% of the maximum zero sequence through fault current. On series compensated lines, the safety margin should be increased to 50% of the maximum zero sequence through fault current.

In many applications, the maximum value of $(I_o\text{-}KI_1)$ on through fault currents may be a net restraint. For this case, it is proposed that $(I_o\text{-}KI)_D$ be set based on a fault at the remote end of the line with the remote end open.

The setting of $(I_o\text{-}KI_1)_D$ tends to be complex when considering a series compensated line with series capacitors on adjacent lines. In general, the quantity $(I_o\text{-}KI_1)$ will tend to be largest when:

(a) the ratio of Z_o/Z_1 at the fault is large
(b) the zero sequence source behind the line terminal remote from the fault is small
(c) the positive sequence impednace of the line and the positive sequence source impedance behind the terminal remote from the fault is larger
(d) load flow is relatively high

In general, the positive sequence current restraint results when set in the order of 0.3.

RATINGS

The Type SLC52A relay is designed for use in an environment where the air temperature outside the relay case does not exceed 65°C.

The Type SLC52A relay requires a ±15 VDC power source which can be obtained from a Type SSA power supply.

The current circuits of the Type SLC52A relay are rated at 5 amperes, rated frequency,for continuous duty and have a one second rating of 300 amperes.

BURDENS

DC BURDEN

The SLC52A relay presents a maximum burden to the Type SSA power supply of:

350 ma from the (+) 15 VDC supply
100 ma from the (-) 15 VDC supply

CURRENT BURDEN

OPERATING CIRCUIT

	3	1
R	.0014	
X	.0143	
Z	.0143	

POLARIZING CIRCUIT

	3	1
R	.0014	
X	.0143	
Z	.0143	

OVERCURRENT FUNCTIONS

The Type SLC52A relay may include all or some of the functions listed below. Refer to unit nameplate to determine which functions and ranges are supplied on a particular SLC52A.

I_1B - Positive Sequence blocking function.

I_1T - Positive Sequence tripping function.

I_1T_D- Positive Sequence direct trip function.

I_2B - Negative Sequence blocking function.

I_2T - Negative Sequence tripping function.

I_2T_D - Negative Sequence direct trip function.

$(I_0-KI_1)_B$- Zero Sequence blocking function.

$(I_0-KI_1)_T$- Zero Sequence tripping function.

$(I_0-KI_1)_{T_D}$-Zero Sequence direct trip function.

D_0F , D_0R - Current Polarized Zero sequence directional units.

The pickup current ranges of the zero sequence units are given for the 3Ω base reach tap. If the 1Ω base reach tap is used, the pickup ranges should be multiplied by three.

CONSTRUCTION

The SLC52A relay is packaged in an enclosed metal case with hinged front cover and removable top cover. The case is suitable for mounting on a standard 19 inch rack. The outline and mounting dimensions of the case and the physical location of the components are shown in Figures 1 and 2 respectively.

The terminal strip for making the AC current connections is located on the rear panel of the unit. The logic connections to the SLC52A are made on ten point plugs on the rear of the unit. The logic units are interconnected by means of ten conductor shielded cables.

The SLC52A relay also contains printed circuit cards identified by a code number such as F112, T105, L111, N105 where F designates filter, T designates time delay, N designates network, and L designates logic. The printed circuit cards plug in from the front of the unit. The sockets are identified by letter designations or "addresses" (D, E, F, etc.) which appear on the guide strips in front of each socket, on the component location diagram, on the internal connection diagram and on the printed circuit card itself. The test points (TP1, TP2, etc.) shown on the internal connection diagram are connected to instrument jacks on a test card in position T or AT with TP1 at the top of the AT card and TP11 at the top of the T card. The internal connections of the printed circuit cards are shown in the Printed Circuit Card Instruction Book GEK-34158.

RECEIVING, HANDLING AND STORAGE

These relays will normally be supplied as a part of a static relay equipment, mounted in a rack or cabinet with other static relays and test equipment. Immediately upon receipt of a static relay equipment, it should be unpacked and examined for any damage sustained in transit. If injury or damage resulting from rough handling is evident, file a damage claim at once with the transportation company and promptly notify the nearest General Electric Sales Office.

Reasonable care should be exercised in unpacking the equipment. If the equipment is not to be installed immediately, it should be stored indoors in a location that is free from moisture, dust, metallic chips, and severe atmospheric contaminants.

Just prior to final installation the shipping support bolt should be removed from each side of all relay units to facilitate possible future unit removal for maintenance. These shipping support bolts are approximately eight inches back from the relay unit front panel. Static relay equipment, when supplied in swing rack cabinets, should be securely anchored to the floor or to the shipping pallet to prevent the equipment from tipping over when the swing rack is opened.

INSTALLATION TESTS

The Type SLC52A relay is usually supplied from the factory mounted and wired in a static relay equipment. The following checks and adjustments should be made by the user in accordance with the procedures given under DETAILED TESTING INSTRUCTIONS before the relays are put into service.

1. Overcurrent function pickup current level.
2. Timer settings.

GENERAL TESTING INSTRUCTIONS

A. INPUT CIRCUITS

The I_1Z and I_2Z input quantities are derived in the associated Type SLYP and Type SLYN relays. These signals enter the SLC52A relay on ten conductor shielded cables; the cable sockets are located on the rear panel of the unit. In order to obtain the proper values of I_1Z and I_2Z from the SLYN and SLYP relays, it is necessary to follow the test procedure described in the instruction books for the associated relays. If the SLC52A relay is not part of a static equipment, the I_1Z and I_2Z quantities may be supplied by means of the test circuit in Figure 4. The test circuits are described in the DETAILED TESTING INSTRUCTIONS SECTION.

B. OUTPUT SIGNALS

Operation of the SLC52A unit can be checked by observing the signals at the twenty test points (TP1 to TP20) in the SLC52A. These test points are located on two test cards in positions T and AT and are numbered 1 to 20 from top to bottom. TP1 is the reference bus for the logic circuits, TP2 is at (-) 15 VDC and TP10 is at (+) 15 VDC. The remaining points are located at various strategic points throughout the logic as shown on the internal connections diagram (Figure 3). Test point voltages can be monitored with a portable high impedance voltmeter, the voltmeter on the test panel of the associated equipment, or an oscilloscope.

Logic signals are approximately (+) 15 VDC for the ON or LOGIC ONE condition, and less than 1 VDC for the OFF or LOGIC ZERO. The D_0F-D_0R filter card in position AL produces outputs which are (+) 15 VDC to (-) 15 VDC square waves.

When the time delay cards are to be adjusted or checked, an oscilloscope which can display two traces simultaneously and which has a calibrated horizontal sweep should be used.

DETAILED TESTING INSTRUCTIONS

A. TIMER ADJUSTMENTS AND TESTS

In order to test the timer cards, it is necessary to remove the card which drives the timer and to place the timer card in a card adapter. The timer test circuit is shown in Figure 5. Opening the N.C. contact causes the output to step up to (+) 15 VDC after the pickup delay of the timer. To increase the pickup time, turn the upper potentiometer on the timer card clockwise. Closing the contact causes the timer output to drop to less than (+) 1 VDC after the reset time delay setting of the card. The reset time delay can be adjusted by the lower potentiometer on the timer card (clockwise increases the reset time).

In order to check the T107 timer in position AP, a slightly modified procedure must be followed. To adjust the shorter pickup time, the test circuit of Figure 5 can be used to adjust the pickup setting; however, the output must be measured at Pin 7 rather than Pin 8. The pickup time can be set by means of the P2 potentiometer. The longer pickup time is adjusted at the factory to provide a pickup time 1.2 ms longer than the shorter pickup time. The pickup, and also the dropout delay, can be checked by using the test circuit of Figure 5 and observing the output at Pin 8. The pickup is adjusted by potentiometer P1, the dropout by potentiometer P3.

B. POSITIVE AND NEGATIVE SEQUENCE CURRENT LEVEL DETECTORS

The I_1T, I_1T_D, I_1B, I_2T, I_2T_D and I_2B functions may all be checked by means of the test set up shown in Figure 6. Since the I_1Z and I_2Z quantities are derived from the associated Type SLYP and Type SLYN relays, these relays must be calibrated before the SLC may be tested. The test current, read on the ammeter, must be set to equal 1.73 I_1 or 1.73 I_2 where I_1 and I_2 are the desired positive and negative sequence current levels. When the test current is adjusted to the proper level, the potentiometer on the card must be adjusted so that the function output, measured at the associated test jack, just picks up. Turning the potentiometer clockwise increases the pickup level of the function.

The reset delay incorporated in these functions is non-adjustable. In order to check the reset delay, it is necessary to remove the N105 card from position D and place the level detector card in a card adapter. The function may then be checked as a timer using the test circuit of Figure 5.

C. ZERO SEQUENCE CURRENT LEVEL DETECTORS

The $(I_0-KI_1)T$, $(I_0-KI_1)T_D$ and $(I_0-KI_1)B$ functions may all be checked by means of the test set up shown in Figure 7a and 7b. The timers associated with these functions should be adjusted using the procedure described above.

The two step procedure described below should be used to check and adjust the Zero Sequence Level Detectors.

STEP 1

Using the test circuit of Figure 7a, adjust the 3Io test current to the desired 3Io pickup level. Adjust the P2 potentiometer on the associated amplitude comparator card until the function just picks up at the desired current (observe the output at the test point after the associated timer). Turning P2 clockwise increases the pickup level.

STEP 2

Using the test circuit of Figure 7a and 7b, adjust the test current (I_{TEST}) to a value determined by the following equation:

$$I_{TEST} = \frac{\text{3Io test current - 3Io pickup current}}{\sqrt{3}\ K}$$

where:

K is the desired portion of the positive sequence used as restraint.

The $3I_0$ pickup current is set in Step 1.

The $3I_0$ test current is set equal to some multiple of $3I_0$ pickup current determined by Table I.

TABLE I

$3I_0$ PICKUP LEVEL (PUL)	$3I_0$ TEST CURRENT
.3 - 1 AMP	2 X PUL
1 - 5 AMP	1.5 X PUL
5 - 20 AMP	1.1 X PUL

The P1 potentiometer should be adjusted so that the function just picks up for the desired value of test current. Turning P1 clockwise increases K and decreases the value of I_{TEST} needed to keep the function from operating.

D. ZERO SEQUENCE DIRECTIONAL UNITS

The D_0F and D_0R functions may be checked by means of the test set up shown in Figure 8 and the connections shown in Table II. The timers associated with these functions should be adjusted using the procedure described above. There are no pickup level adjustments for the D_0F and D_0R functions.

TABLE II

FUNCTION	CONNECTIONS				READ	READ
	A	B	C	D	+15 VDC	0 VDC
D_0F	RA5	RA7	RA8	RA10	TP4	TP6
D_0R	RA7	RA5	RA8	RA10	TP6	TP4

E. 3Io BASE REACH TAP SELECTION

The base reach tap setting is made on the terminal strip on the rear of the unit. The polarizing quantity taps are RA6 (1Ω) and RA7 (3Ω); the operating quantity taps are RA9 (1Ω) and RA10 (3Ω).

MAINTENANCE

A. PERIODIC TESTS

For any periodic testing of the SLC52A, the trip coil circuit should be disconnected from the associated Type SLAT relay by opening the test switches provided for this purpose. The overcurrent operate levels may be checked at periodic intervals using the procedures under DETAILED TESTING INSTRUCTIONS. Cable connections between the SLC52A and the associated Type SLA relay may be checked by observing the test points in the SLA unit.

B. TROUBLE SHOOTING

In any trouble shooting of equipment, it should first be established which unit is functioning incorrectly. The overall logic diagram supplied with the equipment shows the combined logic of the complete equipment and the various test points in each unit. By signal tracing, using the overall logic diagram and the various test points, it should be possible to quickly isolate the trouble.

A test adapter card is supplied with each static relay equipment to supplement the prewired test points on the test cards. Use of the adapter card is described in the card instruction book GEK-34158.

A dual-trace oscilloscope is a valuable aid to detailed trouble shooting, since it can be used to determine phase shift, operate and reset times as well as input and output levels. A portable dual-trace oscilloscope with a calibrated sweep and trigger facility is recommended.

C. SPARE PARTS

To minimize possible outage time, it is recommended that a complete maintenance program should include the stocking of at least one spare card of each type. It is possible to replace damaged or defective components on the printed circuit cards, but great care should be taken in soldering so as not to damage or bridge-over the printed circuit busses, or overheat the semi-conductor components. The repaired area should be recovered with a suitable high-dielectric plastic coating to prevent possible breakdowns across the printed busses due to moisture and dust. The wiring diagrams for the cards in the SLC52A relay are included in the card book GEK-34158.

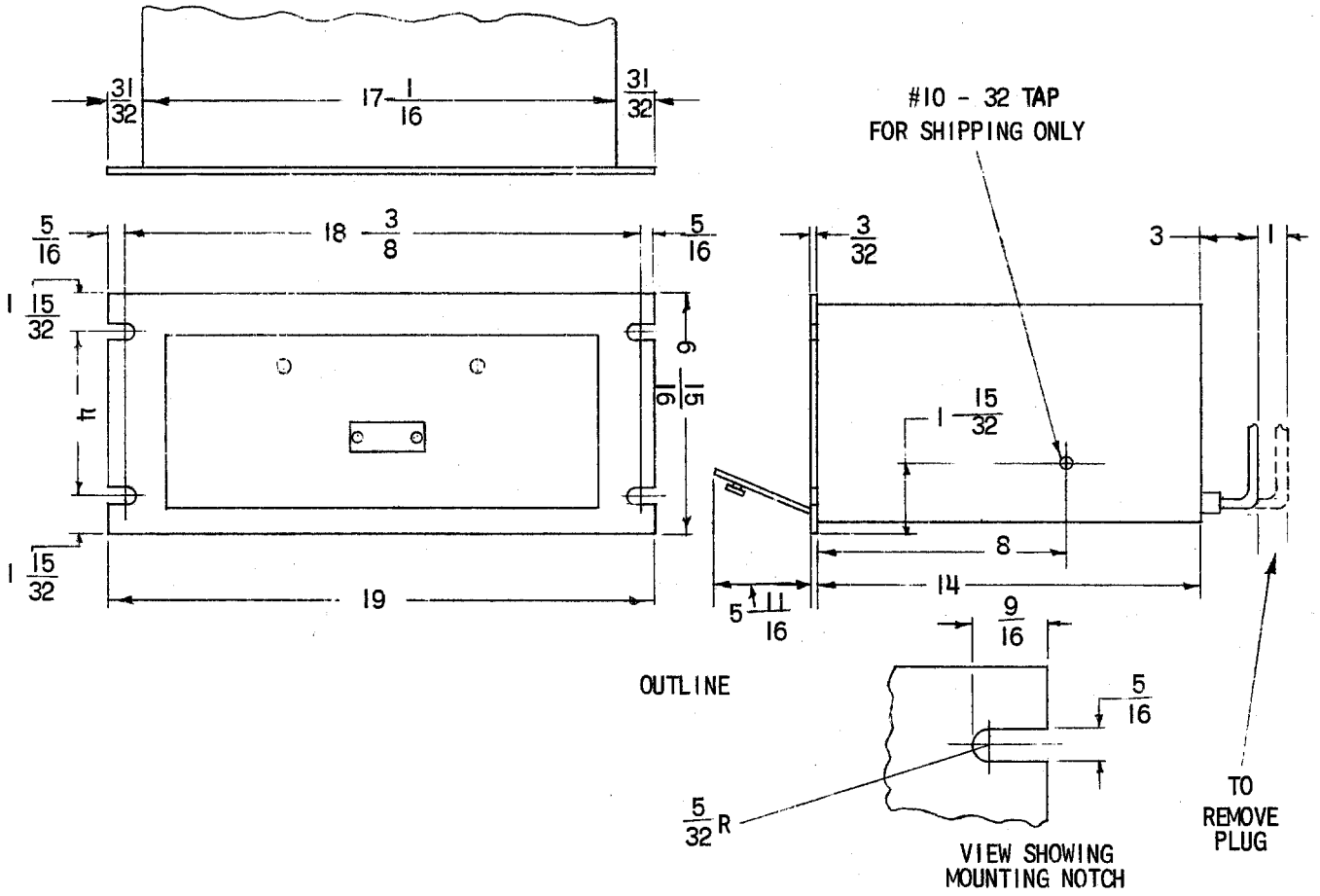


FIG. 1 (0227A2037-0) Outline And Mounting Dimensions For The Type SLC52A Relay

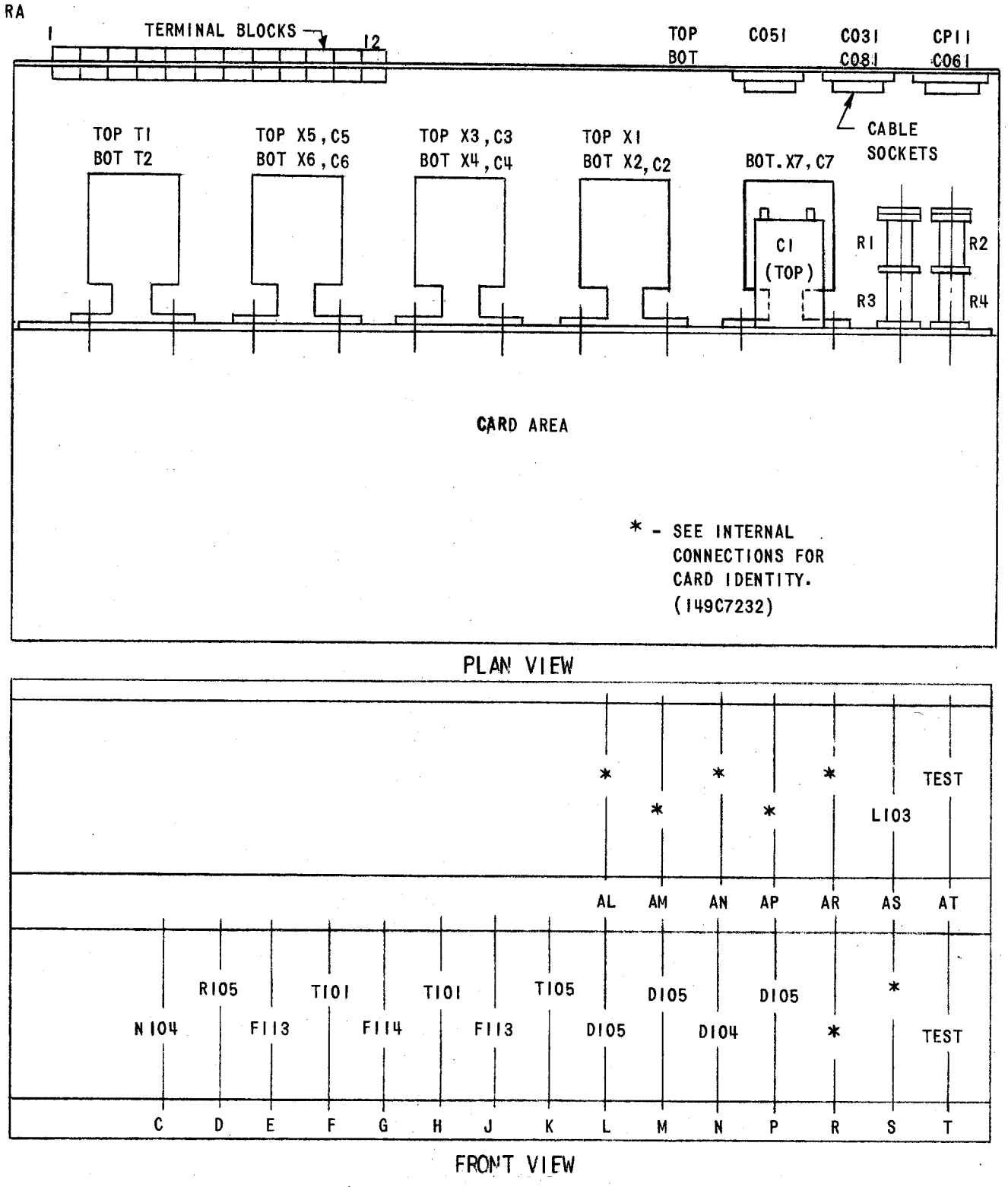


FIG. 2 (0246A3566-2) Component And Card Locations For The Type SLC52A Relay

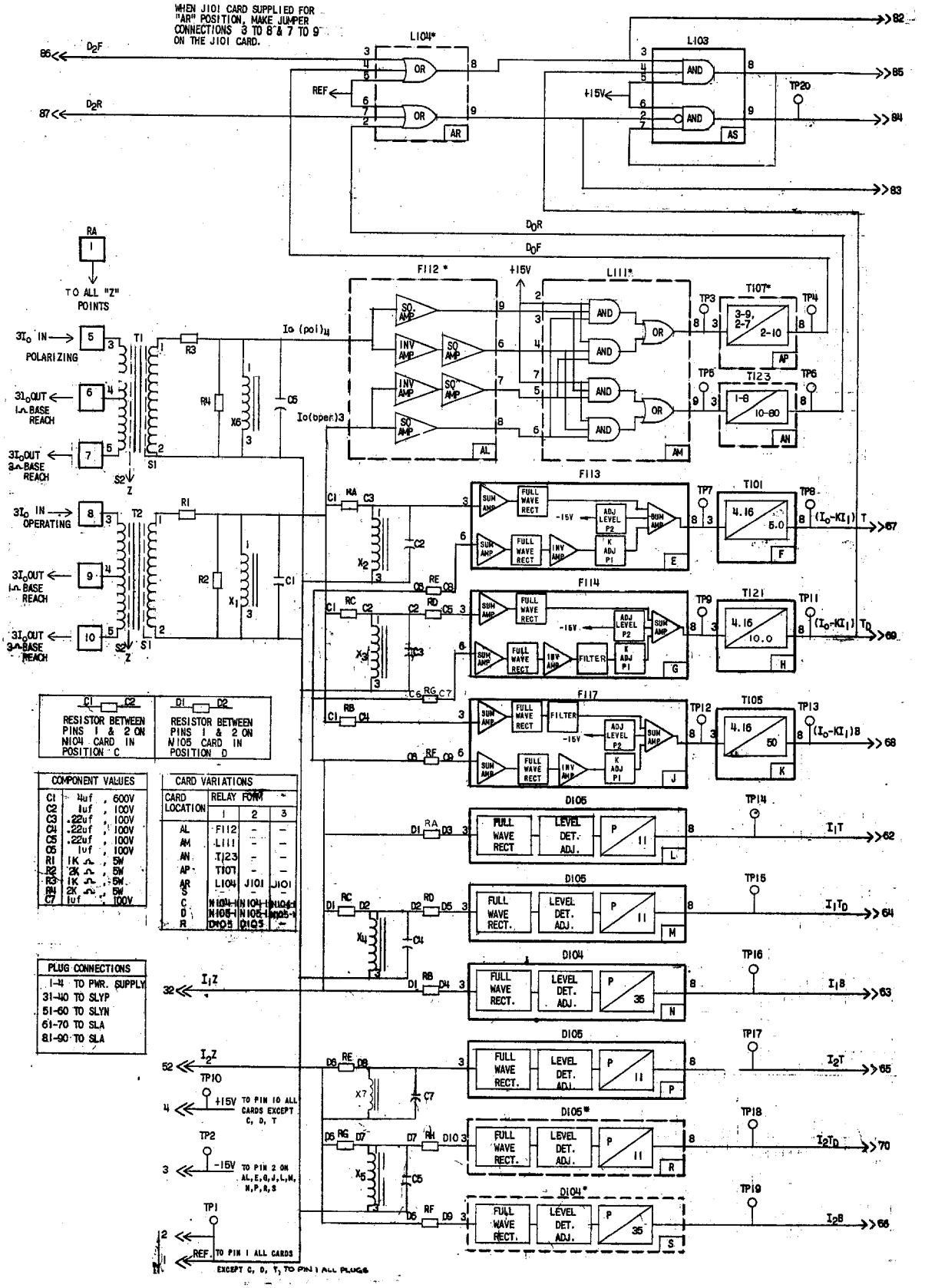
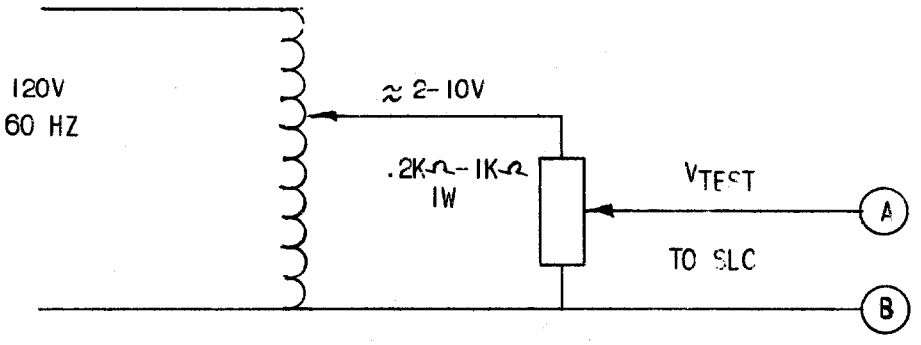


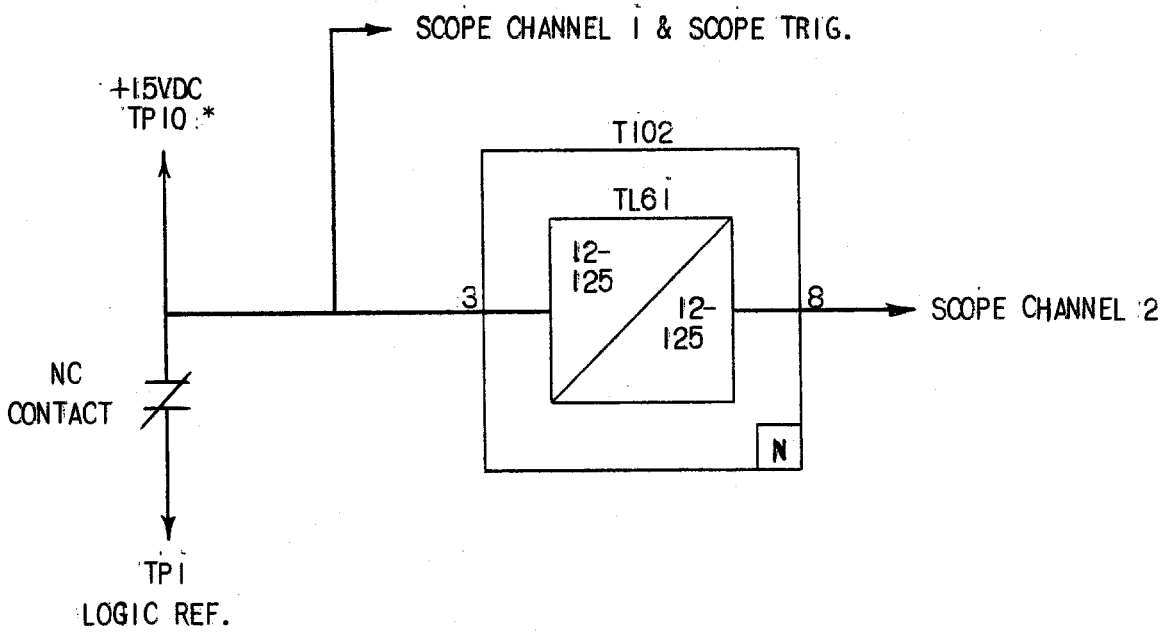
FIG. 3 (0149C7232-9) Internal Connections For The Type SLC52A Relay



CURRENT	A	B
I_1 Z	C032	C031
I_2 Z	C052	C051

NOTE 1: V_{TEST} MUST BE SET TO EQUAL THE VOLTAGE AT C032 OR C052 IN THE ASSOCIATED SLYP OR SLYN RELAY AT THE DESIRED POSITIVE OR NEGATIVE SEQUENCE CURRENT.

FIG. 4 (0227A2118-0) Test Circuit For Testing SLC52A Without SLYP Or SLYN Relays



* THE 15VDC SIGNAL AT PIN 10 HAS A CURRENT LIMITING RESISTOR MOUNTED ON THE TEST CARD.

FIG. 5 (0246A7987-0) Logic Timer Test Circuit

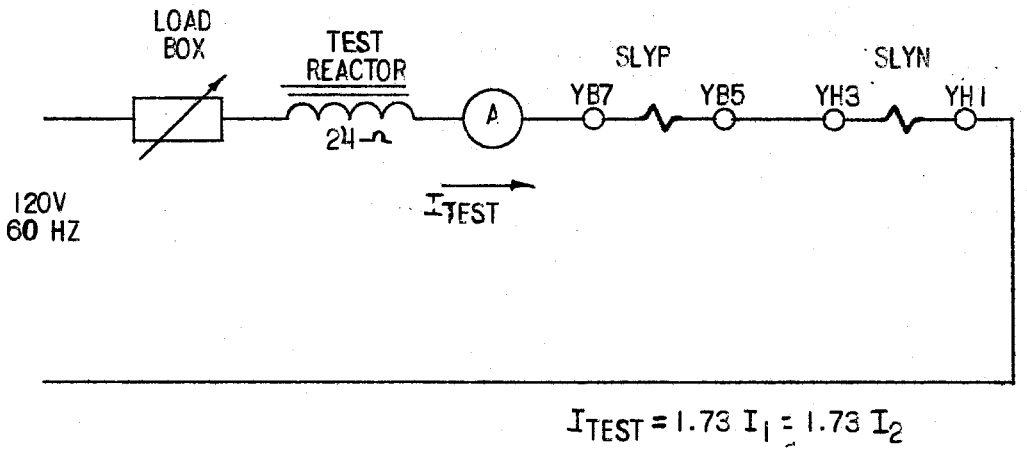
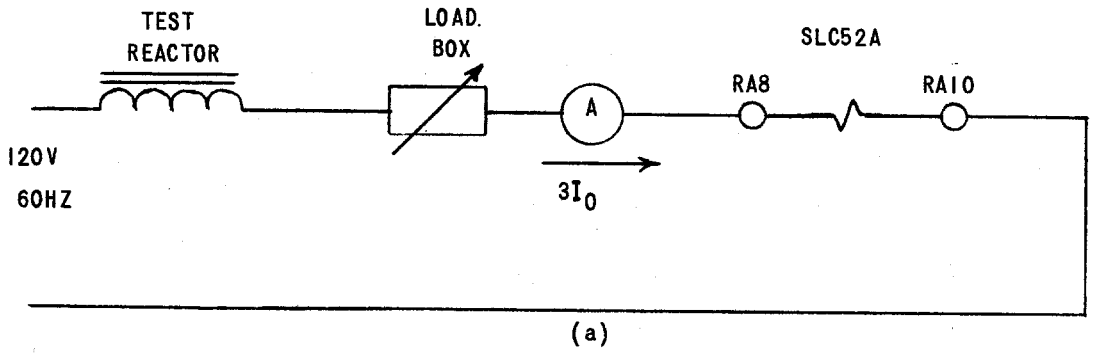
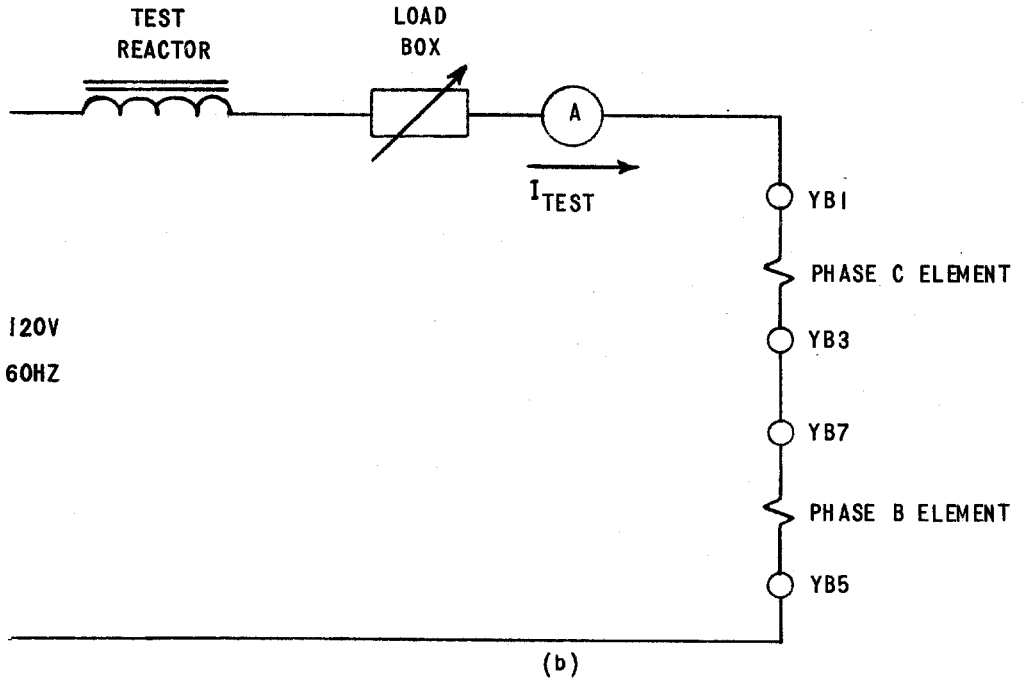


FIG. 6 (0227A2121-0) Test Circuit For The Positive And Negative Sequence Current Level Detectors



(a)



(b)

NOTES

1. SET TEST REACTOR ON HIGHEST OHMIC TAP WHICH WILL PERMIT DESIRED CURRENT LEVEL TO BE OBTAINED.
2. PHASE RELATIONSHIP BETWEEN SOURCES IS NOT CRITICAL.

FIG. 7 (0227A2129-1) Test Circuit For The Zero Sequence Current Level Detectors

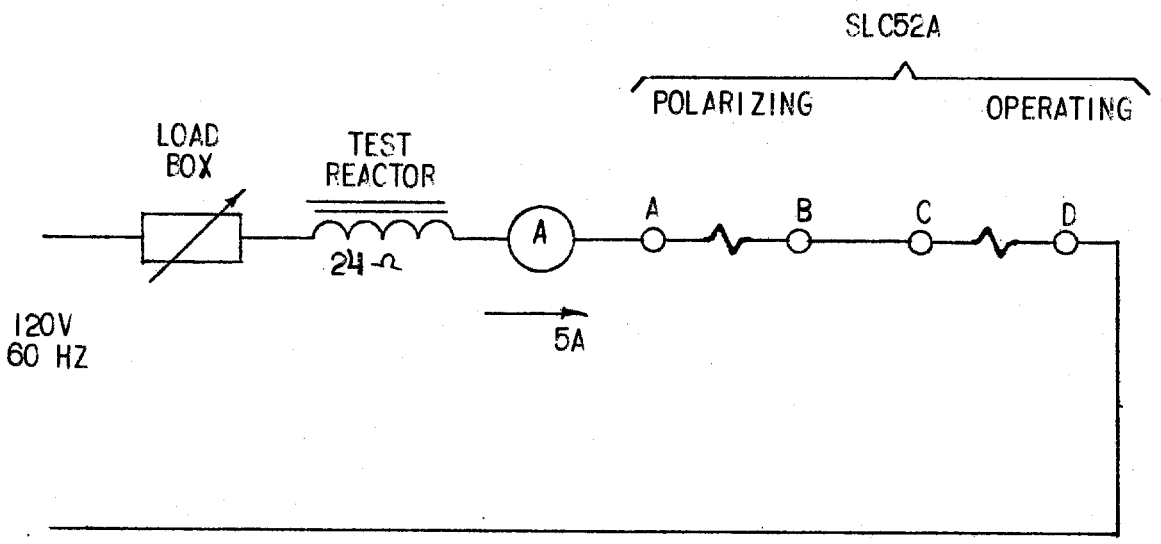


FIG. 8 (0227A2120-0) Test Circuit For The Zero Sequence Directional Units