INSTRUCTIONS

GEK-49779A

SUPERSEDES GEK-49779

OVERCURRENT RELAY

SLC51D

GENERAL ELECTRIC

CONTENTS

*Indicates Revision

OVERCURRENT RELAY

TYPE SLC51D

DESCRIPTION

The SLC51D is a static three phase and ground overcurrent relay which includes both direct tripping and supervising overcurrent functions for phase comparison line protection with phase distance back-up. The SLC51D relay is packaged in one two rack unit case. The outline and mounting dimension of this case is shown in Figure 1. Component locations are shown in Figure 2.

The outputs of the SLC51D are d-c logic signals to the SLA unit employed in the particular scheme. Regulated ±15V d-c power from the equipment SSA power supply is required for operation of the SLC51D circuits. The internal connections for the SLC51D are shown in Figure 3.

The following overcurrent functions are included in the SLC51D:

I3Ø - Three phase overcurrent fault detector for supervision of first and second zone phase distance functions.

PH4 - Three phase direct trip instantaneous overcurrent function.

I_M - Sensitive phase current detector for phase comparison keying control.

G4 - Ground direct trip instantaneous overcurrent function.

APPLICATION

The SLC51D static overcurrent relay is designed to provide the overcurrent required for phase comparison protection with phase distance relay back-up. For a complete description of the overall scheme in which the relay is employed, refer to the overall logic diagram and associated logic description supplied with the specific equipment.

The measuring functions included in the relay are intended for use as indicated below.

I3Ø

I3Ø is a three phase, non-directional overcurrent function that serves the following purposes:

(a) It provides a seal-in function that serves to keep the trip bus energized as long as I3Ø is picked up.

(b) It may be used to provide supervision to the phase mho tripping functions.

The seal-in (a) is required to insure that the trip bus and consequently the breaker failure initiate function (BFI) will remain energized during close-in (zero voltage) faults under a breaker failure condition. When I3Ø is used to provide the seal-in function alone, it must be set sensitive enough to detect the minimum close-in three phase fault. If I3Ø is used to provide supervision to the phase mho tripping functions, then it must be set to detect all faults in the protected line section, in which case the setting for seal-in purposes will automatically be met. Supervision of the phase mho functions by I3Ø is used to provide added security to the scheme and also to prevent undesired tripping by the phase mho functions if an a-c potential is suddenly lost. If the setting required for supervision purposes is above full load, then protection against undesired tripping on loss of a-c potential will be in effect at all times; otherwise, the protection will be only partially effective. It must be remembered that the phase mho functions could still produce undesired tripping if an external fault occurred during the time that the a-c potential is lost.

I3Ø responds to the highest of the three delta currents $I_1 - I_2$, $I_2 - I_3$ or $I_3 - I_1$. The response of I3Ø will be the same for three phase, phase-to-phase and double phase-to-ground faults at the same location.

PH4

PH4 is a three phase, non-directional, direct trip instantaneous overcurrent function that is intended to provide direct tripping for heavy multi-phase faults. The PH4 function must be set to operate at 125 percent or more of the maximum external three phase fault current. Because PH4 is non-directional, faults at the bus directly behind the relay as well as faults at the remote terminal must be considered. PH4, like I3Ø, responds to the delta currents; therefore, it too will have the same response for all multi-phase faults at the same location.

In setting PH4 and I3Ø, the minimum three phase fault current for which each of the functions is to operate should first be determined. Use 86 percent of the value so obtained and follow the instructions given under the section headed DETAILED TESTING INSTRUCTIONS to set the respective functions. With settings made on this basis, the respective functions will then respond to all multi-phase faults within the area for which the minimum three phase fault current was obtained.

G4

G4 is a zero sequence, non-directional, direct trip instantaneous overcurrent function that is intended to provide direct tripping for heavy ground faults. The G4 function must be set to operate at 125 percent or more of the maximum external ground fault current ($3I_0$). Because G4 is non-directional, it is necessary to consider faults at the bus directly behind the relay as well as at the remote terminal.

I_M

The I_M function is a sensitive phase current detector for keying control in the phase comparison protection. It has a fixed pickup of 0.2 amperes rms in any phase, and would therefore normally be picked up by load current any time the line breakers were closed. When I_M is picked up the keying of trip permission in the phase comparison scheme is under the control of the FDH and/or the squaring amplifier. When I_M is reset indicating that the associated line breaker is open a continuous channel keying signal is provided to permit tripping by the remote breaker.

The I_M function has no intentional delay on pickup, but incorporates a 35 millisecond reset delay to assure reset coordination with the FDH trip level fault detector at the remote terminal during fault clearing. Refer to the logic diagram and description for the particular SLD scheme for details of the operation of the phase comparison with the I_M detector.

RATINGS

The Type SLC51D relays are designed for use in an environment where the air temperature outside the relay case does not exceed -20°C or +65°C.

The current circuits of the Type SLC51D relay are rated at 5 amperes, 60 cycles, for continuous duty and have a one second rating of 300 amperes.

The range of adjustment of the functions in the Type SLC51D relay are listed below:

I_M - 0.2 amperes
G4 - 2.5 to 40 amperes
I3Ø - 1 to 15 amperes
PH4 - 5 to 80 amperes

BURDENS

The current burden measured at 5 amps line current is as follows:

Phase Current Burden - R = 0.24, X = 0.155, Z = 0.286 $\angle$ 33°

Neutral Burden - R = 0.009, X = .006, Z = 0.011 $\angle$ 33°

OPERATING PRINCIPLES AND CHARACTERISTICS

The functions in the SLC51D are non-directional overcurrent functions of which G4 is adjustable and operates on residual current, I3Ø and PH4 are adjustable and operate on the highest phase-to-phase current and I_M is non-adjustable and operates on the highest phase current.

CIRCUIT DESCRIPTION

The internal connection diagram of the SLC51D relay (Figure 3) shows the current inputs on the left side, the small squares denote the specific points on the "RA" terminal board at the rear of the unit. The double arrow points on right side represent the plug connections between relay units.

The input currents are passed through transactors whose output voltages are controlled by secondary loading set at the factory. These voltages are filtered, full wave rectified and fed to the level detectors. The detector output pulses are stretched to provide continuous output logic signals routed to the SLA logic unit via cable C071.

CONSTRUCTION

The Type SLC51D relay is packaged in a metal enclosure designed for mounting on a 19 inch rack. The relay is two rack units high (one rack unit is 1 3/4 inches) and has a 90 degree hinged front cover and removable top cover. It contains the magnetics, filtering and printed circuit cards required to provide the phase and ground overcurrent functions previously listed.

The operating level of the overcurrent function is adjustable via a potentionmeter mounted on the printed circuit card associated with the function. (The printed circuit card associated with the I_M function has no potentiometer.) The card identification, such as D102, and its position denoted by a letter in the small square at the lower right corner is shown on the unit internal Figure 3. One test card is included at the extreme right position "T". Test point #1 at the top of the card is connected to relay reference; TP10 at the bottom of the card is connected to the +15 VDC bus. Other test points are located at select points within the logic circuitry to permit test measurement of the various functions and facilitate troubleshooting.

The potentiometers located to the left of the printed circuit cards are factory set to provide the range of operation of the associated overcurrent function.

RECEIVING, HANDLING AND STORAGE

This relay will normally be supplied as a part of a static relay equipment, mounted in a rack or cabinet with other static relays and test equipment. Immediately upon receipt of a static relay equipment, it should be unpacked and examined for any damage sustained in transit. If injury or damage resulting from rough handling is evident, file a damage claim at once with the transportation company and promptly notify the nearest General Electric Sales Office.

Reasonable care should be exercised in unpacking the equipment. If the equipment is not to be installed immediately, it should be stored indoors in a location that is free from moisture, dust, metallic chips, and severe atmospheric contaminants.

Just prior to final installation the shipping support bolt should be removed from each side of all relay units, to facilitate possible future unit removal for maintenance. These shipping support bolts are approximately eight inches back from the relay unit front panel. Static relay equipment, when supplied in swing rack cabinets, should be securely anchored to the floor or to the shipping pallet to prevent the equipment from tipping over when the swing rack is opened.

INSTALLATION TESTS

The Type SLC51D relay is usually supplied from the factory mounted and wired in a static relay equipment.

All units of a given terminal have been calibrated together at the factory and will have the same summary number on the unit nameplates.

These units must be tested and used together.

NECESSARY ADJUSTMENTS

The following checks and adjustments should be made by the user in accordance with the procedures given below under DETAILED TESTING INSTRUCTIONS, before the relays are put in service. Some of the following items

are checks of factory calibrations and settings, or installation connections and hence do not normally require readjustment in the field. Other items cover settings or adjustments which depend on the transmission line, and hence must be made on location. These functions are:

1. G4, Overcurrent operating levels
2. PH4 and I3Ø Overcurrent operating levels
3. I_M Overcurrent operating level

GENERAL TESTING INSTRUCTIONS

INPUT CIRCUITS

The Type SLC51D relay has a terminal block on the rear of the unit identified as "RA". In a static relay equipment the terminal block is usually wired to the test panel where input currents can be supplied through the standard Type XLA test plug. Where other test facilities are used, input currents should be applied to test points which connect to the same RA terminal points as those shown on the job elementary.

OUTPUT SIGNALS

Output signals are measured with respect to the reference bus or TP1. Outputs are continuous signals of approximately +12 to +15 volts for the "ON" condition and 0 volts for the "OFF" condition. This output can be monitored with an oscilloscope, a portable high impedance d-c voltmeter, or with the test panel voltmeter if available. To connect the test panel voltmeter, place the test lead in the proper test point pin jack and the other end in the pin jack on the test panel.

DETAILED TESTING INSTRUCTIONS

REQUIRED ADJUSTMENTS

The overcurrent function settings may be made and tested using a single phase test source. A possible test circuit is shown in Figure 4 with the input connections for the SLC51D given below in Table I.

CAUTION:

THIS RELAY IS RATED AT 5 AMPERES CONTINUOUS DUTY. TO SET FOR HIGHER CURRENT LEVELS, APPLY TEST CURRENT TO THE RELAY ON MOMENTARY BASIS (APPROXIMATELY ONE SECOND).

To set the test circuit for higher current levels it is recommended that a resistance be connected between points "A" and "B" of Figure 4. The value of the resistance should be equal to the impedance of the alternating current circuit to be tested (see above). When the desired current level is established, remove the resistor and connect the relay per Table I. Momentarily apply test current and monitor the output. Adjust the proper potentiometer for the desired operating point (clockwise pot rotation raises the operating point).

TABLE I

FUNCTION	CONNECT "RA" TERMINALS TO TEST CKT POINTS			MONITOR OUTPUT AT	ADJ. POT ON CARD
	A	B	JUMPER		
G4	5	6	–	TP5	"P"
I_M, Ø1	7	8	–	TP8	"N"**
I_M, Ø2	9	10	–	TP8	"N"**
I_M, Ø3	11	12	–	TP8	"N"**
PH4, Ø1-2	7	9	8 TO 10	TP7	"S"
I3Ø, Ø1-2	7	9	8 TO 10	TP6	"R"
PH4, Ø2-3	9	11	10 to 12	TP7	***
I3Ø, Ø2-3	9	11	10 TO 12	TP6	***
PH4, Ø3-1	11	7	12 TO 8	TP7	***
I3Ø, Ø3-1	11	7	12 TO 8	TP6	***

**There is no potentiometer on the printed circuit card in position "N".
***PH4 and I3Ø level detectors operate on the highest phase-to-phase current input; if operating point differences are observed, calibration procedure is described below.

*Indicates revision

CALIBRATION

The SLC51D relay calibration may be checked by applying a reactance limited single phase current per Figure 4 and Table II. Use of the card adapter will provide access to the required measurement points.

TABLE II

FUNCTION	CONNECT "RA" TERMINALS TO TEST CKT. POINTS			I in (AMPS)	ADJ.	MEASURE PIN 3 TO PIN 1	
	A	B	JUMPER			CARD	VOLTAGE
G4	5	6	--	10.0	P3	P	1.4 Vrms
I3Ø Ø1-2	7	9	8 TO 10	1.0	P4	R	0.58 Vo-p
I3Ø Ø2-3	9	11	10 TO 12	1.0	P5	R	0.58 VO-p
I3Ø Ø3-1	11	7	12 TO 8	1.0	P6	R	0.58 Vo-p

The PH4 card input voltage (pin 3 to pin 1 of "S" card) with 5 amps applied at any of the above I3Ø connections should be 0.45 to 0.55 volts zero to peak.

MAINTENANCE

PERIODIC CHECKS

For any periodic testing of the Type SLC51D relay the trip coil circuit of the circuit breaker should be opened by opening the disconnect switches or other test switches provided for this purpose.

TROUBLESHOOTING

Test points are provided at selected points in the Type SLC51D relay to observe outputs if trouble-shooting is necessary. The use of a card adapter will make the pins on any one card available for testing.

For the physical location of components and cards refer to Figure 2, the component location diagram.

SPARE CARDS

The number of spare cards to carry in stock would depend on the total number of static relays, using similar cards, at the same location or serviced by the same test group. For each type of card (different code designation) a suggested minimum number of spare cards would be:

1 spare for 1 to 25 cards
2 spares for 26 to 75 cards
3 spares for 76 to 125 cards

CARD DRAWINGS

Details of the circuits of the printed circuit cards can be obtained in the printed circuit card book GEK-34158.

APPENDIX I

DETERMINATION OF ZERO SEQUENCE

CHARGING CURRENT

In many pilot schemes which operate on the blocking principle on ground faults the blocking signal is initiated by a high-speed, non-directional fault detector operating on zero sequence current, and the tripping level is established by a second fault detector set at a higher value. That is:

$$FD_T = k\ FD_B \qquad \text{V-a}$$

where:

K = Desired margin between blocking and tripping levels = 4/3.

On applications where the zero sequence line charging current is significant, it must be taken into account if the margin k of equation V-a is to be retained:

$$FD_T = k\ FD_B + 3I_{OC} \qquad \text{V-b}$$

I_{OC} = Zero sequence line charging current

Thus, in many applications of schemes involving instantaneous blocking and tripping level detectors it becomes necessary to determine the zero sequence line charging current. The following steps are suggested in approximating this quantity:

Figure 5-2 shows a simplified representation of the sequence network connections for a single-phase-to-ground fault. For a grounded system Z_0 will not exceed $3Z_1$. Therefore, assuming that $Z_0 = 3Z_1$, the voltage E_0 will be 0.6 $E_{\phi N}$.

Figure 5-3 represents the zero sequence network for an external ØG fault beyond B of line A-B. The shunt capacitance in reality would be distributed along the line. The zero sequence charging current could be very closely approximated by assuming that the total shunt capacitance is lumped at the center of the line, and that the zero sequence voltage applied across that capacitance is the average zero sequence voltage across the line as represented by Figure 5-4.

As is apparent from Figure 5-4 however, this average voltage will depend on the magnitude of zero sequence source impedance at A, which in many applications can vary greatly. It will be pessimistic if it is assumed that the lumped shunt capacitance is located at the remote end of the line nearest the fault, and that the voltage applied across this shunt capacitance is E_0 at the fault. If we assume that the zero sequence shunt capacitance (C_0) is equal to 3/4 the positive sequence shunt capacitance (C), then the zero sequence capacitive reactance (X_{co}) will be 4/3 the positive (X_{c1}). Then:

$$I_{c1} = \frac{E_{\phi N}}{X_{c1}}$$

$$I_{oc} = \frac{E_o}{X_{co}} = \frac{0.6\ E_{\phi N}}{(4/3)\ X_{c1}}$$

Substituting I_{c1} for $E_{\phi N}/X_{c1}$:

$$I_{co} = 0.6\ (3/4)\ I_{c1}$$

$$\therefore\ I_{co} = 0.45\ I_{c1}$$

$$\text{or } 3I_{co} = 1.35\ I_{c1}$$

This value should be substituted into equation V-b in determining the required setting of the tripping fault detector FD_T. If the resulting setting of FD_T is low enough to detect the minimum predicted internal fault, with margin, it can be used with assurance that the margin between the blocking and tripping levels will be conservative. If a lower setting is required to provide margin below the minimum internal fault,

then the user will have to use a more precise method of determining I_{CO} in the hope that the resulting lower value of $3I_{CO}$ in equation V-b will result in a sufficiently lower FD_T setting. One such approach would be to assume the lumped shunt capacitance at the center of the line with average E_O applied across it. This requires that the maximum possible source impedance at A (Z_{OSA}) be determined.

If compensating shunt reactors are present, either at one end or at both ends of the protected line, the lagging reactor current will reduce the net zero sequence charging current. This net current then should be used for the $3I_{CO}$ quantity shown in equation V-b.

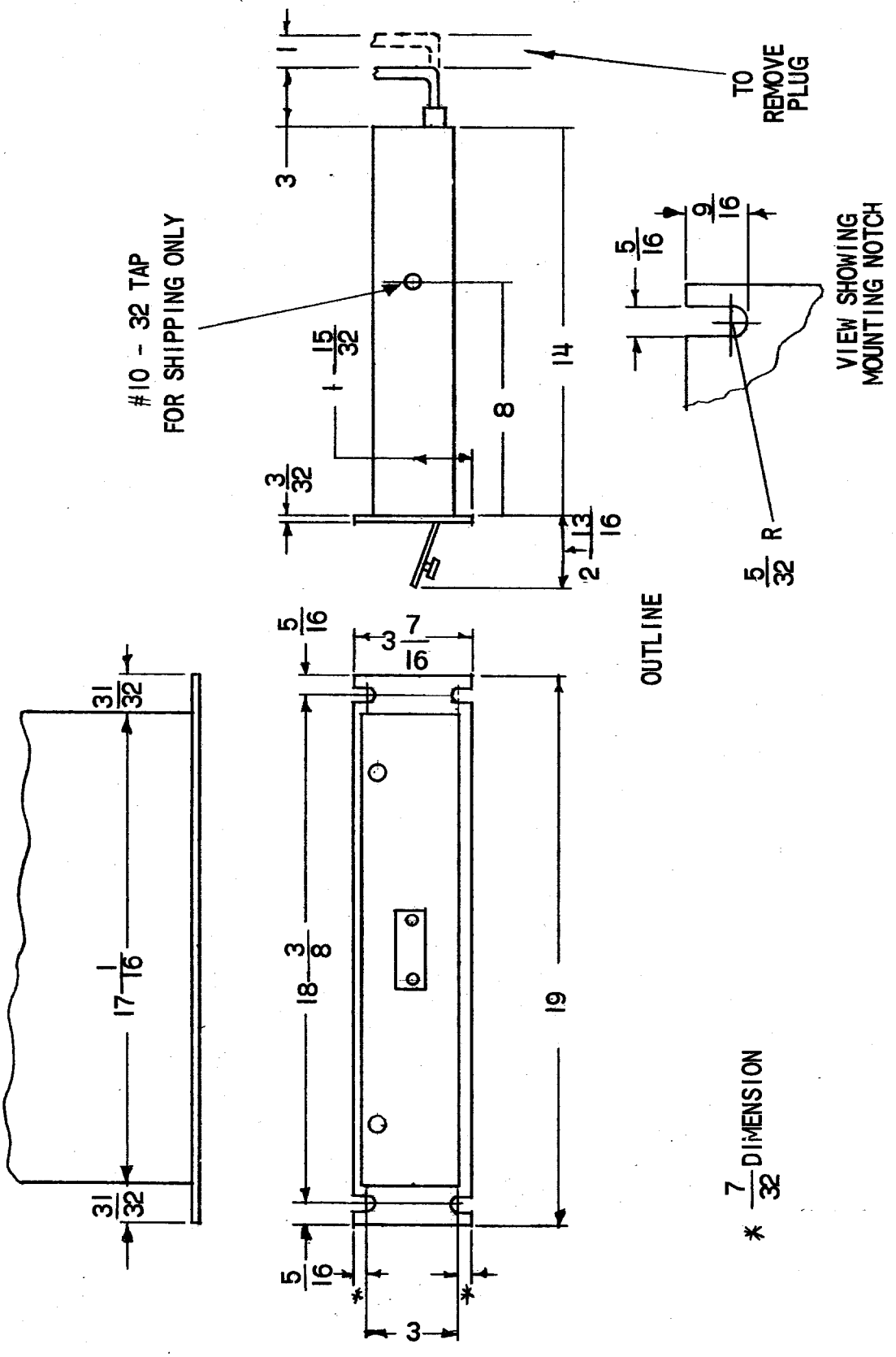
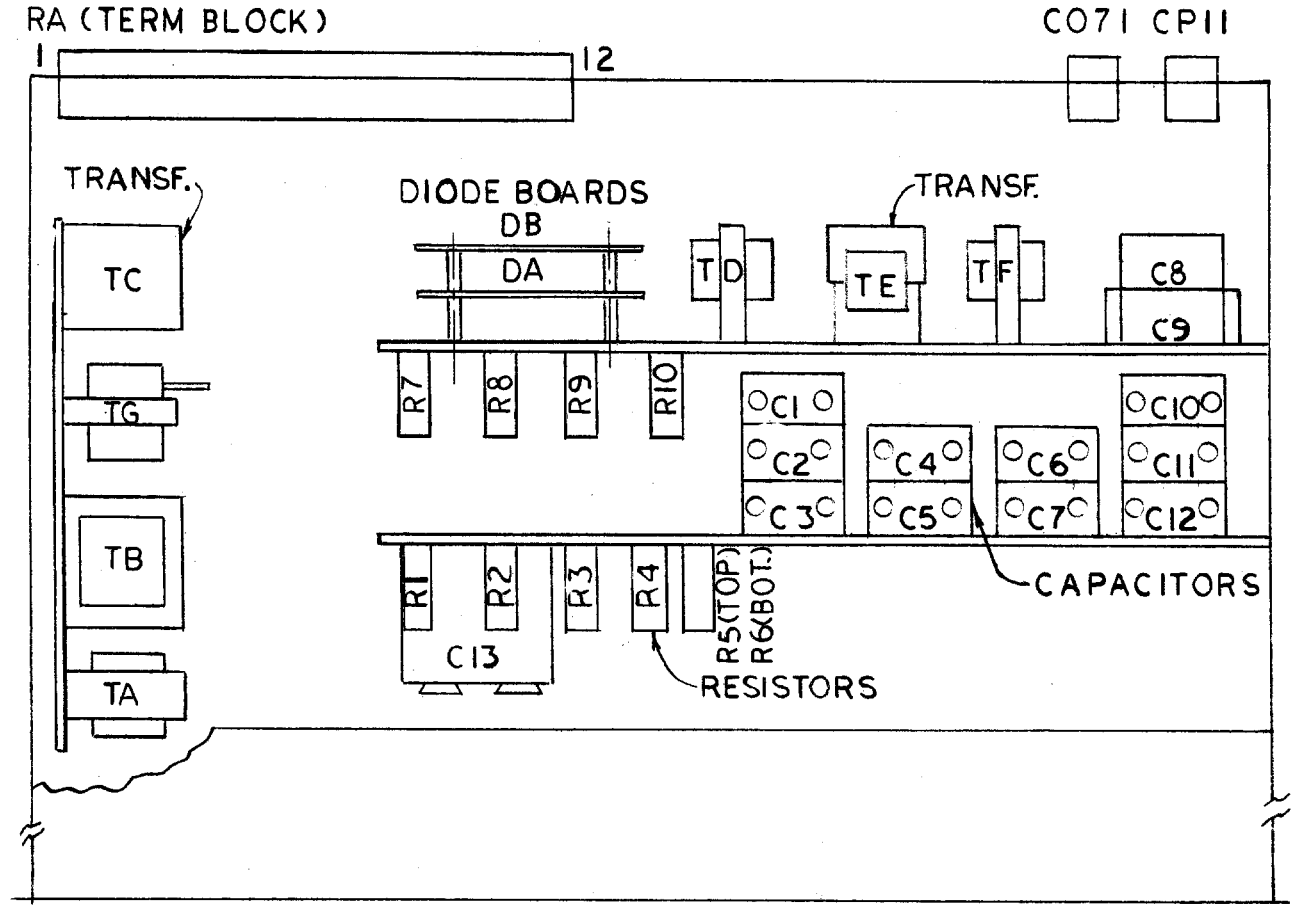
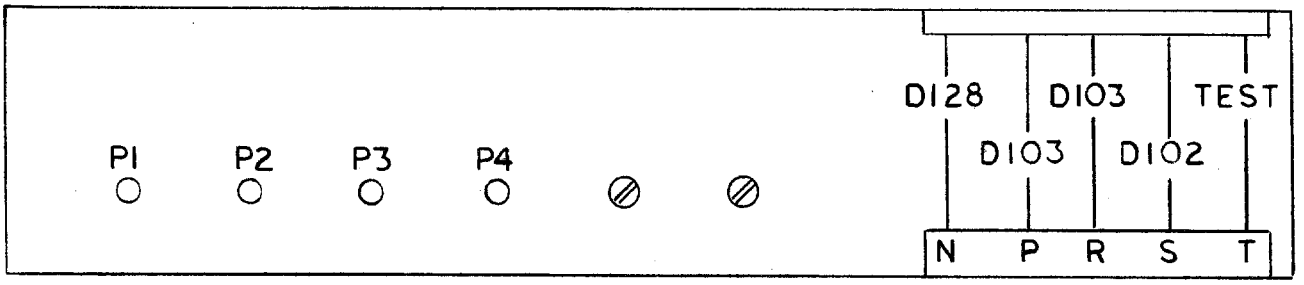


Fig. 1 (0227A2036-0) SLC51D OUTLINE AND MOUNTING DIMENSIONS

FOR INTERNAL REFER TO 0152C7752



PLAN VIEW



FRONT VIEW
(COVER REMOVED)

Fig. 2 (0269A3102-0) SLC51D COMPONENT LOCATION DIAGRAM

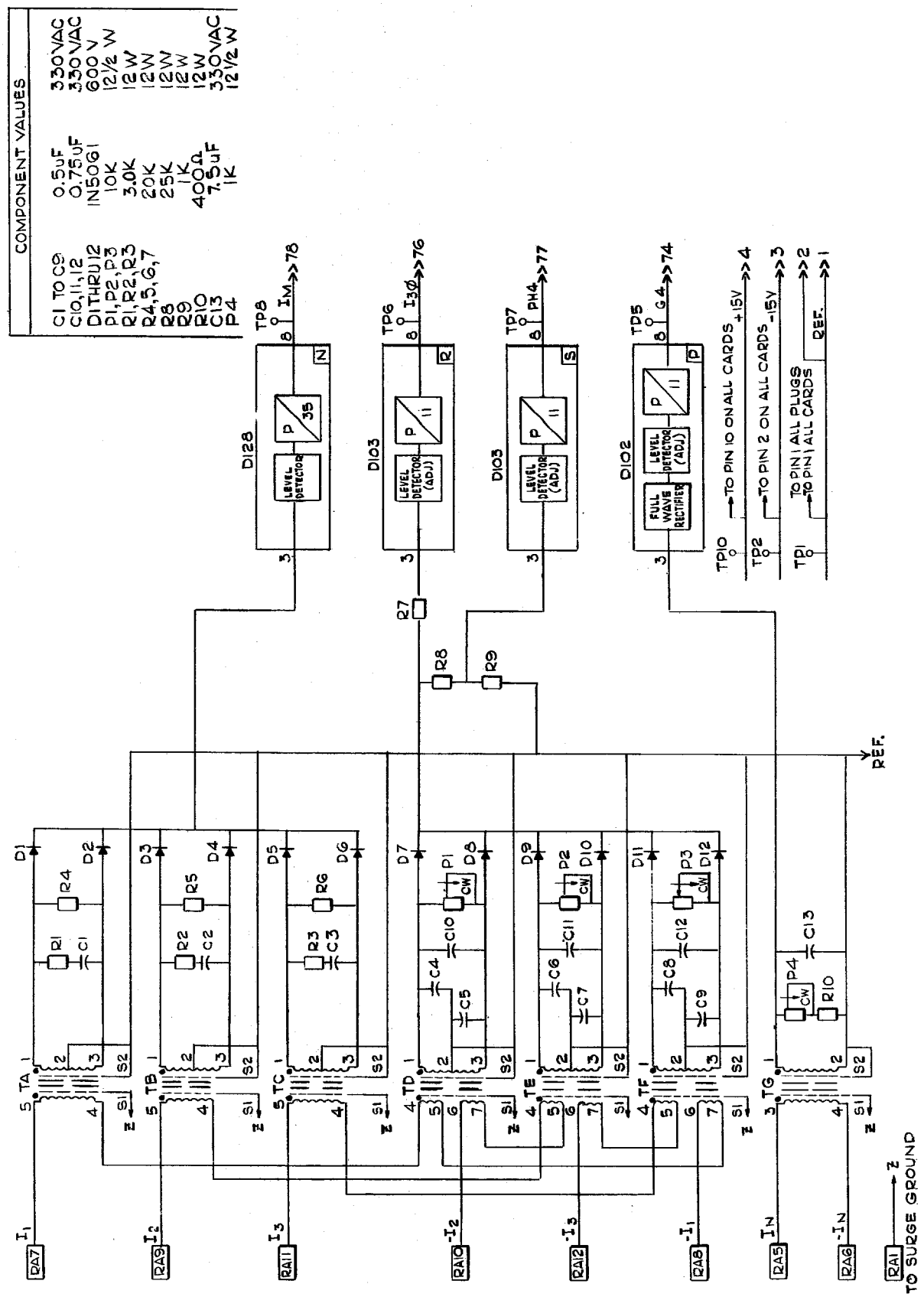


Fig. 3 (0152C7752-0) INTERNAL CONNECTIONS DIAGRAM OF SLC51D

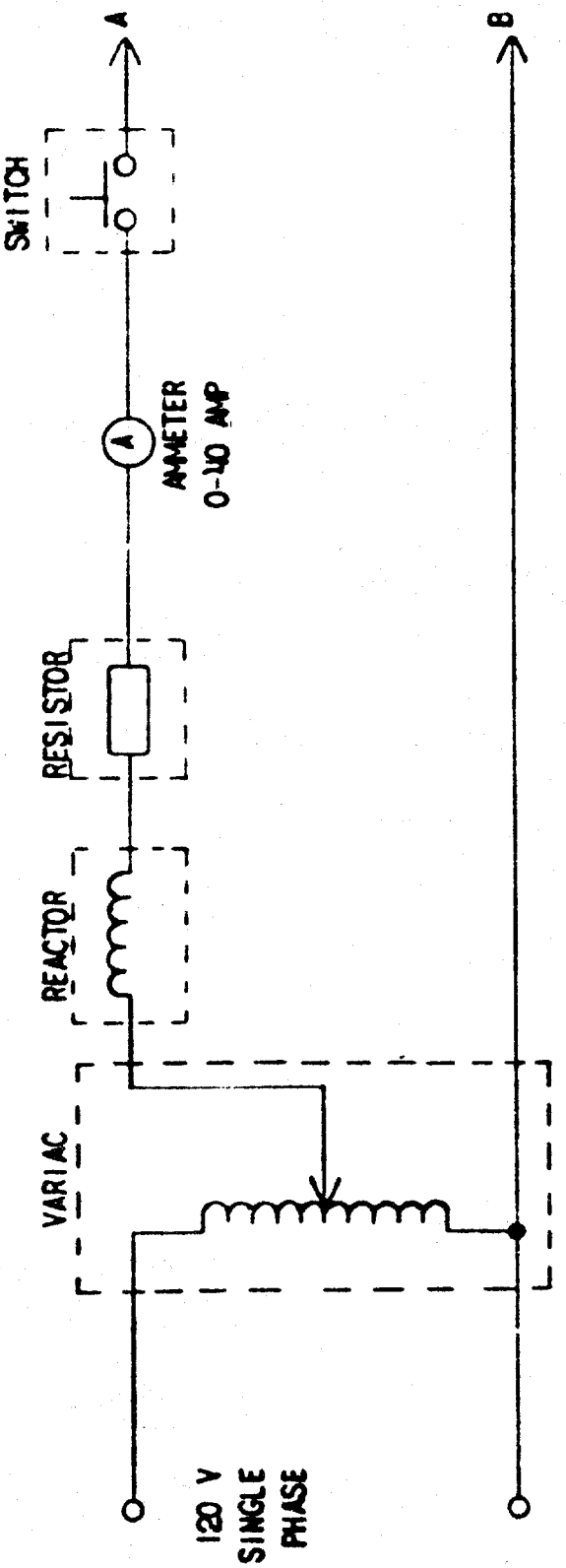
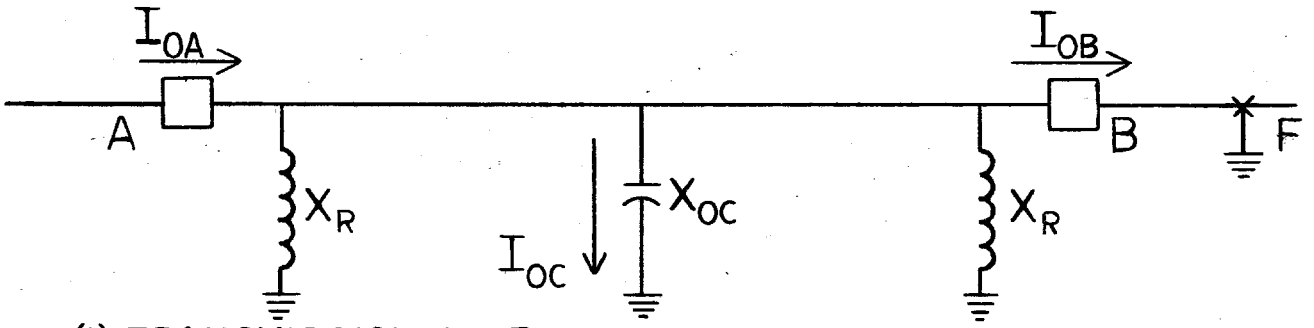
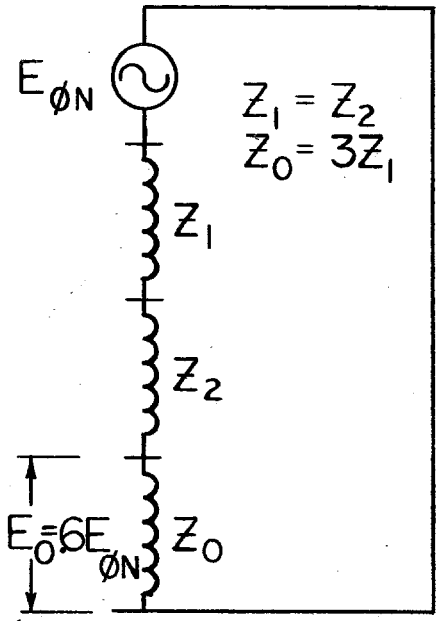


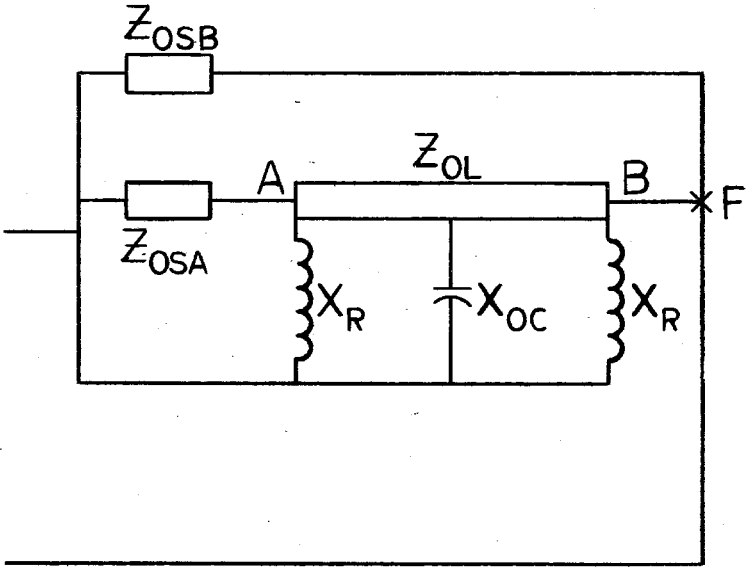
Fig. 4 (0246A3681-1) OVERCURRENT FUNCTION TEST CIRCUIT



(1) TRANSMISSION LINE WITH SHUNT REACTORS



(2) SEQUENCE NETWORK CONNECTIONS FOR A LINE TO GROUND FAULT.



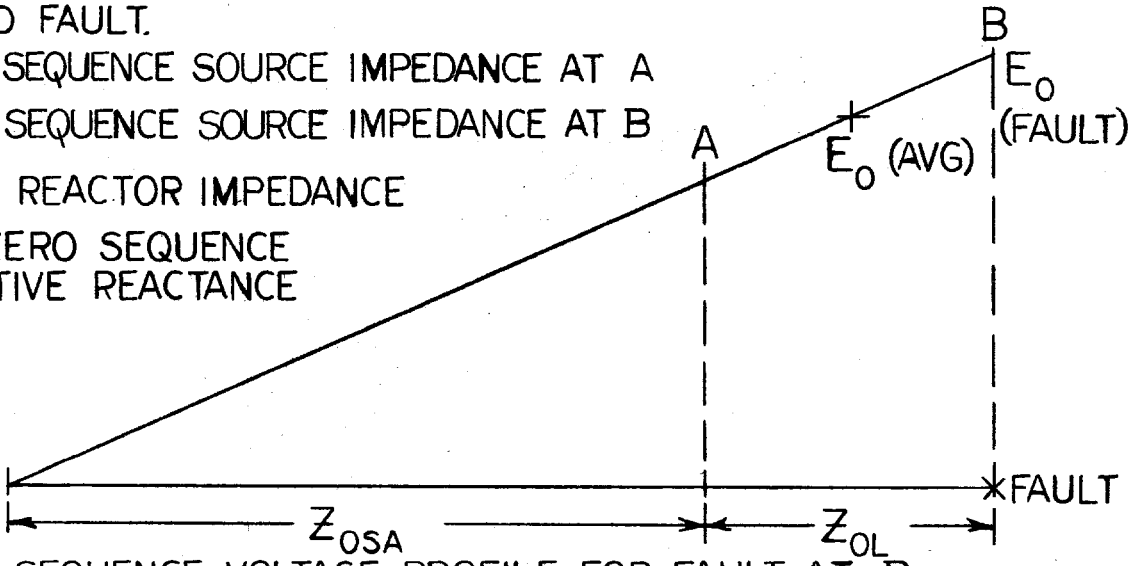
(3) ZERO SEQUENCE NETWORK FOR FAULT AT B.

Z_{OSA} = ZERO SEQUENCE SOURCE IMPEDANCE AT A

Z_{OSB} = ZERO SEQUENCE SOURCE IMPEDANCE AT B

X_R = SHUNT REACTOR IMPEDANCE

X_{0C} = LINE ZERO SEQUENCE CAPACITIVE REACTANCE



(4) ZERO SEQUENCE VOLTAGE PROFILE FOR FAULT AT B

Fig. 5 (0246A6925-0) DETERMINATION OF ZERO SEQUENCE CHARGING CURRENT

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