# INSTRUCTIONS

GEK-26491

STATIC PHASE COMPARISON RELAYS

TYPE SLD

POWER SYSTEMS MANAGEMENT DEPARTMENT

GENERAL ELECTRIC

PHILADELPHIA, PA.

CONTENTS

# STATIC PHASE COMPARISON RELAYS
# TYPE SLD

## DESCRIPTION

The Type SLD designation covers a family of static phase comparison relays designed to respond to positive and negative or negative-sequence currents resulting in high speed protection for all phase and ground faults on transmission lines to which they are applied. A suitable channel must be employed, and a separate channel-control, auxiliary and tripping relay, Type SLA, and/or supervision by a phase distance relay may be required.

The typical SLD is packaged in two separate units: (1) a network unit containing tap blocks and other adjustments for selecting level detector ranges and overcurrent unit operating levels, and (2) a logic unit containing printed circuit cards required for the phase comparison logic functions.

Each SLD relay requires a +17 volt d-c source, with bias voltages, which can be obtained from a Type SSA power supply.

## RATINGS

Type SLD relays are designed for operation in a maximum ambient air temperature of $55^{o}C$ outside the relay case.

The current circuits of the SLD relays are rated at 5 amperes, rated frequency, for continuous duty, and have a one second rating of 250 amperes.

The SCR tripping circuits included in certain SLD types are rated for 48, 125 or 250 volts d-c, depending on the model rating as shown on the nameplate, and each has a 1.0 amp series target. The tripping circuits are designed to carry 30 amps for one second.

The customer should consider the following when applying the SCR trip outputs to his trip circuits.

The GATE SOURCE that operates the SCR devices is pulsed several hundred times a second to provide spikes to fire the SCR's when tripping is to take place. Since silicon-controlled rectifiers (SCR) require some minimum current to maintain conduction, trip circuits with very high inductance-to-resistance ratios (L/R), coupled with high resistance can sometimes inhibit tripping. With the high L/R ratio and a high resistance the current build-up in the SCR trip circuit will be slow. Since the gating pulses are of short duration, the trip current will not have sufficient time to build up to the level that is required to "seal-in" the SCR. It is important to check the associated breakers to ensure that on a trip-free, as well as a regular trip, the SCR circuits do, in fact function as desired.

In the event that the breaker trip circuits do tend to inhibit tripping, the trip circuits should be loaded with the largest ohmic value of resistance that ensures seal-in. A minimum design requirement is that a current of 100 milliamps will flow through the SCR trip circuit in 0.6 milliseconds.

The contact of the telephone-type auxiliary units, such as commonly used for the RI, BFI, or alarm functions, will make and carry 3 amps continuously, and will interrupt up to 0.5 amps (inductive) at 125 volts d-c, or 0.25 amps (inductive) at 250 volts d-c.

## OPERATING PRINCIPLES AND CHARACTERISTICS

### Functions

The following are typical functions included in Type SLD relays.

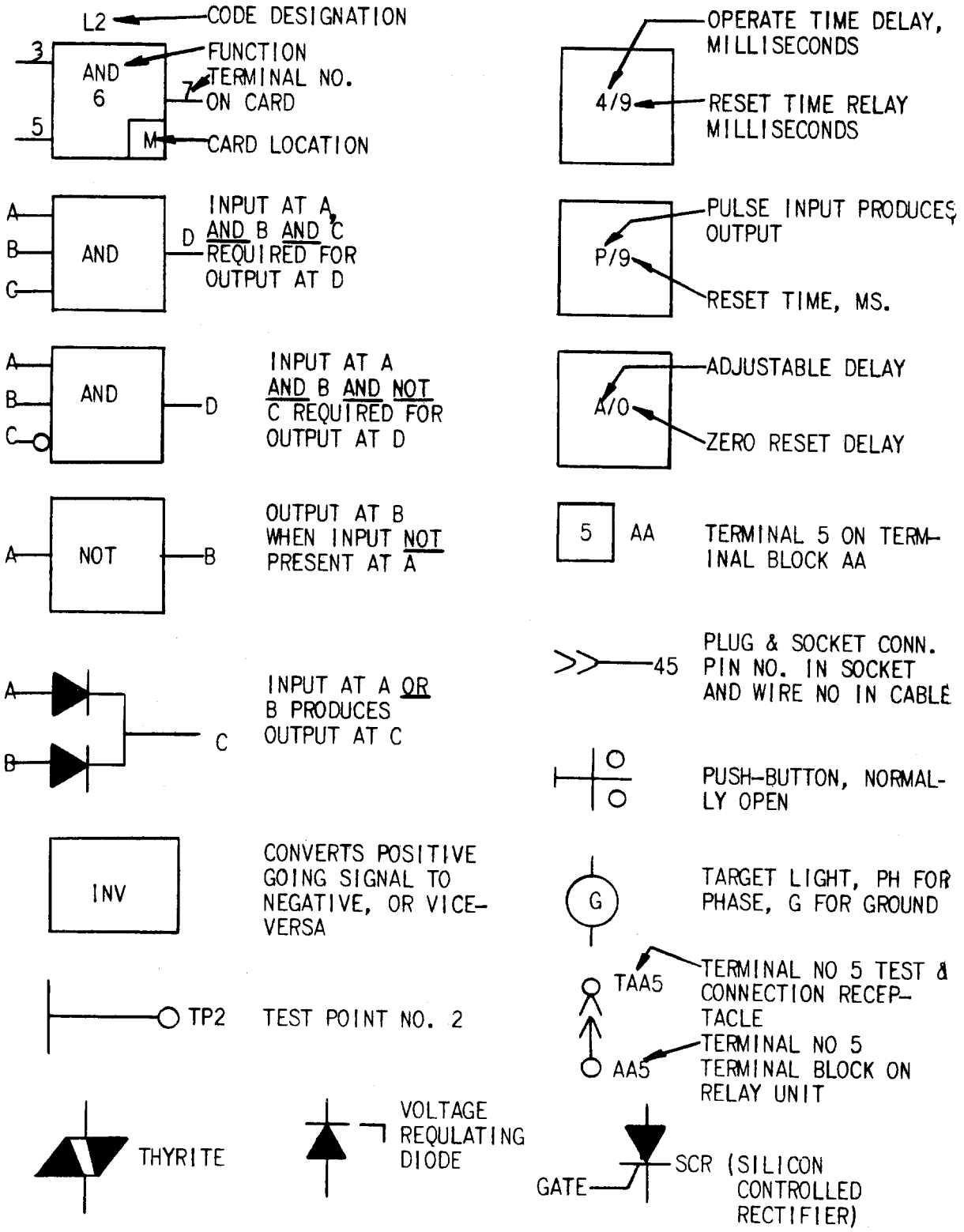



FIG. 1 (0178A7026-2) LEGEND FOR SYMBOLS USED ON STATIC RELAY LOGIC DIAGRAMS ON ALL TRACINGS

Negative Phase-Sequence-Network: produces a single phase output proportional to the negative-sequence component of the input currents and produces no output for the positive or zero-sequence components.

Positive Phase-Sequence-Network: produces a single phase output proportional to the positive-sequence component of the input currents and produces no output for the negative or zero-sequence components.

FDH: a high-set level detector that produces an output when the input signal exceeds the value of its pickup setting; the input signal is either the output of the negative-sequence network or a combination of negative and positive-sequence network outputs.

FDL: a level detector similar to FDH but with a lower pickup setting.

FDM: a level detector whose input is invariably a combination of negative and positive-sequence network outputs used to supervise the squaring amplifier output.

G4: an overcurrent unit that measures residual current and initiates a direct trip.

Squaring Amplifier: provides the logic signal used in the comparison process by rectifying its input signal and limiting the peaks to produce a half-square-wave output in phase with the fault current.

Electrically separate silicon-controlled rectifiers (SCR) tripping circuits, each with a series, hand-reset, mechanical target.

Auxiliary units: these may be telephone-type relay units for such functions as reclosure initiation (RI) breaker failure backup initiation (BFI) or reclosure cancellation (RC).

Target lamps and their control logic to indicate the type of fault and what cleared it. (i.e. overcurrent trip or carrier ground trip)

Channel control circuits to provide the keying of the associated channel in response to the squaring amplifier output and/or other functions.

Various logic functions such as the comparer.

Various timing functions such as the trip integrator associated with the comparer and the transient blocking coordinating timer.

Contact converters to permit external electromechanical contacts to operate into the logic.

All the functions listed above are not necessarily included in every SLD nor does the list purport to be complete. To determine what is included in a particular type of SLD, refer to the internal connections diagram for the specific relay included in the "adder" to this book.

An explanation of the various logic symbols representing these functions is shown in Figure 1.

## Phase Comparison

A phase comparison pilot relaying scheme operates on the basic principle that a fault can be judged to be either internal or external to a protected line section by comparing the relative phase positions of the fault currents at the two ends of the line. In practice the quantities used in making the comparison between the two ends of the line are single phase voltages which are obtained by combining the CT secondary currents at each end. The single phase voltages are used to produce a square wave signal which modulates the channel transmitter and attempts to trip the local breaker on alternate half cycles.

In SLD relays the single phase voltage used for phase comparison is either (1) the output of a negative-sequence network or (2) the combined outputs of a negative and a positive-sequence network with the resultant output weighted to favor the negative-sequence component by a multiplying factor "K". The combined output is then; $I_2 - I_1/K$.

These positive and negative-sequence networks are contained in the network unit. It will be noted that the positive and negative-sequence networks are similar but differ in the way they are connected to the CT secondaries. Both networks consist of two transactors, each with two primary windings and an adjustable resistive load across a secondary winding.

The term "transactor" is a contraction of transformer-reactor. It is essentially an air-gap current transformer with secondary current, and hence, secondary voltage across the loading resistor, proportional to the vector sum of the input currents in the leading direction. The performance of a transactor in a

circuit is described by its transfer impedance $Z_T$ and the associated angle $\theta_T$:

$$Z_T = \frac{Vout}{Iin} \angle \theta_T$$

Where: Vout = Secondary output voltage

Iin = Vector sum of the input currents

$\theta_T$ = Angle by which Vout leads Iin

Negative-Sequence Network

The negative-sequence network will be used to explain the operating principles of the sequence networks used in SLD relays. This network is represented in simplified form in Fig. 3. It consists of two transactors, each with two primary windings and adjustable resistive loading. One transactor is set so that the transfer impedance angle is Ø1. The other is set so that it is Ø2.

The Ø1 transactor primary windings have equal turns and are connected to phase-A and reversed phase-B CT currents. Output voltage is therefore the single-winding transfer impedance times the vector sum of the two currents.

$$\bar{V}_{\emptyset 1} = \bar{Z}_{\emptyset 1} (\bar{I}_A - \bar{I}_B) \tag{1}$$

The Ø2 transactor primary windings have a ratio of turns of 3 to 1. The high-turn winding is connecte to phase-B CT current, and the low-turn winding to reversed CT residual current. Output voltage is, therefore, the high-turn single-winding transfer impedance times the sum of phase-B current and one-third of reversed CT residual current.

$$\bar{V}_{\emptyset 2} = \bar{Z}_{\emptyset 2} \left[ \bar{I}_B - 1/3(\bar{I}_A + \bar{I}_B + \bar{I}_C) \right] \tag{2}$$

The secondaries of the two transactors are connected in series so that the total network output is the vector sum of the individual transactor output voltages.

A balanced negative-sequence network is defined as a network that has a zero positive-sequence transfer impedance, i.e., one that has zero output voltage when pure positive-sequence current is applied. To accomplish this, the two transactor secondary voltages must cancel each other. The necessary relation between magnitude and angle of the two transactor transfer impedances is determined by the following analysis, in which phase A, B and C line currents contain only positive-sequence components.

$$\bar{I}_A = \bar{I}_{A1} \qquad \bar{I}_B = \bar{I}_{B1} \qquad \bar{I}_C = \bar{I}_{C1} \tag{3}$$

$$\bar{V}_T = \bar{V}_{\emptyset 1} + \bar{V}_{\emptyset 2} = 0 \tag{4}$$

$$\bar{Z}_{\emptyset 1}(\bar{I}_A - \bar{I}_B) + \bar{Z}_{\emptyset 2} \left[ \bar{I}_B - 1/3(\bar{I}_A + \bar{I}_B + \bar{I}_C) \right] = 0$$

$$\bar{I}_{B1} = a^2 I_{A1} = \bar{I}_{A1} \angle 240^\circ$$

$$\bar{I}_A - \bar{I}_B = \bar{I}_{A1} - a^2 \bar{I}_{A1} = \sqrt{3}\, \bar{I}_{A1} \angle 30^\circ$$

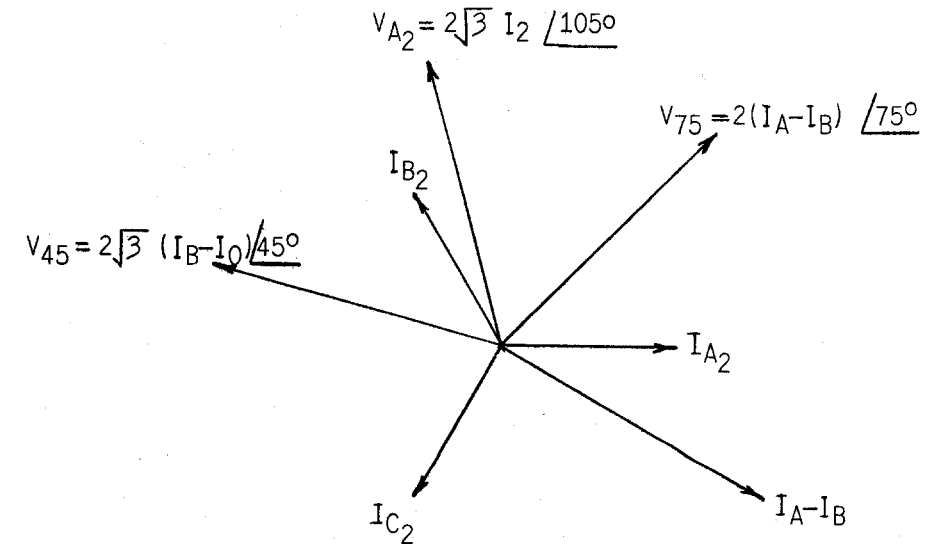
$$\bar{I}_A + \bar{I}_B + \bar{I}_C = 0$$

$$\bar{Z}_{\emptyset 1}(\sqrt{3}\, \bar{I}_{A1} \angle 30^\circ) + \bar{Z}_{\emptyset 2}\, \bar{I}_{A1} \angle 240^\circ = 0$$

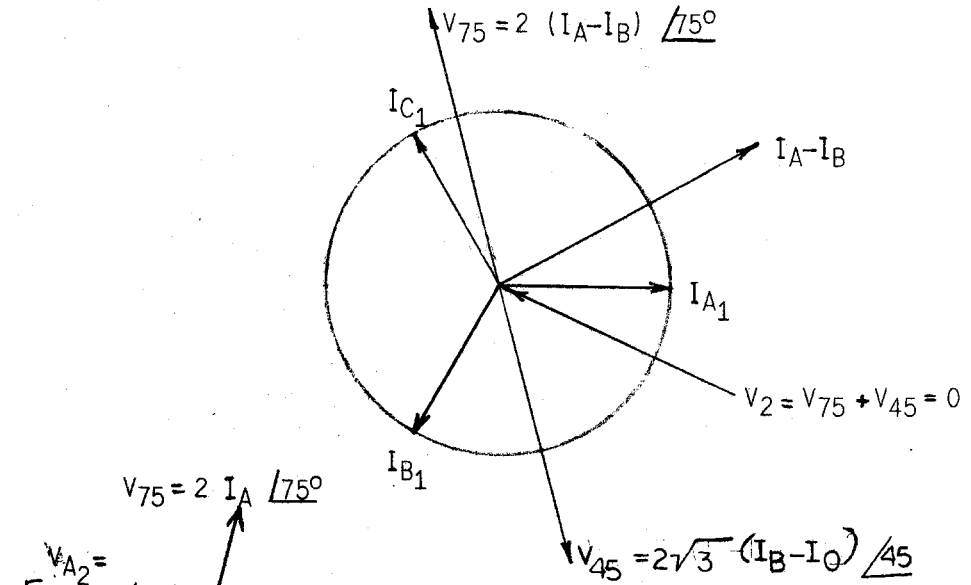
$$\bar{Z}_{\emptyset 1} = Z_{\emptyset 1} \angle \emptyset 1 \qquad \bar{Z}_{\emptyset 2} = Z_{\emptyset 2} \angle \emptyset 2$$

$$\sqrt{3}\, Z_{\emptyset 1}\, \bar{I}_{A1} \angle \emptyset 1 + 30^\circ + Z_{\emptyset 2}\, \bar{I}_{A1} \angle \emptyset 2 + 240^\circ = 0 \tag{5}$$

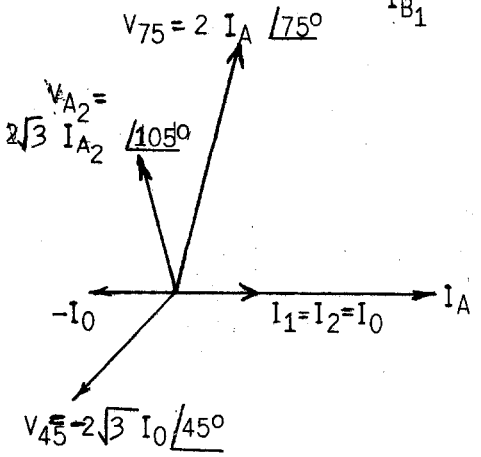
If the following two conditions are met, then equation 5 is satisfied.




A
NETWORK RESPONSE TO A PURE NEGATIVE SEQUENCE SYSTEM




B
NETWORK RESPONSE TO A PURE POSITIVE SEQUENCE SYSTEM




C
NETWORK RESPONSE TO A PHASE-A TO GROUND FAULT

FIG. 2 (0178A9077-1) SLD NEGATIVE-SEQUENCE NETWORK RESPONSE TO NEGATIVE, POSITIVE AND ZERO SEQUENCE SYSTEMS

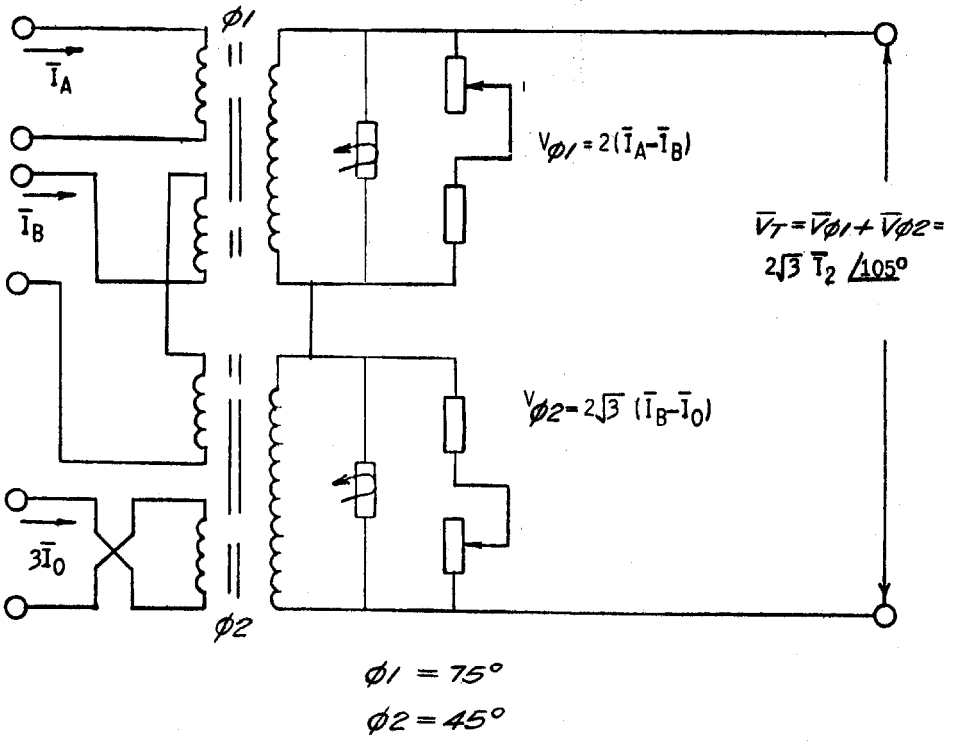



FIG. 3 (0226A7024-0) SIMPLIFIED NEGATIVE-SEQUENCE NETWORK SCHEMATIC

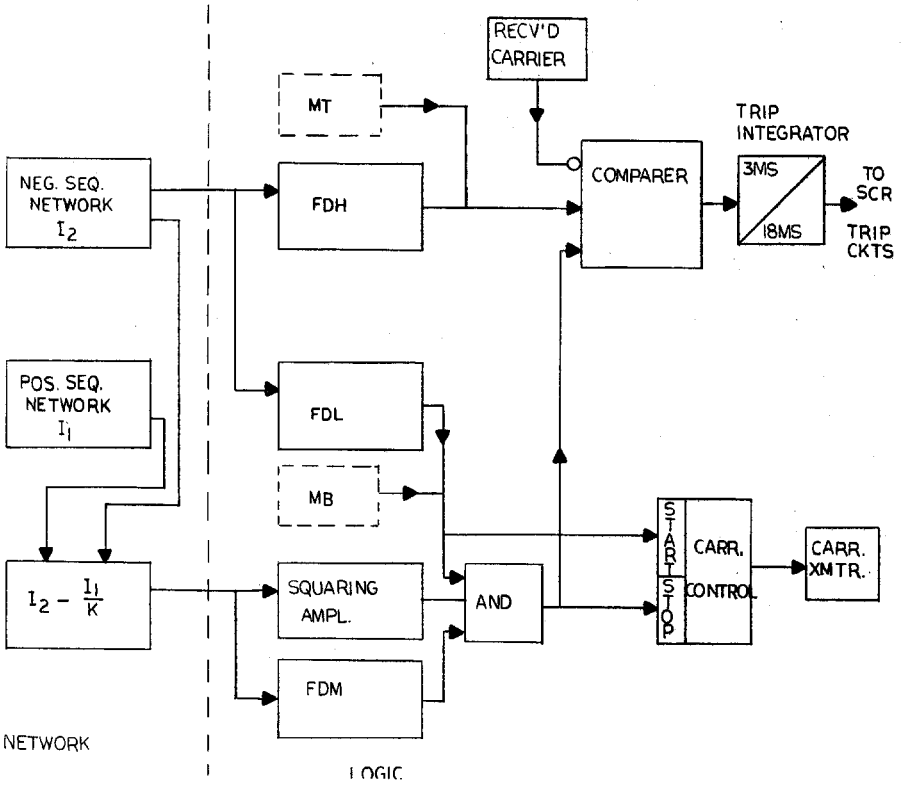



FIG. 4 (0226A6977-0) SIMPLIFIED SLD FUNCTION AND LOGIC DIAGRAM

(a) $Z_{\emptyset 2} = \sqrt{3}\, Z_{\emptyset 1}$

(b) $(\emptyset 1 + 30^{o}) - (\emptyset 2 + 240^{o}) = 180^{o}$

This leads to $\emptyset 1 - \emptyset 2 = 30^{o}$ as the only requirement on angle. In practice $\emptyset 1 = 75^{o}$ and $\emptyset 2 = 45^{o}$. The choice of $75^{o}$ and $45^{o}$ for the transactors is one of practicability, not necessity. However, in order to assure that two terminals coordinate properly, these angles must be the same from network to network.

To obtain a balanced negative-sequence network, it is not only necessary that the transactor transfer impedance angles be $30^{o}$ apart, but that their magnitudes have the ratio of $\sqrt{3}$. In practice this requirement is stated as:

$$\sqrt{3}\, Z_{75} = Z_{45}$$

where $Z_{75} = 2$.

Figure 2B shows the results of this analysis in graphical form.

Having established transactor characteristics that make the positive-sequence transfer impedance zero it is now possible to calculate the negative-sequence transfer impedance. Figure 2A shows the vector relationships for this case.

Figure 2C shows the response of the network to a phase A to ground fault. Here we see that the zero-phase-sequence component of the fault current has been eliminated from the network response by the action of the residual winding of the $45^{o}$ transactor, and the network output voltage is the same as in Figure 2A

$$2\sqrt{3}\, I_{A2} \angle 105^{o} \qquad (6)$$

## Positive-Sequence Network

It can be shown that a positive-sequence network can be obtained by means of the same components used in the negative-sequence network described above, provided only that the phase-C current is used instead of phase-B. That is:

$$\overline{V}_T = \frac{2}{3}(\overline{I}_A - \overline{I}_C) \angle 75^{o} + \frac{2\sqrt{3}}{3}(\overline{I}_C - \overline{I}_o) \angle 45^{o} \qquad (7)$$

$$\overline{V}_T = \frac{2}{3}\sqrt{3}\, \overline{I}_{A1} \angle 105^{o} \qquad (8)$$

The 1/3 factor in equations (7) and (8) results from the use of 1/3 as many primary turns in the positive-sequence transactors.

It should be emphasized that the $105^{o}$ angle which appears in equations (6) and (8) above results from calculations based on the open circuit condition of the network. In practice the loading effect of the low-pass filter will cause the angle of the network output voltage to deviate from the $105^{o}$ calculated value, but since the loading will be practically the same in the network units at the two ends of the line, the angles will also be the same.

## Logic Unit

The operating principles of a phase comparison relaying scheme using SLD's is best described in terms of a diagram of functional blocks interconnected by information flow paths.

The block diagram of Figure 4 is a simplified drawing of a mho-supervised, phase comparison scheme, and does not imply that all SLD's are used in this manner. However, the explanation of carrier keying and comparer operation remains the same for all SLD types.

The negative and positive-sequence networks at the left of Figure 4 produce the single phase voltage which is used to key the transmitter and perform the comparison of the local and remote phase information. The combined positive and negative-sequence output, $I_2 - I_1/K$, is fed into a level detector, FDM, and a squaring amplifier. The squaring amplifier produces a rectangular pulse on alternate half cycles of its sine wave input, and is so designed that this rectangular output becomes symmetrical somewhat below the operating point of FDM. The output of the squaring amplifier under the supervision of FDM and FDL (MB in the case of a three phase fault) keys the transmitter "off" and applies a trip signal to the comparer on alternate half cycles. Supervision of the squaring amplifier output is performed by the 3 input AND.

In standby the transmitter is held in the "off" condition by the carrier control function. Operation of the low-set level detector, FDL, turns on the carrier. The squaring amplifier output pulse actually functions during its active half cycle to key the local transmitter "off" while supplying a trip signal to the comparer.

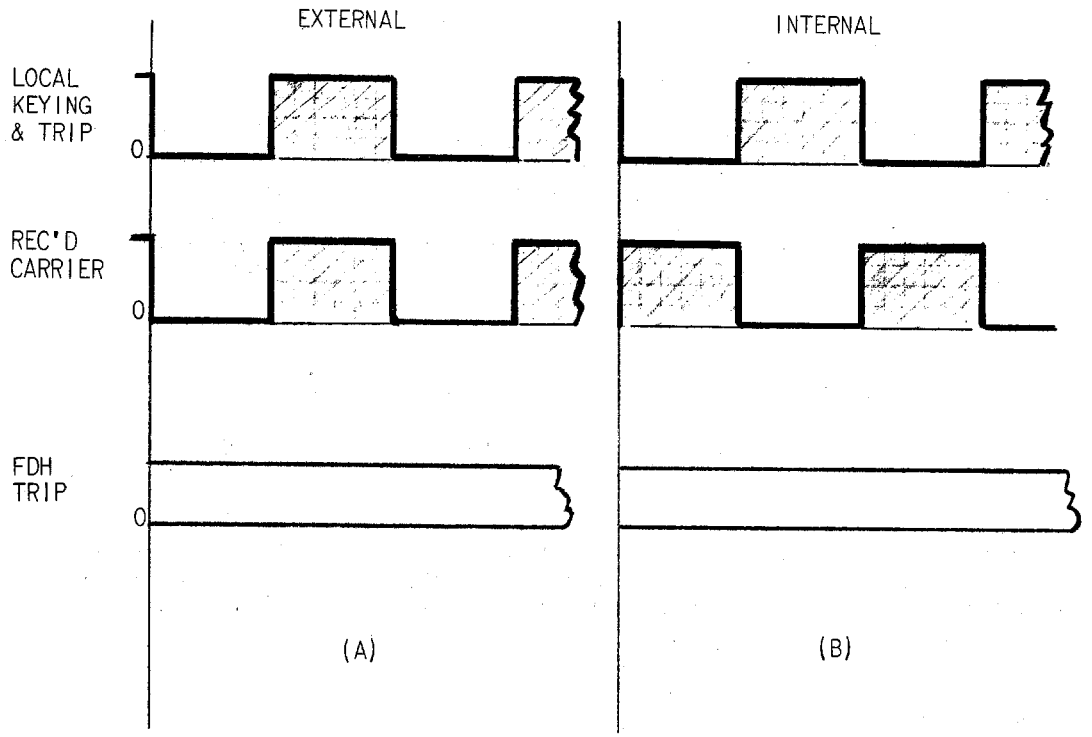



FIG. 5 (0178A9085-1) RELATION OF TRIPPING AND BLOCKING SIGNALS ON EXTERNAL (A) AND INTERNAL (B) FAULTS

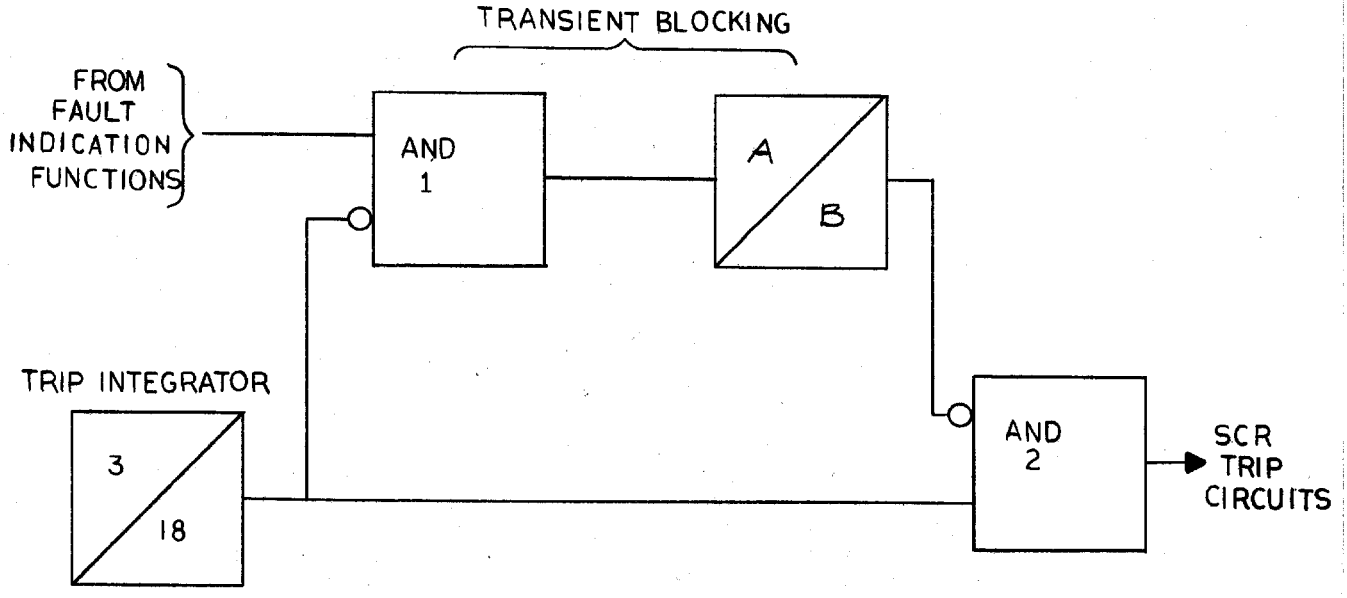



FIG. 6 (0226A6978-2) TRANSIENT BLOCKING FUNCTION

The comparer inputs are provided by the keying signal from the squaring amplifier, the output of a high-set level detector, FDH, and the output from the carrier receiver. The carrier signal is fed into the comparer through a NOT input so it is actually the absence of carrier which applies a permissive signal to the comparer. For the comparer to have an output it must receive simultaneously, signals from the squaring amplifier and FDH in the absence of carrier. The output from the comparer must persist for 3 milliseconds or more before the trip integrator will apply a signal to the SCR trip circuits.

Now consider an external phase-to-phase fault with an equipment represented by the block diagram of Figure 4 at terminal A cooperating with a similar equipment at the remote terminal B. The network units at the two ends are connected to the line current transformers with relative polarities such that for an external fault the keying or tripping signals at the two ends will occur on alternate half cycles, i.e., be $180^{\circ}$ out of phase with each other. During the half cycle end A is producing a keying signal that turns carrier "off" and applies a tripping signal to the comparer, end B will be transmitting carrier which when received at A will cause a blocking signal at the NOT input to the comparer. On the next half cycle conditions will be reversed such that a keying signal will occur at B to turn "off" carrier and apply a tripping signal to the comparer, and end A will be transmitting carrier which will block the comparer at B. This condition is represented graphically in Figure 5A. For the condition of our external fault there is no output from the comparer.

During an internal fault both ends will be transmitting carrier simultaneously during one half cycle and will be applying a trip signal to the comparer simultaneously during the alternate half cycle (see Figure 5B). Consequently, the comparers will both produce an output during the trip half cycle since inputs will be supplied by the keying signal and FDH in the absence of received carrier. After the comparer output has persisted for 3 milliseconds the trip integrator will produce an output which will operate the SCR circuit and trip the circuit breaker.

For the scheme of Figure 4 when a balanced 3 phase fault occurs FDH does not operate because there will be no negative-sequence current, but MT, the mho function of the phase relay, operates and supplies the necessary signal. FDL is, likewise, functionally replaced by MB. Also, the positive-sequence component of $I_2 - I_1/K$, $I_1/K$, controls the squaring amplifier and FDM.

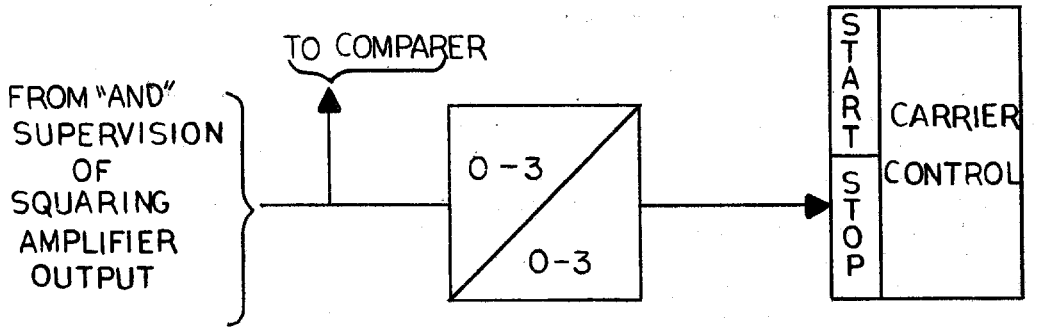
All SLD's contain functions which are not shown in the simplified logic diagram of Figure 4. An A/B timer plus a two-input AND comprise the transient blocking or RB function as shown in Figure 6. If a fault occurs on the system, as indicated by the pickup of a fault indication function (FDH or MT), and there is no trip output from the 3/18 timer within A milliseconds there will be an output from the A/B timer. This output will block AND2 until B milliseconds after the fault is cleared and the fault indication signal drops out. Since the pickup time of the A/B timer is set for a longer time than the maximum operating time of the SLDG for an internal fault, the RB function can only get set-up on external faults. For internal faults the 3/18 timer output will block AND1 and so prevent the A/B timer from timing out and blocking AND2. In this way the transient blocking function acts to block any tripping until B milliseconds after an external fault is cleared. Timer settings A and B for a particular SLD and scheme are contained in the "adder".

Included in the SLD logic is an 0-3/0-3 timer called the symmetry adjustment timer, shown in Figure 7A. Since the build-up and tail-off times of the remote receiver are not exactly equal, a half cycle square wave signal of the local transmitter will not generally produce a half cycle output from the remote receiver. The 0-3/0-3 symmetry adjustment modifies the keying signal to the local transmitter to produce exactly a half cycle output at the remote receiver.

A phase delay adjustment timer is placed between the AND function supervising the squaring amplifier and the comparer. Figure 7B shows the placement of this 0-8/0-8 timer. This circuit provides means of delaying the local half cycle tripping signal applied to the comparer. This delay of the local trip signal is necessary to compensate for channel delay introduced by such things as local receiver filters, the line propagation time, and the shift in the leading edge of the transmitted signal by the symmetry adjustment timer of the remote terminal. Channel delay timed from the instant the remote transmitter is keyed until the local receiver builds up to an output can be from 1 to 5 milliseconds depending on the type of channel. The 0-8/0-8 timer introduces the same delay in the local trip signal to the comparer. In this way the comparison is made on the same basis.

## APPLICATION

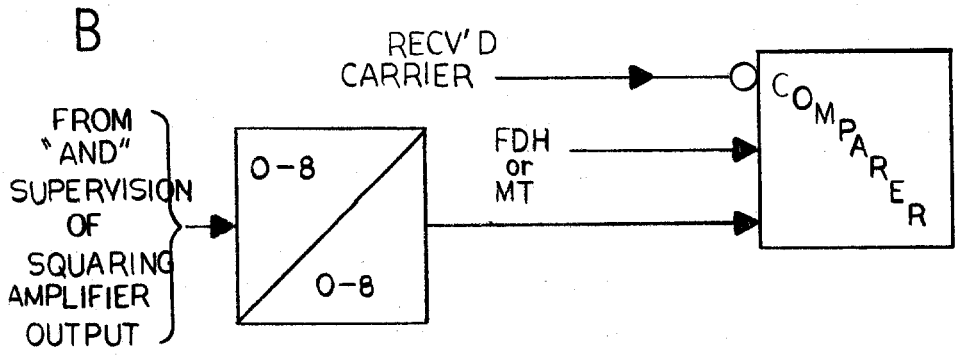
The Type SLD family of static phase comparison relays is designed for the protection of transmission lines against all phase and ground faults. Application considerations and limitations differ widely for the several types of SLD relays covered by these general instructions. Specific application information for a particular type of SLD will be found in the "adder" to this book for that relay. Some general observations can, however, be made.




SYMMETRY ADJUSTMENT TIMER

A

FIG. 7A (0226A6979-1) SYMMETRY ADJUSTMENT TIMER




PHASE DELAY ADJUSTMENT TIMER

FIG. 7B (0226A6979-1) PHASE DELAY ADJUSTMENT TIMER

The phase comparison principle is particularly adapted to the protection of lines where the presence of mutual inductance makes the application of directional comparison relaying difficult or unreliable. On relatively short lines involving minimum fault currents well above full load, the simple basic phase comparison scheme using a relay in the SLD41 series can usually be applied. Since the basic phase comparison scheme does not require an a-c potential source it is sometimes used in conjunction with a phase distance relay and a ground directional relay to provide completely separate primary and backup relaying.

The SLD41 series with mixed excitation has two basic modes of application. The first and simplier mode uses only the SLD41 relay with an SLA auxiliary relay for phase comparison protection on all faults, including three-phase. However, the sensitivity of this arrangement is limited by the fact that it must not operate to produce continuous phase comparison on maximum load current. The second mode of application employs a single-phase SLY relay, in addition to the SLD and SLA, to render the scheme insensitive to load current and permit more sensitive fault current settings. The "adder" for the specific relay lists the application information required and the necessary calculations to determine which mode of application is necessary for a particular installation.

The SLD42 series is typically applied in conjunction with an SLYL relay on lines having series capacitor compensation. Application information for such an installation is included in the "adder" for the specific model.

The type numbers listed above are typical of the SLD relays covered by these general instructions. In all cases specific application information for the particular type will be included in the "adder".

## CHOICE AND CALCULATIONS OF SETTINGS

There are several calculations and settings which must be made before an SLD relaying scheme is put in service. Typically these are level detector settings FDL, FDH and FDM (if used); choice of "K" tap position; and choice of setting for a number of option links. These are discussed in detail in the "adder" for the specific relay type.

## BURDENS

A representative value for maximum current burden of an SLD network unit measured per phase pair at 5 amperes and 60 hertz is 10 volt-amperes.

Should the current burden of a particular SLD differ significantly from the above value the new value will be listed in the "adder" to this book.

## CONSTRUCTION

The network unit and logic unit of SLD type relays are packaged in separate metal-enclosed cases which have removable front and top covers and which are suitable for mounting on standard 19 inch racks.

### Network Unit

The network unit includes the negative-phase-sequence and positive-phase-sequence networks, transformers for coupling the network outputs with the associated level detectors in the logic unit, regulators to limit the output voltage to a safe value during high fault currents, and a tap block for selecting the ratio, K, of positive to negative-sequence sensitivity.

The incoming current connections are made to the DA block on the rear of the network unit. If the SLD is furnished as a part of an equipment with a test panel,the connections to the DA block will be made via a 10-conductor cable which plugs into the TDA test and connection receptacle. This receptacle allows disconnection of the SLD network unit from the line CT's by removal of the connection plug, and AC testing by means of the standard Type XLA test plug.

Output voltage signals appear at a 10-point socket(s) at the rear of the unit for interconnection with the logic unit through a shielded-cable.

### Logic Unit

The logic unit contains printed circuit cards identified by a code number, such as D13, L4 and T32, where D designates discriminator, L designates logic and T designates time delay. There is also a small panel containing test-pushbuttons for simulating selected functions such as Channel Start, links for

selection of optional functions in the logic circuitry and, on certain models, target lamps. Mounted behind the printed circuit cards are isolating transformers, resistors and other discrete circuit compone

The printed circuit cards plug in from the front of the unit into sockets marked with letter designations, or "addresses" (D, E, F, etc.), that appear on the guide strips in front of each socket, on the component location diagram and on the logic unit internal connection diagram. These diagrams for a speci SLD model are included in an associated "adder" to this book. The test points (TP2, TP3, etc.) shown on the internal connection diagram are connected to instrument jacks on a test card in position T with TP1 at the top of the card.

All input signals to the logic unit (with exception of inputs to contact converters) are made through shielded-cable plug sockets on the rear of the case. The sockets and entering cables are identif on the component location diagram for the specific relay, included in the "adder" to this book.

The output connections, as well as input connections to the contact converters, are made through ten-point terminal strips on the back of the unit. These terminal strips are identified as DB, DC, etc. depending on how many are present. On most equipments the points on these terminal strips are connected by way of ten-conductor cables to corresponding points on test and connection receptacles (TDB, TDC) loca ted on the equipment test panel. These receptacles permit disconnection of all relay outputs from the system and, at the same time, provide accessibility to all output points by means of a standard Type XLA test plug.

SLD's that require an associated SLA have their logic unit outputs made through shielded-cable plug sockets on the rear of the case.

When mechanical targets and target lamps are present, a window with one or more reset buttons is located on the front cover.

The outline and mounting dimensions of the case and physical location of the components for both net work and logic unit of a specific SLD are included in an "adder" to this book.

## RECEIVING, HANDLING AND STORAGE

These relays will normally be supplied as a part of a static relay equipment, mounted in a rack or cabinet with other static relays and test equipment. Immediately upon receipt of a static relay equipmen it should be unpacked and examined for any damage sustained in transit. If injury or damage resulting fr rough handling is evident, file a damage claim at once with the transportation company and promptly notif the nearest General Electric Sales Office.

Reasonable care should be exercised in unpacking the equipment. If the equipment is not to be installed immediately, it should be stored indoors in a location that is free from moisture, dust, metall chips, and severe atmospheric contaminants.

Just prior to final installation the shipping support bolt should be removed from each side of all relay units, to facilitate possible future unit removal for maintenance. These shipping support bolts ar approximately 8 inches back from the relay unit front panel. Static relay equipment, when supplied in sw rack cabinets, should be securely anchored to the floor or to the shipping pallet to prevent the equipmen from tipping over when the swing rack is opened.

## INSTALLATION TESTS

The Type SLD relay is usually supplied from the factory mounted and wired in a static relay equipmen All units of a given terminal have been calibrated together at the factory and will have the same summary number on the unit nameplates. These units must be tested and used together.

### Necessary Adjustments

The following checks and adjustments should be made by the user in accordance with the procedures given below under DETAILED TESTING INSTRUCTIONS, before the relays are put in service. Some of the following items are checks of factory calibrations and settings, or installation connections and hence do not normally require readjustment in the field. Other items cover settings or adjustments which depend on installation conditions and, hence, must be made on the installed equipment:

1. Network balance check.
2. CT phasing, polarity and sequence check.
3. Level detector adjustment.
4. Transmitter drive symmetry adjustment.

5. Phase delay adjustment.
6. Trip integrator time check.
7. Transient blocking (RB) timer checks.

Before beginning the installation tests, check for installation of all interconnecting cables from the network unit to the logic unit, from logic unit to power supply, and from logic unit to SLA (if used). If the SLD is being applied with a phase distance relay, as previously described, the interconnecting cables from SLY to SLD, and from SLY to SLA (if used) should also be checked.

## General Testing Instructions

### 1. Input Circuits

The network unit for the SLD has a 10-point terminal block, identified as the DA block mounted on the rear of the unit. When the SLD is used in an equipment having a test panel, the incoming leads from the line CT's will be brought to the DA block via a test and connection receptacle identified as TDA. Test currents can be supplied to the network unit through the standard Type XLA test plug.

If other test facilities are used, input currents should be applied to test points which connect to the same DA terminal points as those shown on the test circuit diagrams.

### 2. Output Circuits

Output voltage signals from the network unit are carried to the logic unit by a 10-conductor shielded cable. Output voltages of the two networks may be checked at test jacks J1 (positive sequence) or J2 (negative sequence), which are located on the front panel of the network unit. These test signals are measured with reference to the "REF" jack on the front of the logic unit or test point TP1 on the test card.

The logic unit includes a test card in the right hand (T) card position. This test card has 10 pin jacks mounted on the outer edge of the card and numbered TP1 to TP10 from top to bottom. The location of these several test-points in the circuit is shown on the logic unit internal connection diagram in the "adder".

Output signals from the logic unit are measured with respect to the reference bus, which is accessible at TP1. Output voltages at the various test points are on the order of +10 to +15 volts for the ON condition of the card being checked, and less than one volt for the OFF condition. This output can be checked with an oscilloscope, a portable high-impedance voltmeter, or with the test panel voltmeter if available. When the test panel voltmeter is available, its negative terminal will normally be connected to the reference bus, so to connect the meter for testing it is only necessary to connect a test lead from the Relay Test Jack on the test panel to the test point pin-jack on the logic unit. The pushbutton adjacent to the Relay Test Jack must be pushed before the meter will read.

Where time delay cards, such as the trip integrator or the phase delay card are to be adjusted or checked, a dual-trace oscilloscope with calibrated horizontal sweep, and with external trigger sweep input, should be used.

## CAUTION

IT IS A DESIGN CHARACTERISTIC OF MOST ELECTRONIC INSTRUMENTS THAT ONE OF THE SIGNAL INPUT TERMINALS S CONNECTED TO THE INSTRUMENT CHASIS. SINCE THE SLD REFERENCE VOLTAGE, WHICH NORMALLY WILL BE CONNECTED O THE GROUND INPUT OF THE INSTRUMENT, IS NEAR THE (+) OR (-) STATION BATTERY VOLTAGE LEVEL, THE INSTRU- ENT CHASIS MUST BE INSULATED FROM STATION GROUND. IF THE INSTRUMENT POWER CORD CONTAINS A THIRD LEAD, HAT LEAD MUST NOT BE CONNECTED TO STATION GROUND. HOWEVER, IF THE INPUT TO THE OSCILLOSCOPE IS A IFFERENTIAL AMPLIFIER AND NEITHER INCOMING VOLTAGE SIGNAL LEAD IS TIED DIRECTLY TO THE INSTRUMENT GROUND, T IS NOT NECESSARY TO OBSERVE THE ABOVE PRECAUTIONS.

## DETAILED TESTING INSTRUCTIONS

Before proceeding with the following installation test program, be sure that the Silicon Controlled ectifier (SCR) tripping circuits in the associated logic unit are open. When a test panel is included n the equipment this can best be accomplished by pulling the connection plug from the associated test eceptacle.

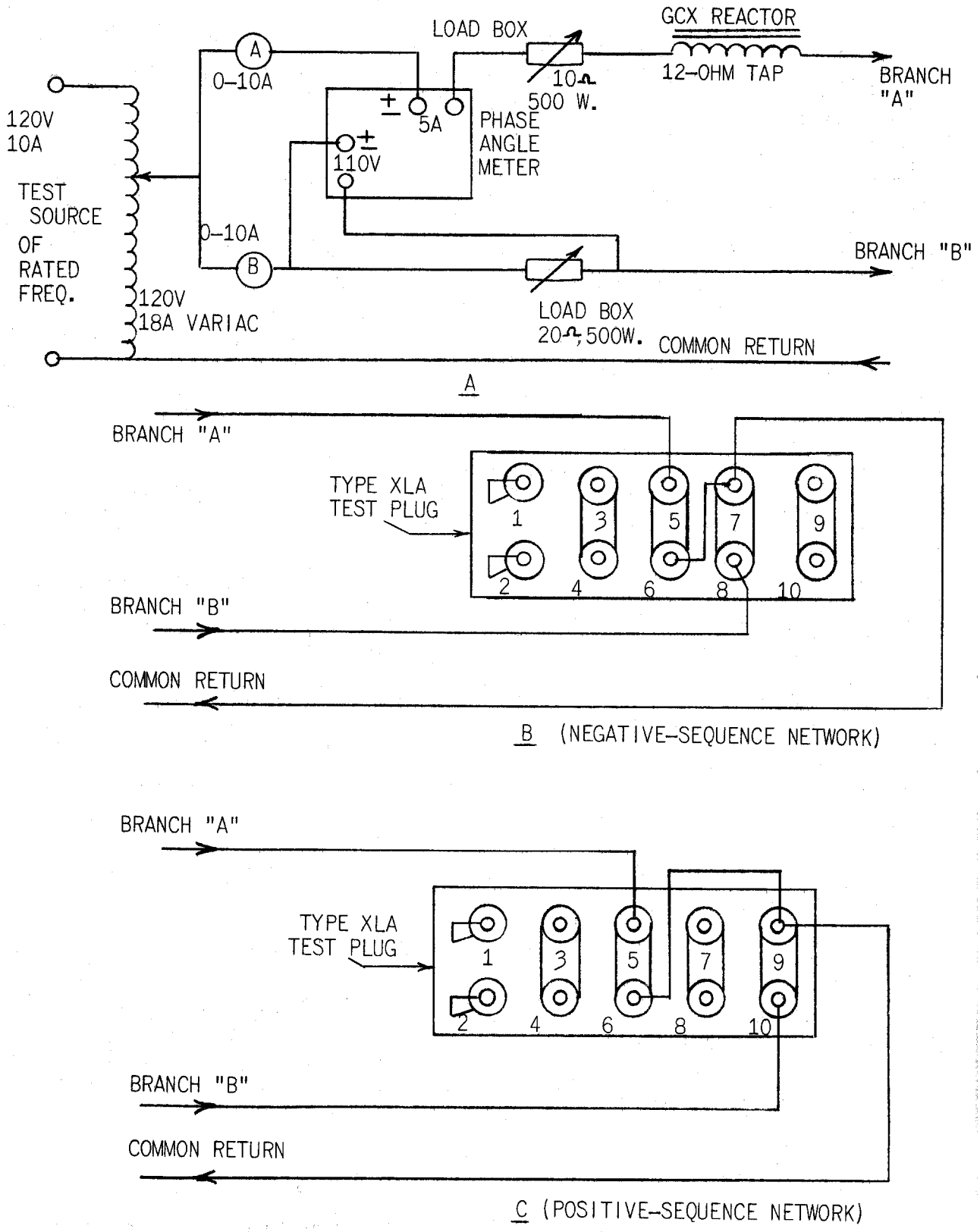



FIG. 8 (0178A9079-1) TEST CONNECTIONS FOR CHECKING BALANCE OF NEGATIVE AND POSITIVE SEQUENCE NETWORKS IN SLD RELAYS

## Network Balance Check

The network unit circuits have been accurately preset at the factory to obtain positive-sequence cancellation in the negative-sequence network and negative-sequence cancellation in the positive sequence network. No further adjustments should be required in the field. It is recommended, however, that the following checks be made at the time of installation to insure that nothing has occurred during shipment to upset the networks. The following paragraphs are written on the premise that a test panel with drawout test receptacles is available in the equipment and that Type XLA test plugs will be used to gain entrance to the networks.

The basic circuit used in checking both networks is shown in Figure 8. This arrangement provides means of obtaining two test currents of equal magnitude but separated by $60^{o}$. Then by appropriate connections to the networks it is possible to simulate either a balanced 3-phase positive-sequence current (Figure 8B) or a balanced negative-sequence current (Figure 8C). During the following tests the basic current level in each branch will be 5 amps, and since these currents will add at a $60^{o}$ angle, the total load in the Variac will be about 8.7 amps. It is desirable that the 110 volt scale of the phase angle meter be used to minimize the effect of this potential circuit on the relation between the two test currents. It is further desirable that the Variac be set near its maximum voltage output and that the load boxes be set to obtain approximately 5 amps as a preliminary step, since this will provide the greatest possible voltage to the phase angle meter and will insure the best possible accuracy.

1. Negative-Sequence Network (Jumper the J1 jack to the Ref. Jack)

To check the negative-sequence network for positive sequence cancellation, arrange a Type XLA test plug as shown in Figure 8B and connect the branch "A", branch "B", and common return leads as shown to simulate a balanced positive-sequence input to the relay. This is accomplished by setting one current (branch "A") to lag a second equal current (branch "B") by $60^{o}$ and by reversing the branch "B" current at the relay. Branch "A" current now simulates phase A relay current and reversed branch "B" current which lags branch "A" by $120^{o}$, simulates phase B relay current. Phase C current is not used in the negative-sequence network.

The above mentioned phase notation assumes relay external connections corresponding to phase sequence A-B-C. For phase sequence C-B-A the external connections to the relay would be such that branch "A" test current would simulate phase C; and the phase A current would not be involved in the negative-sequence network.

The following procedure is suggested:

1. Adjust the branch "B" load box to obtain approximately 5 amps when the Variac is set for 110 volts.
2. Adjust the branch "A" load box until the phase angle meter indicates a $60^{o}$ lag of current with respect to voltage.
3. Readjust the branch "B" load box until branch "A" and "B" currents are equal.
4. Adjust the Variac until both currents are 5 amps.
5. Touch up branch "A" load box for angle trimming and branch "B" load box for magnitude trimming.

Now connect an oscilloscope with its ground at the TP1 test point in the SLD logic unit and its vertical input at the J2 test jack on the network unit. Set the scope sensitivity to observe the waveform with readable deflection. This should be a distorted wave at system frequency. With perfectly balanced currents and a network which has been perfectly adjusted, the waveform observed at J2 should consist solely of harmonics (primarily third and fifth).

Since perfection is seldom realized, the branch "A" and branch "B" load boxes should now be touched up until the waveform contains no fundamental component, and then the Variac readjusted until the branch "B" current is again 5 amps. Branch "A" current should be 5 amps $\pm$ 0.5 amps, and the angle between the "A" and "B" currents should be $60^{o} \pm 3^{o}$. The peak-to-peak value of the network output, which now will consist solely of harmonics, will depend on the system, but should be on the order of a few tenths of a volt.

2. Positive-Sequence Network (Jumper the J2 jack to the Ref. Jack)

To check the positive-sequence network for negative-sequence cancellation use the test plug arrangement and branch "A" and branch "B" connections shown in Figure 8C to simulate a balanced negative-sequence input to the relay. This is accomplished by the same scheme described in the the negative-sequence section above, except that the reversed branch "B" current, which lags branch "A" current by $120^{o}$, now simulates the phase C relay current. Phase B current is not used in the

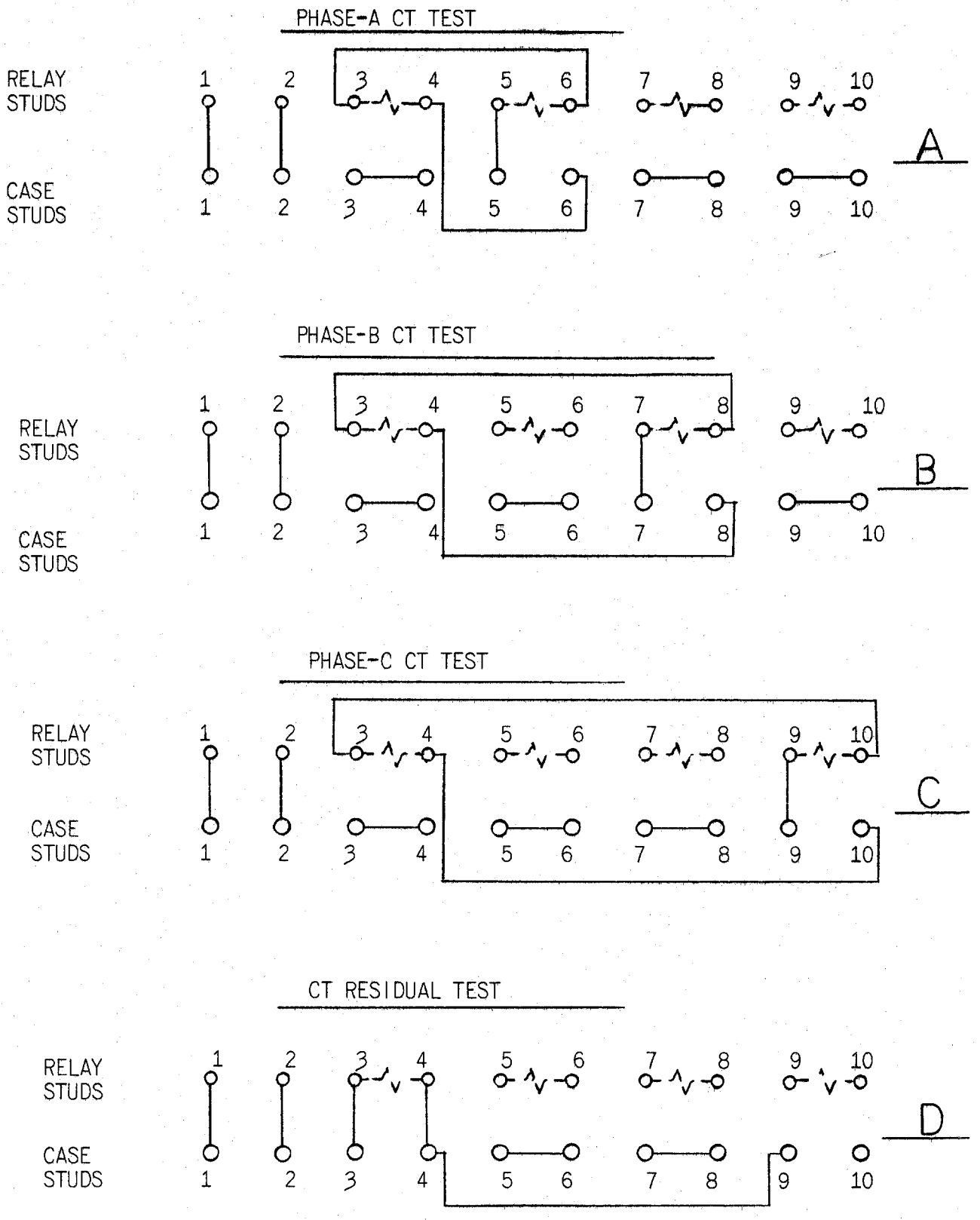



FIG. 9 (0178A9086-0) TEST PLUG CONNECTIONS FOR CT PHASING

positive-sequence network for phase sequence A-B-C.

Follow the same five step procedure described in the negative-sequence section for obtaining the 5 ampere branch "A" and branch "B" currents separated by $60^{o}$. Observe the positive-sequence network output at test jack J1. Trim up the branch "A" and branch "B" currents and the angle to eliminate the fundamental as previously described. With the branch "B" current at 5 amps, the branch "A" current should be 5 amps ± 0.5 amps and the angle $60^{o} \pm 3^{o}$. The peak-to-peak value of network output, as before, will be harmonics of a few tenths of a volt in magnitude.

If the corrected phase angle meter readings and/or the corrected ammeter readings are outside the limits given above, a readjustment of the network should be considered. However, this should be done only after a thorough verification of the previous measurements. The factory adjustments were made with specialized equipment to obtain an accuracy of the current relationships within much tighter limits than those given above. Any readjustments should be attempted only under very carefully controlled conditions.

CT Phasing, Polarity, and Sequence Check

The following tests on CT phasing, polarity and sequence are desirable to assure that coordination between terminals will be realized, and are readily made when power line carrier is used as the pilot channel. The tests provide a means of checking that for phase sequence A-B-C, phase A CT is connected to the DA5-DA6 circuit of the network unit with the same polarity at both terminals, that phase B CT is similarly connected to the DA7-DA8 circuit, phase C CT to the DA9-DA10 circuit, and that the return current path for CT residual current is properly connected to DA3 and DA4. For phase sequence C-B-A, the phase C CT will connect to DA5-DA6, and phase A CT to DA9-DA10. The carrier channel is used to communicate phase angle information between terminals.

In order to make the test it is necessary that load current be flowing in the line. The magnitude of the load current should be at least five times the single-end-feed line charging current to assure readable through-fault current relationships. If charging current is too high relative to load current, the phase difference between currents at the two ends will make it difficult to interpret correctly the results of the following tests. In the following tests, load current in each phase is used independently to simulate a corresponding line-to-ground fault.

Since the carrier pilot channel is used in this test, it is necessary that the simulated phase-to-ground fault current be above the FDL level detector operating point, and that the associated SLA be energized so that the FDL, and squaring amplifier in the SLD will initiate the transmission of carrier RF on alternate half cycles of fault current (i.e. half cycle on, half cycle off). The FDL level detector was set at 0.2 amps negative-sequence.

For a simulated phase-to-ground fault the negative-sequence component is one-third the line current. Therefore, it is necessary that the secondary load current be at least 3 x 0.2 amps, or 0.6 amps. If load current exceeds this value, the low-set level detector FDL (and FDM when used) should both operate and the squaring amplifier will have a nearly symmetrical output.

The test plug connections in Figure 9A, 9B and 9C will yield the correct line-to-ground current flow in the network unit for phase A, phase B, or phase C CT tests respectively. To obtain a current in the CT residual circuit for checking polarity of connections, it will be necessary to bypass one phase current around the network residual current windings temporarily. If the DA3, DA6, DA8 and DA10 points in the network unit connect directly to the relay neutral point, then the phase C current can be safely bypassed as shown in the CT residual test diagram in Figure 9D.

If the DA points do not connect directly to the relay wye point, then the test connections in Figure 9D can be used only if the phase C current can be safely interrupted and the residual current increased to load magnitude in other relays which may be interposed between the DA block and the wye point. (Note that above phase notations refer to phase sequence A-B-C).

The required procedure is outlined below:

1. Connect a Type XLA test plug in accordance with Figure 9A at each terminal of the protected line.

2. Connect the vertical input of a scope to the RF jack of the CS26 carrier receiver and the ground input of the scope to the carrier chassis.

3. Now insert the test plug into the TDA test receptacle at each end of the line. This will simulate a phase A to ground through fault.

4. Two levels of carrier RF should be observed on the scope, the higher from the local transmitter and the lower from the remote transmitter. The two levels of carrier should adjoin each other every half cycle with a dead space between of not more than one-sixth of a half cycle ($30^{o}$). While the width of this dead zone between adjacent blocks of carrier RF is not rigidly limited, it must be small enough to establi that is has not resulted from a CT phasing error. The higher amplitude RF duration is very close to one half cycle long and may be used as a time reference.

Repeat the above steps for each of the phase and ground test plug connections. If the results of eac test are satisfactory, it indicates that CT phasing and polarity are correct. If the carrier signals do not intermesh properly,the connections between the network units and CT's, or the phasing of CT's at opposite terminals, should be investigated.

With CT polarity and phasing established, check that the phase sequence is correct by observing the voltage between jack J2 on the network unit and SLD reference (TP1). If the sequence is not correct, the load current will appear as negative-phase-sequence current to the negative sequence network and the outpu voltage at J2 will be sinusoidal and have an amplitude of approximately 5 times the secondary load current With correct phase sequence the waveform at J2 will contain a much lower fundamental component and will contain a large percentage of harmonic components.

Level Detector Adjustment

The following paragraphs cover the checking and adjustment of level detectors FDL, FDH and FDM (when used). These cards have been set at the factory to operate at the minimum point of their published operating ranges. The procedure for setting the operating level of G4 is also explained.

1. FDL and FDH Level Detectors

The FDL and FDH level detectors should now be set at the operating points determined in the CALCULATION OF SETTINGS section.

a. If the quantity $I_2 - {}^{I}1/K$ is the input quantity to FDL and FDH connect a jumper from jack J1 in the network unit to ref. at TP1 in the logic unit. This shorts down the positive-sequence networ output so that FDL and FDH can be checked and adjusted in terms of negative-sequence current. This i not necessary when FDL and FDH operate from negative-sequence network output only.

b. Prepare a test plug with link arrangement and test source connections as shown in Figure 10. This provides the $\emptyset_A$-$\emptyset_B$ test current.

c. Check for FDH operation by means of a scope connected from the test point located just after the FDH card to TP1.

d. Using a low-range a-c ammeter increase the test current slowly until a deflection of the scope trace indicates that FDH has operated. As set at the factory this card should operate when the current measured in the test setup of Figure 10 is equal to $\sqrt{3}$ x (minimum published pickup) ±4 percent tolerance. Set FDH to operate at the level determined in CALCULATION OF SETTINGS by means of the screw adjustment on the FDH card. Turning the screw clockwise increases pickup.

e. Check FDL operation by means of a scope connected to the appropriate test point and raise the test current until a deflection of the trace indicates operation. As set at the factory, FDL should operate at $\sqrt{3}$ x (minimum published pickup) ±4 percent tolerance. Reset FDL, if necessary to operate at the point determined under CALCULATION OF SETTINGS.

f. The level detectors used in the SLD relays have a very high non-adjustable dropout. Check the dropout of the FDL and FDH cards by reducing the test current after the operating point has been reached. The dropout point will be between 98 and 100 percent of the operating point.

g. If the SLD is being applied without a phase-distance relay check FDH operation on positive-sequence current. Remove the J1-Ref. jumper and connect a jumper from J2 to Ref. Using the Figure 10 test circuit increase test current until FDH operates. This operating point should be approximate K times the negative-sequence setting (Par. d above).

2. FDM Level Detector (When Used)

When the SLD is applied with a phase-distance relay the FDM level detector will be present. FDM was set at the factory to operate at its minimum setting of $\sqrt{3}$ x (minimum published pickup) amps

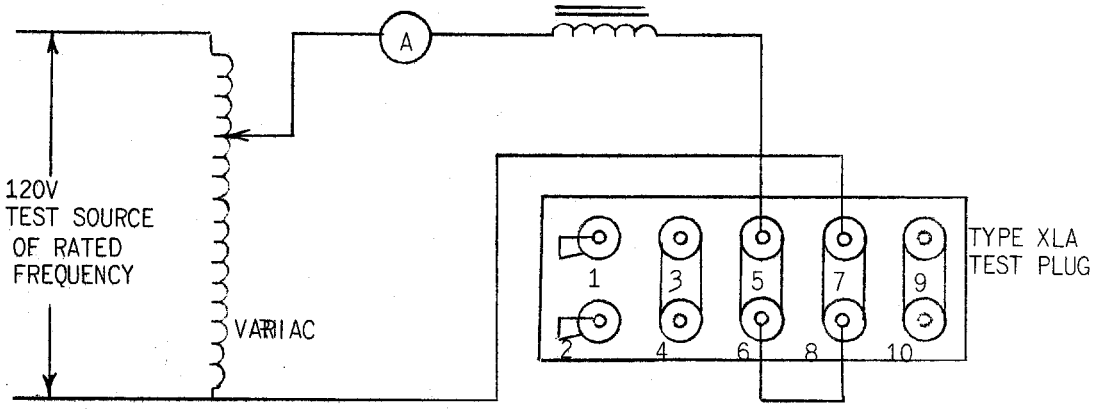



FIG. 10 (0178A9084-1) TEST PLUG CONNECTIONS FOR CHECKING FDL AND FDH

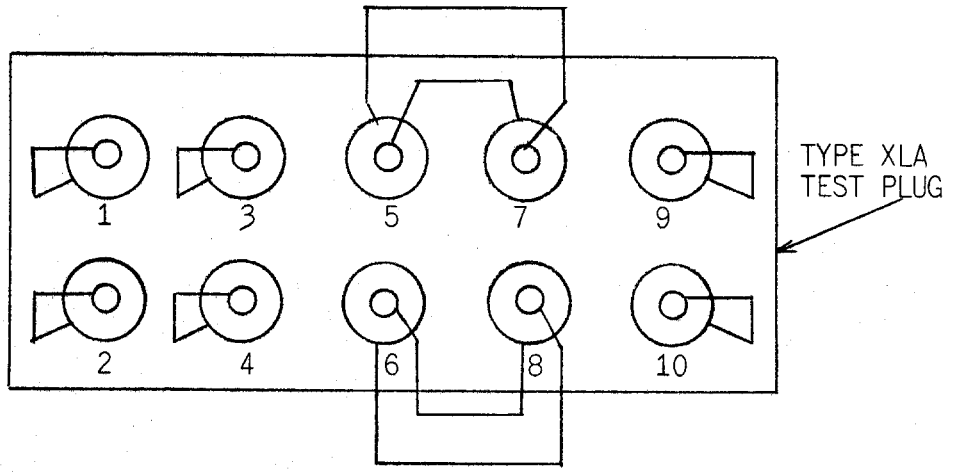



FIG. 11 (0178A9082-0) TEST PLUG CONNECTIONS WHEN LOAD CURRENT IS USED FOR PHASE DELAY ADJUSTMENT

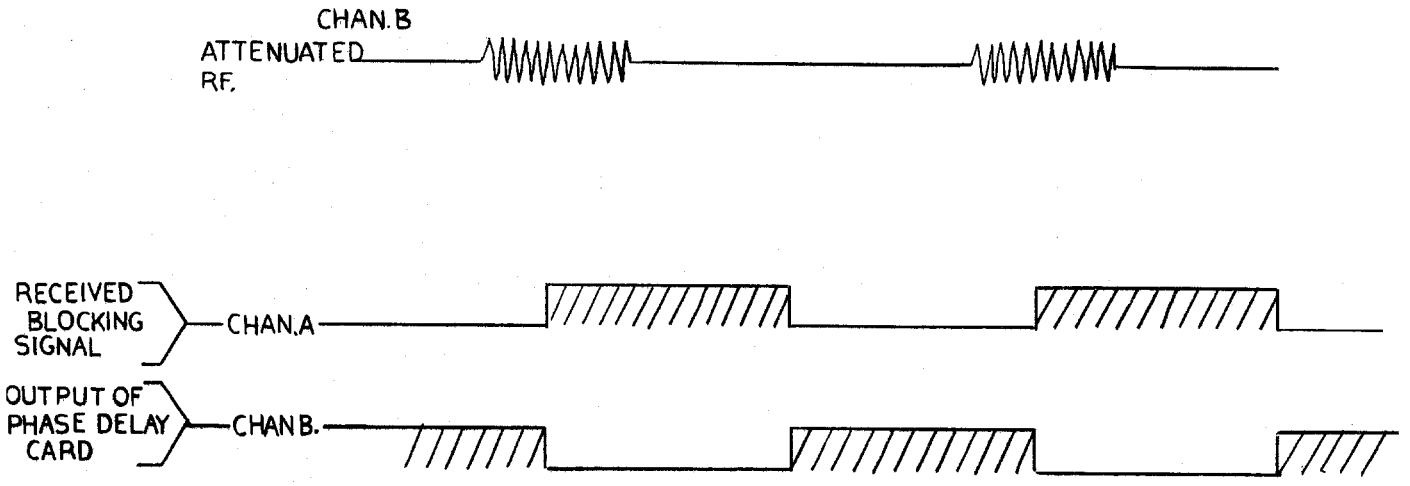



FIG. 12 (0226A6980-0) ADJUSTMENTS OF PHASE DELAY BY LOCAL SIGNAL

Ø-Ø test current (see Figure 10). Its positive-sequence operating point will depend on the setting of the "K" tap screw (see CALCULATION OF SETTINGS).

The operation of FDM can be checked by means of the test circuit of Figure 10. When checking negative-sequence pickup short down the positive-sequence network output by connecting a jumper from test jack J1 to Ref. at TP1.

The positive-sequence operating point of FDM should be checked by means of the same test circuit but with the negative-sequence network output shorted by means of a J2-Ref. jumper. Its operating point should be K x negative-sequence operating point.

3. G4

The G4 pickup level can be checked and adjusted using the test circuit of Figure 10, except the test current leads should be connected to relay side studs 3 and 4 instead of studs 5 and 7. Be sure that the G4 link in the logic unit is in the IN position, and connect an oscilloscope from the test point monitoring G4 output to Ref. The nominal logic ON voltage levels previously specified will indicate a G4 operation, and the pickup level can be adjusted by means of the pot screw on the G4 level detector card (clockwise rotation increases the pickup level).

Transmitter Drive Symmetry Setting

This adjustment of the transmitter drive symmetry card refines the duration of the transmitter blocking output at one terminal to produce equal half cycle of receiver output at the remote terminal. This adjustment compensates for asymmetry in the half cycle blocking signal which may be introduced by the receiver tuned circuit. Since this adjustment depends on operating conditions in service, it cannot be made at the factory. Before this adjustment is made it is essential that the channel receiver and transmitter be adjusted as prescribed in the INSTALLATION ADJUSTMENT section of the channel set instruction book.

Assume that the protected line section is A-B with A the local terminal and B remote. At station B connect a scope to observe the received blocking signal. Supply the network unit at station A with test current using the connections shown in Figure 10. Raise the test current to about 10 percent of the FDH operating point so as to operate FDL but not FDH. This will cause the channel set at station A to key ON and OFF with both ON and OFF times of approximately half cycle duration.

At station B set the scope horizontal sweep so that one full cycle is spread across the screen and observe the duration of the "block" (positive) and "non-block" (zero) half cycle. At station A adjust blocking transmission time by means of the screw adjustment on the symmetry adjustment timer card so that the "block" and "non-block" half cycle at station B are exactly equal. Clockwise rotation of the adjustin screw increases the "non-block" half cycle. Be sure that the red tap lead on the symmetry adjustment time card is in the "S" position. It is necessary to withdraw the card to see this lead.

The symmetry card at station B must also be adjusted to produce equal "block" and "non-block" half cycles at station A. This should be done after the sequence networks and level detector checks have been made at B. On multi-terminal lines, when adjusting the symmetry timer card at a given station observe the receiver output at the nearest remote station.

Phase Delay Adjustment

The object of this adjustment is to set the local trip half cycle, which is applied to the comparer, so that it is in phase with the received blocking half cycle which results from transmission of carrier from the remote terminal during a through fault. This adjustment is necessary to compensate for such things as channel delay introduced by the receiver filters and propagation time in the line, and the shift in the leading edge of the transmitted signal by the transmitter drive symmetry card. Since the phase delay is affected by service conditions, it cannot be made at the factory.

Three possible methods of making the phase delay adjustment are listed below with the limiting conditions shown:

1. Load Current Method

In this test, load current in the line is used to simulate negative-sequence current. It is necessary that the secondary load current be greater than the negative-sequence current setting of th FDL fault detector, or that load current be at least equal to the minimum available setting of FDL in which case it will be necessary to temporarily reduce the FDL setting to its minimum value. If this method is to produce an accurate setting, it is also necessary that the ratio of line charging

current to through load current be low enough so that the phase displacement between currents at the two ends of the line does not exceed 10 degrees.

If these conditions are met, the procedure outlined below should be followed. If the conditions are not met, it will be necessary to use one of the alternate schemes described below.

At each terminal prepare test plugs with connections as shown in Figure 11. This will cause phase A current to flow in phase B relay coils and vice versa, thereby making balanced load current appear as negative-sequence current to the relay.

If necessary, reduce the operating point of the FDL level detector to the minimum value following the procedure described previously.

At station A (local) a continuous signal must be applied to the channel stop circuit of the logic unit to prevent local transmission of carrier.

At station B (remote) a trip output must be prevented from stopping carrier transmission from that end. This can be accomplished by removing the AND card following the trip integrator timer.

Using a dual trace scope at Station A, connect trace A vertical input to the test point monitoring the NOT input to the comparer, trace B vertical to the test point monitoring the input to the comparer from the phase delay timer output and scope ground to TP1.

Now insert the test plugs into the TDA test receptacle at each terminal of the protected line. A half cycle blocking signal (equal "block" and equal "non-block" duration) should appear on trace A as the result of transmission from Station B. The local tripping signal should appear on trace B. The "on" and "off" durations of this half cycle tripping signal should be very nearly equal, but the tripping signal (trace B) probably will not line up with the received blocking signal (trace A) since this adjustment depends on characteristics of individual receiver filters and must be made under service conditions.

Two adjustments are provided on the phase delay card to bring the tripping signal in line with the blocking signal. The pot adjacent to the card controls the leading edge and the pot away from card controls the trailing edge of the signal. Adjust these two pots on the card so that the positive half cycle of the tripping signal lines up with the positive half cycle of the blocking signal.

After the phase delay adjustment is completed remove the Type XLA test plugs at both terminals, remove the connections at Station A that prevented local transmission of carrier and replace the card(s) at Station B removed to prevent a trip output from stopping transmission.

2. Test Source Method

If the line is not loaded, is carrying insufficient load, or if the ratio of charging current to load current is too high, an a-c test source can be used at each station to operate FDL and FDM, provided the sources are in phase. Use the test connections shown in Figure 10 at Station A, and similar connections at Station B except interchange the connections to relay points 5 and 7 of the test plug. This will simulate a through fault.

Before proceeding with phase delay adjustments the phase relation of the two test sources should be checked to insure that the two sources are in phase. If power line carrier is used,the following procedure is applicable. With the test plugs inserted at each terminal of the line raise the test current to approximately 90% of the FDH operating point so that FDL will operate but not FDH. At the local terminal connect the vertical input of the scope to the RF jack of the carrier receiver and the scope ground to the carrier chassis. Two levels of the RF should be observed on the scope, the higher from the local transmitter and the lower from the remote transmitter. If the two test sources are substantially in phase, the two levels of carrier RF should adjoin each other every half cycle with very little dead space of overlap between adjacent levels of carrier. For the phase delay adjustment to have any value the dead space or overlap should not exceed $10^{0}$.

The a-c source for the test connections of Figure 10 will usually be station service a-c, and on long-line applications it will usually be found that the test sources are displaced by too great an angle to be of any use for the installation adjustment of the phase delay.

If at least one of the stations of the protected line is equipped with line-side potential devices or transformers it is possible that substantially in-phase test sources can be obtained at the two ends by supplying the test circuit of Figure 10 from the potential device or transformer and operating the line with the breaker at one end open. The open end is of course the location where line-

side potential is available. With this arrangement the voltages at the two ends will differ only by the drop in the line inductive reactance caused by the line capacitive charging current, and this primarily be a magnitude difference. It is of course essential that the normal installation adjustments be made on the potential devices prior to this test.

Having obtained a-c test sources that are substantially in phase, proceed to adjust the phase delay settings as described in the Load Current section above, using a dual-trace scope and removing the specified cards.

3. Local Signal Method

If neither of the above adjustment methods can be used, an adjustment of the phase delay can be made on the basis of the local keyed-carrier signal. This method assumes that power line carrier is used, and the carrier receiver gain control and attenuator have been temporarily reset to provide the "normal margin" above the cutoff point of the received signal due to local transmission. The recommended "normal margin" is given in the carrier equipment instruction book under INSTALLATION ADJUSTMENTS.

First cause the local transmitter to send a full-strength RF signal by turning the carrier test switch (CTS on test panel) to SEND. Observe and record where receiver attenuator is set, and then turn the receiver attenuator in a counter-clockwise direction until the cutoff point is reached (SA relay will drop out and white lamp on relay test panel goes out). Now turn attenuator back to provide the normal margin (as noted previously) from this cutoff point, as determined by the attenuator dial markings. Presumably with this attenuator setting the local transmitter will drive the local receiver at approximately the same level as the RF signal received from the remote terminal would drive it with the installation settings of the transmitter and receiver.

The a-c test circuit of Figure 10 will be used. Raise the test current (Figure 10) to about 90% of FDH pickup. Connect scope channel B to the RF jack, channel A to the test point monitoring the NOT input to the comparer, and scope ground to relay Ref. at TP1. Observe the signals shown in the top two traces of Figure 12. The Channel A signal should be very close to equal "ON" and "OFF" times since the conditions are very close to those for which the symmetry setting was made.

Now shift channel B input to the test point monitoring the input to the comparer from the phase delay timer output and set the phase delay timer card adjustments so that the local trip signal on the comparer lines up with the "OFF" time of the A trace.

This adjustment method neglects propagation time of the carrier signal between the two terminals which is 1 millisecond for 186 miles of line. The setting can be further refined for long lines by calculating the theoretical propagation time for the line and shifting the trip signal to the right (delayed) by a time interval equivalent to this propagation time.

After the setting is complete reset the attenuator at its original position as recorded at the start of this test. Remove the test plug and replace the TDA connection plug.

Trip Integrator Time Check

The trip integrator card has been adjusted at the factory to provide a delay of 3 milliseconds betwee comparer output to trip integrator output, and sufficient delay on release so that once an output is produced it will be continuous with half cycle repetitive input.

The purpose of the trip integrator card is to insure that tripping does not occur on extraneous spikes of comparer output which may result from transient voltages, network mismatch, phase delay mismatch or CT errors. Adjustment of the trip integrator time is not considered to be part of the normal installation procedure. However, a check on the integration time may be desirable at the time of installation to be sure that unintentional changes have not occurred.

In the field a quick check of the trip integrator may be made by using a scope with a calibrated time base and an external sweep trigger. Specific procedures for timer card checks and adjustments are given in the printed circuit card instruction book, GEK-7364.

Transient Blocking (RB) Logic

The RB transient blocking logic is designed to operate and block phase comparison tripping at the AND following the trip integrator timer if a fault detector operation (either FDL, FDH, MB or MT) is not followed by a comparer and trip integrator output within a set time of A milliseconds. Once established, the RB circuit will maintain blocking for the duration of its release time, B milliseconds.

The operation of the RB function timer can be checked in the field in a similar manner to the trip integrator timer. Once again, refer to GEK-7364.

## MAINTENANCE

### Periodic Tests

CAUTION: BEFORE STARTING ANY PERIODIC TESTS ON SLD RELAYS THE TRIP COIL CIRCUIT OF THE CIRCUIT BREAKER SHOULD BE OPENED BY REMOVING THE CONNECTION PLUG IN THE TEST PANEL ASSOCIATED WITH THE TRIP CIRCUITS, OR BY OPENING OTHER TEST SWITCHES PROVIDED FOR THIS PURPOSE.

During a periodic check of the equipment, the level detector operating points (FDL, FDH and FDM) should be checked against the factory set points or the operating points set druing the installation tests, using the test connections of Figure 10.

Any check of the transmitter drive symmetry or phase delay card requires operators at both terminals of the line and should not require checking during normal periodic test programs. If it is desired to check the adjustment of these functions follow the procedures described in the sections on installation tests.

### Trouble Shooting

In any trouble shooting of equipment, it should first be established which unit is functioning incorrectly. The overall logic diagram supplied with each equipment contains the combined logic of the SLD and other associated relays, and the various test points in each unit. By signal tracing using this overall logic diagram and the various test points it should be possible to quickly isolate the trouble.

A Test Adapter Card, 0128B2221G1, is supplied with each static relay equipment to supplement the pre-wired test points on the test card. This adapter can be plugged into any card position, and then the logic card for that address can in turn be plugged into the adapter. The unit test card can then be plugged into the second socket in the adapter, giving access to all ten connection points by instrument jacks while the logic card is operating in the circuit. The connections to each pin on the adapter logic card socket are individually removable to allow circuit wiring changes to the logic during trouble-shooting.

An oscilloscope is a valuable aid to detailed trouble shooting, since it can be used to determine phase shift, operate and reset times, as well as input and output levels. A portable dual-trace scope with a calibrated sweep is recommended.

### Spare Parts

To minimize possible outage time, it is recommended that a complete maintenance program should include the stocking of at least one spare card of each type. It is possible to repair damaged or defective components on the printed circuit cards, but great care should be taken in soldering so as not to damage or bridge-over the printed circuit busses, or overheat the semiconductor components. The repaired area should be recovered with a suitable high dielectric plastic coating to prevent possible breakdowns across the printed busses due to moisture and dust. The complete wiring diagrams and component values for the various cards of a specific SLD relay are included in the "adder" to this instruction book.