INSTRUCTIONS

GEK-34156A

STATIC PHASE COMPARISON RELAY

TYPE SLD42H4

POWER SYSTEMS MANAGEMENT DEPARTMENT

GENERAL ELECTRIC

CONTENTS

SLD42H4

DESCRIPTION

The SLD42H4 is a static phase comparison relay that employs negative sequence excitation only. It provides high speed protection for unbalanced faults on transmission lines to which it is applied. Since it employs negative sequence excitation this equipment will not protect against balanced three phase faults, nor does it provide any backup protection for faults on the line or the adjacent system.

The static relay is packaged in two separate cases suitable for mounting on standard 19 inch racks. The network unit which is three rack units (1 3/4" equal 1 rack unit) includes the sequence network, adjustment potentiometers, and the tap block. The network unit also includes voltage limiter circuits and isolation transformers to couple the output voltage signals to the logic unit. The accompanying logic unit is two rack units and contains the necessary printed circuit cards to provide the operating functions.

The following table identifies included diagrams which describe these units.

	FIGURE NUMBER	
	NETWORK	LOGIC
OUTLINE & MOUNTING DIAGRAM	1	4
COMPONENT LOCATION DIAGRAM	2	5
UNIT INTERNAL	3	6

The card internals are given in GEK-7364.

These instructions supplement information contained in the basic book GEK-26491, which is attached. It is recommended that the basic book, which includes a detailed discussion of phase comparison principles, be reviewed in conjunction with this book.

A complete terminal of this equipment requires, in addition to the SLD42H4 relay, a suitable auxiliary logic and tripping relay, Type SLA, and a d-c power supply, Type SSA, and usually a distance relay, Type SLY, for 3 phase fault protection.

The measuring functions which are included in the SLD42H3 are noted below:

FDL - low set fault detector that initiates transmitter keying.

FDH_L - low set fault detector that initiates trip attempt.

FDH_H - high set fault detector that initiates trip attempt.

G4 - non-directional zero sequence overcurrent direct trip function.

For a complete description of the overall scheme in which this relay is used, refer to the overall logic diagram and associated memorandum that covers the specific components involved in the scheme.

APPLICATION

The SLD42H4 relay provides protection against unbalanced faults only since it utilizes negative sequence excitation exclusively. The SLD42H4 relay was designed for negative sequence phase comparison protection of lines incorporating series capacitor compensation but is equally suitable to long uncompensated lines. The SLD42H4 utilizes two levels of tripping fault detectors, the lower one having a variable time delay, for those applications where a single tripping fault detector may result in a compromise of sensitivity or security.

INFORMATION REQUIRED FOR APPLICATION

In checking the application of the SLD42H4 relay the following requirements must be met:

1. The CT ratios, on the taps used, must be the same at all terminals of the line.

It should be noted that the SLD42H4 relay will not be applicable unless the requirements on minimum fault conditions as outlined below are met.

2. The minimum negative sequence fault current must be determined at each terminal of the protected line for any internal unbalanced fault under reasonable system conditions. This will establish whether the required FDH level detector settings, as determined in the subsequent section on SETTINGS will provide the required sensitivity. It is necessary that with the FDH setting thus determined, the minimum negative sequence current for an internal fault be at least 1.5 times FDH pickup.

The following system data must be known:

3. Determine the maximum value of negative sequence current that can result from normal system unbalance or heavy load flow. This will establish the minimum permissible setting of FDL to avoid operation on load.

4. The negative sequence charging current of the line during fault conditions must be determined since this may be a factor in determining the margin between FDL and FDH level detector settings. This is covered in the subsequent section on SETTINGS.

It is the responsibility of the user to determine the minimum internal fault current for which the relay must operate based on fault studies under expected system operating conditions, as well as the other information listed above. However, some points are noted below which will simplify the determinatior of the minimum fault conditions.

5. For a particular fault location and system configuration the negative sequence fault current at the relay location for a single phase to ground fault will be less than that for a phase to phase fault. Therefore, phase to phase faults need not be considered separately in checking the application.

6. For a particular fault location and system configuration the negative sequence fault current at the relay for a single phase to ground fault will be less than that for a double phase to ground fault if:

$$Z_0/Z_1 > 1.0$$

where Z_1 and Z_0 are respectively the positive and zero sequence system impedances as viewed from the fault location. Therefore, for the typical case where Z_0/Z_1 is greater than 1.0, the double phase to ground fault need not be considered since the single phase to ground fault will establish the limiting condition as far as negative sequence fault current at the relay is concerned.

It should be noted that different system conditions produce different Z_0/Z_1 ratios resulting in the possibility that a double phase to ground fault may produce the minimum negative sequence fault current.

7. Since fault studies for the systems in question may not include information on double phase to ground faults and providing this data is needed, a method is outlined below for determining the negative sequence current at the relay location for a double phase to ground fault on the basis of three phase fault and a single phase to ground fault at the same location and for the same system configuration. For any given fault location and system configuration, Fig. 7 provides a means for obtaining the negative sequence component of current; I_2' (ØØG), flowing in a line terminal for a double phase to ground fault based on the knowledge of the negative sequence component of current I_2' (ØG) flowing in the same terminal for a single phase to ground fault and of the positive sequence current I_1' (3Ø) flowing in that terminal for a three phase fault at the same location. This curve may be used to simplify the calculation of I_2' (ØØG) for a given set of system conditions and a given fault location by means of the following steps:

   a) Find the three phase fault current flowing in a given terminal I_1' (3Ø).

   b) Find the negative sequence component of current, I_2' (ØG) flowing in the same terminal for a single phase to ground fault.

c) Find the ratio of I_2' (ØG)/I_1' (3Ø) and enter the abscissa of the curve of Fig. 7 at this point, then read the ratio of I_2' (ØØG)/I_2'(ØG) from the ordinate of this curve.

d) Then by multiplying this ratio by the value of I_2' (ØG) obtained in (b) above, the negative sequence component of current for the double phase to ground fault is obtained.

If it can be assumed that the associated relaying that must be present to provide protection for balanced faults will always operate for double phase to ground faults then the minimum negative sequence current need be evaluated for single phase to ground faults only. This will permit a more secure setting for FDH without jeopardizing the sensitivity of the overall protection for double line to ground faults in those cases where a double phase to ground fault produces the minimum negative sequence current.

SETTINGS

The following a-c operated measuring functions must be set in the field to meet field conditions. Preferably calculations should be made when the application is first considered.

PICKUP SETTINGS OF FDL

The FDL level detector should be set as low as possible without the risk of its operating on the maximum expected load unbalance, unless the possibility of continuous keying of the channel is not objectionable. It is desirable that FDL be set at its minimum point of 0.2 amps negative sequence provided this setting is at least 1.25 times the maximum unbalance current.

PICKUP SETTING OF FDH_L

The FDH_L level detector must be such that it will respond to any internal unbalanced fault with a margin of at least 50 percent. That is the minimum negative sequence current for an unbalanced fault at any location on the protected line must be at least 1.5 times the negative sequence pickup of FDH_L. An additional requirement on the FDH_L pickup setting is that it be sufficiently above FDL to insure security on external faults. The setting of FDH_L must establish a margin between the local blocking level (FDL pickup) and the tripping level at the remote terminal (FDH_L pickup). For two terminal line applications the recommended margin is expressed by the following equation:

$$FDH_L = \left(\frac{4}{3}\right) FDL \qquad (1)$$

If there is significant negative sequence charging current flowing into the protected line during an external fault, it will tend to negate some of the margin provided by the above equation.

Therefore, to account for charging current the equation for FDH_L pickup becomes:

$$FDH_L = \left(\frac{4}{3}\right) FDL + I_{C2} \qquad (2)$$

where I_{C2} = the net negative sequence charging current flowing in the protected line section during an external fault.

The net negative sequence charging current in the equation above should be:

$$I_{C2} = 0.5 \times I_{C1} \qquad (3)$$

where I_{C1} = the net positive sequence charging current

$$I_{C1} = \frac{V_{LN}}{Z_{SH}} \qquad (4)$$

where Z_{SH} = total impedance of the distributed shunt capacitance in parallel with the shunt reactors.

PICKUP SETTING OF FDH_H

Since the sensitivity of the scheme is established by the FDH_L setting, the FDH_H setting should be selected to provide transient coordination between FDL at one end and FDH_H at the other, and security on the transient inrush currents when energizing the line. The FDH_H should be set low enough so that severe faults are cleared without the time delay in the FDH_L circuit required for security.

The minimum setting of FDH_H should be:

$$FDH_H = 4/3\ (FDL) + I_{C2} \qquad (5)$$

where I_{C2} is one half the positive sequence charging current of the protected line when the shunt reactors are disconnected.

I_{C2} is an empirically derived value intended to provide transient coordination between FDH_H and the remote FDL established by equation (2). This value of I_{C2} has been found to be generally applicable where breakers with preinsertion resistors are used.

PICKUP SETTING OF G4

This unit is non-directional and therefore must be set above the maximum through ground fault current ($3I_0$) for faults in either direction. A pickup setting equal to 125% of the maximum steady state through ground fault current is considered minimum, and a higher setting is recommended. If series capacitor compensated parallel lines exist, the maximum through fault current may occur for a fault on a parallel line after it opens at one terminal. On series capacitor compensated lines, a pickup setting equal to 200% of the maximum steady state through fault current is recommended.

Consideration must also be given to the possibility of unequal pole closing of the circuit breaker when the line is reclosed at the second terminal. The G4 element must be set above the maximum load transfer over a single phase for the system conditions prevailing at the time of reclosure. The same margins should be obtained in this instance as mentioned previously.

TIMER SETTINGS

One timer in the SLD42H4 is the phase delay timer. The function of this timer is described in the basic book, GEK-26491. Note that the SLD42H4 does not contain the symmetry adjustment timer which is now located in the SLA. Refer to the following section on INSTALLATION TESTS for required time settings.

The second timer is a factory set integrating timer which integrates the output of AND39 as long as FDH_L is energized. Model power system tests indicate a setting of 12 milliseconds provides excellent security.

RANGES OF ADJUSTMENT

FDL - Pickup adjustable from 0.2 - 1.6 Neg. Seq. Amps (I_2)
FDH_L - Pickup adjustable from 0.3 - 2.4 Neg. Seq. Amps (I_2)
FDH_H - Pickup adjustable from 0.5 - 4 Neg. Seq. Amps (I_2)
G4 - Pickup adjustable from 4 - 40 Amps Residual ($3I_0$)

DC BURDEN

The maximum DC burden on the Relay Power Supply is 195 milliamperes.

INSTALLATION TESTS

The installation tests described in the Basic Instruction Book, GEK-26491, are applicable to the SLD42H4 unit. However, as previously noted, the symmetry adjustment is accomplished by a timer located in the Received Carrier circuit in the associated SLA unit rather than the transmitter keying circuit as in older SLD units.

SYMMETRY ADJUSTMENT

Considering the terminal at which symmetry adjustment is being made as the local terminal, supply a 5 amp test current (ref. GEK-26491 , Fig. 10) to the remote terminal to operate FDL, FDHL and the squaring amplifier. Temporarily remove the FDH_H card. The local terminal should then receive approximately half cycle duration ON and OFF carrier signals.

At the local terminal, monitor the received carrier inverter output and the symmetry adjustment timer output in the SLA unit. Adjust the symmetry timer pickup potentiometer for minimum delay. Then adjust the reset potentiometer for equal "block" and "non-block" half cycles.

Should the Received Carrier "ON" signal exceed 8 MS, a symmetry timer pickup delay setting equivalent to the excess is required.

INTEGRATING TIMER

The integrating timer is set at the factory to produce a 10 MS. pickup delay for a continuous input signal. The pickup delay for an 8 MS. pulse width signal train (60 Hertz basis) is approximately 20 ms. (total time) or 12 MS. positive signal input time. Increased operating time for a pulsed input as compared to a continuous input signal is due to the slow reset circuit action during periods of zero input. The potentiometers on the timer are sealed at the factory and no field adjustment is intended. However, field test certification of the function can be made using the following procedure.

Temporarily remove the FDH_H and FDH_L cards. Connect a test switch between TP10 and TP4 to simulate an FDH_L signal. Connect the scope trigger to TP7 and monitor timer output at TP5. Supply 5 amps as above to operate the squaring amplifier. Switch closure produces approximately 20 MS. delayed output at TP5.

Fast Reset may be checked by monitoring the signal at timer card pin 3 using a card adapter. The signal at pin 3 should drop to zero in less than .5 MS when the test switch is opened.

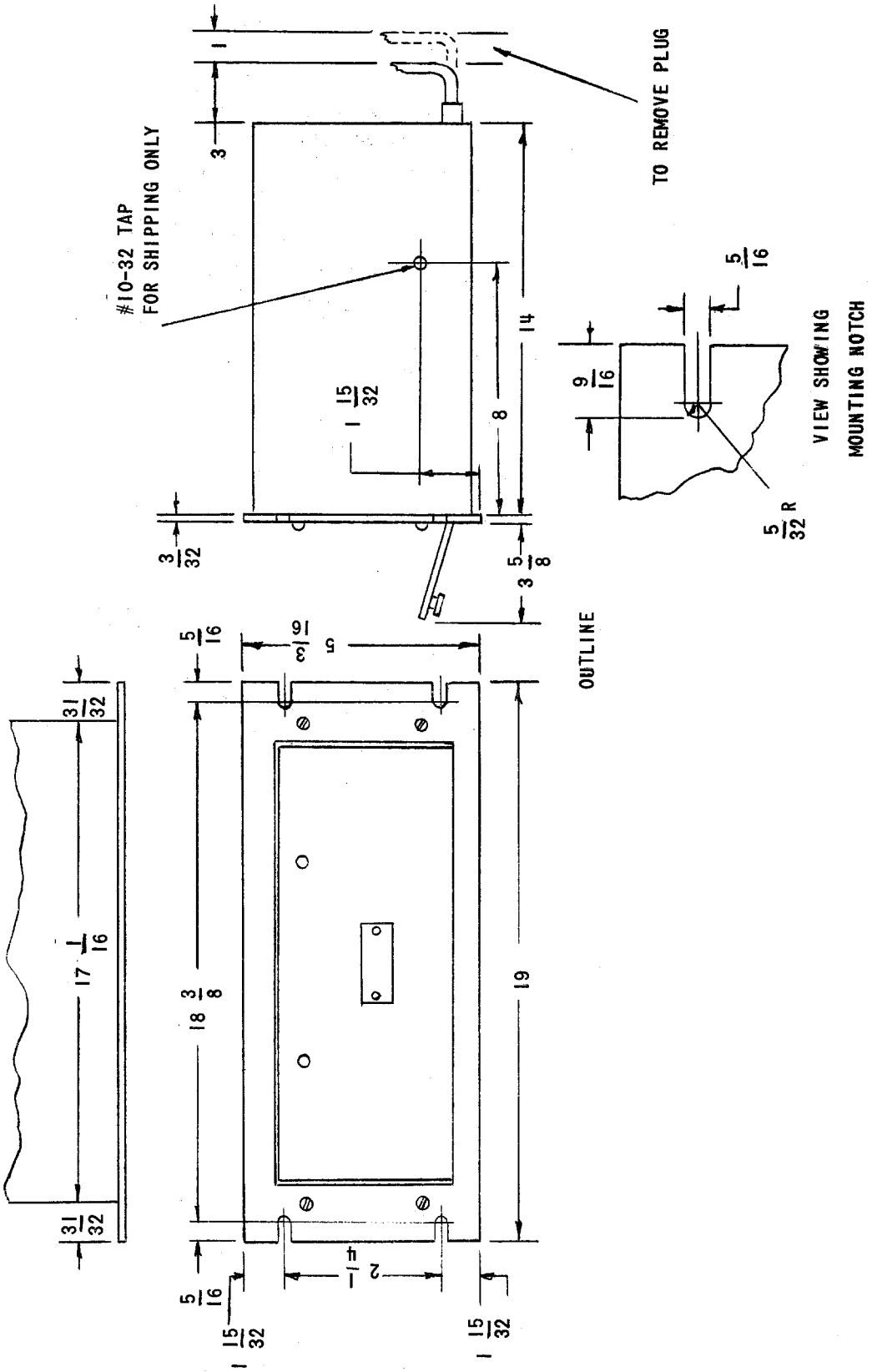


FIG. 1 (0165A7754-1) Outline And Mounting Dimensions For The SLD42H4 Network Unit

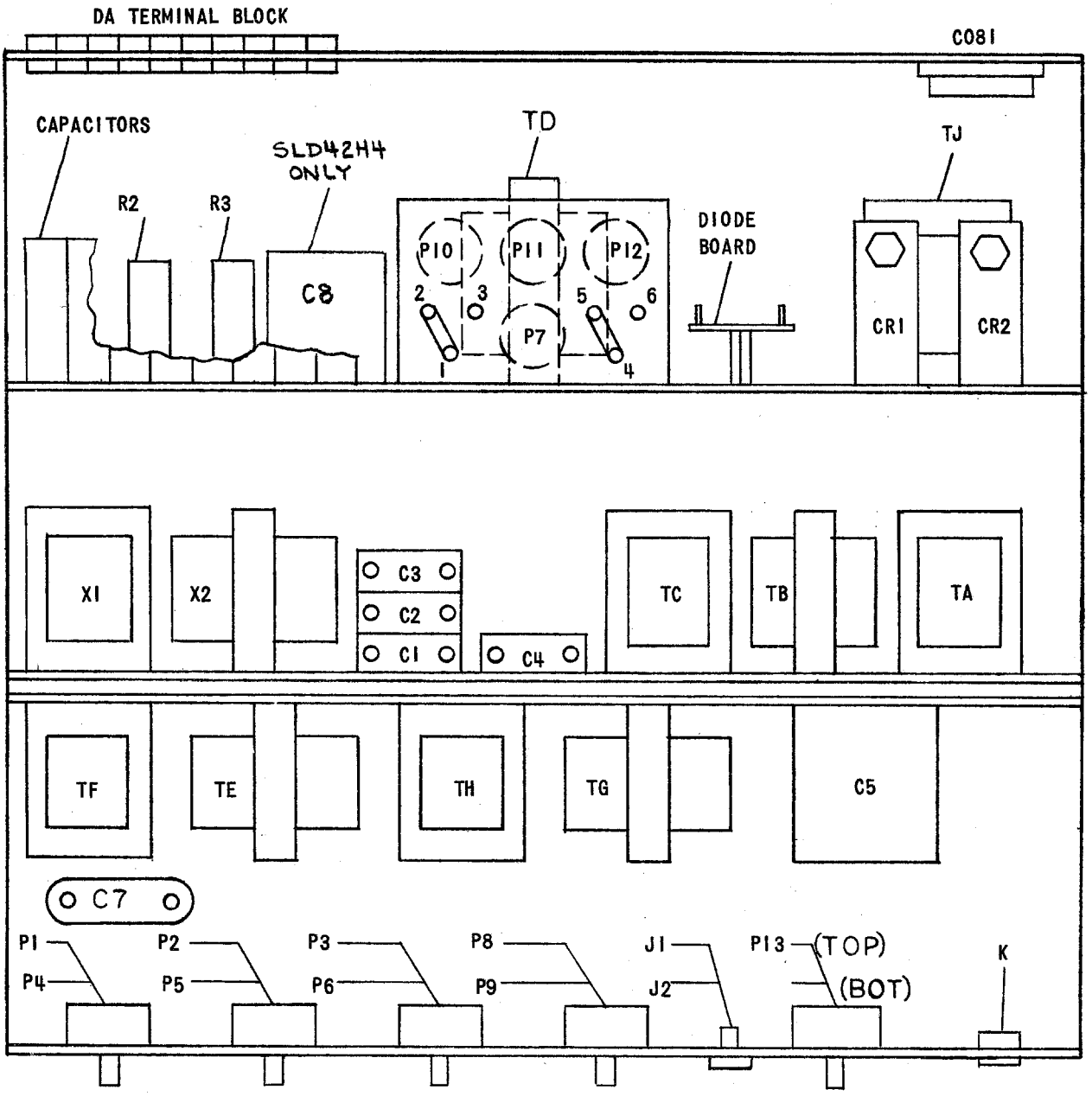


FIG. 2 (0246A2135-1) Component Location Diagram For The SLD42H4 Network Unit

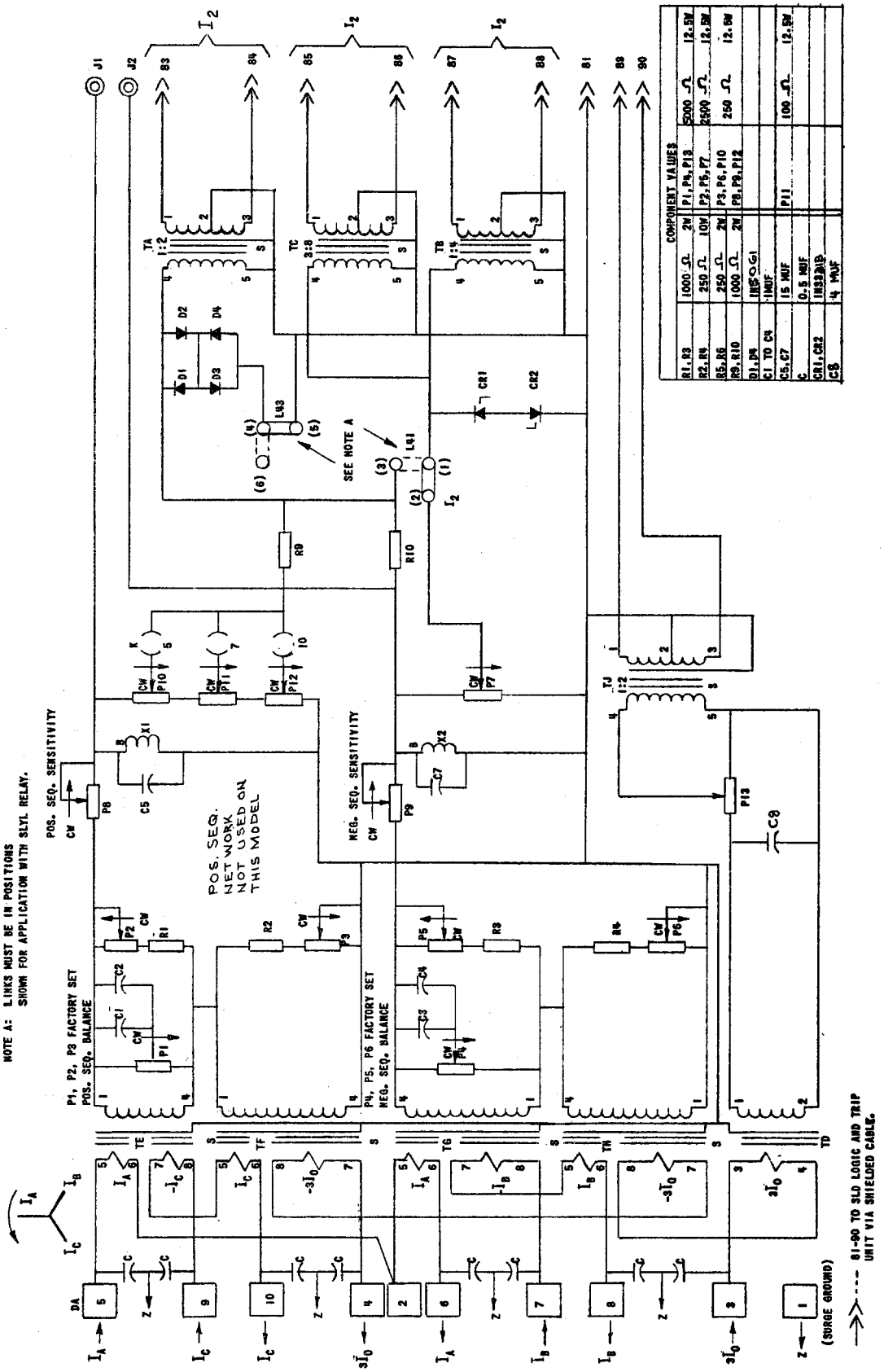


FIG. 3 (0165B2576-0) Internal Connections For The SLD42H4 Network Unit

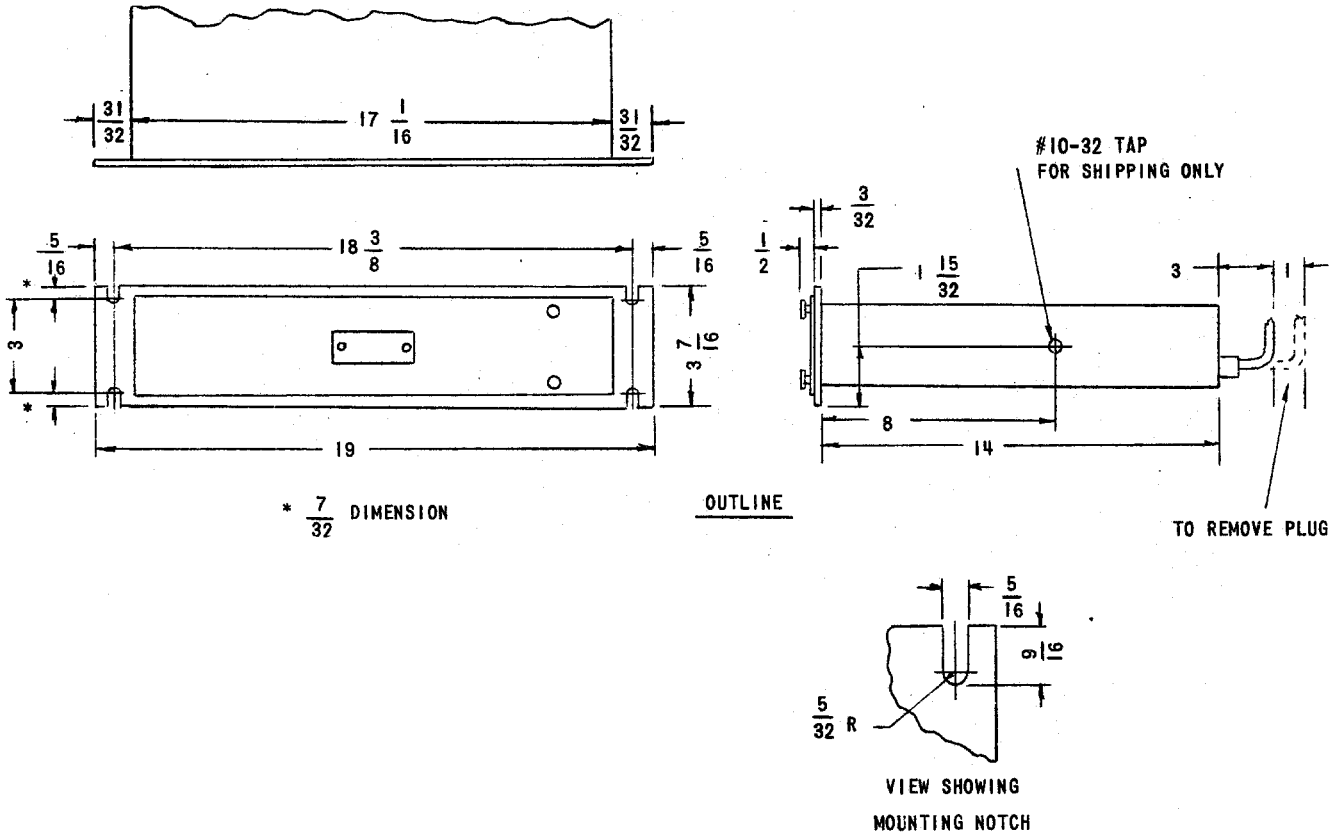
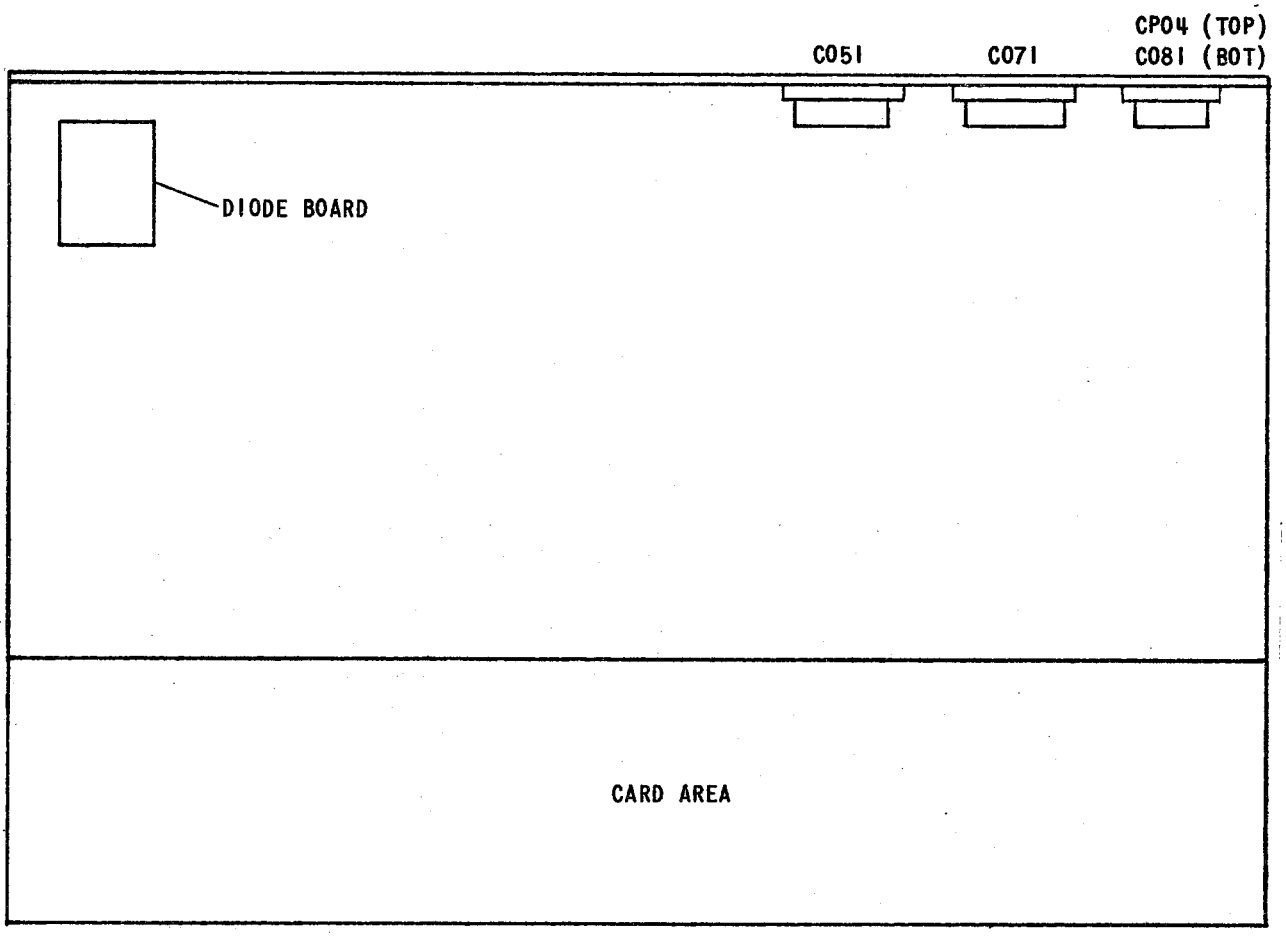
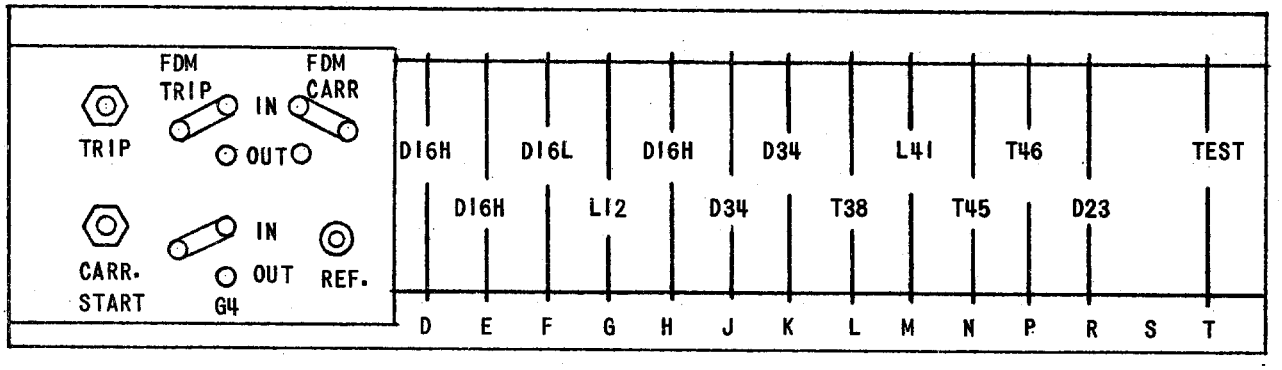


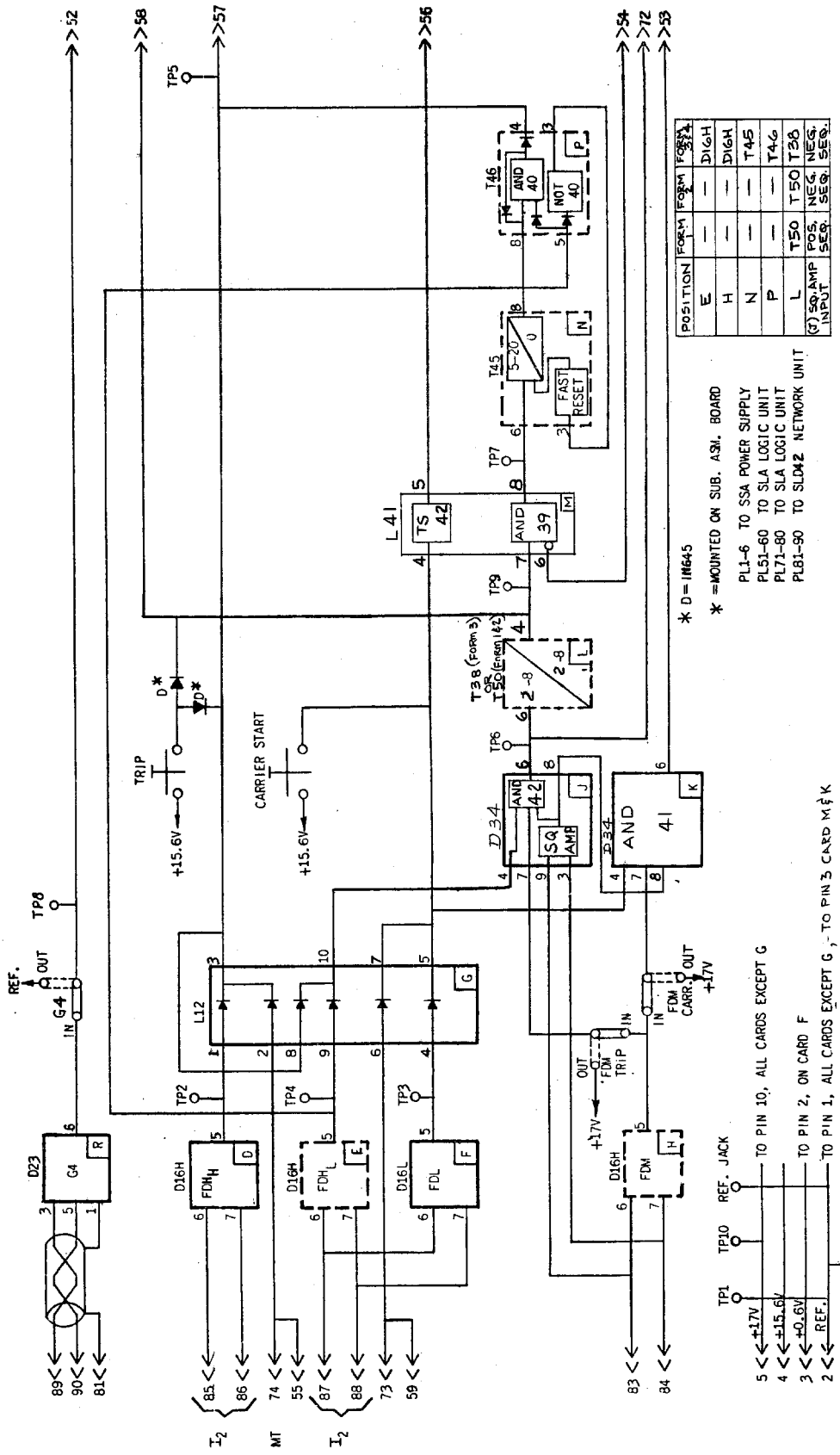
FIG. 4 (0165A7660-0) Outline And Mounting Dimensions For The SLD42H4 Logic Unit





NOTE: REFER TO INTERNAL CONNECTIONS DIAGRAM FOR EXACT CARD USAGE.

FIG. 5 (0246A2138-0) Component Locations Diagram For The SLD42H4 Logic Unit


>52
>58
>57
>56
>54
>72
>53
TP5
TP8
REF.
OUT
G4
IN
D23
G4
R
L12
TP2
TP4
TP3
D16H
FDM H
D
D16H
FDM L
E
D16L
FDL
F
G
TRIP
+15.6V
CARRIER START
+15.6V
D*
D*
TP6
TP7
TP9
L41
TS
42
AND
39
M
T45
5-20
U
FAST
RESET
N
T46
AND
40
NOT
40
P
T38 (FORM 3)
OR
T50 (FORM 1 & 2)
2-8
L
D34
AND
42
J
SQ
AMP
D34
AND
41
K
OUT
FDM
TRIP
IN
+17V
OUT
FDM
CARR.
+17V
IN
D16H
FDM
H
TP1
TP10
REF. JACK
+17V
+15.6V
+0.6V
REF.
TO PIN 10, ALL CARDS EXCEPT G
TO PIN 2, ON CARD F
TO PIN 1, ALL CARDS EXCEPT G, TO PIN 3 CARD M & K
89
90
81
85
86
74
55
87
88
73
59
83
84
5
4
3
2
1,51,71,81
I2
MT
I2
* D = IN645
* =MOUNTED ON SUB. ASM. BOARD
PL1-6 TO SSA POWER SUPPLY
PL51-60 TO SLA LOGIC UNIT
PL71-80 TO SLA LOGIC UNIT
PL81-90 TO SL042 NETWORK UNIT
POSITION
FORM 1
FORM 2
FORM 3 & 4
E — — D16H
H — — D16H
N — — T45
P — — T46
L T50 T50 T38
(2) SQ. AMP INPUT
POS. SEQ.
NEG. SEQ.
NEG. SEQ.

GE Power Management

215 Anderson Avenue
Markham, Ontario
Canada L6E 1B3
Tel: (905) 294-6222
Fax: (905) 201-2098
www.GEindustrial.com/pm