INSTRUCTIONS

GEK-65554

STATIC GROUND PHASE
COMPARISON RELAY
TYPE SLDG54A

GENERAL ELECTRIC

CONTENTS

STATIC GROUND PHASE COMPARISON RELAY

TYPE SLDG54A

DESCRIPTION

The SLDG54A relay is a zero-sequence dual-phase comparison relay specifically designed for use on long EHV transmission lines to provide protection against single phase-to-ground faults. A separate relaying scheme must be employed to provide protection for multi-phase faults.

The SLDG54A relay is packaged in a four-rack unit case. The outline and mounting dimensions of the relay are shown in Fig. 1, the component locations are shown in Fig. 2 and the internal connections are shown in Fig. 3. The printed circuit card internals are given in GEK-34158.

The functions which may be included in an SLDG54A are as follows:

FDH+ - Positive half cycle high set (or low set) fault detector that initiates trip attempt.

FDM+ - Positive half cycle low set fault detector that initiates trip attempt.

SQ AMP+ - Positive half cycle squaring amplifier.

FDH- - Negative half cycle high set (or low set) fault detector that initiates trip attempt.

FDH- - Negative half cycle low set fault detector that initiates trip attempt.

SQ AMP- - Negative half cycle squaring amplifier.

G4 - Non-directional overcurrent direct trip function.

Im - Sensitive current detector.

A complete terminal of protection requires, in addition to the SLDG54A, a suitable phase relay, SLA auxiliary logic unit, SLAT output and tripping unit, SSA power supply and test panel. A typical SLA logic unit is shown in Fig. 5.

For a complete description of the overall scheme in which this relay is used, refer to the overall logic diagram and associated logic description that covers the specific components involved in the scheme. A typical overall logic diagram in shown in Fig. 6.

RANGES

The following pickup ranges are available.

FDH (+ and -)	2-16 amps RMS (residual) or 0.5-4 amps RMS.
FDM (+ and -)	0.5-4 amps RMS (residual)
G4	4-32 amps RMS (residual)
Im	0.4 amps RMS (residual) for continuous output (non-adjustable)

RATINGS

The Type SLDG54A relay is designed for use in an environment where the air temperature outside the relay case is between minus 20°C and plus 65°C.

The Type SLDG54A relay requires a plus or minus 15 volt DC power source which can be obtained from type SSA50 and up power supplies.

The current circuits of the SLDG54A relay are rated at five amperes, 60 hertz for continuous duty and have a one-second rating of 250 amperes.

BURDENS

The AC current burden of the SLDG54A relay with the three current circuits in series (GA2-GA3, GA4-GA5 and GA6-GA7) and with the FDM, FDH and G4 tap blocks in their minimum tap positions is 0.1 + j0.0445 ohms at five amps, 60 hertz. This is equivalent to 2.5 watts and 1.11 vars lagging power factor.

The DC burden that the SLDG54A relay presents to the SSA power supply is:

150 ma from the plus 15 VDC supply
75 ma from the minus 15 VDC supply

APPLICATION

The SLDG54A dual-phase relay was designed to provide protection against single-phase-to-ground faults on long EHV lines with or without shunt reactor compensation. Since the relay is excited by $3I_0$ it will also respond to some double-phase-to-ground faults.

The SLDG54A is intended for use over a frequency shift channel in a tripping mode, and for this reason it does not include any fault detectors for the initiation of a blocking signal. For a complete discussion of the overall phase comparison scheme, refer to the overall logic diagram and the logic description that is supplied with the complete equipment.

SETTINGS

Im FUNCTION

The Im function has a fixed current pickup. It is not field adjustable.

G4 FUNCTION

Set G4 with a pickup of at least 1.25 times the maximum symmetrical through fault current in either direction. A field check should be made to insure that this setting is high enough to prevent operation on line pickup.

FDH AND FDM FUNCTIONS

The FDH and FDM settings will, to some degree, depend on the mode of operation.

A. FDH or FDM Mode

Set FDM so that the minimum internal fault current is at least 1.5 and preferably 2.0 times the setting. Set FDH so that it does not operate on line pickup.

B. FDH and FDM Mode

Set both FDM and FDH so that the minimum internal fault current is at least 1.5 and preferably 2.0 times the setting.

NOTE: Set the positive (+) half and the negative (-) half the same.

RECEIVING, HANDLING AND STORAGE

This relay will normally be supplied as part of a static relay equipment, mounted in a rack or cabinet with other static relays and test equipment. Immediately upon receipt of a static relay equipment, it should be unpacked and examined for any damage sustained in transit. If injury or damage resulting from rough handling is evident, file a damage claim at once with the transportation company and promptly notify the nearest General Electric Sales Office.

Reasonable care should be exercised in unpacking the equipment. If the equipment is not to be installed immediately, it should be stored indoors in a location that is free from moisture, dust, metallic chips, and severe atmospheric contaminants.

Just prior to final installation, the shipping support bolt should be removed from each side of all relay units, to facilitate possible future unit removal for maintenance. These shipping support bolts are approximately eight inches back from the relay unit front panel. Static relay equipment, when supplied in swing rack cabinets, should be securely anchored to the floor or to the shipping pallet to prevent the equipment from tipping over when the swing rack is opened.

INSTALLATION TESTS

NECESSARY ADJUSTMENTS

The following checks and adjustments should be made by the user, in accordance with the procedures given below under **DETAILED TESTING INSTRUCTIONS**, before the SLDG54A relay is put in service. Some of the following items are checks of factory calibrations and settings or installation connections and hence do not normally require readjustment in the field. Other items cover settings or adjustments which depend on installation conditions and hence must be made on the installed equipment. It is suggested that the tests be performed in the order listed below.

A. Trip integrator time check

B. Level detector adjustments

C. Polarity checks

D. Received signal adjustments

E. Phase delay adjustments

Before beginning the installation tests, check for installation of the interconnecting cable from the SLDG54A to the power supply and from the SLDG54A to the SLA logic unit.

GENERAL TESTING INSTRUCTIONS

The AC input circuit to the SLDG54A relay is made through the TGA test and connection receptacle on the test panel. This receptacle is connected via a ten-conductor cable to the GA terminal block on the back of the unit. Test current can be supplied to the network unit through the standard type XLA test plug. Test connections for the Type XLA test plug are shown in Fig. 4.

The output signals from the SLDG54A relay can be measured at the unit test points. These test points are pin jacks located on the two printed circuit cards at the extreme right-hand card positions. Numbered from top to bottom, the test card in the "AT" card position contains TP1 to TP10 and the card in the "T" card position contains TP11 to TP20. Refer to Fig. 2 for the location of these test cards and to Fig. 3 for the identification of the various test points.

Output signals from the SLDG54 relay are measured with respect to the reference bus, TP1. Outputs are signals of approximately plus ten to plus 15 volts for the ON condition, and zero to plus one volt for the OFF condition. These outputs can be monitored with an oscilloscope, a portable high impedance voltmeter, or the test panel voltmeter. When the test panel voltmeter is available, the voltmeter negative terminal will normally be connected to the reference bus, and placing the relay test lead in the proper test point pin jack will connect the meter for testing.

Where time delay cards are to be adjusted or checked, an oscilloscope which can display two traces simultaneously, and which has a calibrated horizontal sweep, should be used.

CAUTION

IT IS A DESIGN CHARACTERISTIC OF MOST ELECTRONIC INSTRUMENTS THAT ONE OF THE SIGNAL INPUT TERMINALS IS CONNECTED TO THE INSTRUMENT CHASSIS. SINCE THE SLDG54A REFERENCE VOLTAGE, WHICH NORMALLY WILL BE CONNECTED TO THE GROUND INPUT OF THE INSTRUMENT, IS NEAR THE POSITIVE (+) OR NEGATIVE (-) STATION VOLTAGE LEVEL, THE INSTRUMENT CHASSIS MUST BE INSULATED FROM STATION GROUND. IF THE INSTRUMENT POWER CORD CONTAINS A THIRD LEAD, THAT LEAD MUST NOT BE CONNECTED TO STATION GROUND. HOWEVER, IF THE INPUT TO THE OSCILLOSCOPE IS A DIFFERENTIAL AMPLIFIER AND NEITHER INCOMING VOLTAGE SIGNAL IS TIED DIRECTLY TO THE INSTRUMENT GROUND, IT IS NOT NECESSARY TO OBSERVE THE ABOVE PRECAUTIONS.

DETAILED TESTING INSTRUCTIONS

TRIP INTEGRATOR TIME CHECK

The trip integrator timer cards, which are located in the SLA logic unit, should be set by means of the standard test circuit for setting timers (see the printed circuit card instruction book GEK-34158). Set the positive and negative half-cycle trip integrators for 3.5 millisecond pickup time delay and 18 millisecond drop-out time delay. Setting these timers as accurately as possible is the first step in assuring balanced operation on both half cycles. If a dual trace oscilloscope with an external trigger input is available, it might be desirable to energize both trip integrators with the same test signal and to display both outputs on the oscilloscope at the same time. This procedure would give greater assurance that timers are set for the same pickup and drop-out time delay.

FDM AND FDH LEVEL DETECTOR ADJUSTMENTS

To balance and to set the pair of FDM fault detectors (both positive and negative half cycle) the first step is to insure that the trip integrators are measuring the output of the FDM detectors only. Remove the FDH fault detectors in card positions "R" and "S" and the 1-8/1-8 phase delay timers in the SLA logic unit. Complete the logic circuit by using a jumper around phase delay positions (TP5 in the SLDG54 to TP5 in the SLA55C and TP6 in the SLDG54 to TP15 in the SLA55C) and by supplying a continuous received signal (remove the M and N card in the SLA55C).

Each FDM card has a potentiometer on it for adjusting the pickup level of the card itself. Also located on the front of the relay is a tap selector and a potentiometer for adjusting the pickup level of the two cards together. To balance the two FDM cards, set the tap selector and adjust the potentiometer on the front of the unit for a minimum pickup level. Apply an AC test current equal to the minimum pickup level of the unit (0.5 amp RMS for FDM) to the relay, and adjust the individual pickup adjustment of each card until it just produces an output from the trip integrator in the SLA logic unit for that particular half cycle. Since there is some interaction between the two individual adjustments, a continual check will have to be made back and forth between the two cards until a balance is obtained. Once the two cards have been balanced, the individual adjustments will not have to be set again. The desired pickup level of the function can be set by using the adjustments on the front of the network unit. The procedure for this is outlined in the basic book.

By using a similar procedure the FDH level detectors can also be balanced and set for the desired pickup level. In the application where the signal to be compared is the result of the output from FDM and FDH, the FDH cards can be set as sensitive as the FDM cards (0.5-4 amps RMS) by adjusting the individual pickup adjustments. There may be a slight phase shift between the FDM and FDH outputs; however, a balance between the fault detectors to produce the necessary signal for tripping at minimum pickup can be obtained.

The setting of the trip integrators and the balancing of the FDM and the FDH fault detectors, at their specified minimum pickup (0.5 amp for FDM, 2.0 amp for FDH) has been done at the factory. However, they should be checked during installation of the equipment to insure that none of the settings have been disturbed.

G4 LEVEL DETECTOR ADJUSTMENT

The G4 overcurrent level detector is a standard level detector, in that it produces a continuous output at TP8 when it is picked up. The range of adjustment of pickup level for G4 is from four to 32 amps. There is a tap selector and a potentiometer for making this adjustment on the front of the relay. To set the pickup level, apply a single phase test current to TGA6 and TGA7 and adjust the G4 function for the desired pickup level.

POLARITY CHECK

A source of test current must be set up. Two possible methods of obtaining the test current are outlined below.

Load Current Method

For this method, Phase-One current is jumpered to ground at each end of the line, thus Phase-One current bypasses the SLDG54A causing the sum of Phase-Two and Phase-Three load currents to flow through the SLDG54A windings.

If this method is to produce an accurate result, it is necessary that the ratio of line charging current to through-load current be low enough to not cause the phase displacement between the currents at the two ends of the line to exceed ten degrees. If this condition cannot be met, it will be necessary to use the test source method.

Test Source Method

If the line is not loaded, is carrying insufficient load, or if the ratio of charging current to load current is too high, an AC test source can be used at each station provided the sources are in phase. Use the test connections shown in Fig. 4 at each end of the line.

By using one of the procedures outlined above, set up a source of test current that offers the minimum phase shift between each end of the line. The current should be limited to a value between one and five amps RMS. It need not be exactly the same magnitude at each end; however, the current should be limited by the same method at each end in order to avoid any extraneous phase shift.

Remove both FDM and FDH fault detector cards (card positions "N," "P," "R" and "S"). In this condition this signals to be compared will be determined entirely by the squaring amplifier output. If the SLDG54A is for use in a three terminal line application, make sure the timers in the "R" and "P" card positions in the SLA55 are set at a minimum.

Apply the test current to the relays at each end of the line, and using a dual trace oscilloscope, compare the local signal at TP12 in the SLDG54A with the received signal at TP3 in the SLA and compare the local signal at TP13 with the received signal at TP18 in the SLA. In both cases the local signal will be approximately a 60 hertz square wave; that is, "ON" time and "OFF" time approximately equal on a 60 hertz basis. In both cases the local signal should lead the received signal by five milliseconds or less. In the two terminal line applications, the received signals will also be approximately equal to 60 hertz square waves. In three terminal line application, the "ON" time of the received signals may be a few milliseconds less than the "OFF" time because the two received signals will not be exactly in phase. These conditions holding, the polarities of the relays at each end of the line are properly aligned.

RECEIVED SIGNAL ADJUSTMENT

This adjustment is necessary only for the SLDG54A when used in a three terminal line application.

In the case of a three terminal line there will be two received signals. Connect the received signal from the closer remote terminal or the one with the lesser amount of phase shift to the relay input marked Receiver #2 (cable connection C161 in the rear of the SLDG54A logic unit). Connect the received signal from the further terminal or the one with the greater amount of phase shift to the relay input marked Receiver #1 (cable connection C151 in the rear of the SLDG54A logic unit).

Apply the test currents and test conditions used for the primary checks and adjust the delay timers (in position "P" and "R" in the SLA) on the leading signal until both received signals are exactly in phase. This can be accomplished by placing the AND52 card (card position "S" in the SLA55) in the test card adapter and by comparing the input signals at pins two and six and the output at pin nine. Refer to the internal diagram, Fig. 3 and the printed circuit card instruction book GEK-34158 for the use of the test card adapter. Use the same procedure for AND42. The outputs of AND42 and AND52 should be half cycle in duration and exactly in phase with their respective inputs. These signals can then be compared with the local signals to set the phase delay timers.

PHASE DELAY TIMER ADJUSTMENTS

To set the phase delay timers, apply the test current and set up the test conditions established for the polarity checks.

To set the phase delay timers, compare the received signals at TP3 or TP18 in the SLA55 with the appropriate local signal at TP5 or TP15 to determine how much the phase delay is needed. Then using the standard circuit for setting timers (Fig. 7), set each of the phase delay timers in the logic chain (in the SLA logic unit) for approximately half the total phase delay needed. Set both the pickup delay time and the drop-out delay time at the same value to prevent changing the width of the block. Then compare

the received signal with the appropriate phase delayed local signal at TP5 or TP15 in the SLA55. Touch up the phase delay, if necessary, so that for each half cycle of comparison, the local and received signals are exactly in phase, and are half cycle in duration. When this is done, the proper phase delay setting has been made.

PERIODIC CHECKS AND ROUTINE MAINTENANCE

PERIODIC TESTS

During a periodic check of the equipment, the level detector operating points (FDH, FDM, G4) should be checked against the factory set points or the operating points set during the installation tests, using the test connections of Fig. 4.

Any check of the transmitter drive symmetry of the phase delay card requires operators at both terminals of the line, and should not require checking during normal periodic test programs. If it is desired to check the adjustment of these functions, follow the procedure described in the section on **INSTALLATION TESTS.**

TROUBLESHOOTING

In any troubleshooting of equipment, it should first be established which unit is functioning incorrectly. The overall logic diagram contains the combined logic diagrams of the SLDG relay and all other associated relays, and various test points in each unit. By signal tracing, using the applicable overall logic diagram and the various test points, it should be possible to quickly isolate the trouble.

A test adapter card (0108B9643), is supplied with each static relay equipment to supplement the prewired test points on the test cards. This adapter can be plugged into any card position, and then the logic card for that address can in turn be plugged into the adapter. The unit test card can then be plugged into the second socket in the adapter, giving access to all ten connection points by instrument jacks while the logic card is operating in the circuit. The connections to each pin on the adapter logic card socket are individually removable to allow circuit wiring changes to the logic card during troubleshooting.

An oscilloscope is a valuable aid to detailed troubleshooting, since it can be used to determine phase shift, operate and reset times, as well as input and output levels. A portable dual-trace oscilloscope with a calibrated sweep and trigger facility is recommended.

SPARE PARTS

To minimize possible outage time, it is recommended that a complete maintenance program should include the stocking of at least one spare card of each type. It is possible to replace damaged or defective components on the printed circuit cards, but great care should be taken in soldering so as not to damage or bridge-over the printed circuit buses, or overheat the semiconductor components. The repaired area should be recovered with a suitable high-dielectric plastic coating to prevent possible breakdowns across the printed buses due to moisture and dust.

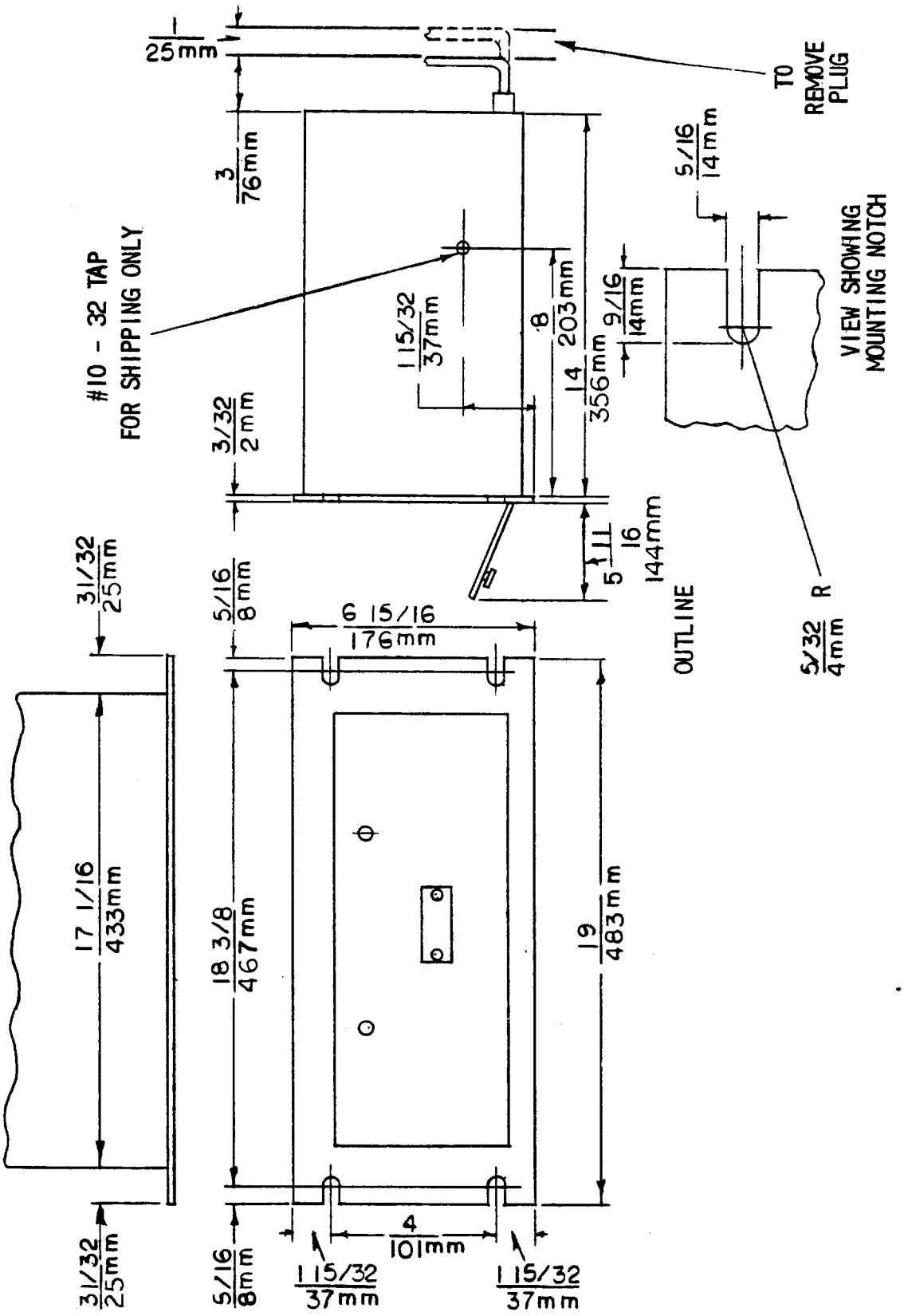
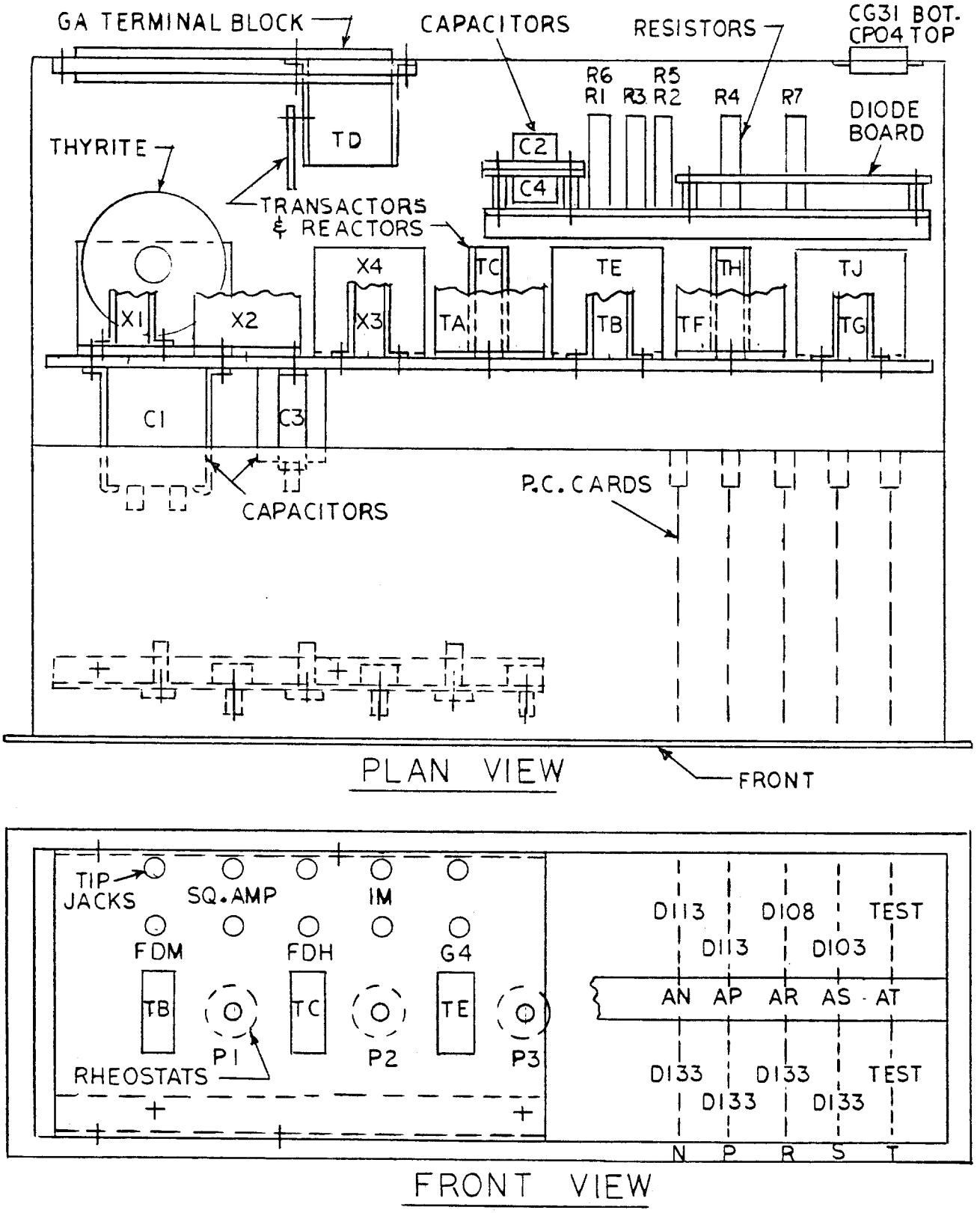
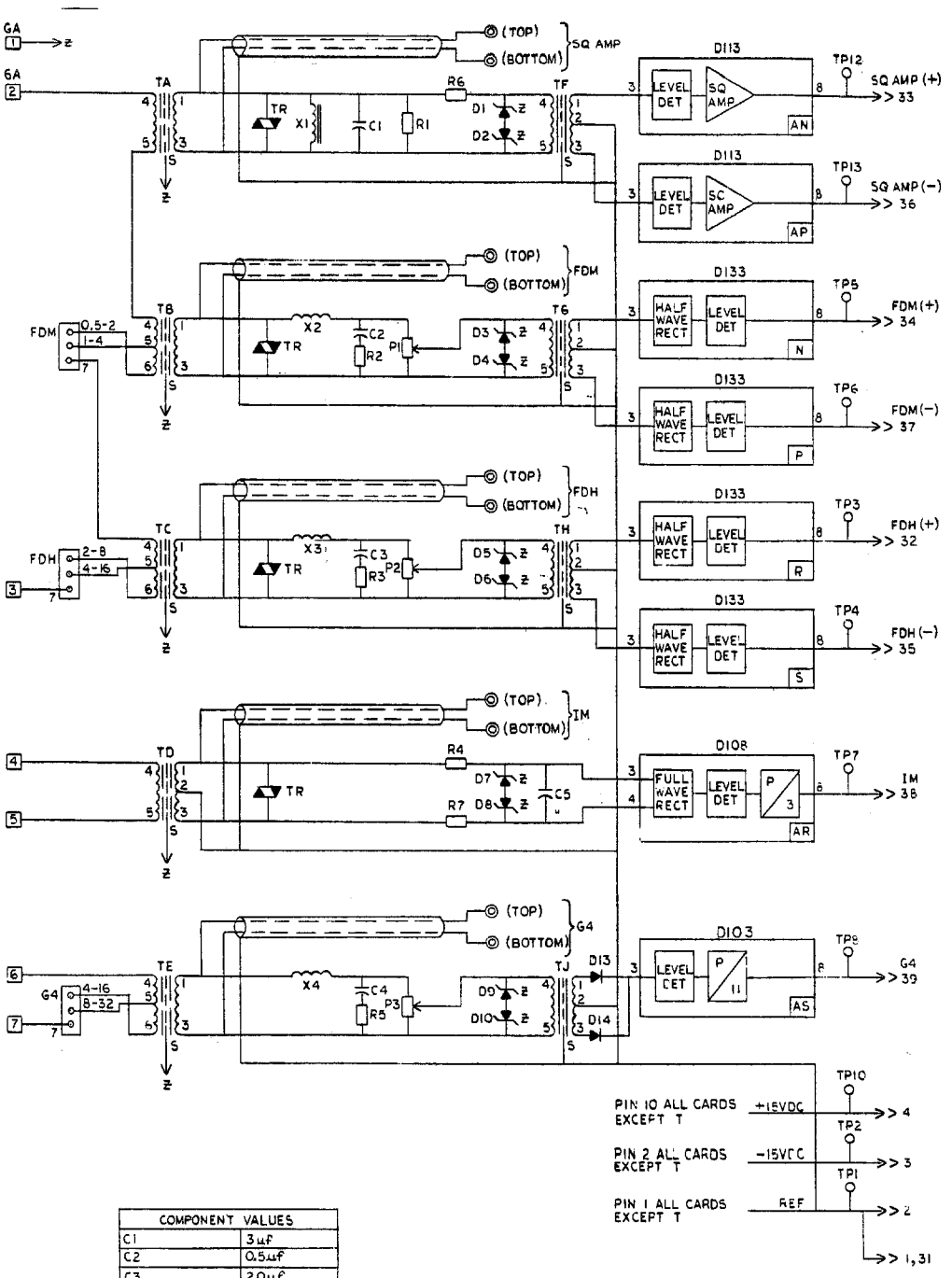


Fig. 1 (0227A2037-1) Outline and Mounting Dimensions for the SLDG54A Relay

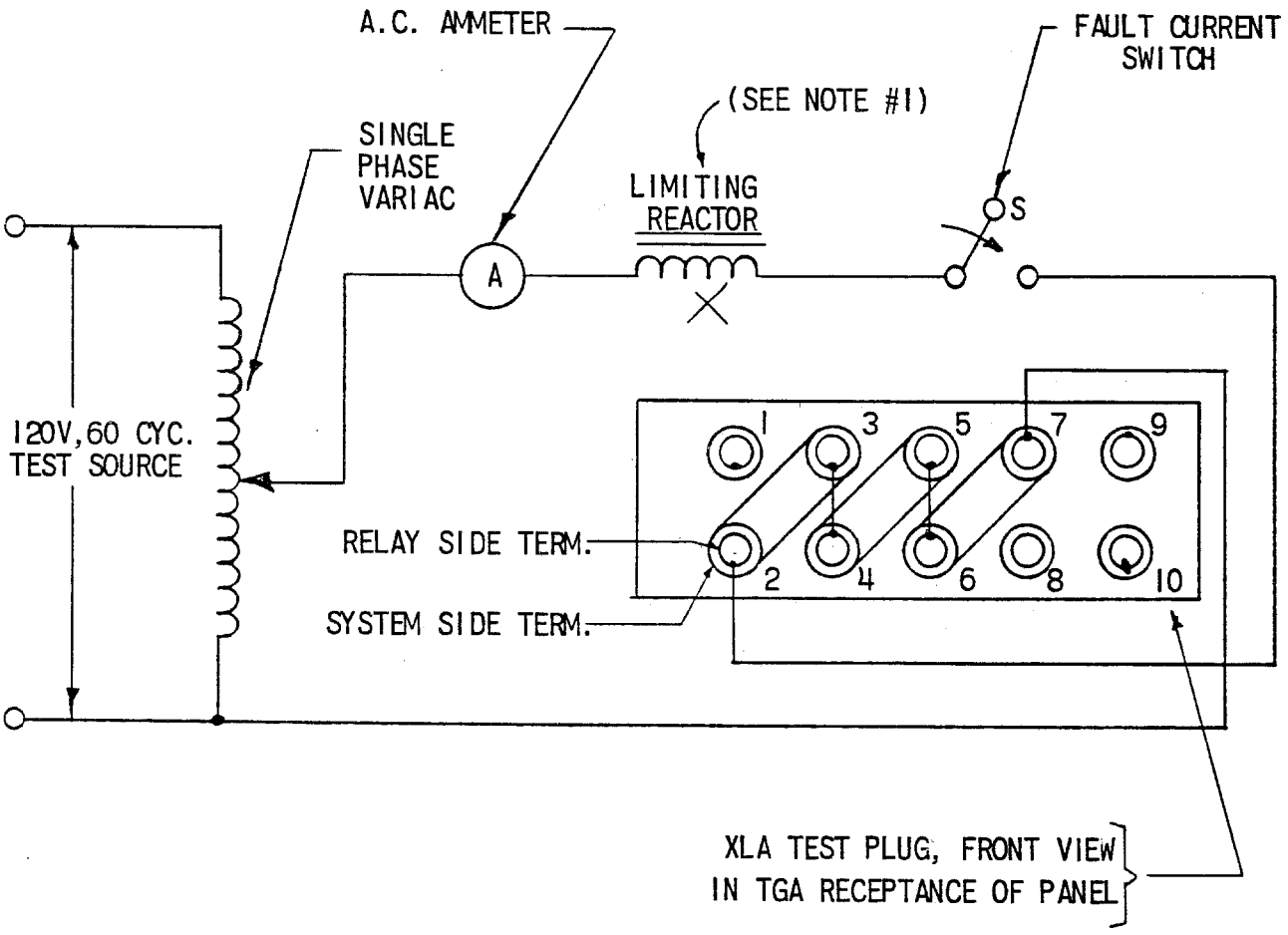


Fg. 2 (0275A4510-0) Component Location Diagram for the SLDG54A Relay



COMPONENT VALUES	
C1	3 μf
C2	0.5 μf
C3	2.0 μf
P1, P2	5K, 12.5W
P3	3.5K, 12.5W
R1, R6	5K, 12.5W
R2, R5	300 Ω, 10W
R3	3K, 10W
R4, R7	10K, 10W
C4	1.0 μf
D3, D4, D5 TO D10	IN968
D1, D2	IN751
D13, D14	IN645
C5	0.1 μfd

Fig. 3 (0172C5149-1) Internal Connections for the SLDG54A Relay



NOTE #1: FOR ALL A.C. TESTING, USE AS MUCH CURRENT LIMITING REACTANCE AS POSSIBLE.

TEST PLUG CONNECTIONS FOR CHECKING THE FDM, FDH, G4 AND I_M LEVEL DETECTORS.

Fig. 4 (0227A2348-0) Test Plug Connections for Testing Fault Detectors in the SLDG54A Relay

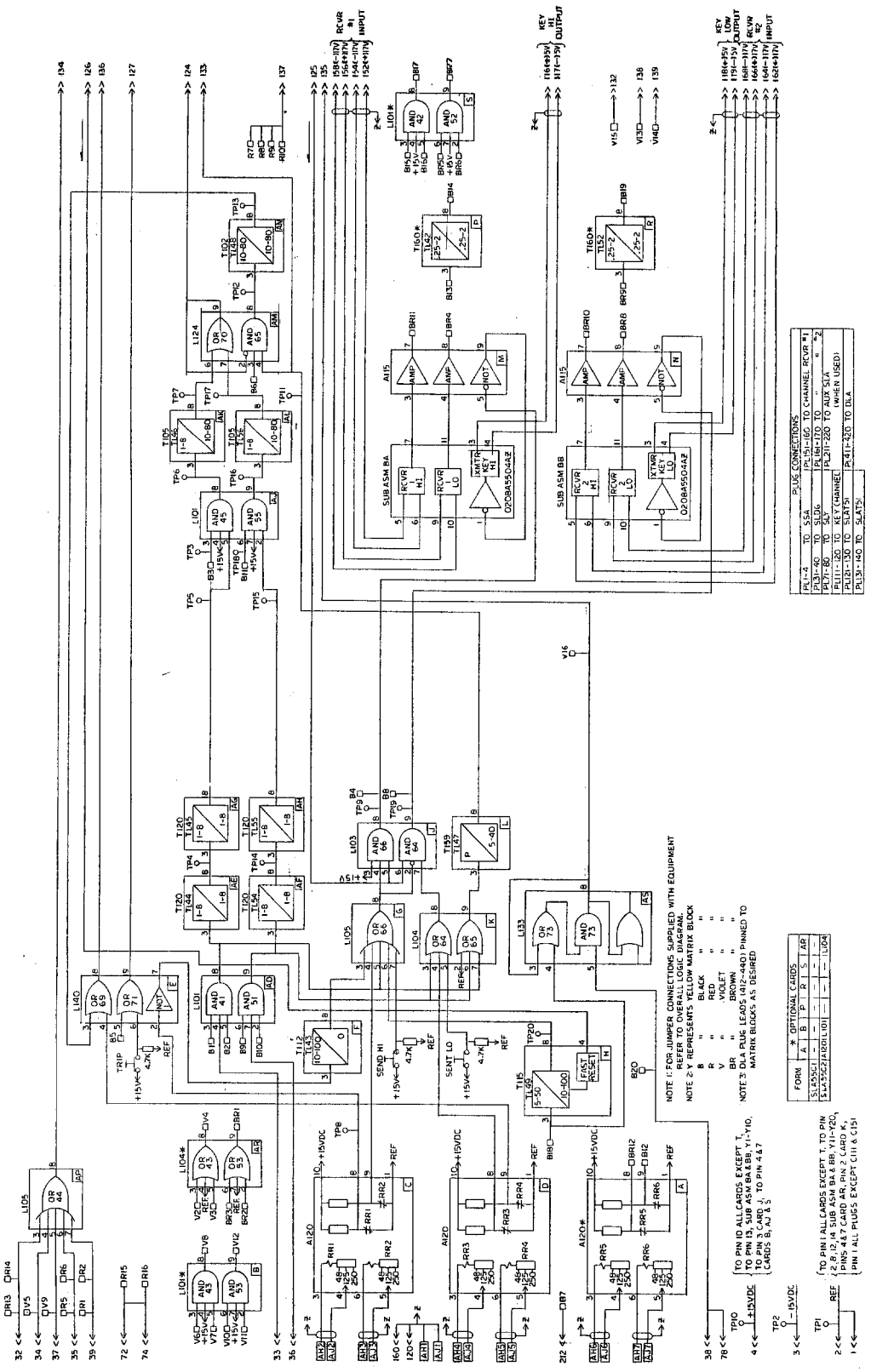


Fig. 5 (0138D3969-2) Typical SLA Logic Unit for Use with the SLDG54A Relay

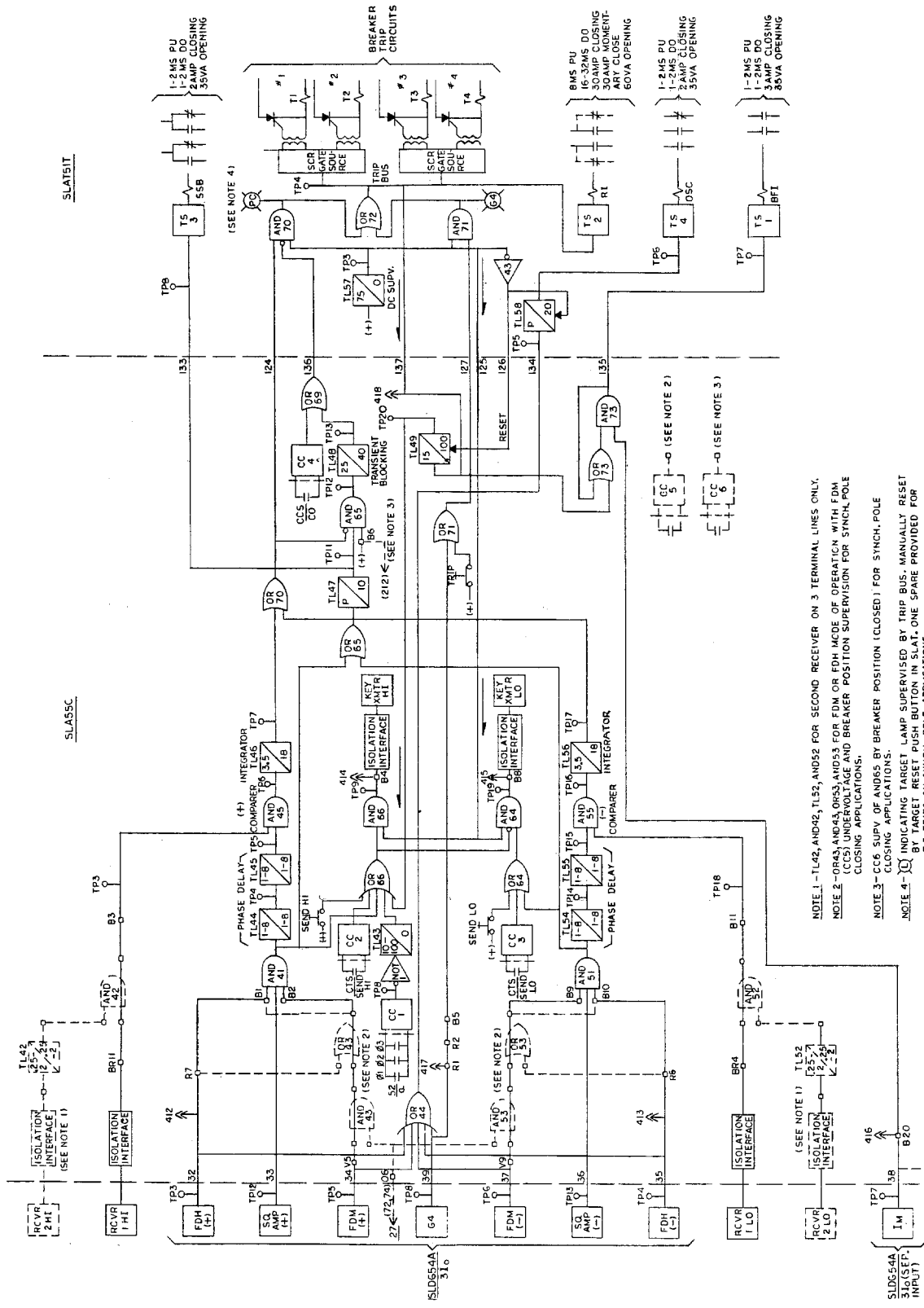
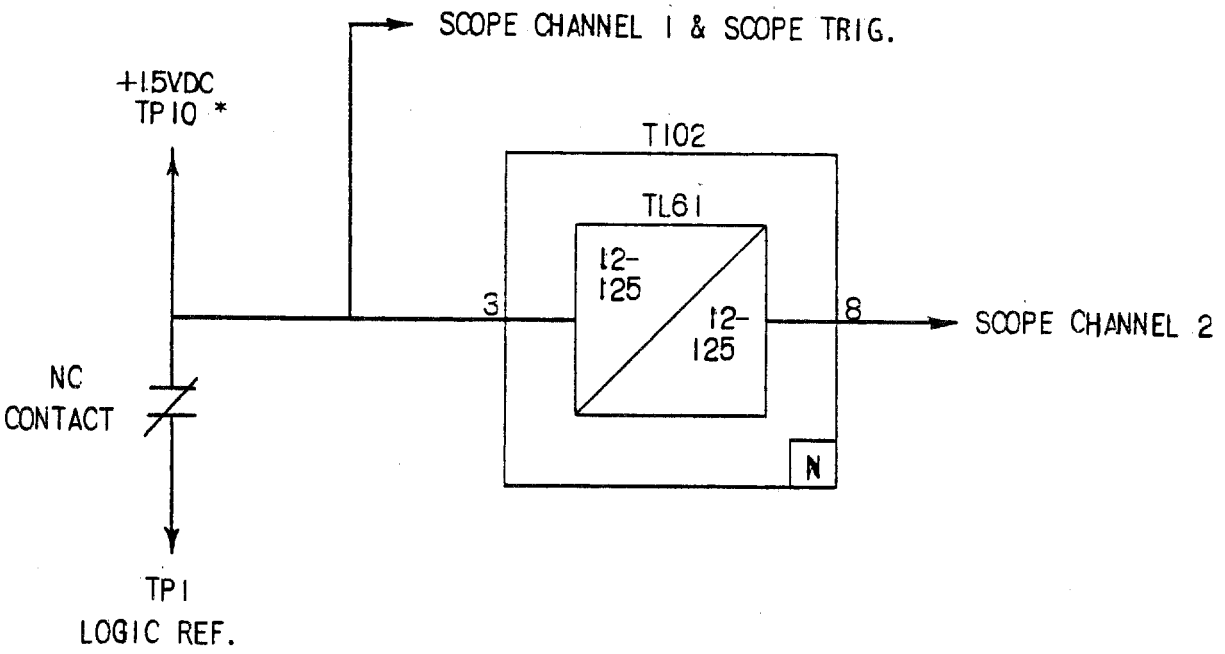


Fig. 6 (0172C5146-1) Typical Overall Logic Using the SLDG54A Relay



* THE 15VDC SIGNAL AT PIN 10 HAS A CURRENT LIMITING RESISTOR MOUNTED ON THE TEST CARD.

Fig. 7 (0246A7987-0) Logic Timer Test Circuit

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