INSTRUCTIONS

GEK-45369C
Supersedes GEK-45369B

STATIC COMBINED POSITIVE SEQUENCE DISTANCE AND NEGATIVE SEQUENCE PHASE COMPARISON RELAY

SLDY51A

GENERAL ELECTRIC

CONTENTS

(Continued ...)

CONTENTS

*NOTE: This book has been revised to include the 50 hertz, one ampere model of the SLDY51A relay.

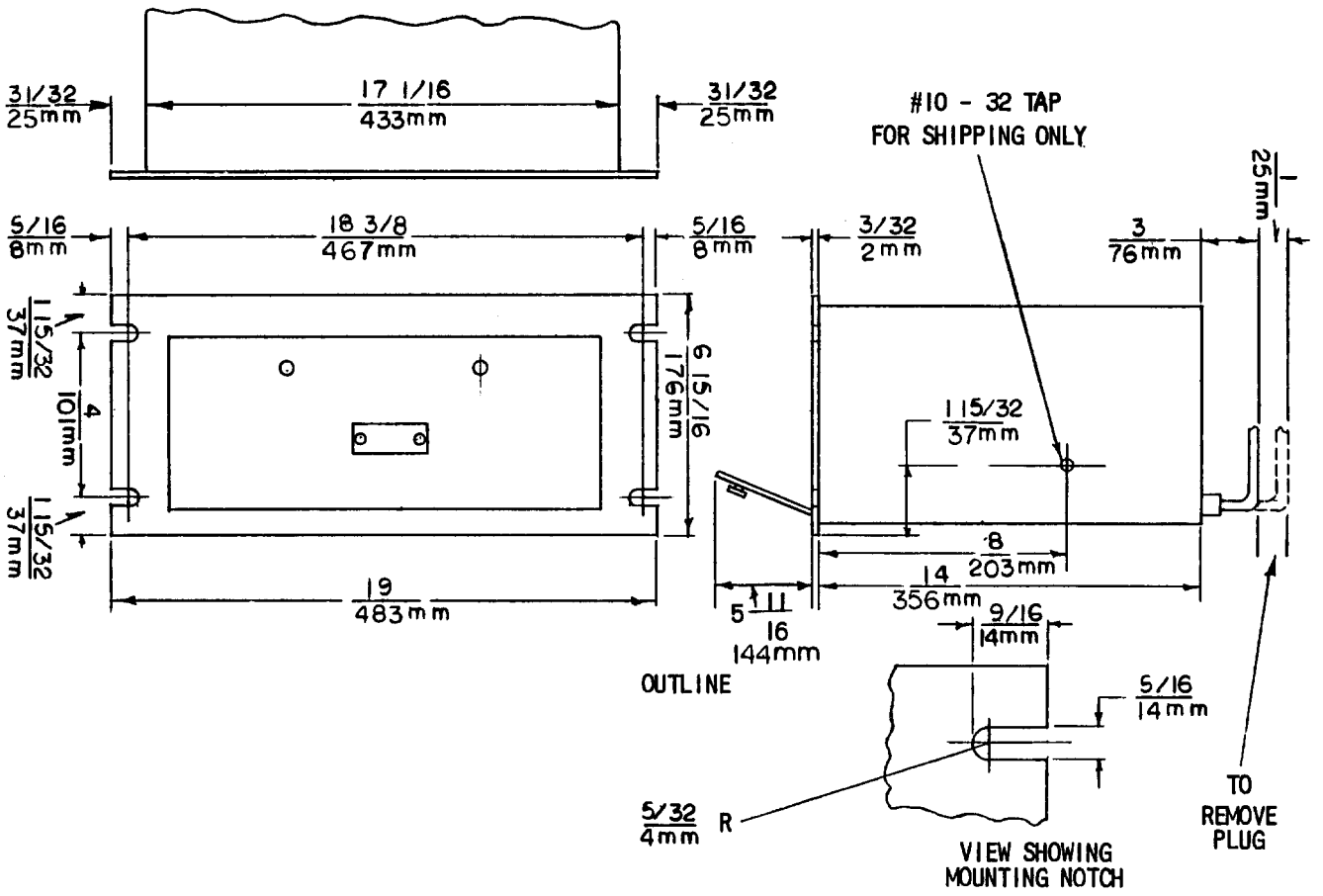


Fig. 1 (0227A2037-0) Outline and Mounting Dimensions of the SLDY51A Relay

STATIC COMBINED POSITIVE SEQUENCE DISTANCE AND NEGATIVE SEQUENCE PHASE COMPARISON RELAY TYPE SLDY51A

DESCRIPTION

The SLDY51A is a static relay comprised of positive sequence mho type distance functions, and positive, negative and zero sequence overcurrent functions. The relay is not intended for use by itself, but rather is designed for use in conjunction with other static logic and output relays to make up a complete terminal of transmission line protection operating in a combined directional and phase comparison mode. The scheme may be applied on uncompensated lines, series compensated lines, or on lines adjacent to series compensated lines. The total complement of functions that may be included in the SLDY51A are noted below:

M1	- short reach positive sequence directional mho tripping function
MT	- long reach positive sequence directional mho tripping function
MB	- offset mho positive sequence blocking function
MOB	- positive sequence out-of-step detection function (operates in conjunction with MT)
I_1T	- positive sequence current tripping supervision
I_1T_D	- positive sequence current direct tripping function
I_1B	- positive sequence current blocking supervision
FDL	- low set negative sequence current blocking and transmitter keying function
FDHL	- intermediate set negative sequence tripping function
FDHH	- high set negative sequence current tripping function
SQ AMP	- negative sequence current squaring amplifier
I_2T_D	- negative sequence current direct tripping function
$(I_0-KI_1)T_D$	- zero sequence current direct tripping function with positive sequence current restraint.
G4	- zero sequence current direct tripping function
V_1	- positive sequence voltage detector

In general, all the above functions may not be included in the SLDY51A since not all are required for all applications. Refer to the overall logic diagram and associated description supplied with each specific scheme to determine which functions have been included. When any function is omitted, this function may be added in the field by simply obtaining the necessary printed circuit cards and inserting them in the proper socket. However, in order to utilize the function, proper logic is required in other relays that comprise the total scheme. If functions are to be added in the field, refer to the relay internal diagrams and other descriptive literature for the means to do so, or contact the nearest General Electric District Sales Office for assistance.

The SLDY51A relay is packaged in a four-rack unit case suitable for mounting in a standard 19-inch rack. Outline and mounting dimensions are illustrated in Fig. 1. The internal connections for the complete SLDY51A are shown in Fig. 2, while the component printed circuit card locations are shown in Fig. 3.

APPLICATION

The SLDY51A relay was designed specifically for use in a combined directional and phase comparison transmission line pilot relaying scheme. The relay has provisions included for positive sequence mho type distance functions and positive, negative and zero sequence overcurrent functions. Other auxiliary logic and tripping type relays are required to form a complete terminal of protection.

The positive sequence distance functions in the SLDY51A, MT and MB, are used to implement the directional comparison portion of the scheme. These functions operate from the positive sequence voltage and current produced at the relay location. They will measure accurately the positive sequence impedance to the fault during three phase faults only. During unbalanced faults, their reach will be considerably shortened and the apparent impedance that they see will be dependent on the particular system configuration and fault location. These functions are only required to perform accurately during three phase faults; therefore, the scheme will always operate in the directional comparison mode whenever this type of fault occurs. MT performs as the tripping function just as in a conventional directional comparison scheme, whereas MB performs as the blocking function. These two functions are always required in the SLDY51A relay.

For all unbalanced faults, the scheme will operate in the phase comparison mode. This is accomplished via the overcurrent level detectors and squaring amplifier which operate from pure negative sequence current. These level detectors are FDL, FDHL, and FDHH. FDL is a low set blocking and transmitter keying level detector. FDHL and FDHH are intermediate and high set tripping level detectors. These level detectors are set to operate from the negative sequence current developed during any unbalanced fault that may occur on the transmission line to be protected. The output of the squaring amplifier, along with FDL pickup, permits a comparison to be made of the phase angle between the positive half cycles of negative sequence current at each end of the line. The tripping level detectors, FDHL and FDHH, permit tripping only when the phase angle between the two currents is favorable, as will be the case for all internal faults. For all external faults, the phase angle will be unfavorable; therefore, tripping will be blocked even in the event the tripping detectors were picked up. FDL and the squaring amplifier (SQ AMP) are required in all schemes. FDHL and FDHH are required on all long lines with shunt reactors. On short lines, or on lines without shunt reactors, FDHH alone is required.

Other required functions are I_1T and I_1B. Both functions operate from pure positive sequence current. I_1T is used to provide overcurrent supervision to the positive sequence distance tripping functions, and the seal-in function required during the three phase zero voltage faults. I_1B provides overcurrent supervision to the positive sequence distance blocking function.

The scheme may be applied with an ON-OFF type channel, or it may be applied with frequency shift type channels over the power line or on microwave. When applied with ON-OFF channels, the scheme is normally operated in a blocking mode. It may be operated in a blocking, unblocking or permissive mode when applied with frequency shift type channels.

The remaining functions that can be included in the SLDY51A relay are optional and may be added at the discretion of the user. These functions, with the exception of V_1, are all used to provide direct tripping independent of the channel. They may be ordered initially along with the required functions, or they may be added in the field at a future date. It should again be noted that changes may also have to be made in the auxiliary logic and/or tripping relays when optional functions are added to the SLDY51A in the field. All changes are made simply via printed circuit cards and/or jumper connections. Following is a brief description of the optional functions included in the SLDY51A.

The M1 function is a positive sequence mho type distance function that operates from pure positive sequence quantities just like MT and MB. It may be used to provide first zone direct tripping for all three phase faults within its reach setting.

The I_1T_D and I_2T_D functions operate from pure positive sequence current and pure negative sequence current, respectively. They are simple, non-directional, instantaneous overcurrent functions that may be used to provide direct tripping for severe close-in faults.

$(I_0-KI_1)T_D$ is a non-directional, instantaneous overcurrent function that operates from pure zero sequence current with some positive sequence current restraint. This function is commonly applied on series compensated lines to provide direct tripping for single-line-to-ground faults. Positive sequence restraint is used to prevent any operations that could be caused by dissymmetrics that may be introduced if asymmetrical gap flashing were to occur during load flow or three phase faults.

For uncompensated lines, a G4 function can be applied in place of the $(I_0-KI_1)T_D$ function. This function operates from pure zero sequence current alone and may be used to provide direct tripping for single-line-to-ground faults.

V_1 is an instantaneous undervoltage function that operates from pure positive sequence voltage. It may be used to monitor system voltage or it can be applied as part of a line pickup option.

For a complete description of the application of this relay, see the overall logic diagram and associated description supplied with each terminal of equipment in which the relay is used.

SETTINGS

The settings to be made on each of the functions in the SLDY51A relay will to a great degree depend on the particular application. For example, some of these functions may require different settings when applied on series compensated lines as opposed to the settings that would be required if the lines were uncompensated. For this reason, the logic description supplied with each scheme should be referred to for the specific recommendations with regards to settings for that application. The following information describes the settings that must be made and outlines, in general form, the setting requirements.

The MT function performs in a tripping capacity, therefore, it must be set to detect any three phase fault on the transmission line. This leads to the requirement that it must be set with a reach that is somewhat greater than the length of the transmission line. In general, reach settings in the order of 125 to 200 percent of the transmission line are required. In making the reach settings, a basic reach is first selected, and then the restraint taps are selected to give the desired reach. The highest basic reach tap that accomodates the desired setting should always be used for any application. On very long lines, load flow or minor swings may cause the apparent impedance seen by the relay to enter the relay characteristic. Where this may be a problem, then the relay characteristic can be made lenticular to avoid it. This change is made by increasing the pickup of the MT characteristic timer to something greater than 4.16 milliseconds (5.0 milliseconds for 50 hertz models).

The MB function acts to block tripping for external faults. In this capacity, it must coordinate with the MT function at the remote end of the line; i.e., MB must operate for any external fault that the remote MT can see. Reach settings in the blocking direction are generally made in the order of 75 percent to 175 percent of the transmission line. In order to facilitate the coordination and to insure continuous pickup on zero voltage three phase volts, MB is also provided with some offset. That is, the relay is offset to include the origin. The base reach setting on MB is common with the base reach setting on MT. Thus, once the base reach setting has been selected for MT, it is only necessary to select the restraint taps for MB in order to implement the desired reach. The offset setting is adjustable to 10, 20 or 30 percent of the reach setting in the blocking direction. The 20 percent setting should be selected for all two-terminal line applications. It may be necessary to consider the 10 or 20 percent tap on three-terminal line aplications if system conditions so warrant it. This setting is made via standoffs located on the N109 card. The MB characteristic is often expanded so that it appears to be "tomato" shaped in order to assure adequate coverage.

The M1 function is used to provide first zone coverage for three phase faults within its reach setting. On uncompensated lines, this function may be set to reach up to 90 percent of the positive sequence impedance of the line. The M1 function may be used on series compensated lines or on lines adjacent to series compensated lines provided the series capacitors are located behind the relay. Here too, the reach may be set up to 90 percent of the positive sequence impedance of the line. M1 may not be used for first zone tripping where the series capacitors are located in the tripping direction; i.e., in front of the relay. The base reach setting for M1 is common to the base reach setting for MT. Thus, once a base reach has been selected for MT, it is only necessary to select the restraint tap settings for M1 in order to implement the desired reach.

FDL, FDHL and FDHH are used to implement the phase comoparison portion of the scheme. They operate from pure negative sequence current so they must be set to detect the minimum negative sequence current that can be produced for any unbalanced fault on the transmission line. The settings must also be selected so that proper coordination is obtained between the blocking and tripping functions.

FDL is a low-set fault detector that acts as a blocking function by keying the transmitter to the blocking frequency. Generally, it is set as sensitively as possible just so it will not operate due to the negative sequence current that can be produced as a result of system unbalances that may be introduced by untransposed lines, unbalanced loading, etc.

FDHL and FDHH are intermediate-set and high-set tripping detectors, respectively. Both functions operate from pure negative sequence current and both are required only on long lines with shunt reactors. The reason for this is that they provide the necessary security in the presence of the transients that are introduced at the inception of the fault when shunt reactors are used to compensate the shunt capacitance of the line. FDHH is set above the transient currents and it will provide high speed tripping when its pickup setting is exceeded. FDHL is set to pick up at some lower level, but it will initiate tripping through time delay, thus allowing time for the transients to die out. In this way, high speed tripping is provided for severe faults, while added security is obtained at low level faults where somewhat longer tripping times can be tolerated. Both functions must be set at a higher pickup level than the remote FDL function to assure proper coordination for external faults. The minimum setting for each will depend on the amount of shunt reactance and shunt capacitance that is involved. In general, higher settings than the minimum should be used just so that the setting will allow the minimum internal fault to be detected with some margin. Where shunt reactors are not involved, FDHH alone is required. It must be set above the remote FDL function with some margin, yet still be able to detect the minimum internal fault. Its minimum setting will be dependent on the shunt capacitance of the line. Again, higher than minimum settings should be used, just so long as the setting permits the minimum internal fault to be detected with some margin.

The overcurrent supervision functions, I_1T and I_1B, are used to provide supervision to the tripping and blocking functions respectively. I_1T must be set to detect the minimum internal three phase fault with some margin. This is necessary to insure that the seal-in function will be maintained in the event a zero voltage three phase fault were to occur. The seal-in insures that the breaker failure initiate function will stay energized during a zero voltage fault, and so provide breaker failure protection in the event a breaker failure were to occur at the same time. Where possible, I_1T should be set above full load current, provided this setting is compatible with the previous stated requirement. The I_1B function must be set with a lower setting than the remote I_1T function.

The direct tripping functions, I_1T_D, I_2T_D, $(I_0-KI_1)T_D$ or G4 are non-directional, instantaneous overcurrent functions that operate from positive, negative and zero sequence currents, respectively. Because these functions are non-directional, they must be set above the maximum value of current for any external fault.

The V_1 function is a positive sequence undervoltage function that may be used to provide loss of voltage protection, or it may be used as part of a line pickup scheme.

Any setting that is within the pickup range and meets the operational requirements may be made on this function.

The MOB function works in conjunction with the MT function to detect an out-of-step condition. This function uses the same magnetics and restraint tap as the MT function, but it has a separate characteristic timer. Thus, it will operate at the same angle and reach as MT, but its characteristic can be expanded with respect to MT by using a lower characteristic timer setting than used with MT. The exact setting to be used will depend on the particular application.

RANGES

All the distance functions (M1, MT, MOB and MB) in the SLDY51A have a common base reach known as the relay base reach. This relay base reach is usually three ohms or one * ohm (15 ohms or five ohms for one ampere models), and is determined by the connections made to the terminal board on the rear of the relay. This relay base reach has an adjustable angle of 60 to 90 degrees. The standard angle setting is 85 degrees.

Table I showns the connections necessary for a relay base reach of three ohms or * one ohm (15 ohms or five ohms for one ampere models). It also shows typical pickup ranges of several overcurrent functions whose pickup ranges depend on the relay base reach. The pickup ranges for I_1B, I_1T and I_1T_D are given in positive sequence amperes. The pickup range for G4 is given in neutral current or $3I_0$.

TABLE I

I_B		I_C		$3I_0$			OVERCURRENT PICKUP RANGES			
IN	OUT	IN	OUT	IN	OUT	RELAY BASE REACH	I_1B	I_1T	I_1T_D	G4
YB3	YB5	YB6	YB8	YB10	YB12	3 OHMS 5A RELAY 15 OHMS 1A RELAY	0.5-4 0.1-0.8	1-8 0.2-1.6	4-32 1.2-6.4	2-20 0.4-4
YB2	YB4	YB6	YB7	YB9	YB11	1 OHM 5A RELAY 5 OHMS 1A RELAY	1.5-12 03.-2.4	3-24 0.6-4.8	12-96 2.4-19.2	6-60 1.2-12

The angle of maximum reach for M1, MT and MB are independently adjustable. The angle of maximum reach is determined by the polarizing phase shift and the relay base reach angle. The polarizing phase shift adjustment range for each of the three functions is minus 15 degrees to plus 30 degrees. The MOB polarizing phase shift is determined by, and is identical to, the phase shift of MT.

The voltage restraint settings for M1, MT and MB (MB in the blocking direction) are independent of each other. The MOB restraint voltage setting is the same as the MT. The range of the restraint voltage is 100 percent down to ten percent. In other words, * if the relay base reach is connected for three ohms (15 ohms for one ampere models),

the M1, MT and MB (reverse reach) can be set independently for a reach of three to 30 ohms by setting the voltage restraint for the five ampere relay, and 15-150 for the one-ampere relay.

The MB reach in the tripping direction is a fixed percentage of the MB reverse reach in the blocking direction. This fixed percent is determined by a jumper on the printed circuit card in position AE in the SLDY51A relay. Typical values for the choices of MB reach as a percentage of MB reverse reach are 10, 20 and 30 percent.

The $(I_0-KI_1)T_D$ function is a zero-sequence direct-tripping function. When the positive sequence current is zero ($I_1 = 0$), the pickup range is 2 to 20 amperes, or 6 to 60 amperes, similar to the G4 function for the five ampere relay. The pickup range for the one ampere relay is 0.4-4 amperes or 1.2-12 amperes and the range of K is 0.15 to 0.45.

The pickup range of the V_1 function is adjustable over the range of 40 to 100 percent of the rated system positive sequence voltage.

The pickup ranges for the negative sequence level detectors are all expressed in negative sequence amperes. These pickup ranges are given in Table II. The FDL, FDHH and FDHL level detectors are used in the negative sequence phase comparison portion of the total relay scheme. The I_2T_D is a direct tripping function. These ranges are obtained using the full current transformer (TH) primary winding 3. The intermediate taps are not used.

TABLE II

FUNCTION	PICKUP RANGE 5 AMP STEADY STATE	PICKUP RANGE 1 AMP STEADY STATE
FDL	0.2 - 1.6	0.04 - 0.32
FDHH	0.25 - 4.0	0.05 - 0.8
FDHL	0.25 - 3.2	0.05 - 0.64
I_2T_D	2.0 - 16	0.4 - 3.2

The sensitivity of the squaring amplifier is expressed in terms of the FDL pickup setting. The squaring amplifier output can be adjusted for a six to seven millisecond block width at the particular FDL pickup setting.

All the functions available in an SLDY51A relay are described in this section. Refer to the unit nameplate for the particular functions and the specific ranges available on a particular SLDY51A.

RATINGS

The SLDY51A relay is designed for use in an environment where the air temperature outside the relay case is between minus 20 degrees and plus 65 degrees Centrigrade.

The SLDY51A relay requires a plus or minus 15 volt DC power source which can be obtained from Type SSA50 and up power supplies .

* The current circuits of the SLDY51A relay are rated at five amperes, 60 hertz or one ampere, 50 hertz continuous duty (depending on model), and have a one second rating of 300 amperes (60 amperes for one ampere models). The potential circuits are rated 120 volts, 60 or 50 hertz, depending on model.

BURDENS

DC BURDEN

The SLDY51A relay presents a burden to the Type SSA power supply of:

390 milliamperes from the plus 15 VDC supply
180 milliamperes from the minus 15 VDC supply

AC BURDEN

The potential circuits present a burden at 120 volts phase-to-phase and at 100 percent restraint of 7.0 volt-amperes to Phase A, 11.5 volt-amperes to Phase B, and 5.5 volt-amperes to Phase C.

The current circuit's burden in the three ohm base reach tap at five amperes phase-to-neutral is as follows:

TABLE III

**	PHASE A	PHASE B	PHASE C	NEUTRAL
R	0.02	0.033	0.06	0.0014
X	0.009	0.022	0.032	0.0143
Z	0.022	0.040	0.068	0.0143

** On the one ampere relay model, multiply by 25

CHARACTERISTICS

OPERATING PRINCIPLES

The SLDY51A relay uses positive sequence voltage and current networks to obtain the V_1 and I_1Z quantities. These quantities are used to derive the various mho characteristics employed in the directional comparison portion of the relay. The SLDY51A relay also uses a negative sequence current network. This network provides the signal for the phase comparison portion of the relay. The operating theory of these networks and functions are explained in the following sections.

Positive Sequence Voltage Network

The positive sequence voltage network used in the SLDY51A relay is shown in Fig. 4. The derivation of the output voltage is described below. For discussion, the output of the positive sequence voltage network will be called V_X.

$$V_X = V_{B-C}\left(\frac{kP1 + R2}{R1+R2+P1}\right) + V_{C-A}\left(\frac{mP2}{mP2 + 1/jwc}\right)$$

where k and m are the percentages of P1 and P2 used.

By design,

$$\frac{kP1 + R2}{R1+R2+P1} = 1/2$$

and

$$\frac{mP2}{mP2 + 1/jwc} = 1/2 \angle 60^o$$

Therefore:

$$V_X = 1/2\ V_{B-C} + 1/2\ V_{C-A} \angle 60^o$$

$$V_A = V_{A0} + V_{A1} + V_{A2}$$

$$V_B = V_{A0} + a^2V_{A1} + aV_{A2}$$

$$V_C = V_{A0} + aV_{A1} + a^2V_{A2}$$

$$V_X = 1/2\left[(V_{A0} + a^2V_{A1} + aV_{A2}) - (V_{A0} + aV_{A1} + a^2V_{A2})\right]$$

$$+ 1/2 \angle 60^o\left[(V_{A0} + aV_{A1} + a^2V_{A2}) - (V_{A0} + V_{A1} + V_{A2})\right]$$

$$V_X = 1/2\left[(a^2 - a)\ V_{A1} + (a - a^2)\ V_{A2}\right] + 1/2 \angle 60^o\left[(a - 1)\ V_{A1} + (a^2 - 1)\ V_{A2}\right]$$

$$V_X = .866\ (V_{A1} \angle -90^o + V_{A1} \angle 210^o + V_{A2} \angle 90^o + V_{A2} \angle -90^o)$$

$$V_X = 1.5\ V_{A1} \angle 240^o$$

For a pure positive sequence input:

$$V_X = .866\ V_{C-A} \angle 90^o$$

This output voltage, V_X, is supplied to the printed circuit cards through a voltage transformer with a tapped secondary winding. These secondary taps provide the 10 to 100 percent restraint voltage available to the distance functions. The full secondary voltage is supplied directly to the printed circuit cards as needed. The tapped secondary voltage is supplied to the printed circuit cards through isolation transformers to provide proper isolation and phasing.

Positive Sequence Current Network

The positive sequence current network used in the SLDY51A relay is shown in Fig. 5. The network consists of two transactors (TB and TC), each with two primary windings and an adjustable resistive load across the secondary winding.

The term "transactor" is a contraction of transformer-reactor. It is essentially an air-gap current transformer with secondary current (and therefore secondary voltage across the loading resistor) proportional to the primary current by its transfer impedance and the associated angle.

$$Z_T = \frac{V_{OUT}}{I_{IN}} \angle\theta_T$$

where:

V_{OUT} = Secondary output voltage

I_{IN} = Vector sum of the input currents

θ_T = Angle by which V_{OUT} leads I_{IN}

The derivation of the positive sequence current network output voltage is given below. For discussion the output voltage of the positive sequence current network will be called V_Y. By design,

$$Z_{TC} = .85\ \sqrt{3}\ Z_{TB}$$

$$\theta_{TB} = 75^o$$

$$\theta_{TC} = 45^o$$

$$V_Y = k\left[Z_{TB}\ (I_C - I_B) \angle 75^o\right] + Z_{TC}\left[I_B - 1/3(I_N)\right] \angle 45^o$$

where k is the percentage of P3 used.

Let k = .85

$$V_Y = .85\ Z_{TB}\ (I_C - I_B) \angle 75^o + .85\sqrt{3}\ Z_{TB}\left[I_B - 1/3(I_N)\right] \angle 45^o$$

$$I_A = I_{A0} + I_{A1} + I_{A2}$$

$$I_B = I_{A0} + a^2 I_{A1} + a I_{A2}$$

$$I_C = I_{A0} + a I_{A1} + a^2 I_{A2}$$

$$I_N = I_A + I_B + I_C = 3I_0$$

$$V_Y = .85\ Z_{TB}\left[I_{A0} + a I_{A1} + a^2 I_{A2} - (I_{A0} + a^2 I_{A1} + a I_{A2})\right] \angle 75^o$$

$$+ .85\sqrt{3}\ Z_{TB}\left[I_{A0} + a^2 I_{A1} + a I_{A2} - 1/3(3I_0)\right] \angle 45^o$$

$$V_Y = .85\left[Z_{TB}\ (a - a^2)\ I_{A1} + (a^2 - a)\ I_{A2}\right] \underline{/75^o}$$

$$+ .85\ \sqrt{3}\ Z_{TB}\left[a^2 I_{A1} + a I_{A2}\right] \underline{/45^o}$$

$$= .85\ Z_{TB}\ (\sqrt{3}\ I_{A1}\ \underline{/90^o} + \sqrt{3}\ I_{A2}\ \underline{/-90^o})\ \underline{/75^o}$$

$$+ .85\ \sqrt{3}\ Z_{TB}\ (I_{A1}\ \underline{/240^o} + I_{A2}\ \underline{/120^o})\ \underline{/45^o}$$

$$= .85\ \sqrt{3}\ Z_{TB}\ (I_{A1}\ \underline{/165^o} + I_{A1}\ \underline{/285^o}$$

$$+ I_{A2}\ \underline{/-15^o} + I_{A2}\ \underline{/165^o})$$

$$V_Y = .85\ \sqrt{3}\ Z_{TB}\ I_{A1}\ \underline{/225^o}$$

By means of similar manipulations it may be shown that the positive sequence networks of the SLDY51A produce no output when pure negative sequence quantities are applied.

This output voltage V_Y is supplied to a bridge resistor-capacitor phase shift circuit. The output of this phase shift circuit is at the midpoint of capacitor C7 and potentiometer P6 with respect to the midpoint of resistors R3 and R4. The phase angle of the output of this phase shift circuit is adjustable with respect to the input by adjusting potentiometer P6. This phase shift circuit provides the adjustable angle for the relay base reach.

The output voltage from the phase shift circuit is supplied to the printed circuit cards through a potential divider consisting of potentiometer P5 and resistor R5. The adjustment of potentiometer P5 provides the proper magnitude of the relay base reach at the desired angle.

Positive Sequence Mho Characteristics

General Operating Principles:

The principle used to derive the mho characteristics is illustrated in Fig. 6. The I_1Z quantity is a voltage proportional to the positive sequence current in the line, and is obtained from the positive sequence current filter. The V_1 quantity is proportional to positive sequence voltage at the relay location and is obtained from the positive sequence voltage network. The quantity $(I_1Z - V_1)$ is the phasor difference between these two quantities. I_1Z' is the reverse reach of the relay. The phase angle between $(I_1Z - V_1)$ and $(I_1Z' + V_1)$ is less than 90 degrees for an impedance point internal to the relay characteristic, equal to 90 degrees at the balance point, and greater than 90 degrees for an external impedance point for which the relay should not operate. The quantities V_1 and I_1Z are combined in operational amplifiers (filter cards) and converted into blocks of voltage representing quantities $(I_1Z - V_1)$ and $(I_1Z' + V_1)$. The coincidence of these blocks is then measured. Blocks which are 90 degrees apart are coincident for 4.17 milliseconds (five milliseconds for 50 hertz models). Blocks which are less than 90 degrees apart are coincident for more than 4.17 milliseconds (or five milliseconds). Blocks which are more than 90 degrees apart are coincident for less than 4.17 milliseconds (or five milliseconds). The mho function consists of a filter card, a coincidence card, and a timer card which measures

the coincidence of (I_1Z - V) and (I_1Z' + V_1). These groups of cards which comprise the various mho functions are shown in Fig. 2. If the characteristic has no reverse reach, the operating principle remains the same as just described, except I_1Z' is zero.

Filter Card:

The filter card (F card) provides amplification and phase shift as well as filtering to the operating signals. The filter card has three input signals, I_1Z, $+V_1$ and $-V_1$, if there is no reverse reach to the particular mho function. If there is a reverse reach, a fourth input signal, I_1Z', is present.

The outputs of the filter card are 30 volt DC square waves (minus 15 volts DC to plus 15 volts DC). The square wave output at pin 9 is the polarizing quantity derived from the $+V_1$ or (I_1Z' + V_1) input. The square wave at pin 8 is the operating quantity derived from (I_1Z - V_1).

In addition to filtering, the F card provides an adjustment of the phase relationship between the output quantities by shifting the polarizing quantity relative to the operating quantity. The mho operation occurs when the coincidence between the outputs at pin 8 and pin 9 are equal to the characteristic timer setting.

Coincidence Card:

The coincidence logic card (C card) produces output blocks equal in width to the coincidence of the polarizing and operating quantities from the output of the filter card. Depending on the particular mho function and the particular filter card, the C card measures the coincidence of like half-cycles (positive with positive and negative with negative) or the coincidence of unlike half-cycles (positive with negative and negative with positive). In either case the result is to measure the coincidence of the polarizing and operating quantities. The outputs of the coincidence card are the inputs to the characteristic timer card.

Typical waveforms are shown in Fig. 7. These waveforms represent the summed input signals to the filter card, the output square waves from the filter card, and the resulting coincidence measurement of the coincidence card.

Characteristic Timer Card:

The characteristic timer card (T card) produces an output when the width of the input blocks exceeds the pickup delay setting of the timer. The typical characteristic timer may have a longer pickup delay on the initial input block than on succeeding input blocks. Refer to the overall logic diagram for the particular relay equipment to determine this first pulse and steady state pickup delay (or pickup delay range) available for each particular mho function.

The shape of the characteristic is determined by the steady state pickup delay setting. At a given angle (other than at the relay base reach angle), the pickup point changes when the steady state pickup setting of the characteristic timer is changed. Increasing the pickup delay decreases the fault voltage required for operation.

Construction of a Mho Characteristic:

The construction of a typical mho characteristic is shown in Fig. 8. The reach at the relay base reach angle is a constant chord of the characteristic. The reach of the mho function at the relay base reach angle can be calculated from the expression:

$$Z = \frac{T_B}{T} \times 100$$

where:

T = Voltage restraint tap setting of the particular mho function in percent

T_B = Basic minimum ohmic tap setting for the relay base reach

There is a resistor between the output of the I_1Z network (positive sequence current network) and the input to the filter card for each mho function. These resistors are mounted on the N109 card in position AE (Fig. 2). The value of this resistor determines the relationship between the base reach of the particular mho function and the relay base reach. Typically the value of this resistor is 10,000 ohms, which makes the particular mho function base reach equal to the relay base reach. For values of this resistor other than 10,000 ohms, the reach of the particular mho function at the relay base reach angle as calculated in the above expression is multiplied by a factor, K.

$$K = \frac{20{,}000}{R + 10{,}000}$$

where:

K = Multiplying factor for the mho function reach

R = Resistance in ohms of the resistor between the I_1Z network and the filter card.

The construction of a mho characteristic for leading and lagging polarizing voltage is shown in Fig. 8 (B) and (C). Note that the reach at the relay base reach angle remains constant. The change in the area of the characteristic is caused entirely by the phase shift in the polarizing quantity on the filter card. A leading phase shift in the polarizing quantity shifts the mho characteristic in the clockwise direction.

The angles $\alpha 1$ and $\alpha 2$ are the apparent angles of coincidence of the polarizing and operating quantities for the two lobes of the characteristic. When the polarizing phase shift is zero, then $\alpha 1$ and $\alpha 2$ are identically equal to the steady state pickup delay of the characteristic timer. If there is a polarizing phase shift, the angles $\alpha 1$ and $\alpha 2$ are determined by the characteristic timer setting (TS) and the polarizing phase shift (ϕ):

$$\alpha 1 = TS - \phi$$

$$\alpha 2 = TS + \phi$$

To construct a mho characteristic, refer to Fig. 9 and follow the steps listed below:

Step 1: Determine the length of the constant chord, Z, which is the reach of the mho function at the relay base reach angle. Calculate this reach per the equation given in the beginning of this section.

Step 2: Determine the steady state pickup delay for the characteristic timer for the particular mho function from the overall logic diagram. Convert this time delay to degrees.

$\not\beta = 21.6 \times TS$

* $\not\beta = 18 \times TS$ (for 50 hertz, one ampere models)

where:

TS = The characteristic timer steady state pickup delay expressed in milliseconds

$\not\beta$ = The pickup delay in degrees

Step 3: Determine the diameter angles of the two lobes.

$$D_1 = \theta - \phi + (90^o - \not\beta)$$

$$D_2 = \theta - \phi - (90^o - \not\beta)$$

where:

D_1 and D_2 = Angles of the diameters in degrees

θ = Relay base reach angle (typically 85 degrees)

ϕ = Polarizing phase shift

$\not\beta$ = Timer pickup delay in degrees

The center for the circle for the lobe is the point on the diameter (D_1 or D_2) which is equidistant from the two ends of the constant chord (Z). These centers can be determined by constructing the perpendicular bisector of the chord (Z). If the mho function has a reach in one direction only, one end of the constant chord is at the origin. If the mho function has both a forward and a reverse reach, then the ends of the chord are at the forward end of the forward chord, and the reverse end of the reverse chord.

Some significant features of the mho characteristic can be pointed out:

a) If the polarizing phase shift is zero, then the characteristic is symmetrical about the relay base reach angle, no matter what the characteristic timer pickup delay is set for.

b) If the steady state pickup delay of the characteristic timer is 4.17 * milliseconds (5.0 milliseconds for the one ampere models), then ϕ is equal to 90 degrees. Therefore, the two diameters, D_1 and D_2, are identical no matter what the polarizing phase shift setting is. In other words, if the characteristic is set for a circle, it will remain a circle.

c) When the characteristic passes through the origin, the diameters D_1 and D_2 are also the angles of maximum reach for the two lobes of the characteristic.

MT Function:

The MT function typically consists of resistor RB on the N109 card in position AE, * an F106 filter card (F132 card for the 50 hertz, one ampere models) in position AG, a C102 coincidence card in position AL and a T133 characteristic timer in position AN (Fig. 2). Usually this characteristic is set for a circle; however, refer to the overall logic diagram for the actual characteristic timer pickup delay. The C102 coincidence card measures the coincidence of unlike half-cycles of the filter card output signals.

MOB Function:

The MOB characteristic is derived from the same filter card and coincidence card as the MT function. It has a separate characteristic timer, usually a T105 card. The pickup delay setting is adjustable. The actual setting, and therefore the shape of the characteristic, are dependent on the application.

M1 Function:

The M1 function typically consists of resistors RA and RG and a capacitor on the * N109 card in position AE, as well as an F123 filter card (F131 card for the 50 hertz, one ampere models) in position AF, a C104 coincidence card in position AJ and a T133 characteristic timer in position AK. The resistor RG and the capacitor on the N109 card provide a necessary phase shift between the V_1 signal and the filter card input. The C104 coincidence card measures the coincidence of like half-cycles of filter card output signals. This characteristic is usually a circle; however, refer to the overall logic diagram for the actual characteristic timer steady state pickup delay.

MB Function:

The MB function typically consists of resistors RC, RD, RE and RF on the N109 card * in position AE, as well as an F108 filter card (F133 card for the 50 hertz, one ampere models) in position AH, a C102 coincidence card in position AP and a T129 characteristic timer in position AR. The C102 coincidence card measures the coincidence of unlike half-cycles of filter card output signals. The steady state pickup delay of the characteristic timer is typically set for 3.5 milliseconds; however, refer to the overall logic diagram for the actual setting.

The MB characteristic has its major reach in the blocking direction. It also has a reach in the tripping direction. Resistor RC is 10,000 ohms, making the base reach in the blocking direction MB (reverse reach) equal to the relay base reach. Resistors RD,

RE and RF are chosen to make the reach in the tripping direction (MB) a fixed percentage of the reach in the blocking direction MB (reverse reach). Typical percentages are 30, 20 and 10 percent for Taps A, B and C, respectively. These taps are also located on the N109 card in position AE (Fig. 2).

Mho Function Operating Characteristics:

The operate and reset times of each mho function is basically determined by the characteristic timer, the type of fault, and the incidence angle. There is no significant time delay in the circuitry ahead of the timer.

* A phase current of one ampere (0.2 ampere for one ampere models) on a three phase fault will cause the SLDY51A relay to pull back to no less than 90 percent of the nomi-
* nal reach, with the basic ohmic tap setting (T_B) of three ohms (15 ohms for the one ampere models).

Positive Sequence Voltage Detectors

The V_1 level detector function is operated by a single input quantity from the positive sequence voltage network. The level detector operates on the magnitude of V_1, independent of phase angle. The level detector has an intentional time delay before resetting, when the input V_1 drops below the pre-set level. The level is adjusted using P1 on the detector card in position AS.

Positive Sequence Overcurrent Functions

The positive sequence overcurrent functions (I_1B, I_1T and I_1T_D) are operated by a single input quantity from the positive sequence current network. The level detectors operate on the magnitude of I_1, independent of the direction of current flow. The pickup level for I_1B is adjusted using potentiometer P1 on the detector card in position M. The pickup level for I_1T is adjusted using potentiometer P1 on the detector card in position P. The pickup level for I_1T_D is adjusted using potentiometer P1 on the detector card in position N.

Negative Sequence Current Network

There are two major components in the negative sequence current network. They are the three phase auxiliary current transformer and the mixing network on the F127 card
* (F176 for 50 hertz, one ampere models) in position B. The three phase auxiliary transformer converts the current received by the relay into low level signals suitable for operation in the printed circuit card. The mixing network produces a single phase voltage which is proportional to the negative sequence portion of the input current.

Three Phase Auxiliary Current Transformer:

The three phase auxiliary current transformer is a wye-delta transformer. This delta secondary connection eliminates zero sequence current. Therefore the only currents available are positive and negative sequence currents. The transformer also steps down the current which steps up the voltage from primary to secondary. The load on the secondary of the transformer is three 5.0 ohm resistors connected in a wye configuration with the neutral connected to relay logic reference. This combination of turns ratio and resistive load makes the transformer output appear as a voltage source

to the F127 printed circuit card (F176 card for 50 hertz, one ampere models). Therefore, the outputs of the three phase auxiliary current transformer circuit are three phase-to-neutral voltages proportional to the three phase current inputs to the SLDY51A relay. The equations for this relationship can be expressed as follows:

$$V_{AB} = .0625\,(I_A - I_B)$$

$$V_{BC} = .0625\,(I_B - I_C)$$

$$V_{CA} = .0625\,(I_C - I_A)$$

V_{AB}, V_{BC} and V_{CA} are the three voltage outputs from the three-phase auxiliary current transformer circuit. They are also the voltage input signals for the mixing network. The multiplying constant 0.0625 is determined by the turns ratio of the transformer at the 5.0 ohm load resistors.

Negative Sequence Network, F127 Printed Circuit Card
(F176 card for 50 hertz, one ampere models):

The negative sequence mixing network is shown in Fig. 10. The three input signals are V_{AB}, V_{BC} and V_{CA}. The output signal for purposes of discussion will be called V_Z. The equation for this output signal is as follows:

$$V_Z = 2.55\,V_{AB}\,\underline{/180^o} + 2.92\,V_{BC}\,\underline{/150^o} + 1.49\,V_{CA}\,\underline{/150^o}$$

The input currents to the three phase auxiliary current transformer are:

$$I_A = I_{A0} + I_{A1} + I_{A2}$$

$$I_B = I_{A0} + a^2 I_{A1} + a I_{A2}$$

$$I_C = I_{A0} + a I_{A1} + a^2 O_{A2}$$

The input signals to the negative sequence mixing network are:

$$V_{AB} = .0625\,(I_A - I_B)$$

$$= .0625\,\left[(I_{A0} + I_{A1} + I_{A2}) - (I_{A0} + a^2 I_{A1} + a I_{A2})\right]$$

$$= .0625\,\left[(1 - a^2)\,I_{A1} + (1 - a)\,I_{A2}\right]$$

$$V_{AB} = .108\,(I_{A1}\,\underline{/30^o} + I_{A2}\,\underline{/-30^o})$$

$$V_{BC} = .0625\,(I_B - I_C)$$

$$= .0625\,\left[(I_{A0} + a^2 I_{A1} + a I_{A2}) - (I_{A0} + a I_{A1} + a^2 I_{A2})\right]$$

$$= .0625\,\left[(a^2 - a)\,I_{A1} + (a - a^2)\,I_{A2}\right]$$

$$V_{BC} = .108\,(I_{A1}\,\underline{/-90^o} + I_{A2}\,\underline{/90^o})$$

$$V_{CA} = .0625\ (I_C - I_A)$$
$$= .0625\ \left[(I_{A0} + aI_{A1} + a^2I_{A2}) - (I_{A0} + I_{A1} + I_{A2})\right]$$
$$= .0625\ \left[(a - 1)\ I_{A1} + (a^2 - 1)\ I_{A2}\right]$$
$$V_{CA} = .108\ (I_{A1}\ \underline{/150^o} + I_{A2}\ \underline{/-150^o})$$

Substituting these expressions for V_{AB}, V_{BC} and V_{CA} into the equation for V_Z gives the following relationship:

$$V_Z = .276\ I_{A1}\ \underline{/180^o + 30^o} + I_{A2}\ \underline{/180^o - 30^o})$$
$$+ .316\ (I_{A1}\ \underline{/150^o - 90^o} + I_{A2}\ \underline{/150^o + 90^o})$$
$$+ .161\ (I_{A1}\ \underline{/150^o + 150^o} + I_{A2}\ \underline{/150^o - 150^o})$$

$$= .276\ (I_{A1}\ \underline{/210^o} + I_{A2}\ \underline{/150^o})$$
$$+ .316\ (I_{A1}\ \underline{/60^o} + I_{A2}\ \underline{/240^o})$$
$$+ .161\ (I_{A1}\ \underline{/300^o} + I_{A2}\ \underline{/0^o})$$

$$= .276\ \left[(-.866 - j.50)\ I_{A1} + (-.866 + j.50)\ I_{A2})\right]$$
$$+ .316\ \left[(.50 + j.866)\ I_{A1} + (-.50 - j.866)\ I_{A2}\right]$$
$$+ .161\ \left[(.50 - j.866)\ I_{A1} + I_{A2}\right]$$

$$= (-.239 - j.138)\ I_{A1} + (-.239 + J.138)\ I_{A2}$$
$$+ (.158 + j.274)\ I_{A1} + (-.158 - j.274)\ I_{A2}$$
$$+ (.081 + j.139)\ I_{A1} + .161\ I_{A2}$$
$$= .236\ I_{A2} - j.136\ I_{A2}$$
$$V_Z = .273\ I_{A2}\ \underline{/210^o}$$

As can be seen from the above expression, the output signal from the negative sequence network is a single phase voltage directly related to the negative sequence component of the input current. Also, there is no output signal due to the positive sequence component of the input current.

Negative Sequence Fault Detectors

The negative sequence fault detectors (FDL, FDHH, FDHL, I_2T_D and SQ AMP) operate on the output signal from the negative sequence mixing network. The complete fault detector function consists of three parts: an adjustable amplifier, a filter card and a level detector card. These groups of cards can be seen in Fig. 2.

The level detector card operates on the output signal from the filter card. When this signal exceeds the threshold of the level detector, it picks up, producing a logic output signal. The filter card insures that the fault detector function has the proper operating characteristics and frequency response for use in the total relaying scheme. The actual pickup level of the fault detector function is determined by the setting of the adjustable amplifier circuit. The input signal to the adjustable amplifier circuit is the output from the negative sequence mixing network.

The pickup level is established in the adjustable amplifier so that no matter what the pickup setting is, the signal level through the filter card is the same. This insures that the fault detector function will have the same operating characteristics no matter what pickup level it is set for. There is a pickup level adjustment on the level detector card itself; however, except for special cases, it is ued to match its threshold with the output level of the filter card.

FDL Fault Detector:

The FDL fault detector function typically consists of the adjustable amplifier circuit on the F127 card (F176 card for 50 hertz, one ampere models) in position B, the F129 filter card (F174 filter card for 50 hertz, one ampere models) in position C, and the D111 level detector card in position H (see Fig. 2). The pickup level for FDL is set by adjusting the potentiometer on the F127 card (or F176 card) in position B. The dropout time delay for FDL is long compared to the other fault detectors to maintain proper coordination on clearing external faults.

Squaring Amplifier:

The squaring amplifier function (SQ AMP) produces output blocks up to one half-cycle wide, corresponding to the positive half-cycles of the output signal from the negative sequence mixing network. These output blocks are used to perform the phase comparison.

The SQ AMP operates from the same adjustable amplifier and filter as FDL. Therefore, its operating level directly depends on the operating level of FDL. Once the pickup level of FDL has been set, the output block width can be set for six to seven milliseconds (eight to nine milliseconds for 50 hertz, one ampere models) at the FDL opeating level. This adjustment is made by adjusting the potentiometer on the SQ AMP card in position G.

FDHH Fault Detector:

The FDHH fault detector function typically consists of one of the adjustable amplifier circuits on the F128 card in position D, the F130 filter card (F175 card for 50 hertz, one ampere models) in position E, and the D112 level detector card (D144 card for 50 hertz, one ampere models) in position J. The pickup level for FDHH is set by adjusting the top potentiometer on the F128 card in position D.

FDHL Fault Detector:

The FDHL fault detector function uses the same adjustable amplifier circuit and filter card as FDHH. This helps to insure the proper coordination of operating

characteristics between FDHH and FDHL. The operating level of FDHH must be set first, then the operating level of FDHL can be set by adjusting the potentiometer on the level detector card in position K.

I_2T_D Fault Detector:

The I_2T_D fault detector function typically consists of one of the adjustable
* amplifier circuits on the F128 card in position D, the F129 filter card (F174 card for
* 50 hertz, one ampere models) in position F, and the D112 level detector card (D144 card for 50 hertz, one ampere models) in position L. The pickup level for I_2T_D can be set by adjusting the bottom potentiometer on the F128 card in position D.

Zero Sequence Overcurrent Functions

There are two zero sequence overcurrent functions available in the SLDY51A relay. The G4 function operates on zero sequence current only. The $(I_0-KI_1)T_D$ operates on zero sequence current with positive sequence restraint. Typically both functions cannot be supplied in one equipment.

G4 Overcurrent Function:

The G4 overcurrent function is operated by a single input quantity representing the zero sequence current in the system. The level detector operates on the magnitude of neutral current ($3I_0$) input to the relay, and it is independent of the direction of current flow. The pickup level for G4 is set by adjusting the potentiometer on the D114
* card (D141 card for 50 hertz, one ampere models) in position R.

$(I_0-KI_1)T_D$ Overcurrent Function:

The $(I_0-KI_1)T_D$ overcurrent function typically consists of an F114 amplitude comparator card in position R and a T121 characteristic timer in position S. This characteristic timer is similar to those already discussed in this book. Refer to the overall logic diagram for the required steady state pickup delay.

The amplitude comparator card has two inputs: the operate signal and the restraint signal. When the operate signal ($3I_0$) exceeds the percentage of the restraint signal (I_1) determined by K, then the amplitude comparator produces an output signal. When the duration of the output signal exceeds the pickup delay of the characteristic timer, then the $(I_0-KI_1)T_D$ function produces an output. This function is also a non-directional overcurrent function.

The $3I_0$ operate level is set by adjusting potentiometer P2 on the F114 card in position R. The K factor is set by adjusting potentiometer P1 on the F114 card in position R.

RECEIVING, HANDLING AND STORAGE

These relays will normally be supplied as part of a static relay equipment, mounted in a rack or cabinet with other static relays and test equipment. Immediately upon receipt of a static relay equipment, it should be unpacked and examined for any damage sustained in transit. If injury or damage resulting from rough handling is

evident, file a damage claim at once with the transportation company and promptly notify the nearest General Electric Sales Office.

Reasonable care should be exercised in unpacking the equipment. If the equipment is not to be installed immediately, it should be stored indoors in a location that is free from moisture, dust, metallic chips, and severe atmospheric contaminants.

Just prior to final installation the shipping support bolt should be removed from each side of all relay units, to facilitate possible future unit removal for maintenance. These shipping support bolts are approximately eight inches back from the relay front panel. STATIC RELAY EQUIPMENT, WHEN SUPPLIED IN SWING RACK CABINETS, SHOULD BE SECURELY ANCHORED TO THE FLOOR OR TO THE SHIPPING PALLET TO PREVENT THE EQUIPMENT FROM TIPPING OVER WHEN THE SWING RACK IS OPENED.

INSTALLATION TESTS

CAUTION

THE LOGIC SYSTEM SIDE OF THE DC POWER SUPPLY USED WITH MOD III STATIC RELAY EQUIPMENT IS ISOLATED FROM GROUND. IT IS A DESIGN CHARACTERISTIC OF MOST ELECTRONIC INSTRUMENTS THAT ONE OF THE SIGNAL INPUT TERMINALS IS CONNECTED TO THE INSTRUMENT CHASSIS. IF THE INSTRUMENT USED TO TEST THE RELAY EQUIPMENT IS ISOLATED FROM GROUND, ITS CHASSIS MAY HAVE AN ELECTRICAL POTENTIAL WITH RESPECT TO GROUND. THE USE OF CONNECTIONS TO THE EQUIPMENT, SUCH AS A TEST LEAD INADVERTENTLY DROPPING AGAINST THE RELAY CASE, MAY CAUSE DAMAGE TO THE LOGIC CIRCUITRY. NO EXTERNAL TEST EQUIPMENT SHOULD BE LEFT CONNECTED TO THE STATIC RELAYS WHEN THEY ARE IN PROTECTIVE SERVICE, SINCE TEST EQUIPMENT GROUNDING REDUCES THE EFFECTIVENESS OF THE ISOLATION PROVIDED.

CONSTRUCTION

The SLDY51A relay is packaged in an enclosed metal case with hinged front cover and removable top cover. The case is suitable for mounting on a standard 19-inch rack. The outline and mounting dimensions of the case, and the physical location of the components, are shown in Fig. 1 and 3, respectively.

The tap blocks for making the voltage restraint settings are located on the front panel of the unit. The method for making restraint tap settings is illustrated in Fig. 11. The connections are made by means of taper pin connectors; special tools are supplied with each equipment for the removal and insertion of these pin connectors.

The current and potential enter the SLDY51A on twelve-point terminal strips located on the rear of the relay case. The potential connections are made on the YA terminal strip, the current connections on the YB and YC terminal strips.

The basic minimum ohmic tap (T_B) for the relay base reach setting is accomplished on the YB terminal strip. The current connections for the one ohm and three ohm taps were shown previously in Table I.

There are three ten-point cable sockets and one four-point cable socket located on the rear of the case. The four-point cable socket, labeled CP03, is the DC power supply connection to the relay. The cable sockets labeled C011 and C021 are the connection

points for logic signals which must go to a suitable SLA or SLAT relay. The cable socket labeled C041 is for connection to another measuring relay, such as the SLLP, if it is used.

The V_1 and I_1Z test jacks, the I_1Z magnitude reach pot (P5), and the angle pot (P6) for the relay base reach are located on the front of the unit beside the voltage restraint taps. The positive sequence filter potentiometers (P1, P2, P3 and P4) are located inside the relay case as shown in Fig. 3.

The taps for selecting the percentage MB reach in the tripping direction, with respect to the MB (reverse reach) in the blocking direction, are located on the N109 card in position AE.

The independent adjustment (P71) of the polarizing phase shift for each mho characteristic is located on the associated filter card.

The SLDY51A relay also contains printed circuit cards identified by a code number, such as F106, C102, D105, T133, N109, where F designates filter, C designates coincidence, D designates level detector, T designates time-delay, and N designates network. The printed circuit cards plug in from the front of the unit. The sockets are marked with letter designations or "addresses" (D, E, F, etc.) which appear on the guide strips in front of each socket, on the component location diagram, on the internal connection diagram, and on the printed circuit card itself. The test points (TP1, TP2, etc.) shown on the internal connection diagram, are connected to instrument jacks on test cards in position T and AT. TP1 is at the top of the test card in position AT and TP11 is at the top of the test card in position T. The internal connections of the printed circuit cards are shown in the printed circuit card instruction book, GEK-34158.

TP1 on the test card in position AT is connected to relay logic reference, TP2 to the minus 15 volt DC power supply, and TP10 to the plus 15 volt DC power supply. Output signals are measured with respect to the logic reference at TP1. Logic signals are approximately plus 15 volts DC for the ON or LOGIC ONE condition, and less than one volt DC for the OFF or LOGIC ZERO condition. Filter card outputs are alternating signals with respect to the relay logic reference, with a maximum magnitude of plus or minus 15 volts peak.

These outputs can be monitored with an oscilloscope, a portable high impedance DC voltmeter, or the test panel voltmeter if available. When the test panel meter is supplied, it will normally be connected to the reference bus. Placing the relay test lead in the proper test point pin jack will connect the meter for testing. When time-delay cards are to be adjusted or checked, an oscilloscope that can display two traces simultaneously and which has a calibrated horizontal sweep, should be used.

TEST AND ADJUSTMENTS REQUIRED

The SLDY51A relay usually is supplied from the factory mounted and wired as part of a complete static relay equipment. The relay includes the following adjustments, some which have been preset at the factory; others must be set by the user. The factory adjustments should be rechecked by the user per the procedures under DETAILED TESTING INSTRUCTIONS to insure that no shipping damage has occurred.

The steps must be performed in the order shown. Since some of the settings are dependent on other settings, performing the steps out of sequence could lead to an improperly installed relay. Also, following the order given below will minimize the number of changes that have to be made to the test setup to test the entire relay.

Positive sequence voltage network null check (user check)
Voltage level detector, V_1, pickup setting (user setting)
Positive sequence current network null check (user check)
Negative sequence current network null check (user check)
Relay base reach adjustment (user setting)
Individual mho characteristic voltage restraint tap setting (user setting)
MB reach tap setting (user setting)
Individual mho characteristic polarizing phase shift setting (user setting)
Individual characteristic timer settings (user setting)
Individual mho characteristic plotting on the R-X diagram (user check)
Positive sequence overcurrent function settings (user setting)
Zero sequence overcurrent function settings (user setting)
CT phasing, polarity and sequence check (user check)
Channel signal symmetry adjustment (user setting)
Phase delay adjustment (user setting)
Negative seqeunce fault detector settings (user setting).

For a detailed discussion on the actual settings to be made on each of the functions in the SLDY51A relay, refer to the overall logic description for the particular scheme in which the relay is being applied.

Before beginning the installation tests, check for installation of all interconnecting cables between the various relays and associated test equipment which may be supplied. Also check that all terminal board connections are tight.

Be sure that the trip circuits from the associated SLAT relay are open before performing any tests on the relay.

DETAILED TESTING INSTRUCTIONS

Positive Sequence Voltage Network Null Check

The positive sequence voltage network has been adjusted for a null in the factory. It should not require readjustment in the field; however, the network adjustment should be checked to be sure that nothing has been disturbed in transit. Instructions for checking the null adjustment and for making the null adjustment (if necessary) are given below.

A balanced three phase voltage (approximately 120 volts phase to phase) will be applied to the relay. The voltage source should be balanced within one to two percent. If the line voltage from the potential source is within this limit, it may be used for this test.

Apply voltage to the relay using one of the circuits shown in Fig. 12. Use any of the three circuits which will provide voltages balanced within one to two percent.

Set the MB (reverse reach) voltage restraint taps for 100 percent.

Connect an oscilloscope between the V_1 test jack on the front of the SLDY51A relay
* and relay logic reference (TP1). Essentially there should be no 60 (or 50) hertz signal observed at the V_1 test jack. The signal should be all harmonics, primarily third and fifth, and should be less than 0.3 volts peak-to-peak.

If necessary, the null can be improved by adjusting P1 and P2. Refer to Fig. 3 for the location of P1 and P2. First adjust P1 for a minimum signal at the V_1 test jack. Then adjust P2 for a new minimum. Continue to alternately adjust P1 and P2 until the null is achieved. Tighten the locknuts on P1 and P2, being careful not to disturb the settings.

Voltage Level Detector, V_1, Pickup Setting

The positive sequence voltage level detector and its pickup setting are discussed in the overall logic description for the scheme in which the SLDY51A relay is used. To set the pickup level use the test circuit in Fig. 12, which was used to check the positive sequence voltage network. The test connections for the circuits in Fig. 12 were made to simulate pure negative sequence voltage. For this test, reverse the ØB and ØC connections to simulate pure positive sequence voltage.

Adjust the applied voltages to obtain the desired positive sequence voltage, remembering that the applied phase-to-phase voltage is $\sqrt{3}$ times the positive sequence voltage. Adjust P1 on the V_1 level detector card in position AS until it just picks up for the applied voltage. Clockwise adjustment of P1 increases the pickup setting. Raise and lower the applied voltage several times to make sure that the output signal at TP9 steps from less than one volt DC to 12 to 15 volts DC at the desired level.

The dropout time delay of the V_1 level detector is non-adjustable. It can be checked using the test set-up of Fig. 16 and the procedure for checking dropout time delays of the characteristic timers, which will be discussed later. The dropout delay should fall within 25 percent of the value given on the internal connection diagram for the SLDY51A relay in Fig. 2.

Positive Sequence Current Network Null Check

The positive sequence current network has been adjusted for a null in the factory. It should not require readjustment in the field; however, the network adjustment should be checked to be sure that nothing has been disturbed in transit. Instructions for checking the null adjustment and for making the null adjustment (if necessary) are given below using both a three phase test source and a single phase test source. Either method will give satisfactory results.

Single Phase Test Method:

The basic circuit used in checking the network is shown in Fig. 13. This arrangement provides the means of obtaining two test currents of equal magnitude, but separate by 60 degrees. Then by appropriate connections to the network, it is possible to simulate a balanced positive sequence current or negative sequence current. During
* the following tests, the basic current level in each branch will be five amperes (one ampere for one ampere models), and since these currents will add at a 60 degree angle,
* the total load in the variac will be about 8.7 amperes (1.73 amperes for one ampere models). It is desirable that the 110 volt scale of the phase angle

meter be used to minimize the effects of this potential circuit on the relation between the two test currents. It is further desirable that the variac be set to obtain approximately five amperes (or one ampere for one ampere models) as a preliminary step, since this will provide the greatest possible voltage to the phase angle meter and will insure the best possible accuracy.

The sequence current is simulated by setting one branch current to lag an equal current in the second branch by 60 degrees, and then reversing the second branch current at the relay. The first branch current now leads the reversed second branch current by 120 degrees.

The following procedure is suggested:

1. Make the positive sequence hook-up per Fig. 13 and the test connection points shown in the table for the positive sequence network.

2. Note that the phase angle meter is hooked up with current leading voltage, then the meter reading will be 360 degrees relay angle. If the meter is hooked up with voltage leading current, then the meter reading will equal the relay angle.

3. Adjust the branch "2" load box to obtain approximately five amperes (one ampere for one ampere models) when the variac is initially set for 110 volts (this voltage may change during the following adjustment).

4. Adjust the branch "1" load box until the phase angle meter indicates a 60 degree lag of current with respect to voltage.

5. Readjust the branch "2" load box until branches "1" and "2" currents are equal.

6. Adjust the variac until both currents are five amperes (one ampere for one ampere models).

7. Touch up branch "1" load box for angle trimming and branch "2" load box for magnitude trimming.

Connect an oscilloscope between the I_1Z test jack on the front of the SLDY51A relay and relay logic reference (TP1). There should be essentially no 60 hertz (or 50 hertz for 50 hertz, one ampere models) signal observed at the I_1Z test jack. The signal should be essentially all harmonics, primarily third and fifth, and should be less than 0.2 volts, peak-to-peak.

If necessary, the null can be improved by adjusting P3 and P4. Refer to Fig. 3 for the location of P3 and P4. First adjust P3 for a minimum signal at the I_1Z test jack. Then adjust P4 for a new minimum. Continue to alternately adjust P3 and P4 until the null is achieved. Tighten the locknuts on P3 and P4, being careful not to disturb the settings.

Three Phase Test Method:

The circuit for checking the network using a three phase source is shown in Fig. 14. The three ammeters should be calibrated in series to assure that the three test currents are as nearly equal as possible. Make the connections for checking the null of the positive sequence current network. Adjust the three ammeters for 5.0
* amperes (1.0 ampere for one ampere models), and adjust them as nearly equally as possible.

Connect an oscilloscope between the I_1Z test jack on the front of the SLDY51A
* relay and relay logic reference (TP1). There should be essentially no 60 hertz (or 50 hertz) signal observed at the I_1Z test jack. The signal should be essentially all harmonics, primarily third and fifth, and should be less than 0.2 volts, peak-to-peak.

If necessary, the null can be improved by adjusting P3 and P4. Refer to Fig. 3 for the location of P3 and P4. First adjust P3 for a minimum signal at the I_1Z test jack. Then adjust P4 for a new minimum. Continue to alternately adjust P3 and P4 until the null is obtained. Tighten the locknuts on P3 and P4, being careful not to disturb the settings.

If three load boxes or ammeters are not available, the test using a three phase source can be done, using two load boxes and ammeters. Again use the test circuit of Fig. 14, leaving connections H and J open circuited, and omit the ammeter and load box in that branch. This setup produces the two currents similar to the single phase test setup described previously.

For this test method, it is important that the three phase current source is well balanced. Also, this current source must be stiff enough to remain well balanced even with the unbalanced test setup connected to it.

Make the test connections for the two current setup as given in the table associ-
* ated with Fig. 14. The two currents should be adjusted for 5.0 amperes (one ampere for the one ampere models) and be as nearly equal as possible. The null should be checked as described above.

Negative Sequence Current Network Null Check

The negative sequence current network, as designed, is non-adjustable; however, the balance should be checked to make sure that no damage has occurred during transit. Each of the methods described for checking the null of the positive sequence network is also applicable for checking the null of the negative sequence network. Simply observe the proper connections as given in Fig. 13 and 14.

The negative sequence current network has all three phase curents as inputs; therefore, if it is checked using one of the test methods providing two test currents, then it will have to be checked twice to check all three input circuits. The table in each of the figures gives the necessary connections to make the complete check.

The output of the negative sequence current network can be observed by connecting an oscilloscope to TP15 in the SLDY51A relay with reference to relay logic reference at
* TP1. For balanced test currents at 5.0 amperes (1.0 amperes for one ampere models)

within five percent, the output at TP15 should be less than 0.10 volts peak-to-peak with little or no 60 hertz (or 50 hertz) signal. Most of the signal should be third and fifth harmonics.

Relay Base Reach Adjustment

There are three factors involved in establishing the relay base reach: the basic minimum ohmic tap, the angle adjustment and the magnitude adjustment. Make the connections on the YB terminal strip per Table I for the three ohm (15 ohm for one ampere models) basic minimum tap. Use the test circuit of Fig. 15 to adjust the angle and magnitude of the relay base reach. Make the connections as given in the table for Fig. 15. This test setup simulates a single phase to ground fault; therefore, the positive sequence voltage is equal to one-third of the applied voltage (V_{test}) and the positive sequence current is equal to one-third of the applied current (I_{test}). Follow the procedure given below for adjusting the angle and magnitude of the relay base reach. Make sure that the DC power supply voltage is being supplied to the relay for these adjustments.

1. Set the MB (reverse reach) voltage restraint taps for 100 percent.

2. Set the voltage, V_{test}, for 22.5 volts.

3. Set the current, I_{test}, for 7.5 amperes (1.5 amperes for one ampere models).

4. Adjust the phase shifter for the desired relay base reach angle. This angle is set at the factory for 85 degrees. Note that if the phase angle meter is connected with current leading voltage, the meter reading will be 360 degrees minus the desired angle. If the phase angle meter is connected to read voltage leading current, then the desired angle can be read directly.

5. Observe the I_1Z and V_1 voltages at the test jacks on the front of the SLDY51A relay with respect to relay logic reference at TP1. The test jack voltages should be measured with an accurate voltmeter; the phase relationship can be determined by viewing the test jack voltages on an oscilloscope.

6. With the current and voltage set per steps 2, 3 and 4 above, adjust the angle adjustment potentiometer, P6, on the front of the SLDY51A relay, so that the V_1 and I_1Z test jack voltages are exactly in phase. Next, adjust the I_1Z magnitude potentiometer, P5, on the front of the SLDY51A relay so that the V_1 and I_1Z test jack voltages are exactly equal. Since there is some interaction between these adjustments, it may be necessary to alternately adjust the two potentiometers to obtain the equal and in-phase voltages. Tighten the locknuts on P5 and P6, being careful not to disturb their settings.

Once these settings have been made, make the connections to the YB terminal strip per Table I for the basic minimum ohmic tap desired for the application of this relay. For a discussion on which basic minimum ohmic tap to use, refer to the overall logic description for the particular scheme in which the relay is being used.

Individual Mho Characteristic Voltage Restraint Tap Settings

Determine the desired reach for each of the mho characteristics (M1, MT and MB) at the relay base reach angle. Refer to the overall logic description for a discussion on the determination of this reach. Once the reach at the relay base reach angle has been determined and the basic minimum ohmic tap has been selected, then the necessary restraint voltage can be calculated from the equation:

$$T = \frac{T_B}{Z} \times 100$$

where:

T = Voltage restraint tap setting in percent

T_B = Basic minimum ohmic tap setting for the relay base reach

Z = Reach of the mho characteristic at the relay base reach angle.

Make the voltage restraint tap settings as described in the **CONSTRUCTION** section of this book and in Fig. 11. It should be noted that there are two positions available for each tap. These two positions are in common; therefore, either position can be used for any mho function. It is unlikely that the same ten percent tap would be required for all three functions (M1, MT and MB) but it is possible that the same one percent tap is calculated for each function. In such a case, one of the functions (probably MB) would have to be set off by one percent since only two functions can be set for any given tap.

MB Reach Tap Setting

The reach of MB in the tripping direction is a fixed percentage of the reach of MB (reverse reach) in the blocking direction. Refer to the overall logic description for the scheme in which this relay is applied to determine in which tap to place the MB reach. Remove the N109 card from position AE in the SLDY51A relay (make sure the associated SSA power supply is turned off). Place the movable lead in position A, B or C, as determined for the application, and return the card to the AE position, making sure it fits securely. Typically the A, B and C positions have the values of 30, 20 and 10 percent, respectively.

Individual Mho Characteristic Polarizing Phase Shift Setting

The filter card for each mho function has an adjustable phase shift in the polarizing circuit. The choice of setting the phase shift of the polarizing quantity with respect to the operating quantity is covered in the overall logic description. The effects of leading and lagging polarizing phase shift are covered in the OPERATING PRINCIPLES section of this book and are depicted in Fig. 8.

The test circuit and the connections of Fig. 15 can be used for these settings. Use the following procedure:

1. Jumper the I_1Z test jack on the front of the relay to relay logic reference at TP1.

2. Set the voltage, V_{test}, to 120 volts

3. Connect a dual-trace oscilloscope to pins 8 and 9 of the filter card under test.

4. Adjust P71 on the filter card under test for the desired phase shift.

For filter cards like the F106 and F108 (F132 and F133 cards for 50 hertz, one ampere models), the outputs at pins 8 and 9 are exactly in phase for a zero degree phase shift. Turning P71 counterclockwise causes the polarizing voltage (pin 9) to lag the operating voltage (pin 8); turning P71 clockwise casues the polarizing voltage to lead the operating voltage.

* For filter cards like the F123 (F131 card for 50 hertz, one ampere models) the outputs at pins 8 and 9 are exactly 180 degrees out of phase for zero degree phase shift. Also on these cards there is a four-pin plug with two positions, labelled OL and OM. Placing the plug in the OL position produces a leading phase shift, and placing the plug in the OM position produces a lagging phase shift. If a phase shift other than zero degrees is desired, invert one of the channels on the oscilloscope, making the two signals in phase for a zero degree phase shift. Then place the plug in the proper position and adjust P71 for the desired phase shift. Turning P71 clockwise moves the polarizing voltage in the lagging direction.

The phase shift as measured on an oscilloscope is measured in milliseconds. On a 60 hertz basis, the relationship between time and degrees is:

$$t = \frac{\emptyset}{21.6}$$

* and on a 50 hertz basis:

$$t = \frac{\emptyset}{18}$$

where:

$\emptyset$ is the desired polarizing phase shift in degrees

t is the desired polarizing phase shift expressed in milliseconds.

Individual Characteristic Timer Settings

The individual mho characteristic timer setting can be checked and adjusted (where required) using the test circuit in Fig. 16. Refer to the overall logic diagram and overall logic description for the exact values for which the timers should be set. All of these settings should be set.

In order to test the timer cards it is necessary to remove the card which supplies the timer input, and to place the timer card under test in a card adapter. The timer test circuit is shown in Fig. 16. Opening the normally closed contact causes the output to step up to plus 15 volts DC after the pickup delay of the timer. To increase the pickup time, turn the upper potentiometer on the timer card clockwise. Closing the contact causes the timer output to drop out after the reset delay setting of the card. To increase the reset time, turn the lower potentiometer on the card clockwise (on the T133 adjust the middle potentiometer).

The functions having a characteristic timer are given in Table III. This table lists the position of the characteristic timer for each function and the position of the printed circuit card to be removed for each test. Also listed is the typical timer type for each function.

TABLE III

FUNCTION	TIMER POSITION	REMOVE CARD IN POSITION	TYPICAL TIMER TYPE
M1	AK	AJ	T133
MT	AN	AL	T133
MOB	AM	AL	T105
MB	AR	AP & M**	T129
$(I_O-KI_1)T_D$	S	R	T121

** The I_1B level detector in position M must be removed to test the MB timer in order to remove the fast reset input to the MB timer.

Timers like the T121 and T129 are integrating timers. Their pickup delay under normal operation, or when plotting the characteristic, may be slightly different than the setting made following the above procedure. The setting made following the above procedure is known as the "first pulse" pickup delay. The pickup delay in normal operation is known as the "steady state" pickup delay. If the timer is set for the first pulse pickup delay per the procedure given above, it will also have the proper steady state pickup.

The T133 timer is an integrating timer with an adjustable amount of integration. In other words, the steady state pickup delay is adjustable as well as the first pulse pickup delay. This steady state pickup delay is adjusted by the bottom potentiometer on the card when it is inserted in its proper position in the unit. This steady state pickup delay is adjusted while plotting the characteristic.

Individual Mho Characteristic Plotting on the R-X Diagram

After the polarizing phase shift and the characteristic timer have been set, a plot of the characteristic should be made. These plots will confirm that the settings have been made properly. Also, they can be used as a reference for future periodic testing.

If the basic minimum ohmic tap for the relay is connected for three ohms (15 ohms for one ampere models), then the mho characteristic can be plotted using the test circuit and connections of Fig. 15. A test current level of 4 to 7.5 amps (0.8-1.5 amps for one ampere models) should give satisfactory results. For a basic minimum ohmic tap of one ohm (five ohms for one ampere models) the test current would have to be at least 12 amps (2.4 amps for one ampere models) to give a proper plot. This higher current may push the rating of the test equipment as well as the rating of the relay.

Fig. 17 gives a test setup which simulates balanced three phase operation rather than the phase-to-ground operation as in Fig. 15. The applied voltage and applied current of Fig. 17 are equal to the positive sequence voltage and current. Therefore, for the three ohm (15 ohms for one ampere models) basic minimum tap, an applied current of 1.3 amps (0.26 amps for one ampere models) or greater should give satisfactory results. For the one ohm (five ohms for one ampere models) basic minimum tap, an applied current of four amps (0.8 amps for one ampere models) or greater should give satisfactory results. The test circuit of Fig. 17 does require a three phase current source. The phase angle meter as connected in Fig. 17 measures phase current and phase-to-phase voltage; therefore, there is a 30 degree phase shift introduced. If the relay base reach angle is set for 85 degrees, it will appear to be at 55 degrees on the plot on the R-X diagram because of this phase shift. Depending on how well balanced the three phase voltage source and the three phase variac are, it may give better results to measure phase-to-phase voltage rather than phase-to-neutral. If so, the applied voltage will equal $\sqrt{3}$ times the positive sequence voltage.

The procedure for plotting the mho characteristic is essentially the same for either test setup.

1. Set up the test circuit of Fig. 15 or 17.

2. Set the current for a convenient value per the guidelines given above for the particular test setup and basic minimum ohmic tap.

3. Connect an oscilloscope trace to the output of the function under test. (This output is TP3 for M1, TP5 for MT, TP6 for MOB and TP8 for MB.)

4. Set the phase angle for the relay base reach angle by adjusting the phase shifter. Lower the applied voltage from maximum value to the point where the function fully picks up. (The signal steps from a level less than one volt DC to a level from 12 to 15 volts DC.) Record the voltage and angle.

5. Adjust the phase shifter in either direction from the relay base reach angle and record the voltage at which the mho function picks up for various angles until the characteristic is clearly defined.

For a circular characteristic, the voltage required for pickup at any angle can be calculated from the following expression:

$$V = \frac{I\ T_B Z \cos(\alpha - \beta)}{T} \times 100$$

where:

V = Applied voltage (V_{test}) in Fig. 15 or 17 (if phase-to-phase voltage is measured for the test setup in Fig. 17, then the calculated V must be multiplied by the $\sqrt{3}$).

I = Applied current (I_{test}) in Fig. 15 or 17.

T_B = Basic minimum ohmic tap for the relay base reach.

T = Voltage restraint setting in percent.

α = Mho characteristic angle of maximum reach.

β = Test angle

Z = Ratio of the maximum reach of the characteristic under test to the relay base reach.

The mho characteristic angle of maximum reach (α) can be determined by the following expression for the test setup of Fig. 15.

$$\alpha = \text{Relay base reach angle} + \phi$$

where:

ϕ = Polarizing phase shift.

For the test setup of Fig. 17, the angle α can be determined by the following expression:

$$\alpha = \text{Relay base reach angle} + \phi + 30^{o}$$

where:

ϕ = Polarizing phase shift

30^{o} = Phase shift caused by the manner in which the phase angle meter is connected in Fig. 17.

The ratio (Z) of the maximum reach of the characteristic under test to the relay base reach for the test setup of Fig. 15 can be determined by the following expression:

$$Z = \frac{1}{\cos \phi}$$

where:

$\emptyset$ = Polarizing phase shift

The ratio (Z) for the test setup of Fig. 17 can be determined by the following expression:

$$Z = \frac{1}{\cos(\emptyset + 30^{o})}$$

where:

$\emptyset$ = Polarizing phase shift

30^{o} = Phase shift caused by the connections to the phase angle meter

For a characteristic that is non-circular, it is best to construct the characteristic following the procedure given in the OPERATING PRINCIPLES section of this book. This constructed characteristic can be used as a reference to which the actual test data can be compared. If the test circuit of Fig. 17 is used to plot the characteristic, then a plus 30 degree phase shift must be added to the actual polarizing phase shift for the constructed characteristic.

There are certain symptoms of improper settings that occur when comparing the plotted characteristic to the constructed characteristic. These symptoms are listed below.

1. If the reach of the characteristic at the relay base reach angle is incorrect, or if the relay base reach angle itself is off, then recheck the magnitude and angle adjustments of the relay base reach.

2. If one lobe of the characteristic is "blown out" and the other lobe is "pulled-in," then the polarizing phase shift should be rechecked.

3. If both lobes of the characteristic are "blown out" or "pulled in," then the pickup delay setting of the characteristic timer should be rechecked. A clockwise adjustment of the potentiometer increases the pickup delay and pulls in both lobes of the characteristic.

If the T133 card is used as the characteristic timer, then the adjustable integration potentiometer (bottom potentiometer on the card) is used to determine the shape of the characteristic. Set the first pulse pickup delay. Dropout delay is described earlier in the section, "Individual Characteristic Timer Settings." For an approximate setting of the adjustable integration potentiometer, set the applied voltage and phase angle of the test setup of Fig. 15 or 17 for input pulses into the T133 card (pin 3). The width of these pulses should equal the desired steady-state pickup delay. Set the bottom potentiometer on the T133 card so that it just picks up for these input pulses. Then plot the characteristic and make any touch-up adjustment necessary to the bottom potentiometer to obtain the correct shape.

The test circuit of Fig. 17 simulates three phase operation; therefore, a complete check of all input circuits is made plotting one characteristic. The test circuit and connections of Fig. 15 simulate a phase B-to-ground operation. If it is desired to check the other two phases, it can be done using the test setup of Fig. 15 and the test connections given in Table IV. Use the connections for the three ohm or one ohm base tap according to the actual relay settings. Each of the three plotted characteristics should fall within five percent of the constructed characteristic.

TABLE IV

TEST	BASIC MINIMUM OHMIC TAP		TEST CONNECTIONS					
	5 AMPS	1 AMP	A	B	C	D	E	F
ØA-G	3 OHMS	15 OHMS	YA2	YA3, YA4	YB10	YB12	F	E
ØA-G	1 OHM	5 OHMS	YA2	YA3, YA4	YB9	YB11	F	E
ØC-G	3 OHMS	15 OHMS	YA4	YA2, YA3	YB6	YB8	YB10	YB12
ØC-G	1 OHM	5 OHMS	YA4	YA2, YA3	YB6	YB7	YB9	YB11

Positive Sequence Overcurrent Function Settings

The positive sequence overcurrent functions can be set using the current circuit portion of Fig. 15 or 17. Remove the phase angle meter to avoid damage to the meter at higher current levels. For the circuit of Fig. 15, the desired positive sequence current is one-third of the applied current. For the circuit of Fig. 17, the desired positive sequence current is equal to the applied current. Connect the test circuit for the three ohm or one ohm (15 ohms or five ohms for one ampere models) minimum base tap according to which relay base reach angle is chosen for this application.

Adjust the applied test current to give the desired positive sequence current pickup level. Observe the output of the function under test and adjust the potentiometer on the level detector to obtain the desired pickup level. A clockwise adjustment of the potentiometer increases the pickup level. Raise and lower the applied current several times to make sure that the output steps from less than one volt DC to 12 to 15 volts DC at the desired level of applied current.

Table V lists the positive sequence overcurrent functions. The table also gives the card position of the level detector and the test point at which the output of the given function can be observed.

TABLE V

FUNCTION	CARD POSITION	OUTPUT
I_1B	M	TP14
I_1T	P	TP12
I_1T_D	N	TP13

* The long term current rating of the relay is five amps (one ampere for one ampere models). Currents larger than this rating should be applied to the relay for as short a period of time as possible. When applying a large current to the relay, place a jumper across the relay terminals. Energize the test circuit and adjust the applied current to obtain the desired positive sequence current with the relay shorted out. De-energize the test circuit, remove the jumper from the relay terminals, and then re-energize the test circuit, applying the pre-set current level to the relay and making the setting as quickly as possible.

The dropout time delays of the positive sequence overcurrent functions are non-adjustable. If desired, they can be checked using the test circuit of Fig. 16 and the same procedure as for checking the dropout time delays of the characteristic timers. The dropout delay should fall within 25 percent of the value given for each function on the internal connection diagram in Fig. 2.

Zero Sequence Overcurrent Function Settings

There are two functions available in the SLDY51A relay that operate on zero sequence current. The G4 function operates on zero sequence current only. The $(I_0-KI_1)T_D$ function operates on zero sequence current and is restrainted by K amount of positive sequence current. Only one of the two functions can exist in any given relay. Both functions can be set using the current circuit of Fig. 15. Use the connections for
* the three or one ohm tap (15 or five ohm tap for one ampere models) according to the application for this relay. Refer to the overall logic description for a discussion on the desired settings for these functions.

G4 Function:

The G4 function can be set using exactly the same procedure as is used to set the positive sequence overcurrent functions. In this situation, since the applied current is equal to $3I_0$ and since the function operates on $3I_0$, the function is set for the actual value of the applied current.

Adjust the applied current for the desired pickup level and follow the procedure given for the positive sequence overcurrent functions. The G4 level detector is in position R and the output can be observed at TP11.

$(I_0-KI_1)T_D$ Function:

The $(I_0-KI_1)T_D$ function is set in two steps - the setting of the characteristic timer in position S is covered in this section under "Individual Characteristic Timer Settings." Before setting the current pickup level, place the card from position R (usually an F114 card) in a card adapter and jumper pin 6 to pin 1. Then adjust the $3I_0$ operating level by adjusting potentiometer P2 on the card in position R and observing the output at TP11. Use the same procedure as for setting the positive sequence overcurrent function, remembering that the applied test current will be exactly equal to the $3I_0$ operating current. Adjusting P2 clockwise increases the pickup setting.

Remove the jumper from pin 6 to pin 1 and increase the applied test current to a value given by the equation:

$$I_{test} = \frac{3I_0 \text{ Pickup Setting}}{1-K}$$

where the $3I_0$ pickup setting is the setting just made with pin 6 jumpered to pin 1 and K is the desired restraint factor. Adjust potentiometer P1 on the card in position R so that the function just picks up for the new value of test current. Adjusting P1 clockwise increases the setting of K.

CT, Phasing, Polarity and Sequence Check

The following tests on CT phasing, polarity and sequence are desirable to assure proper coordination for phase comparison between terminals. These tests are easily made using the pilot channel to communicate phase angle information between terminals. Before making these checks, the pilot channel must be properly installed and adjusted for in-service conditions.

The CT phasing, polarity and sequence checks provide a means of checking that for the phase sequence A-B-C, phase A CT is connected to the YC1-YC4 winding of the three phase auxiliary current transformer with the same polarity at both terminals; that phase B CT is similarly connected to YC5-YC8, and that phase C CT is similarly connected to YC9-YC12.

In order to make the test, it is necessary that load current be flowing in the line. The magnitude of the load current should be at least five times the single-end feed line charging current to assure readable through-fault current relationships. If charging current is too high relative to load current, the phase difference between currents at the two ends will make it difficult to correctly interpret the results of the following tests. In the following tests, load current in each phase is used independently to simulate a corresponding line-to-ground fault.

Since the pilot channel is used in this test, it is necessary that the simulated phase-to-ground fault current be above the FDL level detector operating point. The associated SLA or SLAT relay must be energized so that the FDL and SQ AMP in the SLDY51A will key the transmitter to send trip and block signals on alternate half-cycles. The
* FDL level detector was set in the factory for 0.2 amps (0.04 amps for one ampere models)
* negative sequence. The SQ AMP was set for 7.0 milliseconds (9.0 milliseconds for 50 hertz, one ampere models) output block width at 0.2 amps (or 0.04 amps) negative

sequence. A test current of at least 0.3 amps (0.06 amps for one ampere models) negative sequence should be used.

For a simulated phase-to-ground fault, the negative sequence component is one-third of the line current. Therefore, it is necessary that the secondary load current be at least 0.9 amps (0.18 amps for one ampere models). If the load current exceeds this value, FDL will operate and the SQ AMP will have a nearly symmetrical output. Observe the output of FDL at TP17 in the SLDY51A to be sure that it is picked up for the input test current. Observe the output on the SQ AMP in TP16 in the SLDY51A relay. Check that its output is nearly symmetrical for the input test current.

It may be necessary to temporarily readjust the setting of the SQ AMP sensitivity to improve the symmetry of its output signal. A clockwise adjustment of the potentiometer on the SQ AMP card in position G in the SLDY51A relay will decrease its output block width. Adjust the potentiometer as necessary to achieve an output signal with on time and off time as nearly equal as possible for the given input test current.

Temporarily increase the FDHH and FDHL pickup level by adjusting the upper potentiometer on the amplifier card in position D in the SLDY51A relay fully clockwise. This will avoid getting a trip signal for this test condition which would result in the transmission of a continuous trip signal on the pilot channel.

To simulate a phase-A-to-ground fault, connect the input current circuits so that phase A current flows through the relay, but phase B and C currents bypass the relay. To simulate a phase-B-to-ground fault, connect phase B current to flow through the relay, but phase A and C currents to bypass the relay. To simulate a phase-C-to-ground fault, connect phase C current to flow through the relay but phase A and B currents to bypass the relay. For each phase check, the same test setup must be used at each terminal.

Using a dual-trace oscilloscope, observe the output of the local SQ AMP on one trace. This output can be observed at TP16 on the SLDY51A relay or at an equivalent test point in the associated SLA or SLAT relay. Be sure to observe the local SQ AMP signal prior to its passing through any timers or logic which would supervise it by any signal other than FDL. On the second trace of the oscilloscope, observe the received channel signal in the SLA or SLAT. Be sure to observe the received signal prior to its passing through any timers or logic which would supervise the signal with some other signal.

Compare the local SQ AMP signal trip attempt, which is the positive going half-cycle, with the received blocking half-cycle. Refer to the overall logic description and the overall logic diagram to determine whether the received signal is positive or zero for the blocking half-cycle at the chosen test point. The local trip half-cycle should lead the received block half-cycle by less than eight milliseconds. Typically, the local trip half-cycle should lead the received block half-cycle by an amount of time equal to the channel response time plus the propagation time of the line. However, because of a lack of symmetry in the channel and because of the amount of charging current relative to load current, this will not be very accurate. Compare the leading edges of both signals and the trailing edges of both signals. The channel response time can usually be determined from the channel equipment instruction book. The propagation time delay of the line is approximately one millisecond for 186 miles or 300 kilometers.

Compare the local trip signal with the received blocking signal for all three phases. The results for all three phases should be similar. If the three results are not similar or if the local trip signal leads the received blocking signal by more than eight milliseconds, then there is probably a connection error somewhere in the CT circuits.

With CT phasing and polarity established, check that the phase sequence is correct by properly connecting three phase load current to the relay. Check the signal at the output of the negative sequence current mixing network at TP15 in the SLDY51A relay. If the phase sequence is correct, the signal at TP15 will be similar to the null signal observed when the network balance was checked. If the phase sequence is incorrect, a * much larger 60 (or 50) hertz signal will be observed at TP15.

Channel Signal Symmetry Adjustment

The adjustment of the channel signal symmetry refines the duration of the block and trip half-cycles of the channel signal. This adjustment compensates for asymmetry in the channel signal which may be caused by the receiver tuned filters. Since this adjustment depends on operating conditions in service, it cannot be made at the factory. Before this adjustment is made, it is essential that the channel receiver and transmitter be adjusted as prescribed in the INSTALLATION ADJUSTMENT section of the channel set instruction book. The actual channel symmetry adjustment is made in the associated SLA or SLAT relay of a complete phase comparison scheme. The procedure is given here because it is necessary to energize the SLDY51A to make the adjustment.

Assume that the protected line is A to B, with A being the local terminal and B the remote terminal. At station B, connect an oscilloscope to observe the received channel signal in the SLA or SLAT relay. Supply the SLDY51A at A with a single phase test current. Use the current circuit portion of Fig. 15 and the single-phase-to-ground test connections of Table VI. The FDL level detector was set in the factory for 0.2 * amps (0.04 amps for one ampere models) negative sequence. The SQ AMP was set for a 7.0 * millisecond (9.0 millisecond for 50 hertz, one ampere models) output block width at the * same current level. A test current of at least 0.3 amps (0.06 amps for one ampere models) negative sequence should be used. Therefore, the applied test current should * be a minimum of 0.9 amps (0.18 amps for one ampere models).

TABLE VI

TYPE OF CONNECTIONS	TEST CONNECTIONS				$\frac{I_{test}}{I_2}$
	C	D	E	F	
Ø-G	YC1	YC4	F	E	3
Ø-Ø	YC1	YC4	YC8	YC5	$\sqrt{3}$

Observe the output of the SQ AMP at TP16 in the SLDY51A relay. Check that its output is nearly symmetrical for the input test current. It may be necessary to

temporarily readjust the setting of the SQ AMP sensitivity to improve the symmetry of its output signal. A clockwise adjustment of the potentiometer on the SQ AMP card in position G in the SLDY51A relay will decrease its output block width. Adjust the potentiometer as necessary to achieve an output signal with on time and off time as nearly equal as possible for the given input test current.

Temporarily increase the FDHH and FDHL pickup level by adjusting the upper potentiometer on the amplifier card in position D in the SLDY51A relay fully clockwise. This will avoid getting a trip signal for this test condition which would result in the transmission of a continuous trip signal on the pilot channel.

At station B, set the oscilloscope horizontal sweep such that one full cycle of the received signal can be observed. Note the duration of the block and the trip half-cycles. Adjust the pickup and/or the dropout time delay of the symmetry adjustment timer to make the duration of the block and the trip half-cycles as nearly equal as possible. The frequency of this signal should be 60 (or 50) hertz. In many cases this symmetry adjustment timer will be located in the received signal logic in the SLA or SLAT relay at B. In some cases, this symmetry adjustment timer may be located in the keying signal logic of the SLA or SLAT relay at A. In either case, the received signal must be symmetrical. Refer to the instruction book for the associated SLA or SLAT relay or to the overall logic description for more specific information which may be required about this timer.

Observe the input and the output of the symmetry adjustment timer. Note the difference between the leading edge of the input signal and the output signal. Also note the difference between the trailing edge of the input signal and the output signal. This information can be used as a reference for future periodic testing.

The received channel signal at station A must also be adjusted by symmetry between the block and the trip half-cycle. This should be done in the same manner as just described.

Phase Delay Adjustment

The object of the phase delay adjustment is to set the local trip half-cycle at A to be in phase with the received block half-cycle from B. This condition results from a through fault. This adjustment is necessary to compensate for things such as channel delay introduced by the receiver filters and propagation time of the line. Since the phase delay is affected by service conditions, it cannot be made at the factory. The actual phase delay adjustment is made in the associated SLA or SLAT relay of a complete scheme. The procedure for the adjustment is contained here because it is necessary to energize the SLDY51A to make the adjustment.

Three possible methods of making the phase delay adjustment are given below with the limiting conditions of each given.

Load Current Method:

In this test, load current in the line is used to simulate negative sequence current. It is necessary that the secondary load current be greater than the negative sequence current setting of the FDL and FDHH fault detectors. If this method is to produce an accurate setting, it is also necessary that the ratio of line charging

current to through-load-current be low enough so that the phase displacement between currents at the two ends of the line does not exceed ten degrees.

If these conditions are met, the procedure outlined below should be followed. If the conditions are not met, it will be necessary to use one of the alternate schemes.

At each terminal connect the system load current to the relay; however, reverse the phase B and C connections. In other words, connect phase A current to go in YC1 and out YC4, connect phase B current to go in YC9 and out YC12 and connect phase C current to go in YC5 and out YC8. This will make the balanced load current look like negative sequence current. This current must be greater than the negative sequence current * pickup level of FDL and FDHH. FDL is set at the factory for 0.2 amps (0.04 amps for one * ampere models) negative sequence. The minimum pickup level of FDHH is 0.25 amps (0.05 amps for one ampere models) negative sequence.

Temporarily reduce the pickup level of FDHH to its minimum by adjusting the top potentiometer on the card in position D fully counterclockwise. Observe the outputs of FDL and FDHH at TP17 and TP18 in the SLDY51A relay to make sure that both functions have operated for the input current level available. Observe the output of the SQ AMP at TP16 to be sure that its output is symmetrical. If necessary, adjust the potentiometer on the card in position G to make the trip half-cycle and block half-cycle as nearly equal as possible. A clockwise adjustment of the potentiometer decreases the output signal block width.

At station A (local), a continuous blocking signal must be applied to the channel control logic in the SLA or SLAT relay to prevent the local transmission of a trip signal. At station B (remote), a trip output must be prevented from transmitting a continuous trip signal from that end. Before applying test signals to, or removing cards from the logic circuitry, be sure to refer to the instruction book for the particular SLA or SLAT relay, and the MOD III printed circuit card instruction book, GEK-34158, for the proper precautions and limitations.

Using a dual-trace oscilloscope at A, connect one trace to the received signal from B (after the symmetry adjustment timer), and the other to the output of the phase delay timer at A. The received signal from B will be a symmetrical square wave with equal block and trip half-cycles. The output signal from the phase delay timer will also be nearly symmetrical. However, the trip half-cycle of the local signal will probably lead the block half-cycle of the remote signal by a few milliseconds. Adjust the pickup delay and the dropout delay of the phase delay timer so that the local trip half-cycle is exactly in phase with the received block half-cycle, and so that the local block half-cycle is exactly in phase with the received trip half-cycle.

When these adjustments are complete, do not readjust the phase delay timer. Place one oscilloscope trace on the input to the phase delay timer, and the other trace on the output. Note the time delay between the leading edge of the input signal and the output signal. Also note the time delay between the trailing edge of the input signal and the output signal. These time delays can be used as a reference for future periodic testing.

Adjust the phase delay timer at B in a similar manner, and then return the relay connections to their proper locations. Go on to set the pickup levels of the negative sequence fault detectors.

Test Source Method:

If the line is not loaded, is carrying insufficient load, or if the ratio of charging current to load current is too high, an AC test source can be used at each station to operate FDL, FDHH and the SQ AMP provided the sources are in phase. Use the current portion of the test circuit of Fig. 15 and the phase-to-phase connections of Table VI. Use the connections exactly as they appear in Table VI at terminal A (local), but reverse the C and F connections at terminal B (remote) to simulate a through-fault condition. In other words, at A (local) connect C to YC1 and F to YC5, while jumpering YC4 to YC8. At B (remote) connect C to YC5 and F to YC1 while jumpering YC4 to YC8.

Before proceeding with phase delay adjustments, the phase relation of the two test sources should be checked to insure that the two sources are in phase. If an on-off type channel equipment is being used, the check of the phase relationship between the two sources is fairly simple. With the test connections as given in the preceding paragraph, raise the applied test current to pick up FDL at TP17 in the SLDY51A relay and to give a symmetrical SQ AMP output at TP16. FDL is set in the factory for 0.2 amps (0.04 amps for one ampere models) negative sequence current. It may be necessary to temporarily readjust the sensitivity of the SQ AMP by adjusting the potentiometer on the card in position G in order to obtain trip and block half-cycles as nearly equal as possible. A clockwise adjustment of the potentiometer decreases the width of the trip half-cycle. Also temporarily increase the pickup of FDHH to its maximum level by adjusting the top potentiometer on the card in position D fully clockwise. Before making the actual phase delay setting, it will be necessary to return the pickup of FDHH to its minimum level.

At the local terminal, connect the traces of the oscilloscope to observe the transmitted and received RF signals. For some channel equipment, these two signals can be seen at the same point. Most likely the transmitted signal will be larger in magnitude than the received signal. The blocks of RF, both transmitted and received, should be a half-cycle in duration on a 60 (or 50) hertz basis. Also the two blocks of RF should be within ten degrees of being exactly 180 degrees out of phase.

If a frequency shift type of channel equipment is used, there is no simple way of checking the phasing of the two test sources. The AC source for the test circuit of Fig. 15 is usually station service. Usually on long line applications test sources are displaced by too great an angle to be of any use for the installation adjustment of the phase delay timer.

An alternative would be to use the system potential source as a test source. If at least one of the stations of the protected line is equipped with line-side potential devices or transformers, it is possible that substantially in-phase test sources can be obtained at the two ends by supplying the test circuit of Fig. 15 from the potential device or transformer, and operating the line with the breaker open at one end. The open end is, of course, the location where line-side potential is available. With this arrangement, the voltages at the two ends will differ only by the drop in the line inductive reactance caused by the line capacitive charging current, and this will primarily be a magnitude difference. It is, of course, essential that the normal installation adjustments be made on the potential devices prior to this test.

Having obtained AC test sources that are substantially in phase, proceed to adjust the phase delay settings as described in "Load Current Method." Be sure to return FDHH to its minimum pickup level by adjusting the top potentiometer on the card in position D fully counterclockwise.

Local Signal Method:

If neither of the above adjustment methods can be used, an adjustment of the phase delay timer can be made on the basis of the local keyed-carrier signal. This method assumes that an on-off type power line carrier is used. It also assumes that the carrier receiver gain control and attenuator have been temporarily reset to provide the "normal margin" above the cutoff point of the received signal caused by local transmission rather than remote transmission. The recommended "normal margin" is given in the carrier equipment instruction book, in the section on installation adjustments.

First, cause the local transmitter to send a full-strength RF signal. Observe and record where received attenuator is set, and then turn the receiver attenuator in a counterclockwise direction until the cutoff point is reached. Now turn the attenuator back to provide the normal margin (as noted previously) from this cutoff point, as determined by the attenuator dial markings. Presumably, at this attenuator setting the local transmitter will drive the local receiver at approximately the same level as the RF signal received from the remote terminal would drive it, with the installation settings of the transmitter and receiver.

The test circuit of Fig. 15 will be used with the phase-to-phase connections of Table VI. Apply a test current which will cause FDL and FDHH to operate producing output signals at TP17 and TP18. FDL has been set at the factory for a pickup level of * 0.2 amps (0.04 amps for one ampere models) negative sequence. Temporarily reduce the pickup of FDHH to its minimum level by adjusting the top potentiometer on the card in position D fully counterclockwise. Observe the output of the SQ AMP at TP16. This signal should be as nearly symmetrical as possible for this test. It may be necessary to temporarily readjust the sensitivity of the SQ AMP by adjusting the potentiometer on the card in position G to obtain a symmetrical output square wave. A clockwise adjustment of the potentiometer decreases the output block width.

Using a dual-trace oscilloscope, connect one scope input to the RF jack on the carrier set and connect the other scope input to the received carrier signal. Connect scope reference to relay logic reference. The received carrier signal should be very close to equal block time and equal trip time, since these conditions are very close to those for which the symmetry adjustment was made. Now shift the scope input which was monitoring the RF to the output of the phase delay timer. Adjust the pickup and dropout delay of the phase delay timer, so that the trip output from the phase delay timer is exactly in phase with the received trip signal, and that the block output from the phase delay timer is exactly in phase with the received block signal.

This adjustment neglects propagation time of the carrier signal between the two terminals. This propagation time is one millisecond for 186 miles or 300 kilometers of line. The phase delay setting can be further refined for long lines by calculating the thereotical propagation time for the line, and shifting the trip signal to the right (delaying) by a time equivalent to this propagation time.

When these adjustments are complete, do not readjust the phase delay timer. Place one oscilloscope trace on the input to the phase delay timer and the other trace on the output. Note the time delay between the leading edge of the input signal and the output signal. Also note the time delay between the trailing edge of the input signal and the output signal. These time delays can be used as a reference for future periodic testing.

Adjust the phase delay timer at B in a similar manner and then return the relay connections to their proper location. Reset the receiver attenuator to its regular installation position as recorded at the beginning of this test. Go on to set the pickup levels of the negative sequence fault detectors.

Negative Sequence Fault Detector Settings

The negative sequence fault detectors can be set by using the current circuit portion of the test setup of Fig. 15. Be sure to remove the phase angle meter from the setup. The fault detectors are set in terms of negative sequence current. For the test setup of Fig. 15, the applied test current is equal to three times the actual negative sequence current for a phase-to-ground connection. For a phase-to-phase connection the applied test current is equal to $\sqrt{3}$ times the actual negative sequence current. The connections to the relay for phase-to-ground or phase-to-phase operation are given in Table VI. The procedure for setting the fault detectors is the same for either set of connections.

FDL Fault Detector:

The FDL fault detector has been set in the factory for 0.2 amps (0.04 amps for one ampere models) negative sequence. Adjust the input test current to produce 0.2 (or 0.04) amps negative sequence. Observe the output of the adjustable amplifier for FDL at pin 8 on the card in position B. For 0.2 (or 0.04) amps negative sequence current, this output signal should be 0.15 to 0.18 volts, and the FDL level detector card should pick up, producing an output signal at TP17. If the output signal of the amplifier is not in the proper range, adjust the adjustable amplifier for FDL by adjusting the potentiometer on the card in position B. A clockwise adjustment will decrease the signal level. If the FDL level detector card does not operate for this signal level, adjust the potentiometer on the card in position H. A clockwise adjustment will increase the pickup setting. Once this setting has been made, do not readjust the potentiometer on the card in position H. This adjustment assures the proper filter characteristic for the FDL function.

Adjust the input test current to produce the desired FDL negative sequence current pickup level. By adjusting the potentiometer on the card in position B, set the adjustable amplifier for FDL so that the function just picks up for the given input current. A clockwise adjustment of the potentiometer increases the pickup setting. Raise and lower the input current several times to make sure that the FDL output at TP17 operates at the desired level.

The dropout time delay of the FDL level detector is non-adjustable. It can be checked using the test circuit of Fig. 16 and the same procedure as for checking the dropout time delay of the characteristic timers. The dropout time delay should fall within 25 percent of the value given for FDL on the internal connection diagram for the SLDY51A relay in Fig. 2.

Squaring Amplifier:

The squaring amplifier function can only be set after FDL has been properly set. Using the same test setup as for setting FDL, adjust the input test current to the level that just produces FDL pickup. Observe the output of SQ AMP at TP16, and adjust the * potentiometer on the card in position G for a six to seven millisecond (eight to nine millisecond for 50 hertz, one ampere models) output block width. A clockwise adjustment of the potentiometer decreases the output block width.

FDHH Fault Detector:

Setting the FDHH fault detector requires a procedure very similar to that for * setting FDL. Adjust the input test current to produce 0.25 amps (0.05 amps for 50 hertz, one ampere models) negative sequence. Observe the output of the adjustable amplifier for FDHH at pin 8 on the card in position D. Also observe FDHH output at * TP18. For 0.25 (or 0.05) amps negative sequence, set the adjustable amplifier for FDHH by adjusting the top potentiometer on the card in position D for an output signal of 0.20 to 0.29 volts. A clockwise adjustment of the potentiometer decreases the input signal. Check that the FDHH output picks up for this signal level. If it does not, adjust the potentiometer on the FDHH level detector card in position J so that it just operates for the given signal. Once this setting has been made, do not readjust the potentiometer on the card in position J. This adjustment assures the proper filter characteristic for the FDHH function.

Adjust the input test current to produce the desired FDHH negative sequence current pickup level. Set the adjustable amplifier for FDHH by adjusting the top potentiometer on the card in position D, so that the function just picks up for the given input current. A clockwise adjustment of the potentiometer increases the pickup setting. Raise and lower the input current several times to make sure that the FDHH output at TP18 operates at the desired level.

The dropout time delay of the FDHH level detector is non-adjustable. It can be checked using the test circuit of Fig. 16 and the same procedure as for checking the dropout time delay of the characteristic timers. The dropout time delay should fall within 25 percent of the value given for FDHH on the internal connection diagram for the SLDY51A relay in Fig. 2.

FDHL Fault Detector:

The FDHL fault detector can only be set after FDHH has been properly set. Using the same test setup as for setting FDHH, adjust the input test current to produce the desired FDHL negative sequence current pickup level. Observe the FDHL output at TP19 and adjust the potentiometer on the FDHL level detector card in position K so that FDHL just picks up for the desired input current. A clockwise adjustment of the potentiometer increases the pickup setting. Raise and lower the input current several times to be sure that FDHL operates at the desired level.

The dropout time delay of the FDHL level detector is non-adjustable. It can be checked using the test circuit of Fig. 16 and the same procedure as for checking the dropout time delay of the characteristic timers. The dropout time delay should fall within 25 percent of the value given for FDHL on the internal connection diagram for the SLDY51A relay in Fig. 2.

I_2T_D Fault Detector:

Setting the I_2T_D fault detector requires a procedure very similar to that for setting FDL. Adjust the input test current to produce two amps (0.4 amps for 50 hertz, one ampere models) negative sequence. Observe the output of the adjustable amplifier for I_2T_D at pin 9 on the card in position D. Also observe I_2T_D output at TP20. For two (or 0.4) amps negative sequence, set the adjustable amplifier for I_2T_D by adjusting the bottom potentiometer on the card in position D for an output signal of 0.29 to 0.36 volts. A clockwise adjustment of the potentiometer decreases the signal. Check that the I_2T_D output picks up for this signal level. If it does not, adjust the potentiometer on the I_2T_D level detector card in position L so that it just operates for the given signal. Once this setting has been made, do not readjust the potentiometer on the card in position L. This adjustment assures the proper filter characteristic for the I_2T_D function.

Adjust the input test current to produce the desired I_2T_D negative sequence current pickup level. Set the adjustable amplifier for I_2T_D by adjusting the top potentiometer on the card in position D, so that the function just picks up for the given input current. A clockwise adjustment of the potentiometer increases the pickup setting. Raise and lower the input current several times to make sure that the I_2T_D output at TP20 operates at the desired level.

The dropout time delay of the I_2T_D level detector is non-adjustable. It can be checked using the test circuit of Fig. 16 and the same procedure as for checking the dropout time delay of the characteristic timers. The dropout time delay should fall within 25 percent of the value given for I_2T_D on the internal connection diagram for the SLDY51A relay in Fig. 2.

PERIODIC CHECKS AND ROUTINE MAINTENANCE

PERIODIC TESTS

All functions included in the SLDY51A relay may be checked at periodic intervals using the procedures described in the section, DETAILED TESTING INSTRUCTIONS. Cable connections between the SLDY51A relay and the associated Type SLA relay can be checked by observing the SLDY51A outputs at test points in the SLA relay.

The following checks should be performed as part of a periodic testing and maintenance program:

Voltage level detector, V_1, pickup setting
Individual mho characteristic plotting on the R-X diagram
Positive sequence overcurrent function settings
Zero sequence overcurrent function settings
Negative sequence fault detector settings

A comparison of the data taken during periodic checks with data taken during installation will show if the relay is in good calibration. The periodic checks need not be as involved as the detailed checks described previously.

Voltage Level Detector, V_1, Pickup Setting

The setting of the V_1 voltage level detector should be checked using the same procedure that was used to set it originally. Refer to "Voltage Level Detector, V_1, Pickup Setting," of the DETAILED TESTING INSTRUCTIONS. The pickup setting should be within plus or minus ten percent of the original setting. If not, check both the balance of the positive sequence voltage network and the operation of the V_1 voltage level detector before making any changes.

Individual Mho Characteristic Plotting on the R-X Diagram

For instructions on plotting the individual mho characteristics, refer to "Individual Mho Characteristic Plotting on the R-X Diagram," in the DETAILED TESTING INSTRUCTIONS. The entire characteristic may be plotted or the pickup at three or four specific angles can be measured as a check of the characteristic.

Any errors in the positive sequence voltage or positive sequence current network nulls, or in the relay base reach settings, angle of maximum reach, polarizing phase shift, or characteristic timer settings, will be apparent when the data from the periodic checks is compared with the data taken during the original installation. If necessary, any or all of the individual settings can be checked using the procedures given in the DETAILED TESTING INSTRUCTIONS.

An alternative method of plotting the mho characteristic is to use the distance relay portable test equipment. The test setup for this equipment is in Fig. 18. For complete instructions on testing with the portable test equipment, refer to GET-3474, "Testing Distance Relays with Portable Test Equipment."

The test box setting for a circular characteristic can be calculated by the following equation:

$$\text{Calculated Test Box Setting} = \frac{K\, Z_1 \cos(\alpha - \beta)}{Z_L}$$

where:

Z_1 = mho characteristic reach at relay base reach angle

$$Z_1 = \frac{T_B}{T} \times 100$$

T_B = basic minimum ohmic tap setting of the relay

T = voltage restraint tap setting of the particular mho function

Z_L = reactor-resistor impedance in ohms (must be greater than the numerator)

α = mho characteristic angle of maximum reach

β = angle of Z_L

K = ratio of the maximum reach of the characteristic under test to the relay base reach.

For a non-circular characteristic, the reach of the function can be determined by measurement of the plot of the characteristic which was made during the installation testing. In this case, the test box setting can be calculated by means of the following equation:

$$\text{Calculated Test Box Setting} = \frac{Z_M}{Z_L}$$

where:

Z_L = reactor-resistor impedance in ohms

Z_M = reach of function measured at the angle of Z_L

The MT and M1 functions may be checked at three angles: 30, 60 and 86 degrees. The 86-degree angle is obtained by using the reactor without the resistor. This angle closely approximates the typical relay base reach angle. The MB, in addition to the angles above, may be checked at 240 degrees.

The test procdure is outlined below:

1. Use the test setup of Fig. 18 and its Test I connections. Current should be limited to less than 7.5 amps (1.5 amps for one ampere models).

2. For 86 degrees, use the reactor only. Choose a tap value greater than the reach of the mho function (e.g., if the relay base reach angle is three ohms (15 ohms for one ampere models), and K is 1.25, then tap value must be greater than 3 x 1.25 = 3.75 (or 15 x 1.25 = 18.75 for 50 hertz, one ampere models).

3. Calculate test box settings for this angle for each mho function. Use either of the above equations.

4. Find the transformer tap value which causes the function under test to pick up. Observe pickup at the test point following the characteristic timer; pickup may be observed with an oscilloscope or a DC voltmeter. Tap value should be within plus or minus three of the calculated tap setting.

5. Repeat steps 3 and 4, using the resistor-reactor combination for angles of 30 and 60 degrees.

6. Interchange A and B connection points to reverse the voltage to the relay. Calculate test box settings for a 240-degree angle for the MB function. Check the actual transformer tap which causes pickup. This tap value should be within plus or minus three of the calculated tap setting.

7. Repeat steps 1 through 6 using the Test II connections of Fig. 18. This will assure that all input windings are checked.

Positive Sequence Overcurrent Function Settings

The pickup levels of the positive sequence overcurrent functions can be checked using the current circuit portion of the test setup of Fig. 15 or 17, and the procedure outlined in "Positive Sequence Overcurrent Function Settings," of the DETAILED TESTING INSTRUCTIONS. Do not make any adjustments to the relay. Simply apply the test current and determine the function's positive sequence pickup level. This level should be within plus or minus ten percent of the original setting.

If the positive sequence network calibration has changed (as evidenced by previous checks), this will affect the pickup level of all the positive sequence overcurrent functions. If the calibration of only one function has changed, then the network probably is not affected, and the particular function involved should be checked further.

Zero Sequence Overcurrent Function Settings

The operating level of G4 or $(I_0\text{-}KI_1)T_D$ can be checked using the current circuit portion of the test setup of Fig. 15 and the procedure outlined in "Zero Sequence Overcurrent Function Settings," of the DETAILED TESTING INSTRUCTIONS. Do not make any adjustments to the relay. Simply apply test current and determine the function's operating level. This level should be within plus or minus ten percent of the original setting.

If the $(I_0\text{-}KI_1)T_D$ operating level is out of calibration, a further check must be made to determine if the $3I_0$ pickup level is out of calibration, or if the K setting is out of calibration. Any change in calibration of the positive sequence current network will affect the setting of this function.

Negative Sequence Fault Detector Settings

The pickup levels of the negative sequence fault detectors can be checked using the current circuit portion of the test setup of Fig. 15 or 17 and the procedure given in "Negative Sequence Fault Detector Settings," of the DETAILED TESTING INSTRUCTIONS. Do not make any adjustments to the relay. Simply apply the test current and determine the function's pickup level. This level should be within plus or minus ten percent of the original setting.

If one (or more) of the functions appears to be out of calibration, a further check must be made to determine if the problem is in the balance of the negative sequence current network, in the adjustable amplifier for the particular function, or in the actual level detector card.

No matter what the pickup setting for FDL, FDHH or I_2T_D, the output of the adjustable amplifier for that function at pickup should be the same level that was measured for the minimum pickup level during installation tests. In other words, the output of the adjustable amplifier for FDL at pin 8 of card position B should be at the same level of 0.15 to 0.18 volts at pickup, no matter what the FDL pickup is set for. In a similar manner, the output of the adjustable amplifier for FDHH at pin 8 on the card in position D should be at the same level of 0.20 to 0.29 volts at pickup, no matter what FDHH pickup is set for. Also, the output of the adjustable amplifier for I_2T_D at pin 9 on the card in position D should be at the same level of 0.29 to 0.36 volts at pickup, no matter what the I_2T_D pickup is set for.

TROUBLESHOOTING

In troubleshooting a complete relay equipment, it should first be established which unit is functioning incorrectly. The overall logic diagram supplied with the equipment shows the combined logic of the complete equipment and the various test points in each unit. By signal tracing, using the overall logic diagram, and the various test points, it should be possible to quickly isolate the trouble.

The output of every function in the SLDY51A relay has a test point associated with it. These test points can be identified on the internal connection diagram in Fig. 2 or on the overall logic diagram. Using these test points, and the various tests described in **PERIODIC TESTS AND ROUTINE MAINTENANCE** and the DETAILED TEST INSTRUCTIONS in this book, it should be easy to determine which functions are operating properly, and which are not.

If it becomes necessary to check the balance of the various sequence networks, a rough check can be made using the system voltages and currents, providing they are fairly well balanced. With balanced system voltages and currents supplied to the relay in the normal connections, the output of the positive sequence voltage and current * networks at V_1 and I_1Z test jacks on the front of the relay should be clean 60 hertz (or 50 hertz for 50 hertz, one ampere models) hertz signals. The output of the negative sequence current network should be a null signal similar to the signal observed when the calibration of the unit was performed. Reversing the ØB and ØC voltage and current connections to the relay should produce null signals at the V_1 and I_1Z test jacks, and a * 60 hertz (or 50 hertz) signal at TP15.

A test adapter card, 0149C7259G2, is supplied with each static relay equipment to supplement the pre-wired test points on the test cards. Use of the adapter card is described in the MOD III printed circuit card instruction book, GEK-34158.

A dual-trace oscilloscope is a valuable aid to detailed troubleshooting, since it can be used to determine phase shift and operate and reset times, as well as input and output levels. A portable dual-trace oscilloscope with a calibrated sweep and trigger facility is recommended.

SPARE PARTS

To minimize possible outage time, it is recommended that a complete maintenance program should include the stocking of at least one spare card of each type. It is possible to replace damaged or defective components on the printed circuit cards, but great care should be taken in soldering so as not to damage or bridge-over the printed circuit buses, or overheat the semiconductor components. The repaired area should be recovered with a suitable high-dielectric plastic coating to prevent possible breakdowns across the printed buses due to moisture and dust. The wiring diagrams for the cards in the SLDY51A relay are included in the printed circuit card instruction book GEK-34158. The card types are shown on the component location diagram, Fig. 3.

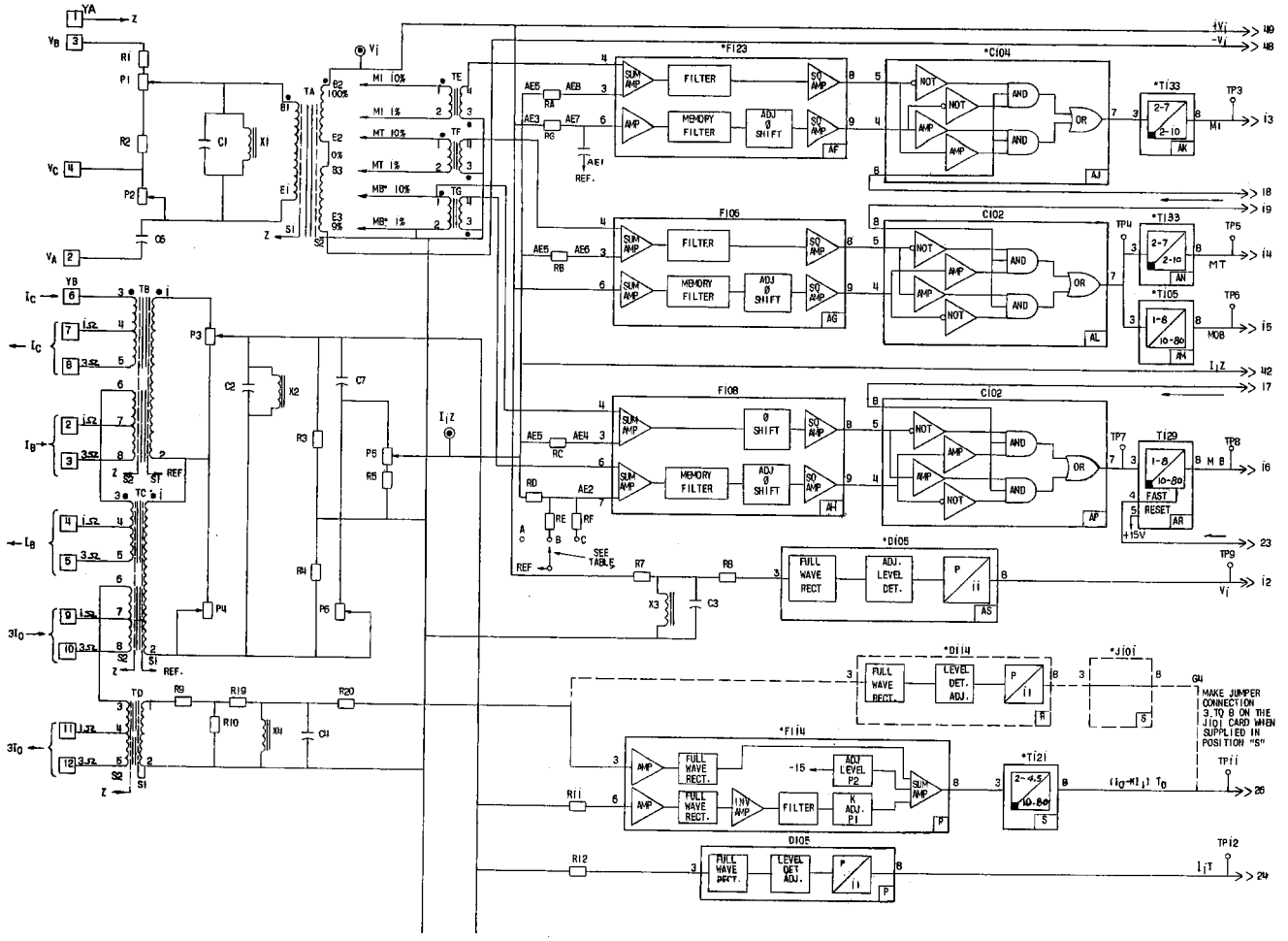


Fig. 2A (0126D6226-7) Internal Connections Diagram
for the SLDY51A Relay

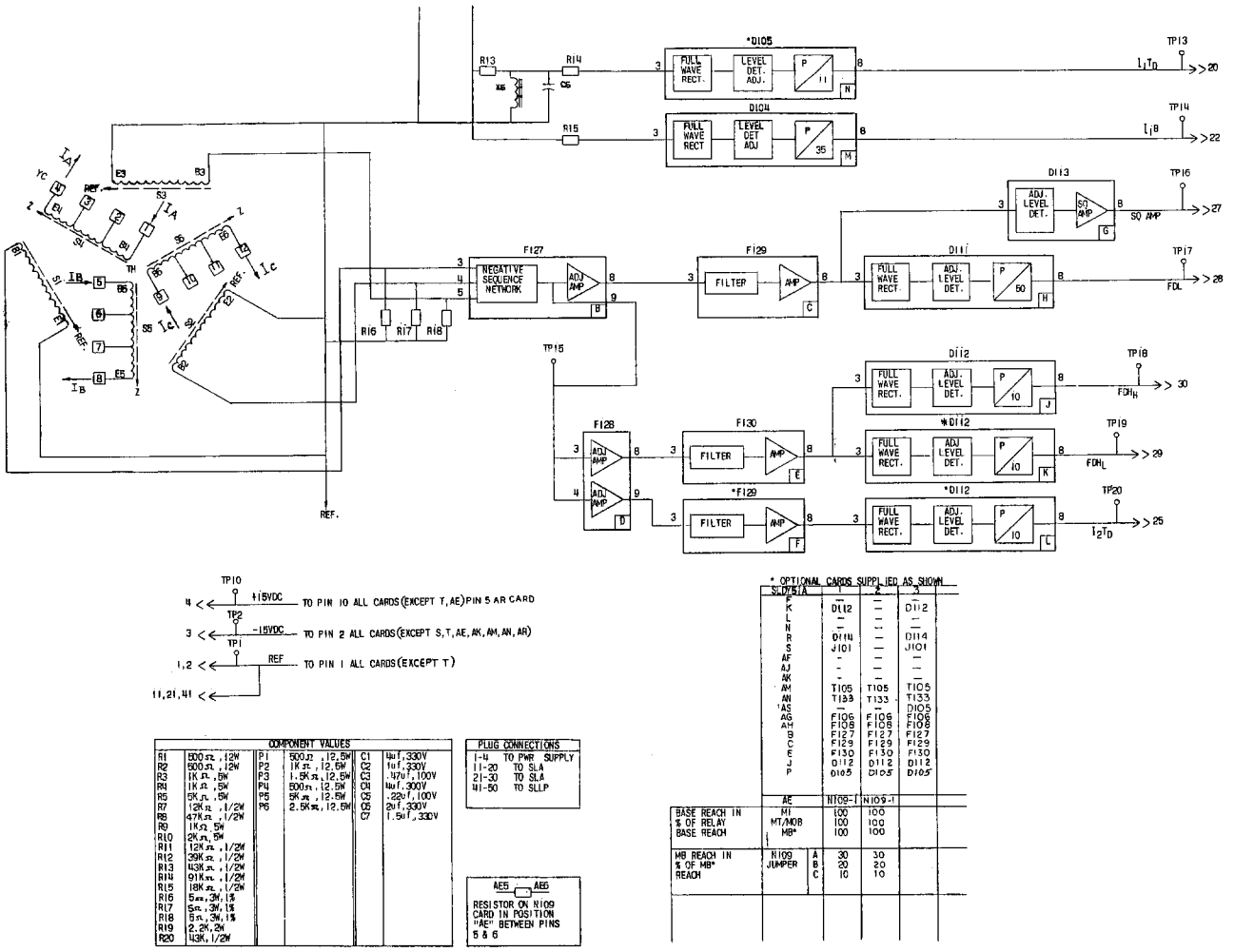


Fig. 2B (0126D6226-0) Internal Connections Diagram for the SLDY51A Relay

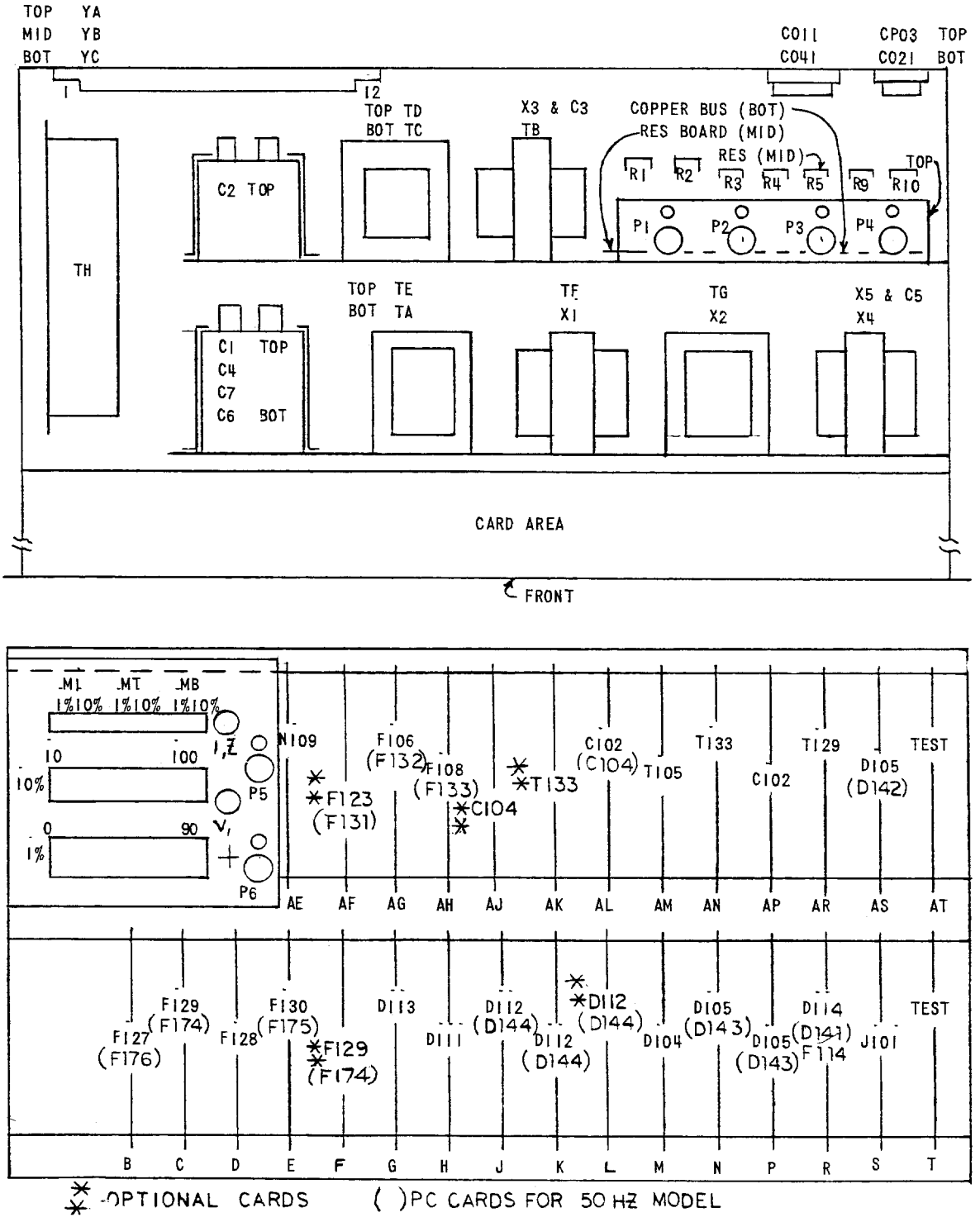


Fig. 3 (0257A6255-2) Component Location Diagram for the SLDY51A Relay

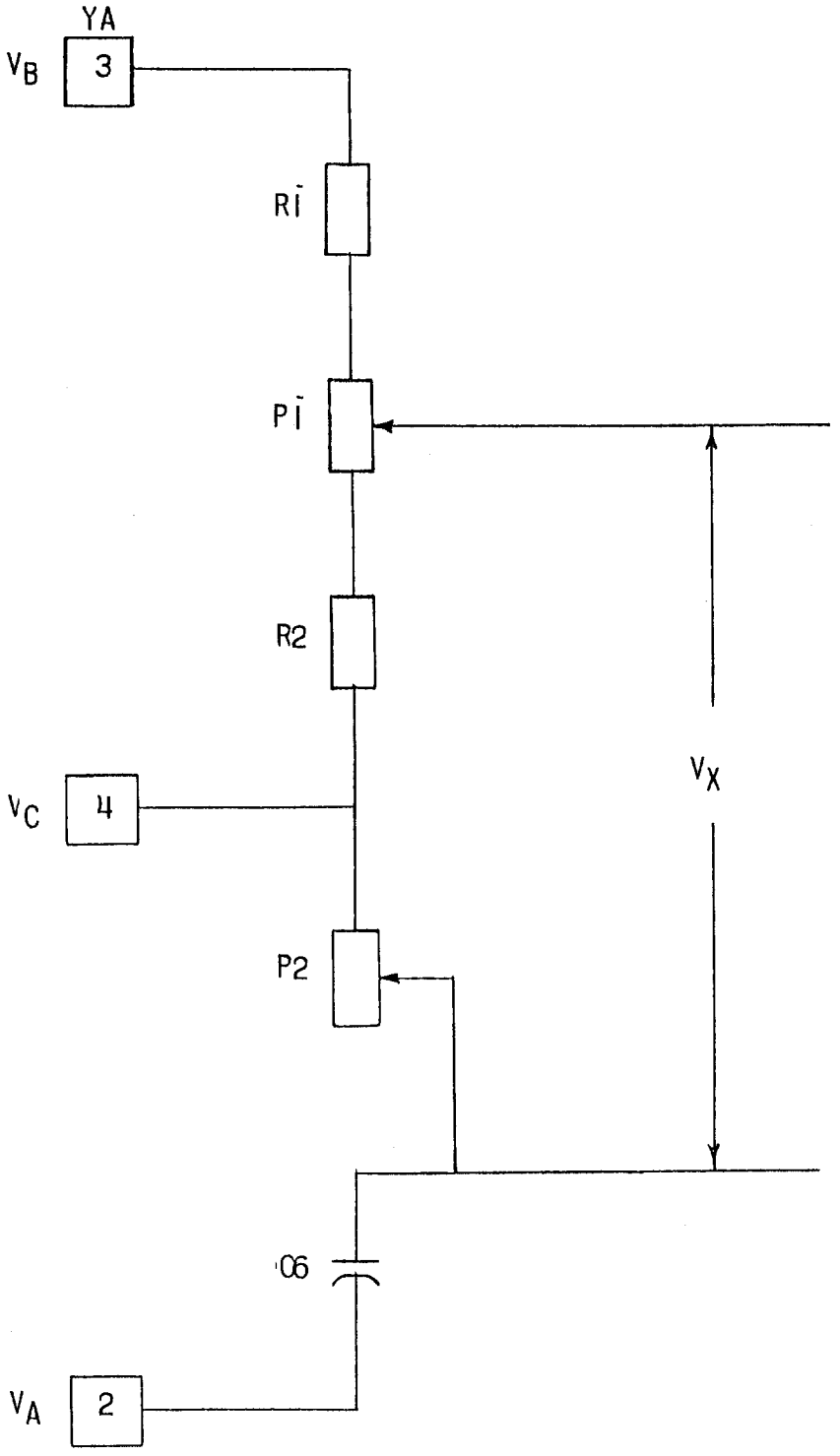
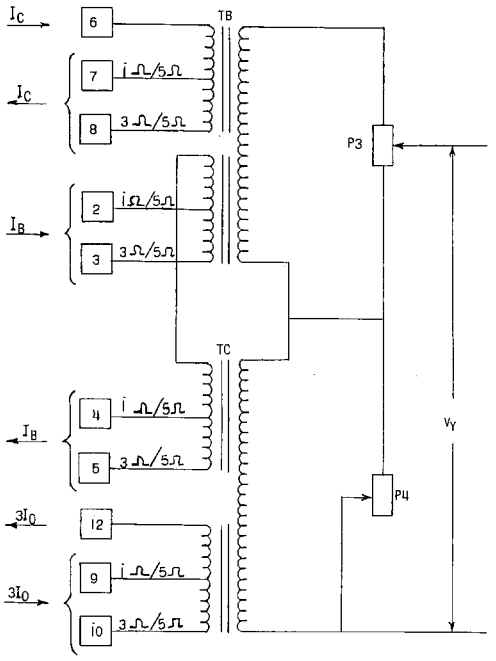


Fig. 4 (0257A6283-0, Sh. 1) SLDY Positive Sequence Voltage Network



* Fig. 5 (0257A6283-1, Sh. 2) SLDY Positive Sequence Current Network

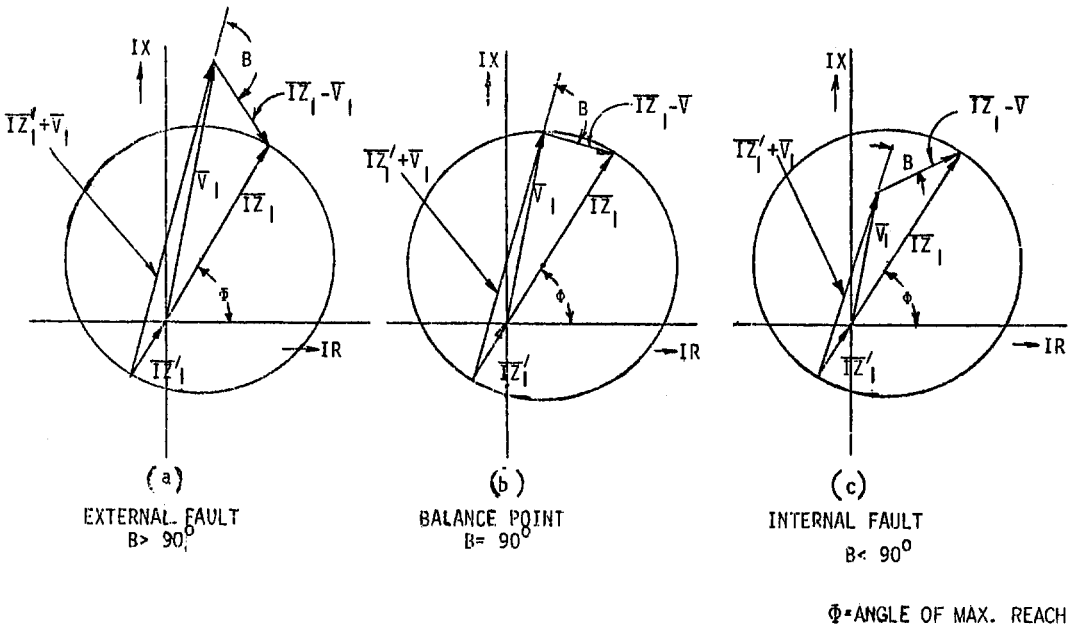


Fig. 6 (0246A7984-0) Offset Mho Characteristic by Phase Angle Measurement

*Indicates Revision

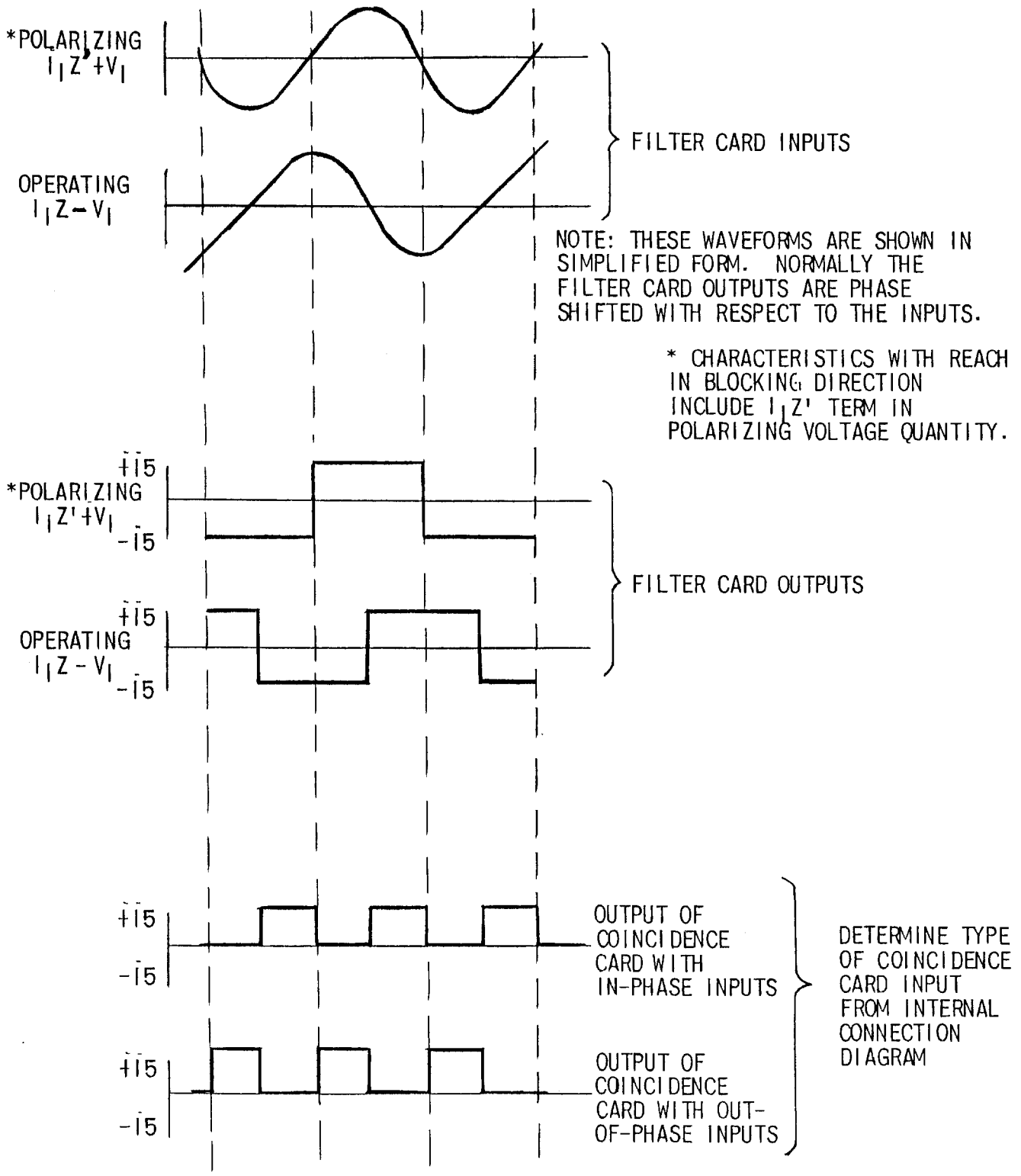
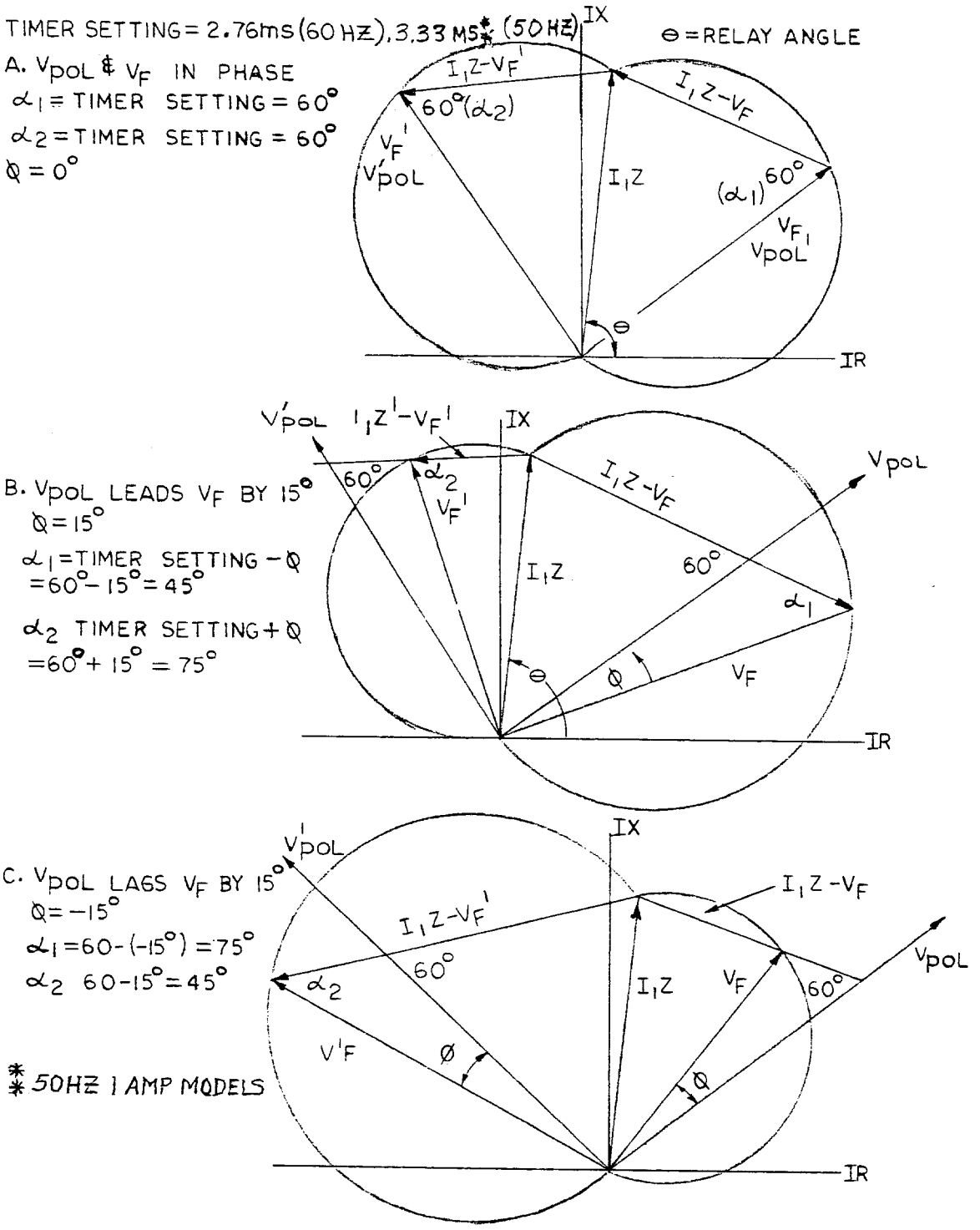


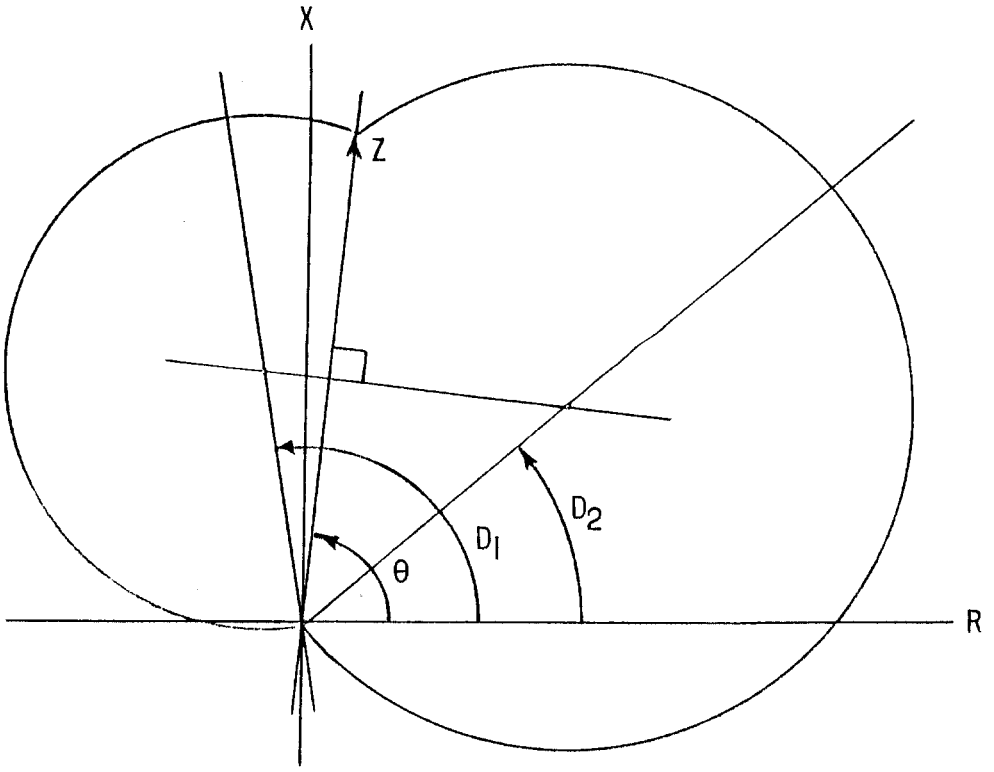
Fig. 7 (0257A6283-0, Sh. 3) SLDY Mho Function Operating Quantity Waveforms

*Indicates Revision



* Fig. 8 (0246A6866-4) Effect of Polarizing Quantity Phase Shift on Mho Characteristic

*Indicates Revision



θ = RELAY BASE REACH ANGLE.
Z = REACH OF MHO FUNCTION AT THE RELAY BASE REACH ANGLE.
TS = CHARACTERISTIC TIMER STEADY STATE PICKUP DELAY IN MILLISECONDS.
β = 21.6 (18*) X TS = CHARACTERISTIC TIMER STEADY STATE SETTING IN DEGREES.
ϕ = POLARIZING PHASE SHIFT IN DEGREES.
$D_1 = \theta - \phi + (90^\circ - \beta)$
$D_2 = \theta - \phi - (90^\circ - \beta)$
} ANGLES OF THE DIAMETERS OF THE TWO LOBES OF THE CHARACTERISTIC.

THE CENTERS OF THE TWO LOBES ARE THE POINTS ON D_1 AND D_2 THAT ARE EQUIDISTANT FROM THE ENDS OF Z.

* 50 HZ, 1 AMP MODELS

Fig. 9 (0257A6283-1, Sh. 4) Construction of a Mho Characteristic

*Indicates Revision

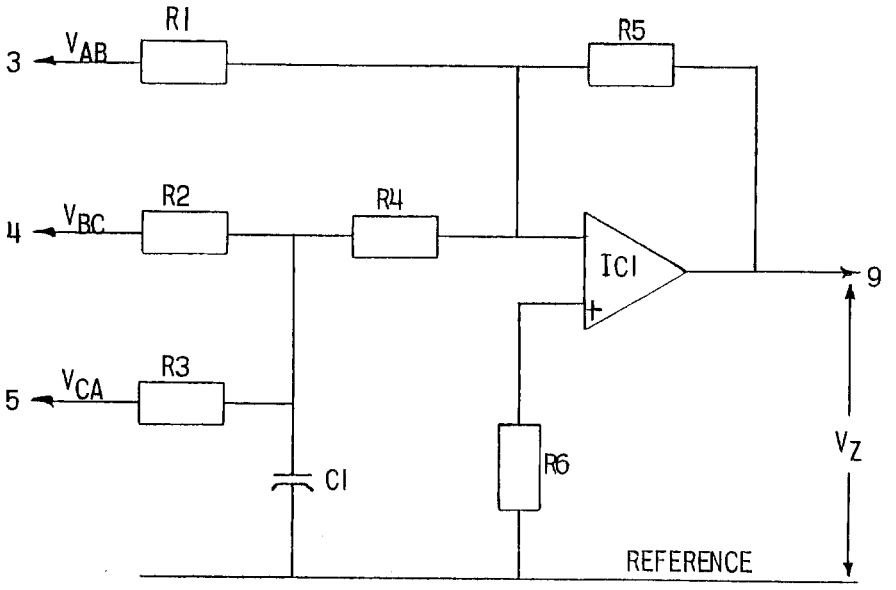
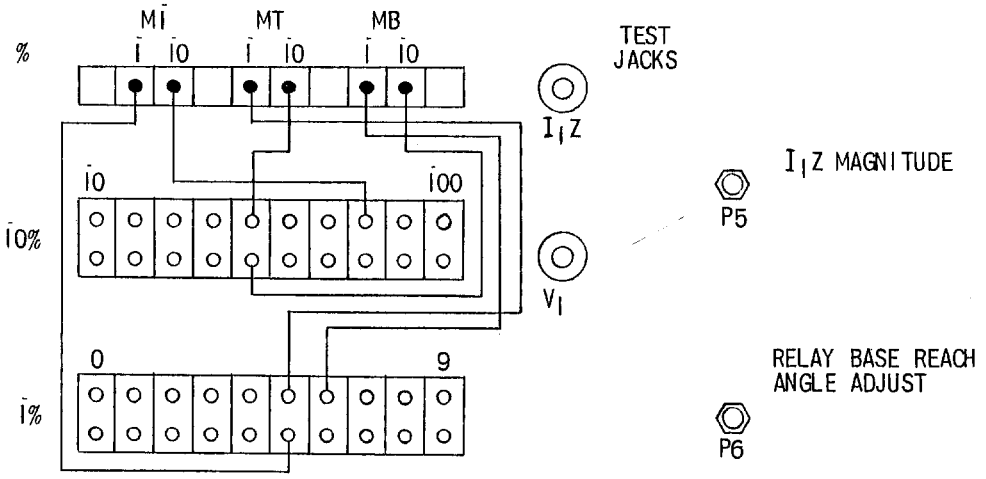


Fig. 10 (0257A6283-0, Sh. 5) Negative Sequence Current Mixing Network



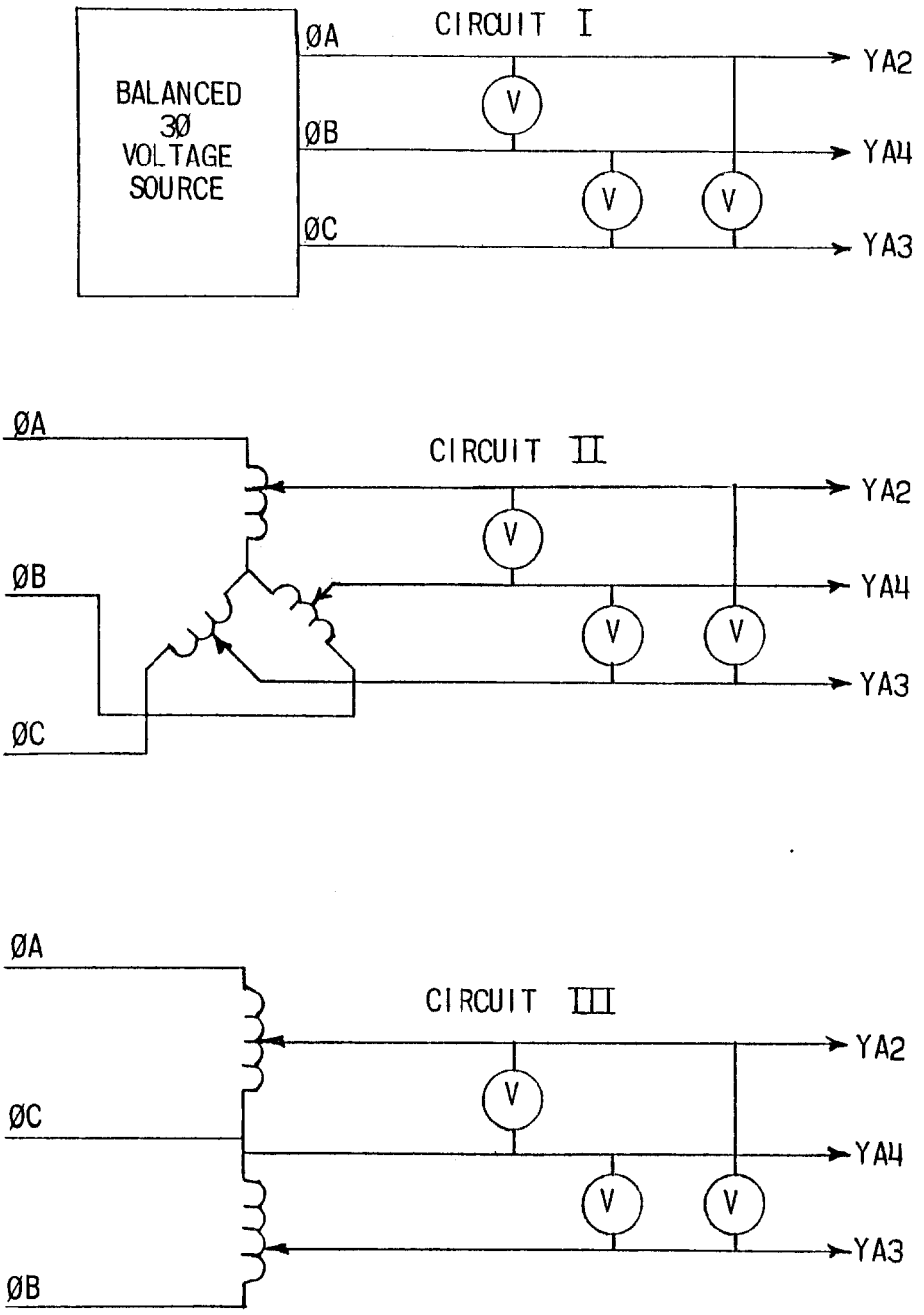
● FIXED TAP

○ VARIABLE TAP

MI SET FOR 85% RESTRAINT
MT SET FOR 55% RESTRAINT
MB SET FOR 56% RESTRAINT

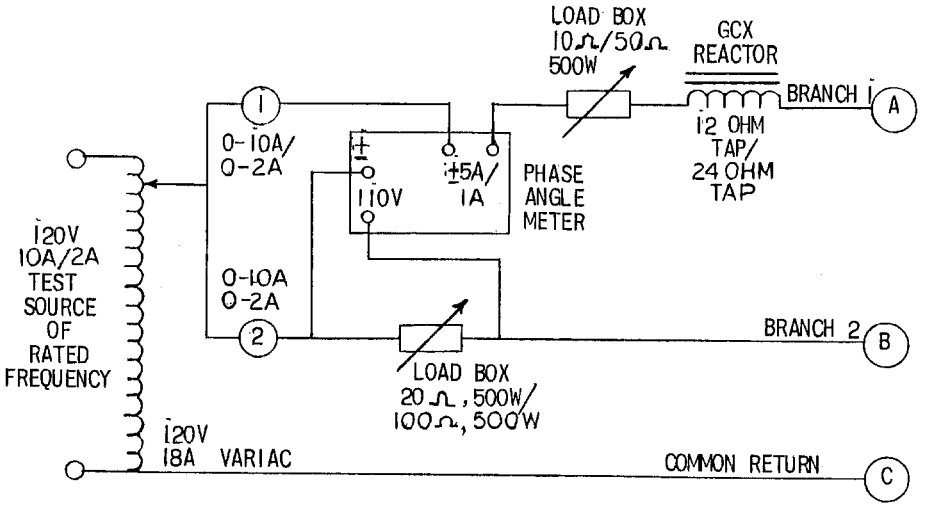
BE SURE TO USE THE PROPER TOOLS FOR INSERTING AND REMOVING THE VOLTAGE RESTRAINT TAP LEADS.

Fig. 11 (0257A6283-0, Sh. 6) Typical SLDY51A Voltage Restraint Tap Settings



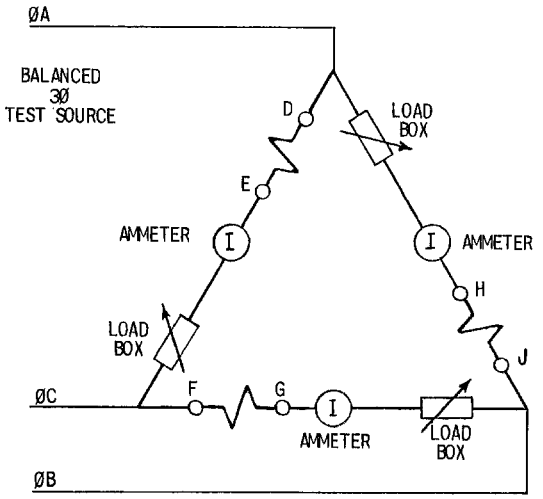
1. THE THREE PHASE TO PHASE VOLTAGES SHOULD BE APPROXIMATELY 120 VOLTS AND BALANCED WITHIN 1 TO 2%.
2. SET MB RESTRAINT VOLTAGE FOR 100% FOR PROPER VOLTAGE READINGS AT THE V_1 TEST JACK.

Fig. 12 (0257A6283-0, Sh. 7) Positive Sequence Voltage Network Null Check



CURRENT NETWORK NULL	TEST CONNECTIONS		
	A	B	C
POSITIVE SEQUENCE NETWORK	YB6	YB5	YB8, YB3
NEGATIVE SEQUENCE NETWORK	YC5	YC1	YC4, YC8
	YC9	YC5	YC8, YC12

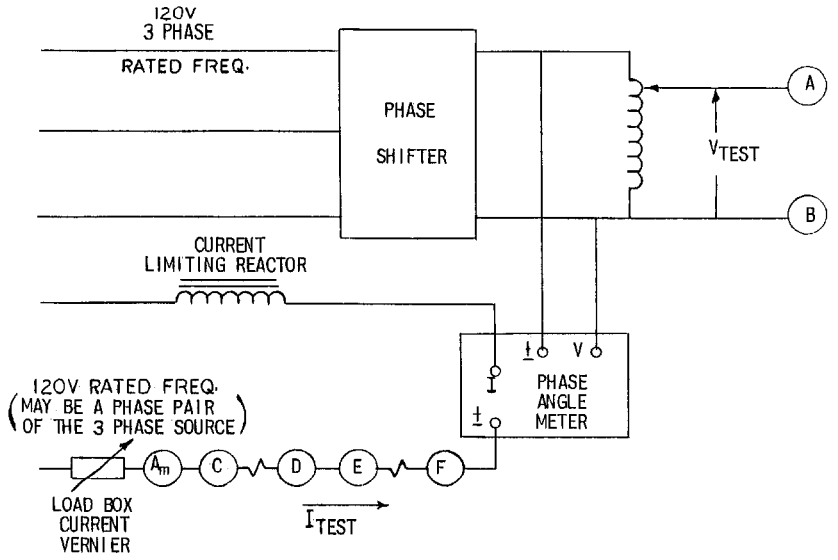
* Fig. 13 (0257A6283-1, Sh. 8) Single Phase Current Network Null Check



CURRENT NETWORK NULL	2 CURRENT OR 3 CURRENT TEST	TEST CONNECTIONS					
		D	E	F	G	H	J
POSITIVE SEQUENCE	3 CURRENT	YB5	YB3	YB8	YB6	J	H
	2 CURRENT	YB5	YB3	YB8	YB6	OPEN	OPEN
NEGATIVE SEQUENCE	3 CURRENT	YC8	YC5	YC4	YC1	YC9	YC12
	2 CURRENT	YC1	YC4	YC8	YC5	OPEN	OPEN
		YC5	YC8	YC12	YC9	OPEN	OPEN

* Fig. 14 (0257A6283-0, Sh. 9) Three Phase Current Network Null Check

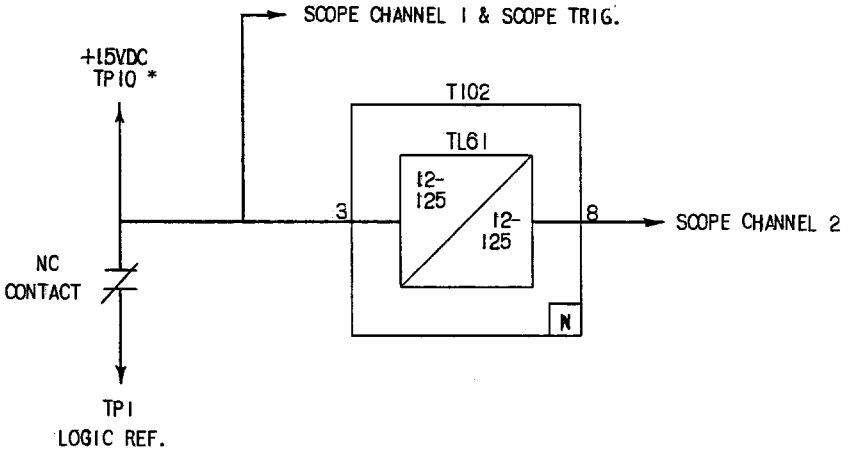
*Indicates Revision



$V_1 = 1/3\ V_{TEST}$
$I_1 = 1/3\ I_{TEST}$
WHEN TESTING OVERCURRENT FUNCTIONS
REMOVE THE PHASE ANGLE METER FROM THE CIRCUIT.

BASE MINIMUM OHMIC TAP 5AMP/1AMP	TEST CONNECTIONS					
	A	B	C	D	E	F
3 OHMS/15 OHMS	YA3	YA2, YA4	YB3	YB5	YB10	YB12
1 OHM/5 OHMS	YA3	YA2, YA4	YB2	YB4	YB9	YB11

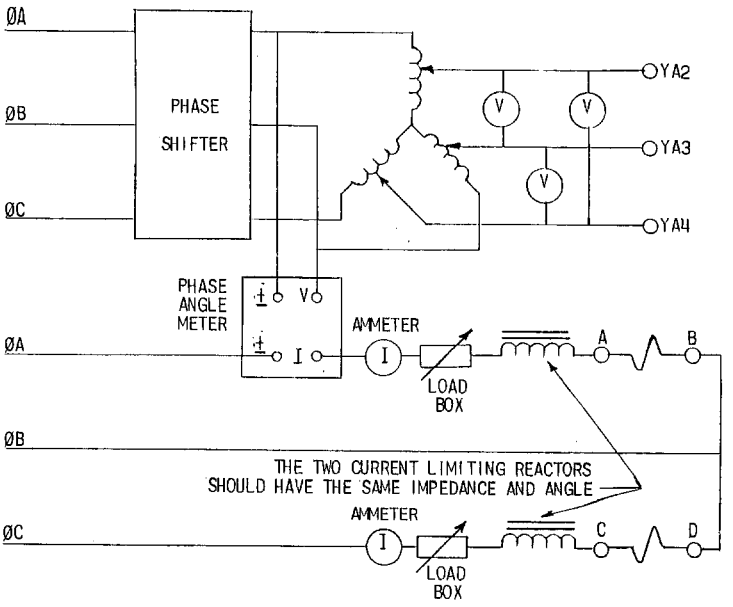
* Fig. 15 (0257A6283-1, Sh. 10) Single Phase Test Setup for the SLDY51A Relay



* THE 15VDC SIGNAL AT PIN 10 HAS A CURRENT LIMITING RESISTOR MOUNTED ON THE TEST CARD.

Fig. 16 (0246A7987-0) Typical Timer Test Circuit

*Indicates Revision



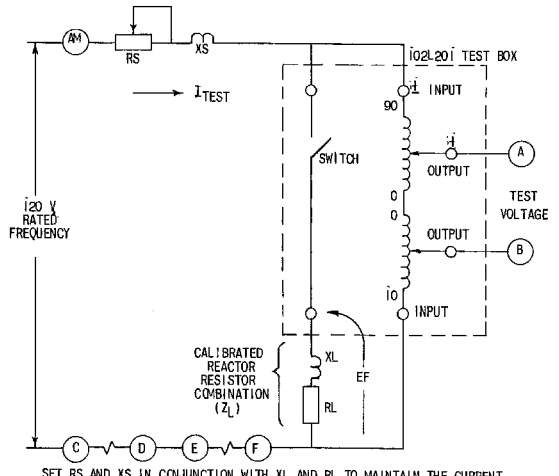
BASIC MINIMUM OHMIC TAP	TEST CONNECTIONS			
	A	B	C	D
3 OHMS/15 OHMS	YB5	YB3	YB6	YB8
1 OHM / 5 OHMS	YB4	YB2	YB6	YB7

$V_{\phi} - \phi = \sqrt{3}\ V_I$

$I_{TEST} = I_I$

WHEN TESTING OVERCURRENT FUNCTIONS, REMOVE THE PHASE ANGLE METER FROM THE CIRCUIT.

* Fig. 17 (0257A6283-2, Sh. 11) Three Phase Test Setup for the SLDY51A Relay



SET RS AND XS IN CONJUNCTION WITH XL AND RL TO MAINTAIN THE CURRENT THROUGH THE RELAY AT APPROXIMATELY 5 AMPS/1 AMP

	5 AMPS/1 AMP RELAY BASE REACH	TEST CONNECTIONS					
		A	B	C	D	E	F
TEST I	3/15 OHMS	YA3	YA2, YA4	YB3	YB5	YB10	YB12
TEST I	1/5 OHMS	YA3	YA2, YA4	YB2	YB4	YB9	YB11
TEST II	3/15 OHMS	YA4	YA2, YA3	YB6	YB8	YB10	YB12
TEST II	1/5 OHMS	YA4	YA2, YA3	YB6	YB7	YB9	YB11

* Fig. 18 (0257A6283-1, Sh. 12) SLDY Test Setup Using the R-X Test Set

*Indicates Revision

GENERAL ELECTRIC COMPANY
POWER SYSTEMS MANAGEMENT BUSINESS DEPT.
MALVERN, PA 19355

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