INSTRUCTIONS

GEK-34081B

SUPERSEDES GEK-34081A

STATIC POSITIVE SEQUENCE OUT-OF-STEP RELAY

TYPE SLLP51A

GENERAL ELECTRIC

CONTENTS

STATIC POSITIVE SEQUENCE OUT-OF-STEP RELAY

TYPE SLLP51A

DESCRIPTION

The Type SLLP51A relay is a static positive sequence relay designed to provide out-of-step blocking and tripping. The SLLP51A is packaged in one two rack unit case , the outline and mounting dimensions of which are shown in Figure 1. Component and card locations are shown in Figure 2.

The SLLP51A is not designed to be used by itself, but rather as part of a complement of equipment that forms a protective relaying scheme. A Type SLYP relay must be present to provide the input measurement quantities to the SLLP51A; a Type SSA power supply must be present to provide the ± 15V d-c required by the static logic circuits. The Type SLLP51A relay outputs are d-c logic signals that feed into a Type SLA logic relay, the circuitry of which depends upon the overall protection scheme. For a complete description of the overall scheme in which this relay is employed, refer to the overall logic diagram and its associated logic description that is supplied with each terminal of equipment.

The Type SLLP51A relay contains measurement logic for a mho function plus three independent timers to provide three separate LOB characteristics. These characteristics may be circular, lens or tomato shaped depending upon the timer pickup settings. Links are present to permit the use of only two LOB characteristics rather than three to detect an out-of-step condition. Refer to the section on CHARACTERISTICS for an explanation of how to select this option. The internal connections for the SLLP51A are shown in Figure 3.

APPLICATION

The Type SLLP51A relay provides out-of-step blocking and tripping when applied to either transmission lines or generators. Since the SLLP51A measures positive sequence impedance, there is less chance of setting up blocking for non-swing conditions (such as close-in single phase to ground faults on series compensated lines where gap flashing and capacitor reinsertion can cause the fault impedance to vary greatly) than for a relay that measures phase impedance. Because of this greater security due to the positive sequence measurement it may be possible to reduce the number of LOB characteristics from 3 to 2. The advantage of using only two LOB characteristics is that the outer LOB characteristic can generally be set smaller reducing its exposure to operate on minor swings.

In some applications it may be necessary to revert to the 2 LOB characteristic option because the combination of a fast moving swing locus (high slip frequency) and restricted LOB settings due to heavy load transfer prevent even the minimum settings on the TL62, TL63 and TL64 logic timers from setting up the proper logic sequence to detect the out-of-step condition.

RANGES

The LOB function has a range of adjustment as shown below.

Reach in forward direction 1.33 T_B - 12 T_B
Reach in reverse direction 1.33 T_B - 13.3 T_B

T_B is the base reach setting made in the SLYP.

The angle of the LOB function is determined by the line angle setting in the SLYP relay. For confirmation of the ranges, check the unit nameplate.

RATINGS

The Type SLLP51A relay is designed for use in an environment where the air temperature outside the relay case does not exceed 65°C.

The Type SLLP51A relay requires a ±15 VDC power source which can be obtained from a Type SSA power supply.

These instructions do not purport to cover all details or variations in equipment nor to provide for every possible contingency to be met in connection with installation, operation or maintenance. Should further information be desired or should particular problems arise which are not covered sufficiently for the purchaser's purposes, the matter should be referred to the General Electric Company.

To the extent required the products described herein meet applicable ANSI, IEEE and NEMA standards; but no such assurance is given with respect to local codes and ordinances because they vary greatly.

BURDEN

The Type SLLP51A relay presents a burden to the Type SSA power supply of:

150 ma from the +15 VDC supply
15 ma from the -15 VDC supply

OPERATING PRINCIPLES AND CHARACTERISTICS

A. GENERAL INTRODUCTION

A set of possible mho characteristics for the Type SLLP51A relay is shown in Figure 4. The principle used to derive the characteristics is illustrated in Figure 6. The I_1Z quantity is a voltage proportional to the positive sequence current in the line. This voltage is obtained from the current network in the associated SLYP relay. The tap setting of this quantity in the SLYP relay establishes the base reach of the SLLP51A relay. The V_1 quantity is the positive sequence voltage at the relay location. The V_1 quantity is also obtained from the SLYP relay. The quantity $(I_1 Z-V_1)$ is the phasor difference between these two quantities. I_1Z' is the reverse reach of the relay. The quantity $(I_1Z' + V_1)$ is the phasor sum of I_1Z' and V_1. The timer setting for the characteristics shown in Figure 6 is 4.15 ms. which corresponds to an angle of 90^o. The angle B between $(I_1 Z-V_1)$ and $(I_1 Z' + V_1)$ is less than 90^o an impedance point internal to the relay characteristic, equal to 90^o at the balance point and greater than 90^o for an external impedance point for which the relay should not operate. The quantities V_1 and I_1Z are the relay input quantities which are converted into blocks of voltage representing the quantities $(I_1 Z-V_1)$ and $(I_1Z' + V_1)$. The coincidence of these blocks is then measured. Blocks which are 90^o apart are coincident for 4.15 ms. Blocks which are less than 90^o apart are coincident for more than 4.15 ms. Blocks which are more than 90^o apart are coincident for less than 4.15 ms. The mho function consists of a filter card, a coincidence card, and a timer to measure the coincidence of (I_1Z-V_1) and $(I_1Z'+V_1)$. This circuit is shown in Figure 3.

B. LOB FUNCTION

The LOB function is comprised of three offset mho characteristics which do not pass through the origin on the R-X diagram (Figure 12). Relay operation occurs when the angle between (I_1Z-V_1) and $(I_1Z'+V)$ is equal to some angle $\emptyset$ determined by the settings of the three timers.

The angle of maximum reach of the LOB function is the same as the angle of the SLYP. This angle is normally set to be equal to the line angle. If the 100% voltage tap is used, the reach of the relay at the angle of maximum reach is equal to 1.33 times the basic minimum ohmic tap selected in the associated SLYP. If a voltage tap ~~other than~~ 100% is chosen, the relay reach is increased in inverse proportion to the voltage tap. ~~For example~~, if the 50% tap is used, relay operation still occurs for the same voltage applied to the measuring circuit, but since the line voltage is now twice this amount, the relay reach is doubled. The LOB reach, at the angle of maximum reach, may be calculated from the expression:

$$Z_{MAX} = \frac{1.33\ T_B}{T} \times 100$$

T = Voltage restraint tap setting expressed in percent
T_B = Basic minimum ohmic tap setting in SLYP

The V_1 used with I_1Z may be adjusted separately from the V_1 used with I_1Z'. The forward (along the protected line) taps are identified as LOB, and the reverse (away from the protected line) taps are identified as LOB*. These are 1% voltage taps in both directions.

OPERATING TIME

The exact operating time for a given fault varies considerably with the incidence angle of the fault. For a timer setting of 4.15 ms, the maximum operating time is 12 ms. and the minimum operating time is 4.15 ms.

CIRCUIT DESCRIPTION

A. LOB FUNCTION

The F106 filter card (position A) is supplied with three inputs I_1Z, $(+V_1)$ and $(-V_1)$. The resistors R1 and R2 (Figure 3) provide the 1.33 multiplying factor for I_1Z. The outputs of the filter card are 30 VDC square waves (-15 VDC to +15 VDC) which have the same phase relationship as $(I_1Z' + V_1)$ and $(-(I_1Z-V_1))$.

The C101 coincidence measurement card (position B) compares the positive half cycle of one square wave with the negative half cycle of the other; when both are present simultaneously an output is produced. The output blocks are thereby produced when $(I_1Z' + V_1)$ and $(I_1 Z-V_1)$ are coincident. These waveforms are shown in Figure 7.

The output blocks of the C101 card are the inputs to the three T101 timer cards (positions C, D, and E). The timer cards produce an output when the width of the input blocks exceeds the pickup time of the timer. At angles other than the line angle, a shorter timer setting results in a greater reach than a longer setting at the same fault angle. At the line angle, the reach does not vary with timer setting.

B. LOGIC CIRCUITS

The operating principles of the SLLP51A relay are best described in terms of a function diagram consisting of logic symbols interconnected by formation of flow paths as shown in Figure 3. The legend for symbols used is shown in Figure 8.

The R-X diagram of Figure 9 shows three LOB characteristics and the locus of an assumed out-of-step swing impedance. The proper operation of the scheme depends upon the impedance entering the OUTER LOB characteristic and passing into the INNER LOB characteristic with the proper timing between characteristics. Once the swing has entered the INNER LOB characteristic, the decision is made to trip. The choice to trip immediately or to delay tripping until the swing has passed through the OUTER LOB characteristic again is made by the position of link L3. It should be noted that tripping will take place regardless of the direction which the swing leaves the OUTER LOB characteristic.

The operation of the logic is explained in the following paragraphs.

STEP 1

The power swing enters the OUTER LOB characteristic. Thus AND61 will have one input from the OUTER LOB and a second input from OR61 since NOT61 has no input. If the swing impedance remains between the OUTER and MIDDLE LOB characteristics for the pickup setting of TL61, TL61 operates; seals in one input of AND61, and provides an out-of-step blocking signal at pin 276.

On the occurrence of a fault, the OUTER and MIDDLE LOB's would have operated almost simultaneously, the MIDDLE LOB would have blocked AND61 through NOT61 and prevented TL61 from picking up.

STEP 2

The swing now enters the MIDDLE LOB characteristic but remains outside the INNER LOB characteristic. One input of AND62 is energized by TL61, a second input is provided by the MIDDLE LOB, and the last is supplied by NOT62. If the swing impedance remains between the MIDDLE and INNER LOB characteristics long enough for TL62 to pickup, TL62 provides two inputs to AND62. AND62 is thereby controlled by TL61, which is in turn controlled by the OUTER LOB characteristic.

STEP 3

The swing now enters the INNER LOB characteristic. One input to AND63 is provided by TL62, the second by the INNER LOB, and the third from an overcurrent unit in the associated relays. If the swing impedance remains inside the INNER LOB characteristic for the pickup setting of TL63, TL63 provides two inputs to AND63. Thus AND63 is dependent solely on TL62.

At this point the decision to trip has been made and sealed in. The out-of-step tripping output will be provided immediately if link L3 is in the TRIP IN position (1-2).

STEP 4

The swing now leaves the INNER LOB characteristic in any direction, but remains inside the MIDDLE LOB characteristic. One input to AND64 is provided by TL63, a second input is supplied by the OUTER LOB, the third input is energized by NOT62 through OR64. If the output from AND64 lasts for the pickup setting of TL64, TL64 provides two inputs to AND64. The third input is supplied by TL63. The output of TL64 also energizes one input of AND65.

STEP 5

With link L3 in the TRIPOUT position (1-3), tripping is not initiated until the swing has passed through the OUTER LOB characteristic for the second time. When the OUTER LOB resets, the second input

of AND65 is supplied by NOT63. AND65, through OR65, provides an out-of-step tripping output at pin 278. This output lasts for 50 ms. after the OUTER LOB drops out, this is the dropout time of TL61.

The SLLP51A relay contains an option to use two LOB characteristics instead of three. In order to remove the middle characteristic, it is necessary to place links L1 and L2 in the (1-2) position and remove the cards in positions D, H, and P.

CALCULATION OF SETTINGS

The following description on determination of settings assumes that three LOB characteristics are utilized.

OUT-OF-STEP BLOCKING

Out-of-step blocking results when the swing locus passes from the outer to the middle characteristic in a time equal to or greater than the pickup setting of the A/50 timer. Therefore, proper out-of-step blocking operation requires that the middle characteristic of the SLLP51A surround the largest tripping function characteristic for which out-of-step blocking is required. However, this criteria may not be practical due to other considerations, and in many instances the middle characteristic must be set inside the limiting trip characteristic. If the trip characteristic should extend past the middle MOB characteris tic, the swing locus could conceivably plot inside the trip characteristic before the A/50 timed out. In this case the pickup setting of the A/50 must be based on the time it takes the swing to pass from the outer LOB characteristic to the trip characteristic.

OUT-OF-STEP TRIPPING

The preferred sequence of determining characteristic reach and included angle (i.e. 2-7/9 timer pick-up settings) begins with the inner characteristic. The inner characteristic is set as narrow as possible; an included angle of larger than 150^{o} is not permissable since the characteristic may become unstable for a narrower setting. A second consideration for the inner characteristic is that it should be set inside any swing for which the system could recover. The 150^{o} unstable point is usually the limiting case.

The reason for setting the inner characteristic initially as narrow as possible is so that an ad-equate separation-angle differential between the outer and inner characteristics can be selected allowing reasonable TL62, TL63, and TL64 timer settings for possible fast swings. The setting of the outer characteristic is now determined from system swing studies and a consideration of breaker operating capability. The outer characteristic should be set large enough so that when it resets, the breaker that is tripped will not have to interrupt an out-of-phase condition of greater than 90^{o} between the two systems Considering only the breaker interrupting capability the optimum setting of the outer characteristic for the simple system of Fig. 4 would be:

(forward reach) LOB = B

(reverse reach) LOB* = A

4.167/5 timer setting

The forward and reverse reaches are exactly at the respective ends of the system. This surrounds the system with a circle of diameter AB which is the loci of 90^{o} separation angles for all ratios of E_A/E_B. The angles of maximum reach of LOB and LOB* are the same as the maximum reach angle of the SLYP characteristics which is normally set to be equal to the line angle. Generally, this prevents the LOB and LOB* reach settings from being set for exactly the end points of the system. On the basis of system swing studies, the known setting of the inner characteristic and the range of settings on the TL62, TL63 and TL64 timers included angle of the outer characteristic must be selected to permit reasonable TL62, TL63 and TL64 timer settings. If the swing is fast the outer characteristic must have a smaller included angle (larger setting) as compared to a slower swing setting. If the swing study indicates an included angle of greater than 90^{o} the breaker interrupting duty should become the limiting factor and a 90^{o} characterist would result. If the swing study indicates an included angle less than 90^{o} then this criteria becomes the limiting factor. However, the outer characteristic should not be set so large that it picks up on maximum load transfer across the line. The middle characteristic setting is between the inner and outer, and if th TL62 and TL63 pickup time allow, it should be set outside the largest tripping element for which out-of-ste blocking is desired.

With all the characteristics determined the TL61, TL62, TL63 and TL64 pickup times may be set. The actual timer pickup values have already been considered in selecting characteristic sizes in conjunction with system swing studies. These timer settings are graduated to some extent since as the swing enters the outer characteristic its speed will probably be increasing.

Considering the simplified system of Fig. E the sequential procedure is as follows:

(a) Establish LOB and LOB* reaches

For the example assume that the best values of LOB and LOB* on a per-unit basis are:

LOB = 15

LOB* = 5

(b) This establishes the reach settings as close as possible to the end points of the system. Determine the value of the included angle, β_3, of the inner characteristic. For this example the stability limit criteria of $\beta_3 = 150^0$ is selected.

$$\beta_3 = 150^0$$

(c) Set the inner characteristic 2-7/5 timer pickup time to:

$$\text{P.U.} = (\beta_3/360^0)\ (16.67\ \text{ms})$$

$$\text{P.U.} = 6.95\ \text{ms}$$

(NOTE: The pickup times calculated are approximate values. To determine accurately that the desired included angle has been achieved with a particular pickup setting the characteristic should be plotted and a graphical vertification of the angle made).

(d) Determine the value of the included angle, β_1, of the outer characteristic. Here it is assumed that system swing studies and load considerations have dictated an angle of $_1 = 70^0$.

(e) Set the outer characteristic 2-7/5 timer pickup to

$$\text{P.U.} = (\beta_1/360^0)\ (16.67\ \text{ms})$$

$$\text{P.U.} = 3.24$$

(f) Determine the value of the included angle, β_2, of the middle characteristic. Here the angle $_2$ is chosen as 100^0 to position the middle characteristic approximately half way between the inner and outer characteristics.

$$\beta_2 = 100^0$$

(g) Set the middle characteristic 2-7/5 timer pickup time to:

$$\text{P.U.} = (\beta_2/360^0)\ (16.67\ \text{ms})$$

$$\text{P.U.} = 4.63\ \text{ms}$$

(h) Set the pickup times of the TL61, TL62, TL63 and TL64 timers based on system swing studies.

CONSTRUCTION

The SLLP51A relay is packaged in an enclosed metal case with hinged front cover and removable top cover. The case is suitable for mounting on a standard 19 inch rack. The outline and mounting dimensions of the case and the physical location of the components are shown in Figures 1 and 2 respectively.

The tap blocks for making the reach settings of the LOB function are located on the rear of the unit. The method of making reach tap settings is illustrated in Figure 10. The 10% voltage taps are at the top of the tap block arrangement. Settings are made by connecting jumpers from the fixed taps LOB and LOB* (forward and reverse reach respectively) to the desired 10% tap. The 1% voltage taps are located below the 10% voltage taps. Settings are made in the same manner as the 10% voltage taps.

The basic minimum ohmic tap (T_B) setting is made in the associated SLYP relay.

The SLLP51A relay also contains printed circuit cards identified by a code number such as F106, C101, T101, L104 where F designates filter, C designates coincidence, T designates time delay, and L designates logic. The printed circuit cards plug in from the front of the unit. The sockets are marked with letter designations or "addresses" (D, E, F, etc.) which appear on the guide strips in front of each socket, on the component location diagram, on the internal connection diagram, and on the printed circuit card. The test points (TP1, TP2, etc.) shown on the internal connection diagram are connected to instrument jacks on a test card in position T with TP1 at the top of the card.

The links (L1, L2, and L3), which are used to select the logic options, are mounted on the rear of the unit as shown in the component location diagram in Figure 2.

RECEIVING, HANDLING AND STORAGE

These relays will normally be supplied as a part of a static relay equipment, mounted in a rack or cabinet with other static relays and test equipment. Immediately upon receipt of a static relay equipment, it should be unpacked and examined for any damage sustained in transit. If injury or damage resulting from rough handling is evident, file a damage claim at once with the transportation company and promptly notify the nearest General Electric Sales Office.

Reasonable care should be exercised in unpacking the equipment. If the equipment is not to be installed immediately, it should be stored indoors in a location that is free from moisture, dust, metallic chips, and severe atmospheric contaminants.

Just prior to final installation the shipping support bolt should be removed from each side of all relay units, to facilitate possible future unit removal for maintenance. These shipping support bolts are approximately 8 inches back from the relay unit front panel. Static relay equipment, when supplied in swing rack cabinets, should be securely anchored to the floor or to the shipping pallet to prevent the equipment from tripping over when the swing rack is opened.

INSTALLATION TEST

The Type SLLP51A relay is usually supplied from the factory mounted and wired in a static relay equipment. The following checks and adjustments should be made by the user in accordance with the procedures given under DETAILED TESTING INSTRUCTIONS before the relays are put into service.

1. LOB and LOB* reach by voltage tap settings
2. Positioning of links
3. Timer settings

GENERAL TESTING INSTRUCTIONS

A. INPUT CIRCUITS

The V_1 and I_1Z input quantities are derived in the associated Type SLYP relay. These signals enter the SLLP51A on a 10 conductor shielded cable; the socket is located on the rear of the unit. In order to obtain specific values of V_1 and I_1Z for testing purposes, it is necessary to follow the test procedure described in the instruction book for the associated SLYP relay.

B. OUTPUT SIGNAL

The SLLP51A relay has a test card in the T position. This card has ten pin jacks mounted on the outer edge of the card which are numbered 1 to 10 from top to bottom. These jacks are the test points shown as TP1 to TP10 on the SLLP51A logic diagram. Pin number 10 is tied to +15 VDC through a 1.5 K resistor. This resistor limits the current when pin 10 is used to supply a logic signal to a card.

Output signals are measured with respect to the reference bus, TP1 on the test card. Logic signals are approximately +15 VDC for the ON condition, and less than 1 VDC for the OFF condition. Filter card outputs are either +15 VDC or -15 VDC for the ON condition. These outputs can be monitored with an oscilloscope, a portable high impedance DC voltmeter, or the test panel voltmeter is available. When the test panel voltmeter is supplied, it will normally be connected to the reference bus. Placing the relay test lead in the proper test point pin jack will connect the meter for testing.

When the time delay cards are to be adjusted or checked, an oscilloscope which can display two traces simultaneously and which has a calibrated horizontal sweep should be used.

DETAILED TESTING INSTRUCTIONS

A. REACH TAP SETTING

The arrangement of the LOB reach tap blocks is described under the section on CONSTRUCTION, and the choice of tap settings is discussed under the section on CHOICE AND CALCULATION OF SETTINGS.

B. TESTING THE LOB CHARACTERISTICS

The three mho characteristics may be checked by using the test circuit and test procedure described in the instruction book for the associated Type SLYP relay. The OUTER characteristic should be monitored at TP3, the MIDDLE at TP5, and the INNER at TP6.

TIMER ADJUSTMENTS AND TESTS
LOB TIME DELAY CARDS

These cards should not be adjusted unless a plot of the mho characteristic indicates an improper pickup time or if the reset time is too short to produce a continuous logic signal.

In the SLLP51A relay, the pickup time of each of the three LOB timers (positions C, D, and E) is adjustable between 2 and 7 milliseconds. The setting determines the shape of the mho characteristic. Increasing the timer pickup setting tends to narrow the characteristic; decreasing the setting widens the characteristic. The reset time delay (drop out time) of the timer provides an overlap of the next half cycle measurement and produces a continuous logic signal.

* The following procedure may be used to set characteristic timers for 6 milliseconds or less; for timer settings greater than 6 milliseconds the procedure outlined under "Logic Time Delay Cards" must be used.

Connect current and voltage inputs as described in the instruction book for the associated SLYP relay. Place appropriate timer card in a card adapter. Reduce the applied voltage until the fault condition applied to the relay is within the relay characteristic. Connect timer card input (Pin 3) to one channel of the oscilloscope and the timer card output (Pin 8) to the second channel.

* Input to the timer card should be blocks slightly longer than the desired pickup delay (if necessary, adjust the applied AC voltage to obtain this). In order to observe the operating delay time, the reset time must be reduced (turn P3 counterclockwise so that the timer resets each half-cycle. The operating delay time can now be measured on the oscilloscope. Adjust P2 to obtain the desired pickup delay time (turn P2 clockwise to increase pickup time). The reset time should then be adjusted until the output becomes continuous. P2 should be adjusted one full turn clockwise after the output becomes continuous. The mho characteristic should be plotted and compared to the desired characteristic. Readjust the timer if necessary to obtain the desired characteristic.

LOGIC TIME DELAY CARDS

* Time-delay cards are provided in the logic circuit to coordinate the operation of the SLLP51A. In order to test the timer cards, it is necessary to remove the card previous to the timer and to place the timer card in a card adapter. The timer test circuit is shown in Figure 11. Opening the normally closed contact causes the output to step up to +15 VDC after the pickup delay of the timer. To increase the pickup time turn the upper potentiometer on the timer card clockwise. Closing the contact causes the timer output to drop out after the reset time delay setting of the card. If the timer card is provided with a variable reset delay, it can be adjusted by the lower potentiometer on the timer card (clockwise increases reset time).

TABLE I

TIMER	POSITION	REMOVE CARD IN POSITION
TL61	N	J
TL62	P	K
TL63	S	L
TL64	R	F

ANGLE OF MAXIMUM REACH ADJUSTMENT

The characteristic angle of maximum reach can be reset if necessary by adjusting P71 potentiometer on the F106 card in position A.

* Indicates revision

MAINTENANCE

A. PERIODIC CHECKS

For any periodic testing of the SLLP51A relay, the associated SLAT trip outputs should be disconnected from the circuit breaker.

The reach of the LOB functions may be checked at periodic intervals using the instructions in the section DETAILED TESTING INSTRUCTIONS.

B. TROUBLE SHOOTING

Test points are provided at selected points in the SLLP51A logic and may be used to observe outputs if trouble shooting is necessary. The use of a card adapter will make all the pins on any one card available for testing.

All output voltages at the test points are measured with respect to the reference bus, TP1. When no signal is present the voltage is less than one volt, the output signal voltage is +15 VDC.

C. SPARE CARDS

The number of spare cards to carry in stock would depend on the total number of static relays, using similar cards, at the same location or serviced by the same test group. For each type of card (different code designation) a suggested minimum number of spare cards would be:

1 spare for 1 to 25 cards
2 spares for 26 to 75 cards
3 spares for 76 to 150 cards

D. CARD DRAWINGS

Internal connections of the printed circuit cards can be found in the printed circuit card instruction book GEK-34158.

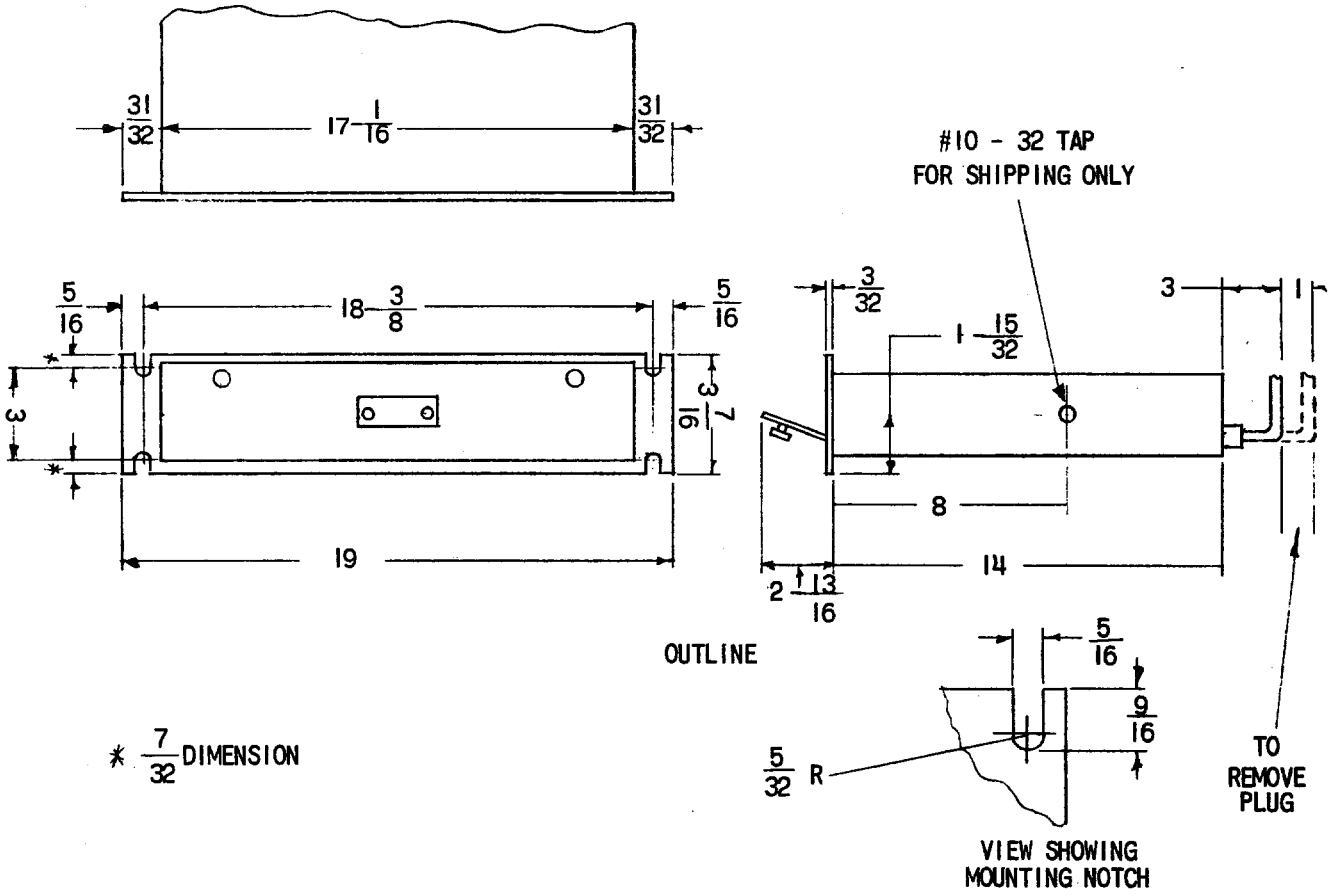
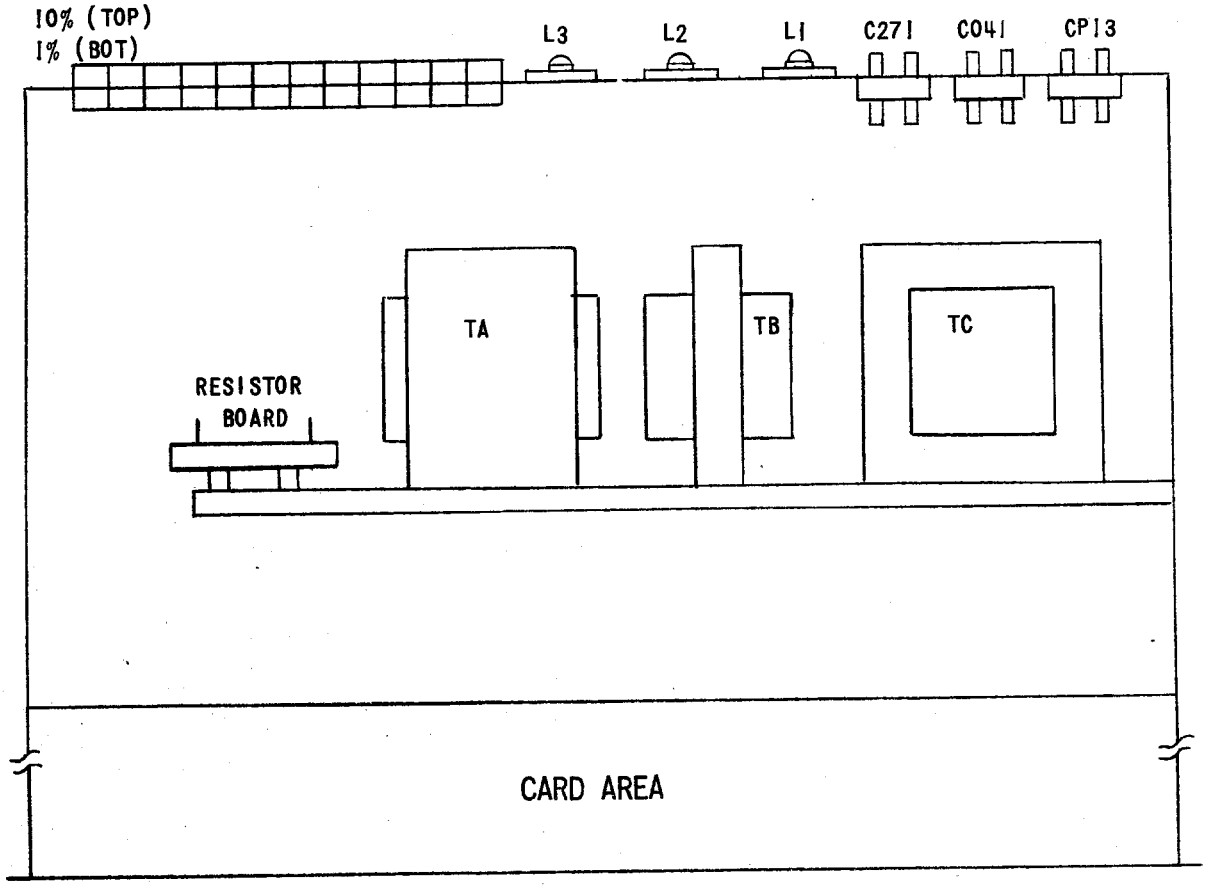
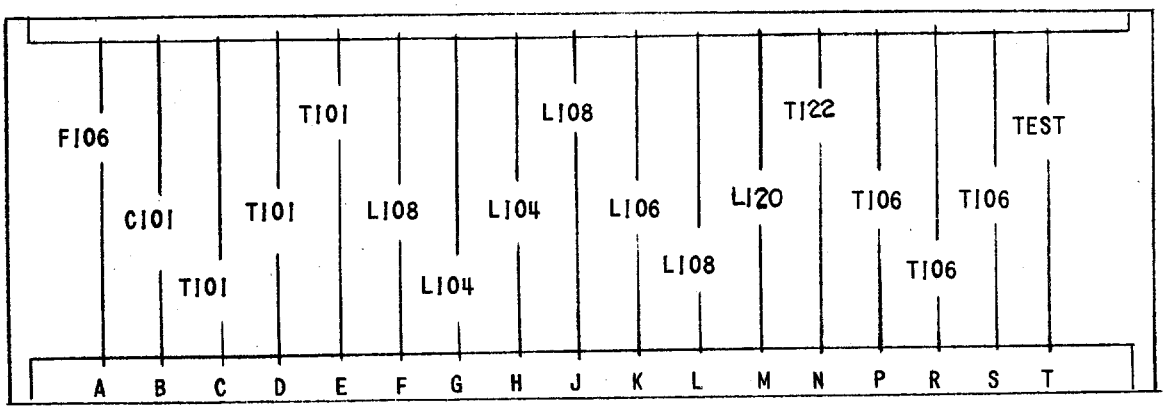


FIG. 1 (0227A2036-0) Outline And Mounting Dimensions For The Type SLLP51A Relay

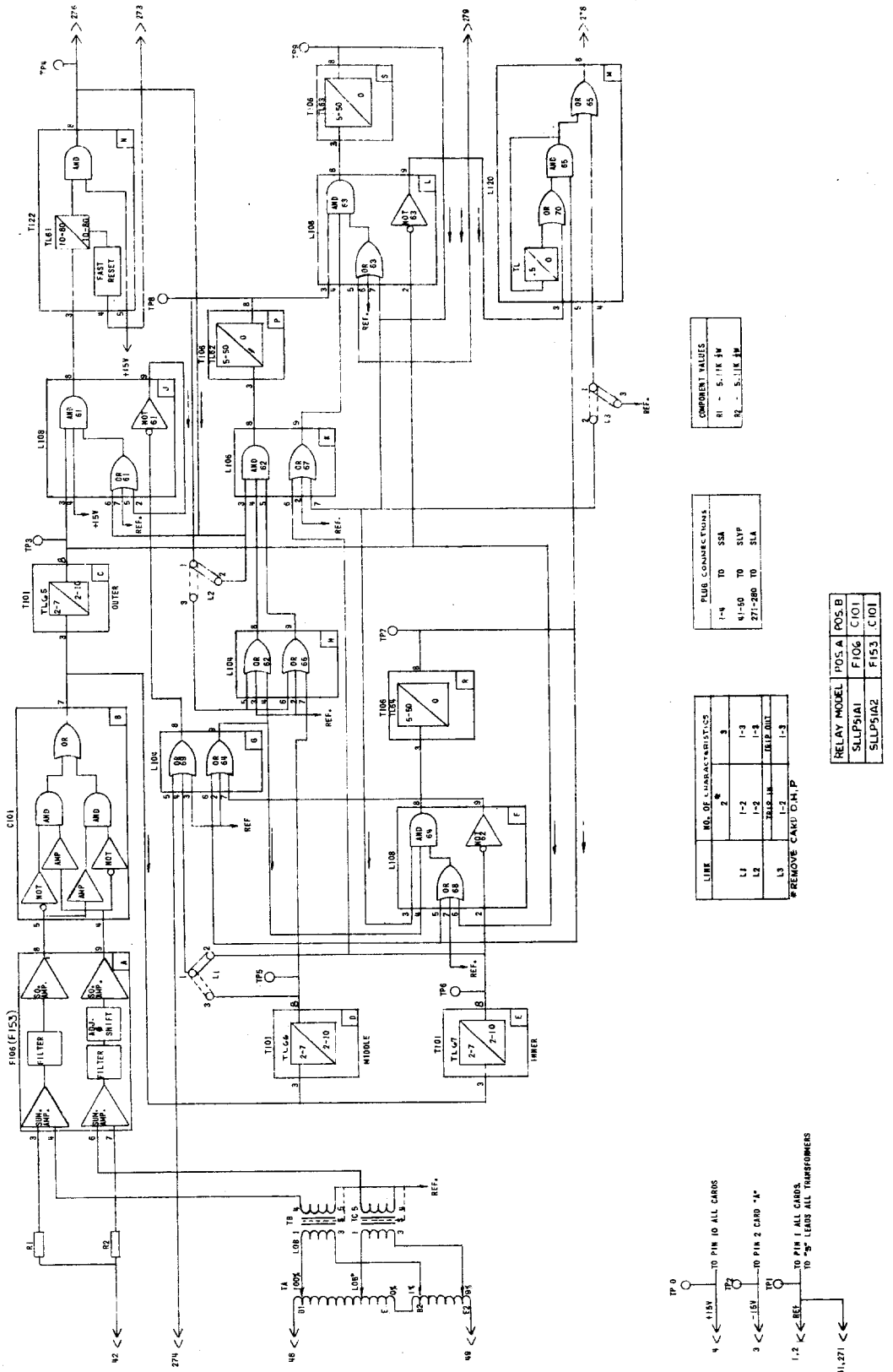


TOP VIEW



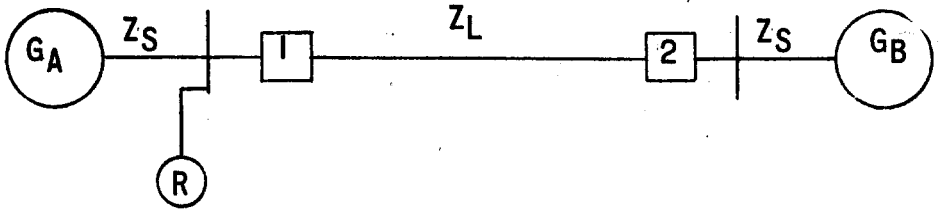
FRONT VIEW

FIG. 2 (0246A3506-1) Component And Card Locations For The Type SLLP51A Relay



* FIG. 3 (0149C7223-10) Internal Connections for the Type SLLP51A Relay

dicates revision



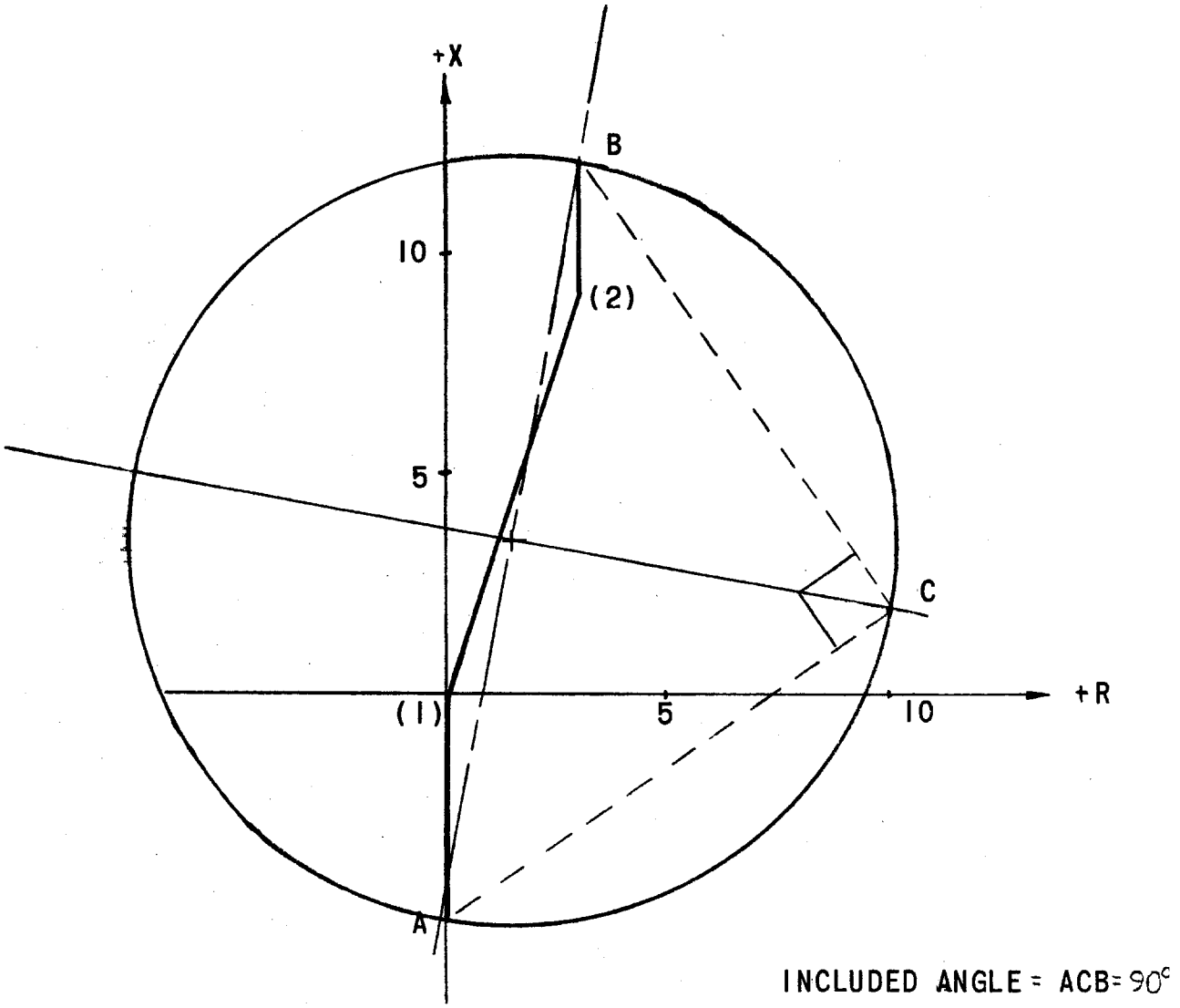


FIG. 4 (0227A2452-0) Optimal Setting For System Shown

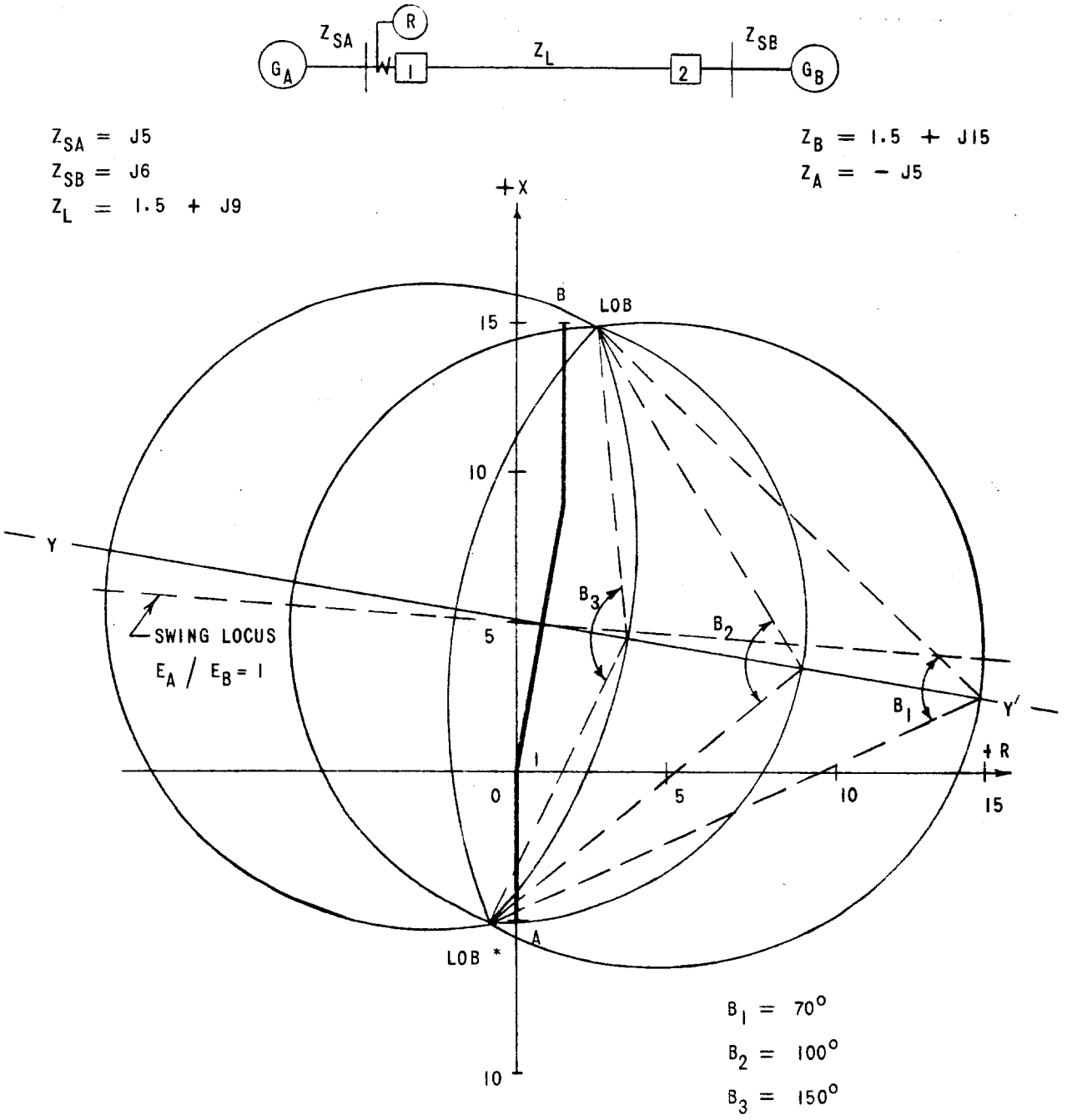


FIG. 5 (0246A7983-0) Practical SLLP51A Setting For System Shown

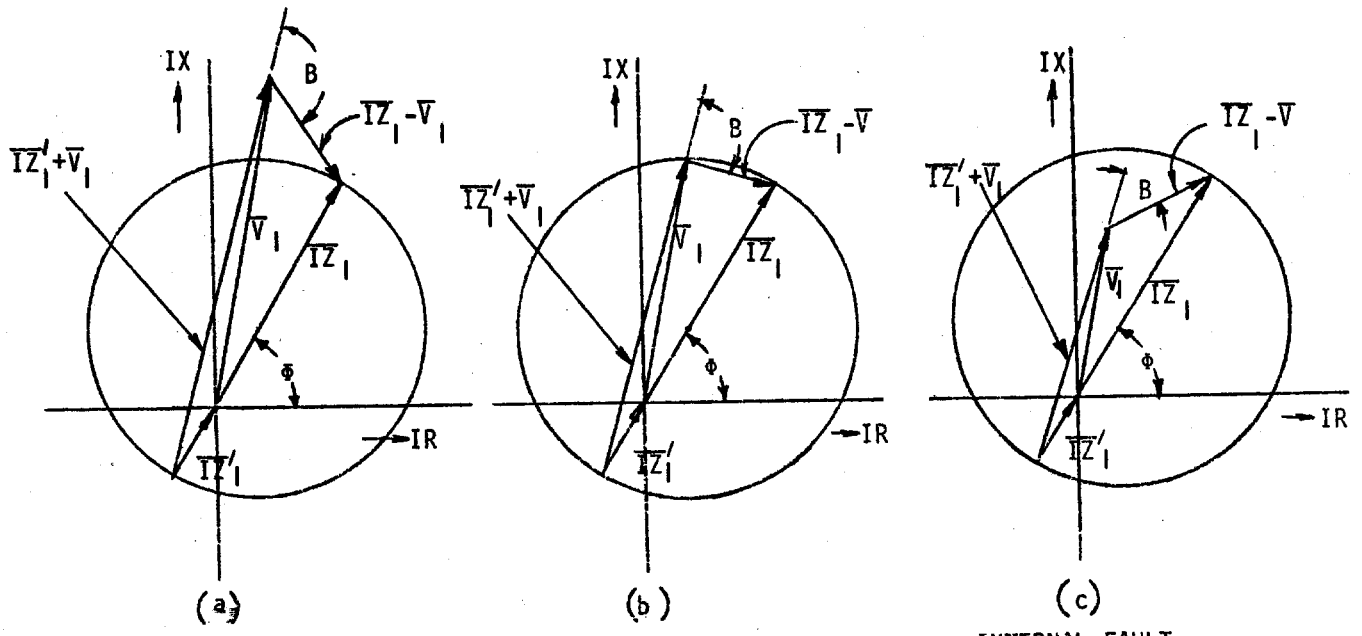
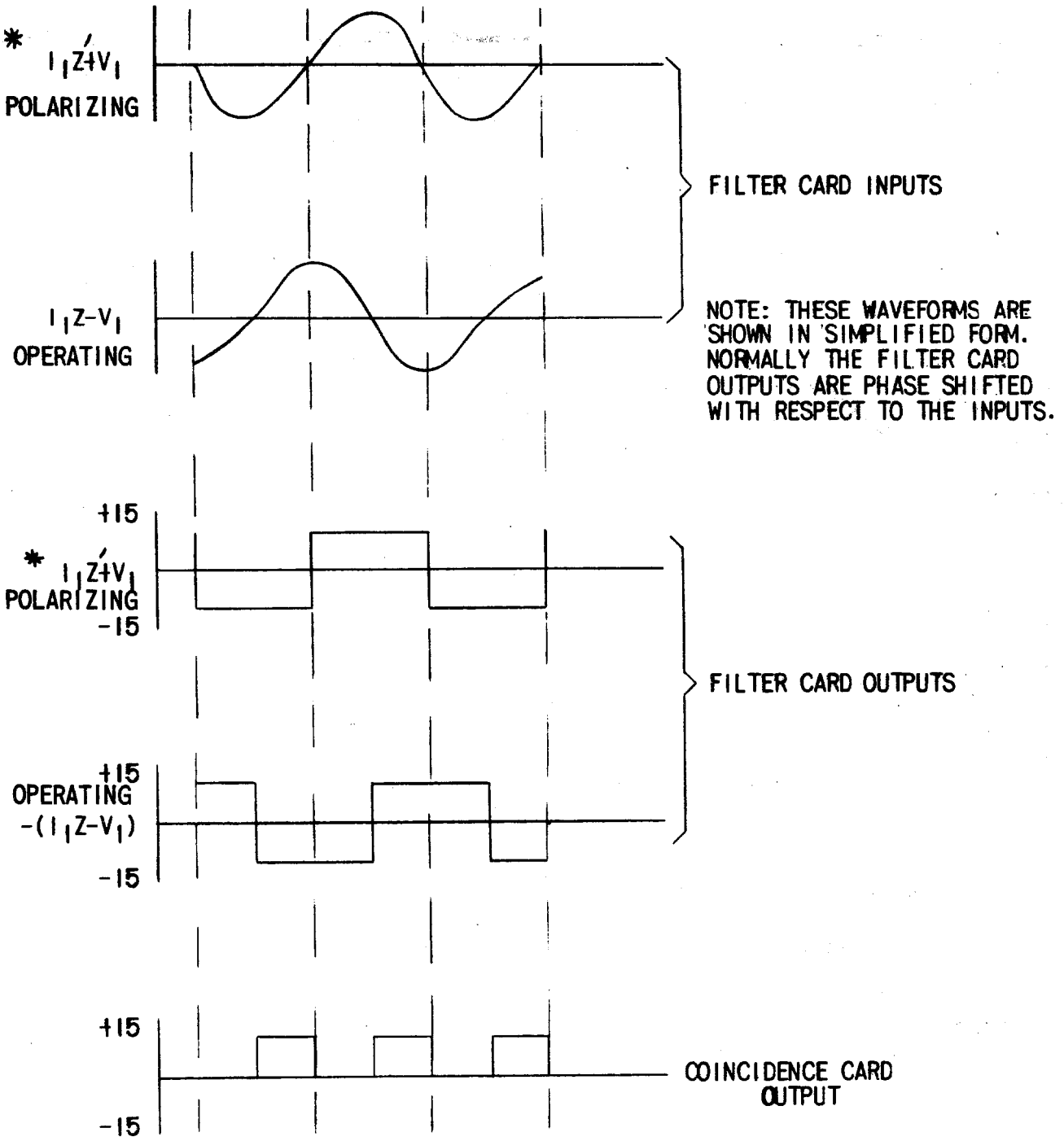
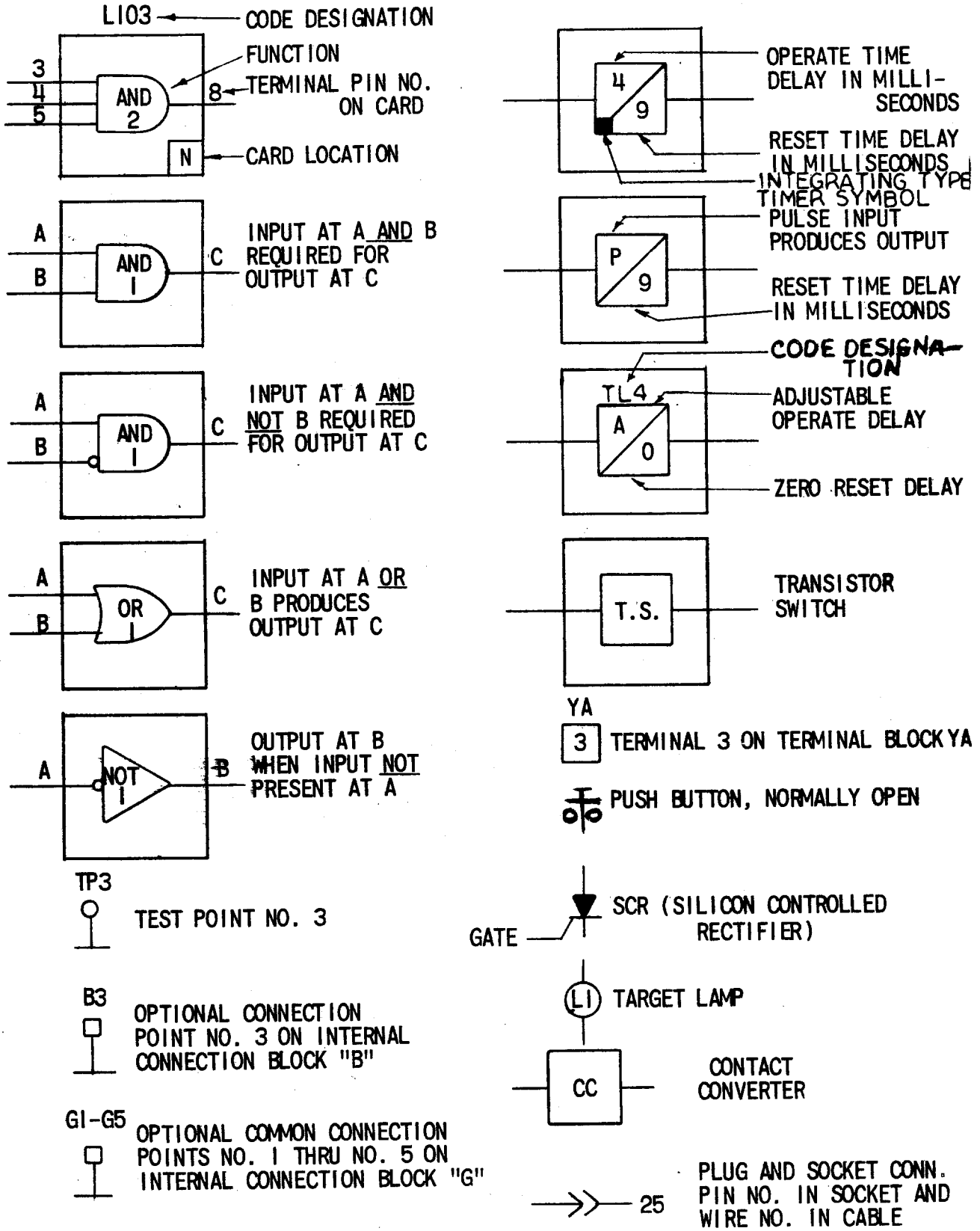


FIG. 6 (0246A7984-0) Offset Mho Characteristic By Phase Angle Measurement



* FIG. 7 (0246A7985-2) SLLP Operating Quantity Waveforms



* FIG. 8 (0227A2047-1) Logic and Internal Diagram Legend

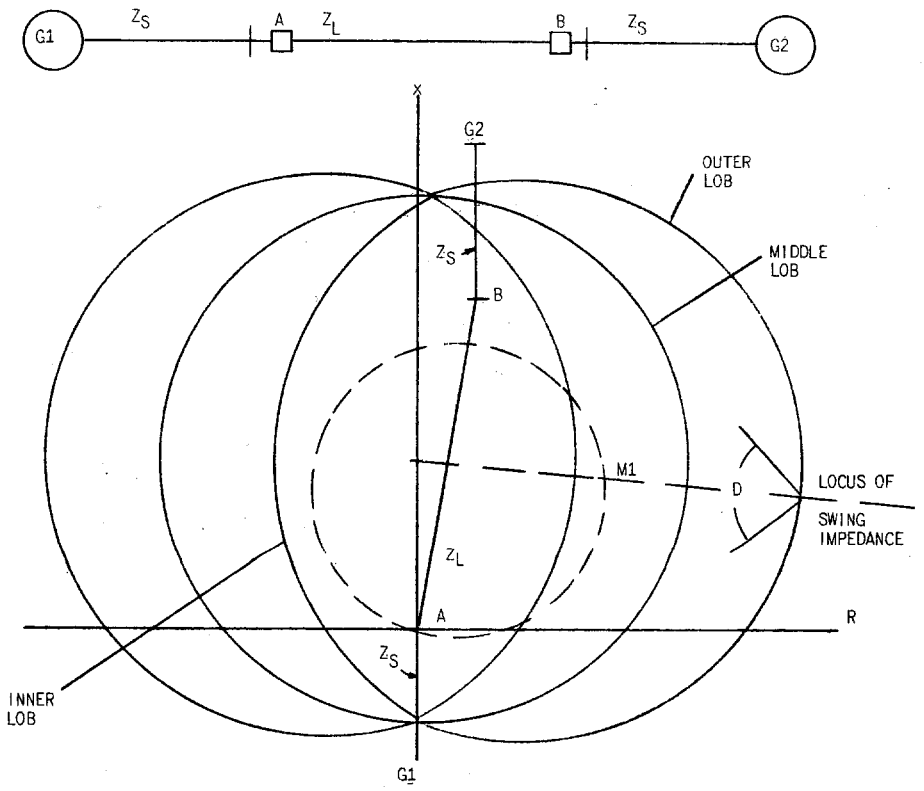
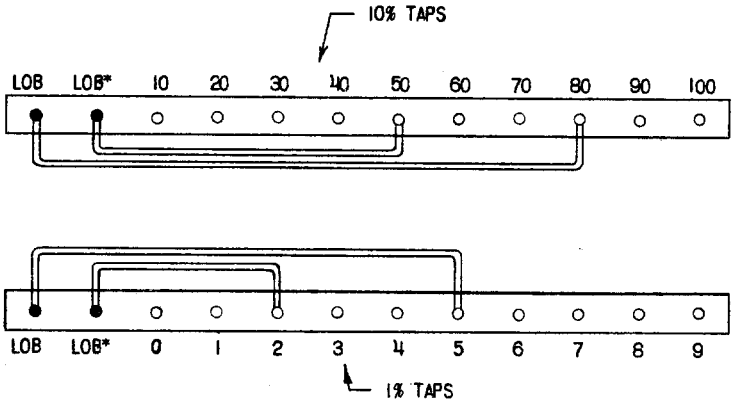


FIG. 9 (0227A2518-1) Typical SLLP Relay Settings On A System

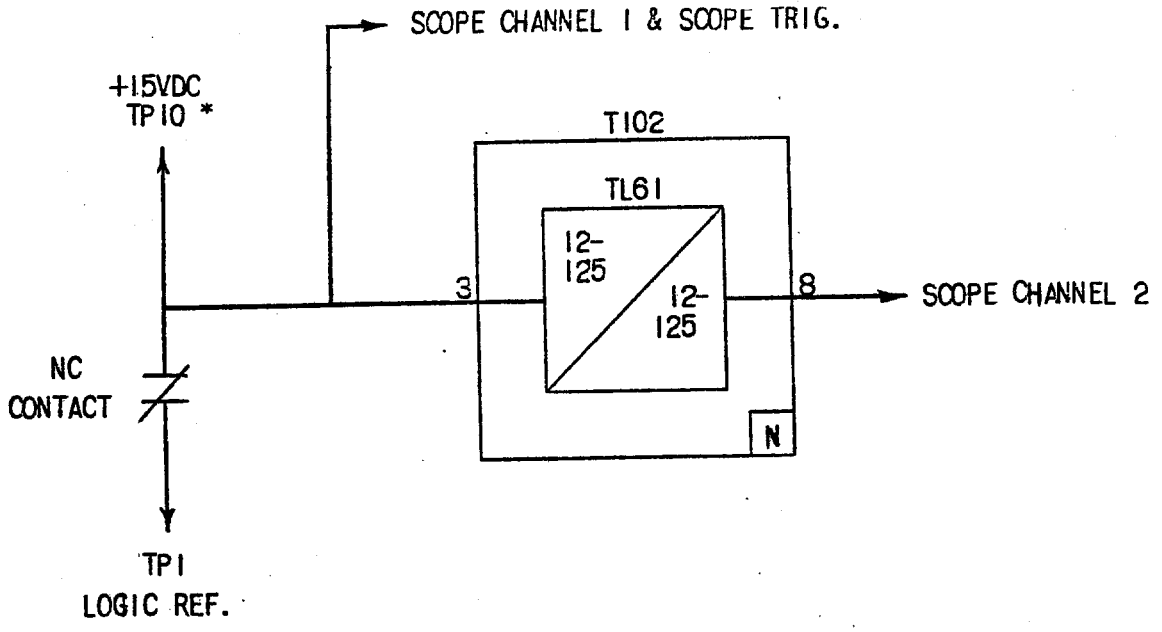


FUNCTION	VOLTAGE TAP	REACH
LOB	85 %	1.57 I_1Z
LOB*	52 %	2.57 I_1Z

● FIXED TAP

○ ADJUSTABLE TAP

FIG. 10 (0246A7986-0) Typical SLLP Tap Block Connections



* THE 15VDC SIGNAL AT PIN 10 HAS A CURRENT LIMITING RESISTOR MOUNTED ON THE TEST CARD.

FIG. 11 (0246A7987-0) Logic Timer Test Circuit

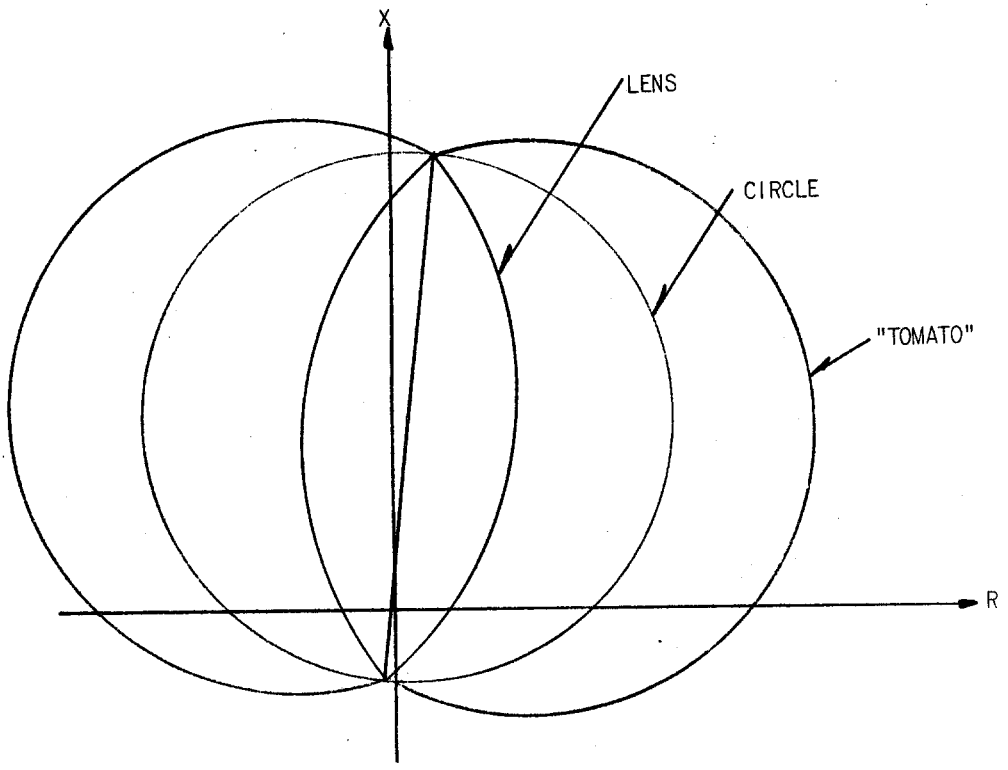


FIG. 12 (0227A2515-0) Mho Characteristics For The Type SLLP51A Relay