GEK-65600

INSTRUCTIONS

STATIC POSITIVE SEQUENCE OUT-OF-STEP RELAY

TYPE SLLP52A

GENERAL ELECTRIC

CONTENTS

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TYPE SLLP52A

DESCRIPTION

The Type SLLP52A relay is a static positive sequence relay designed to provide out-of-step blocking and tripping. The SLLP52A is packaged in one four-rack unit case, the outline and mounting dimensions of which are shown in Fig. 1. Component and card locations are shown in Fig. 2.

The SLLP52A is not designed to be used by itself, but rather as part of a complement of equipment that forms a protective relaying scheme. A Type SSA power supply must be present to provide the plus or minus 15 volt DC required by the static logic circuits. The Type SLLP52A relay outputs are DC logic signals that feed into a Type SLA logic relay, or a Type SLAT output and tripping relay, the circuitry of which depends upon the overall protection scheme. For a complete description of the overall scheme in which this relay is employed, refer to the overall logic diagram and its associated logic description that is supplied with each terminal of equipment.

The Type SLLP52A relay contains measurement and logic circuits for a mho function plus three independent timers to provide three separate LOB characteristics. These characteristics may be circular, lens or tomato shaped, depending upon the timer pickup settings. Links are present to permit the use of only two LOB characteristics rather than three to detect an out-of-step condition. Refer to the section on **CHARACTERISTICS** for an explanation of how to select this option. The internal connections for the SLLP52A are shown in Fig. 3.

APPLICATION

The Type SLLP52A relay provides out-of-step blocking and tripping when applied to either transmission lines or generators. Since the SLLP52A measures positive sequence impedance, there is less chance of setting up blocking for non-swing conditions (such as close-in single phase-to-ground faults on series compensated lines where gap flashing and capacitor reinsertion can cause the fault impedance to vary greatly) than for a relay that measures phase impedance. Because of this greater security due to the positive sequence measurement it may be possible to reduce the number of LOB characteristics from three to two. The advantage of using only two LOB characteristics is that the outer LOB characteristic can generally be set smaller, reducing its exposure to operate on minor swings.

In some applications it may be necessary to revert to the two-LOB characteristic option because the combination of a fast moving swing locus (high slip frequency) and restricted LOB settings, due to heavy load transfer, prevent even the minimum settings on the TL62, TL63 and TL64 logic timers from setting up the proper logic sequence to detect the out-of-step condition.

RANGES

The SLLP52A has an adjustable system reach of 1-30 ohms (five amperes) or 5-150 ohms (one ampere), with one and three ohm (five amperes) or 5 and 15 ohm (one ampere) base reach taps in the current circuits and one percent restraint taps in the voltage circuits.

The LOB function has a range of adjustment as shown below.

Reach in forward direction $1.33\ T_B$ - $13.3\ T_B$
Reach in reverse direction $1.33\ T_B$ - $13.3\ T_B$

T_B is the base reach setting.

The relay system angle is adjustable from 60 degrees to 90 degrees. The standard factory setting is 85 degrees.

RATINGS

The Type SLLP52A relay is designed for use in an environment where the air temperature outside the relay case does not exceed 65°C.

The Type SLLP52A relay requires a plus or minus 15 volt DC power source which can be obtained from a Type SSA power supply.

The current circuits of the Type SLLP52A relay are rated at five or one ampere, 60 or 50 hertz for continuous duty and have a one-second rating of 300 amperes on five amp relays and 60 amperes on one amp relays. The potential circuits are rated 120 volts, 60 or 50 hertz.

BURDENS

AC

Potential	5A, 60 Hz Relay	1A, 50 Hz Relay
ØA-ØB	1.9K ohms $\angle 41^o$	1.9K ohms $\angle 41^o$
ØB-ØC	1.4K ohms $\angle 3^o$	1.4K ohms $\angle 3^o$
ØC-ØA	1.3K ohms $\angle -89^o$	1.3K ohms $\angle -89^o$

AC (Continued)

Current	5A, 60 Hz Relay	1A, 50 Hz Relay
ØB (three ohms)	0.035 ohm $\angle$ 8°	0.66 ohm $\angle$ 9°
ØC (three ohms)	0.014 ohm $\angle$ 14°	0.19 ohm $\angle$ 21°
$3I_0$ (three ohms)	0.014 ohm $\angle$ 1°	0.16 ohm $\angle$ 2°
ØB (one ohm)	0.020 ohm $\angle$ 2°	0.20 ohm $\angle$ 3°
ØC (one ohm)	0.010 ohm $\angle$ 3°	0.06 ohm $\angle$ 7°
$3I_0$ (one ohm)	0.011 ohm $\angle$ 0°	0.06 ohm $\angle$ 0°

DC

The Type SLLP52A relay presents a burden to the Type SSA power supply of

200 milliamperes from the +15 VDC supply
100 milliamperes from the -15 VDC supply

OPERATING PRINCIPLES

INTRODUCTION

The Type SLLP52A relay employs positive sequence voltage and current networks to obtain the V_1 and I_1Z signals that are used to derive the LOB characteristics included in the SLLP52A relay. The voltage at the V_1 test jack is given by the expression:

$$V_1 \text{ test jack voltage} = (0.0866)\left(\frac{T}{100}\right)(V_{1sys}) \angle 240^\circ$$

where V_1 system is the magnitude of positive sequence voltage applied to the relay, and T is the LOB restraint tap setting in percent.

The voltage at the I_1Z test jack is given by the expression:

$$I_1Z \text{ test jack voltage} = 0.0866\ T_B\ I_1 \angle(300^\circ - 330^\circ)$$

where I_1 is the magnitude of positive sequence current applied to the relay and TB is the basic ohmic tap setting, the angle is factory set to 325 degrees, which is a relay system angle of 85 degrees.

A set of possible mho characteristics for the Type SLLP52A relay is shown in Fig. 5. The principle used to derive the characteristics is illustrated in Fig. 6. The I_1Z quantity is a voltage proportional to the positive sequence current in the line. This voltage is obtained from the current network. The tap setting of this quantity establishes the base reach of the SLLP52A relay. The V_1 quantity is the positive sequence voltage at the relay location. The quantity (I_1Z - V_1) is the phasor

difference between these two quantities. I_1Z' is the reverse reach of the relay. The quantity $(I_1Z' + V_1)$ is the phasor sum of I_1Z' and V_1. The timer setting for the characteristics shown in Fig. 6 is 4.15 milliseconds which corresponds to an angle of 90 degrees. The angle B between $(I_1Z - V_1)$ and $(I_1Z' + V_1)$ is less than 90 degrees for an impedance point internal to the relay characteristic, equal to 90 degrees at the balance point and greater than 90 degrees for an external impedance point for which the relay should not operate. The quantities V_1 and I_1Z are the relay quantities which are converted into blocks of voltage representing the quantities $(I_1Z - V_1)$ and $(I_1Z' + V_1)$. The coincidence of these blocks is then measured. Blocks which are 90 degrees apart are coincident for 4.15 milliseconds. Blocks which are less than 90 degrees apart are coincident for more than 4.15 milliseconds. Blocks which are more than 90 degrees apart are coincident for less than 4.15 milliseconds. The mho function consists of a filter card, a coincidence card, and a timer to measure the coincidence of $(I_1Z - V_1)$ and $(I_1Z' + V_1)$. This circuit is shown in Fig. 3.

LOB FUNCTION

The LOB function is comprised of three offset mho characteristics which do not pass through the origin on the R-X diagram (Fig. 12). Relay operation occurs when the angle between $(I_1Z - V_1)$ and $(I_1Z' + V)$ is equal to some angle $\emptyset$ determined by the settings of the three timers.

The angle of maximum reach of the LOB function is the same as the relay system angle. This angle is normally set to be equal to the line angle. If the 100 percent voltage tap of LOB is used, the reach of the relay at the angle of maximum reach is equal to 1.33 times the basic minimum ohmic tap selected. If an LOB voltage tap other than 100 percent is chosen, the relay reach is increased in inverse proportion to the voltage tap. For example, if the 50 percent tap is used, relay operation still occurs for the same voltage applied to the measuring circuit, but since the line voltage is now twice this amount, the relay reach is doubled. The LOB reach, at the angle of maximum reach, may be calculated from the expression:

$$Z_{MAX} = \frac{1.33\ T_B}{T} \times 100$$

where,

T = Voltage restraint tap setting expressed in percent
T_B = Basic minimum ohmic tap setting

The V_1 used with I_1Z may be adjusted separately from the V_1 used with I_1Z'. The forward (along the protected line) taps are identified as LOB, and the reverse (away from the protected line) taps are identified as LOB*. These are one percent voltage taps in both directions.

CIRCUIT DESCRIPTION

LOB FUNCTION

The F153 (60 hertz) or F152 (50 hertz) filter card (position A) is supplied with three inputs I_1Z, (+ V_1) and (- V_1). The resistors R7 and R8 (Fig. 3) provide the 1.33 multiplying factor for I_1Z. The outputs of the filter cards are 30 volt DC square waves (minus 15 volts DC to plus 15 volts DC) which have the same phase relationship as (I_1Z' + V_1) and (- (I_1Z - V_1)).

The C101 coincidence measurement card (position B) compares the positive half-cycle of one square wave with the negative half-cycle of the other; when both are present simultaneously an output is produced. The output blocks are thereby produced when (I_1Z' + V_1) and (I_1Z - V_1) are coincident. These waveforms are shown in Fig. 7.

The output blocks of the C101 card are the inputs to the three T101 timer cards (positions C, D and E). The timer cards produce an output when the width of the input blocks exceeds the pickup time of the timer. At angles other than the line angle, a shorter timer setting results in a greater reach than a longer setting at the same fault angle. At the line angle, the reach does not vary with timer setting.

LOGIC CIRCUITS

The operating principles of the SLLP52A relay are best described in terms of a function diagram consisting of logic symbols interconnected by formation of flow paths as shown in Fig. 3. The legend for symbols used is shown in Fig. 8.

The R-X diagram of Fig. 9 shows three LOB characteristics and the locus of an assumed out-of-step swing impedance. The proper operation of the scheme depends upon the impedance entering the OUTER LOB characteristic and passing into the INNER LOB characteristic with the proper timing between characteristics. Once the swing has entered the INNER LOB characteristic, the decision is made to trip. The choice to trip immediately or to delay tripping until the swing has passed through the OUTER LOB characteristic again is made by the position of link L3. It should be noted that tripping will take place regardless of the direction which the swing leaves the OUTER LOB characteristic.

The operation of the logic is explained in the following paragraphs.

STEP 1

The power swing enters the OUTER LOB characteristic. Thus AND61 will have one input from the OUTER LOB and a second input from OR61 since NOT61 has no input. If the swing impedance remains between the OUTER and MIDDLE LOB characteristics for the pickup setting of TL61, TL61 operates, seals in one input of AND61 and provides an out-of-step blocking signal at pin 276.

On the occurrence of a fault, the OUTER and MIDDLE LOB's would have operated almost simultaneously, the MIDDLE LOB would have blocked AND61 through NOT61 and prevented TL61 from picking up.

STEP 2

The swing now enters the MIDDLE LOB characteristic but remains outside the INNER LOB characteristic. One input of AND62 is energized by TL61, a second input is provided by the MIDDLE LOB, and the last is supplied by NOT62. If the swing impedance remains between the MIDDLE and INNER LOB characteristics long enough for TL62 to pick up, TL62 provides two inputs to AND62. AND62 is thereby controlled by TL61, which is, in turn, controlled by the OUTER LOB characteristic.

STEP 3

The swing now enters the INNER LOB characteristic. One input to AND63 is provided by TL62, the second by the INNER LOB, and the third from an overcurrent unit. If the swing impedance remains inside the INNER LOB characteristic for the pickup setting of TL63, TL63 provides two inputs to AND63. Thus AND63 is dependent solely on TL62.

At this point the decision to trip has been made and sealed in. The out-of-step tripping output will be provided immediately if link L3 is in the TRIP IN position (1-2).

STEP 4

The swing now leaves the INNER LOB characteristic in any direction, but remains inside the MIDDLE LOB characteristic. One input to AND64 is provided by TL63, a second input is supplied by the OUTER LOB, the third input is energized by NOT62 through OR64. If the output from AND64 lasts for the pickup setting of TL64, TL64 provides two inputs to AND64. The third input is supplied by TL63. The output of TL64 also energizes one input of AND65.

STEP 5

With link L3 in the TRIP OUT position (1-3), tripping is not initiated until the swing has passed through the OUTER LOB characteristic for the second time. When the OUTER LOB resets, the second input of AND65 is supplied by NOT63. AND65, through OR65, provides an out-of-step tripping output at pin 278. This output lasts for 50 milliseconds after the OUTER LOB drops out, this is the drop-out time of TL61.

The SLLP52A relay contains an option to use two LOB characteristics instead of three. In order to remove the middle characteristic, it is necessary to place links L1 and L2 in the (1-2) position and remove the cards in positions D, H, and P.

The SLLP also provides for mho supervision by an associated distance relay, if provided. With link L4 in the 1-3 position, a pickup of the distance relay can block out-of-step blocking and tripping via C274.

Contact converter CC7 is provided as an input to block out-of-step tripping, if such a blocking signal is received by the relay. CC7 can be set to accept contact input signals of 48, 125 or 250 volts DC by adjustment of the link on the A120 card in position AG. Contact converter inputs are brought in through terminal strip connection YK11 (+) and YK12 (-) on the back of the SLLP.

Four electrically separate reed relay contacts are available for monitoring the pickup of the outer (two contacts), middle (one contact) and inner (one contact) characteristics. The contacts are wired out through a ten-point socket connection located on the back of the SLLP.

The reed relays have ratings shown on the following table:

ABSOLUTE MAXIMUM RATINGS	
10 VA Resistive 3 VA Inductive**	Interruption Capacity
0.5 Ampere make and carry continuous 0.5 Ampere make and carry short time	

**The inductive rating is based on the inductance of a coil having an X_L/R ratio of three-to-one.

Reed relay contact outputs can be provided in either normally open or normally closed configuration. The contacts operate within 0.5 millisecond from the time logic signals from the characteristic timers change state.

The D101 card in position AJ provides current level detection for supervision of out-of-step tripping.

OPERATING CHARACTERISTICS

The operate and reset time of the LOB function is basically determined by the characteristic timers, the type of fault and the incidence angle. There is no significant time delay in the circuitry ahead of the timer.

For a timer setting of 4.15 milliseconds, the maximum operating time is 12 milliseconds, and the minimum operating time is 4.15 milliseconds.

A phase current of one ampere (five ampere relay) or 0.2 ampere (one ampere relay) on a three phase fault will cause the SLLP52A relay to pull back to no less than 90 percent of the nominal reach, with the basic ohmic tap setting (T_B) of three ohms (five amperes) or 15 ohms (one ampere).

RECEIVING, HANDLING AND STORAGE

These relays will normally be supplied as part of a static relay equipment, mounted in a rack of cabinets with other static relays and test equipment. Immediately upon receipt of a static relay equipment it should be unpacked and examined for any damage sustained in transit. If injury or damage resulting from rough handling is evident, file a damage claim at once with the transportation company and promptly notify the nearest General Electric Sales office.

Reasonable care should be exercised in unpacking the equipment. If the equipment is not to be installed immediately, it should be stored indoors in a location that is free from moisture, dust and metallic chips, and severe atmospheric contaminants.

Just prior to final installation the shipping support bolt should be removed from each side of all relay units, to facilitate possible future unit removal for maintenance. These shipping support bolts are approximately eight inches back from the relay unit front panel. STATIC RELAY EQUIPMENT, WHEN SUPPLIED IN SWING RACK CABINETS, SHOULD BE SECURELY ANCHORED TO THE FLOOR OR TO THE SHIPPING PALLET TO PREVENT THE EQUIPMENT FROM TIPPING OVER WHEN THE SWING RACK IS OPENED.

INSTALLATION TESTS

CAUTION

THE LOGIC SYSTEM SIDE OF THE DC POWER SUPPLY USED WITH MOD III STATIC EQUIPMENT IS ISOLATED FROM GROUND. IT IS A DESIGN CHARACTERISTIC OF MOST ELECTRONIC INSTRUMENTS THAT ONE OF THE SIGNAL INPUT TERMINALS IS CONNECTED TO THE INSTRUMENT CHASSIS. IF THE INSTRUMENT USED TO TEST THE RELAY EQUIPMENT IS ISOLATED FROM GROUND, ITS CHASSIS MAY HAVE AN ELECTRICAL POTENTIAL WITH RESPECT TO GROUND. THE USE OF A CONNECTION TO THE EQUIPMENT, SUCH AS A TEST LEAD INADVERTENTLY DROPPING AGAINST THE RELAY CASE, MAY CAUSE DAMAGE TO THE LOGIC CIRCUITRY.

NO EXTERNAL TEST EQUIPMENT SHOULD BE LEFT CONNECTED TO THE STATIC RELAYS WHEN THEY ARE IN PROTECTIVE SERVICE, SINCE TEST EQUIPMENT GROUNDING REDUCES THE EFFECTIVENESS OF THE ISOLATION PROVIDED.

CONSTRUCTION

The SLLP52A relay is packaged in an enclosed metal case with hinged front cover and removable top cover. The case is suitable for mounting on a standard 19-inch rack. The outline and mounting dimensions of the case and the physical location of the components are shown in Fig. 1 and 2, respectively.

The tap blocks for making the voltage restraint settings are located on the front panel of the unit. The method of making restraint tap settings is illustrated in Fig. 10. The connections are made by means of taper pin connectors; special tools are supplied with each equipment for the removal and insertion of these pin connectors.

The current and potential enter the SLLP52A on twelve-point terminal strips located on the rear of the relay case. The potential connections are made on the YK terminal strip, the current connections on the YL terminal strip.

The basic minimum ohmic tap (T_B) setting is accomplished on the YL terminal strip on the rear panel of the unit. The current connections for the one ohm/five ohm and three ohm/fifteen ohm taps are shown in Table I.

TABLE I

	I_C		I_B		$3I_0$	
	IN	OUT	IN	OUT	IN	OUT
1 OHM OR 5 OHM BASE REACH	YL1	YL2	YL4	YL6	YL9	YL10
3 OHM OR 15 OHM BASE REACH	YL1	YL3	YL5	YL7	YL8	YL10

The V_1 and I_1Z test jacks, the I_1Z magnitude reach pot (P5), and the angle pot (P6) for the relay system reach are located on the front of the unit.

NOTE: On relay form 1 through 4, P5 and P6 are located inside the relay case.

The positive sequence filter potentiometers (P1, P2, P3 and P4) are located inside the relay case as shown in Fig. 2.

The SLLP52A relay also contains printed circuit cards identified by a code number such as F146, C104 D101, T133, N112, where F designates filter, C designates coincidence, D designates level detector, T designates time delay and N designates network. The printed circuit cards plug in from the front of the unit. The sockets are identified by letter designations or "addresses" (D, E, F, etc.) which appear on the guide strips in front of each socket, on the component location diagram, on the internal connection diagram, and on the printed circuit card itself. The tests points (TP1, TP2, etc.) shown on the internal connection diagram, are connected to instrument test jacks on test card positions T and AT with TP1 at the top. The internal connections of the printed circuit cards may be found in the printed circuit card instruction book, GEK-34158.

Pin number 1 on the test card in position AT is connected to relay reference, number 2 to minus 15 volt DC and pin number 10 to plus 15 volt DC. Output signals are measured with respect to the reference bus on the test card (TP1). Logic signals are approximately plus 15 volt DC for the ON or LOGIC ONE condition, and less than one volt DC for the OFF or LOGIC ZERO condition. Filter card outputs are either plus 15 volt DC or minus 15 volt DC for the ON condition.

These outputs can be monitored with an oscilloscope, a portable high-impedance DC voltmeter, or the test panel voltmeter if available. When the test panel meter is supplied, it will normally be connected to the reference bus. Placing the relay test lead in the proper test point pin jack will connect the meter for testing. When time-delay cards are to be adjusted or checked, an oscilloscope which can display two traces simultaneously and which has a calibrated horizontal sweep should be used.

The links (L1, L2, L3 and L4), which are used to select the logic options, are mounted on the rear of the unit as shown in the component location diagram in Fig. 2.

CALCULATION OF SETTINGS

The following description on determination of settings assumes that three LOB characteristics are utilized.

OUT-OF-STEP BLOCKING

Out-of-step blocking results when the swing locus passes from the outer to the middle characteristic in a time equal to or greater than the pickup setting of the A/50 timer. Therefore, proper out-of-step blocking operation requires that the middle characteristic of the SLLP52A surround the largest tripping function characteristic for which out-of-step blocking is required. However, this criteria may not be practical due to other considerations, and in many instances the middle characteristic must be set inside the limiting trip characteristic. If the trip characteristic should extend past the middle MOB characteristic, the swing locus could conceivably plot inside the trip characteristic before the A/50 timed out. In this case the pickup setting of the A/50 must be based on the time it takes the swing to pass from the outer LOB characteristic to the trip characteristic.

OUT-OF-STEP TRIPPING

The preferred sequence of determining characteristic reach and included angle (that is, 2-7/9 timer pickup settings) begins with the inner characteristic. The inner characteristic is set as narrow as possible; an included angle of larger than 150 degrees is not permissible since the characteristic may become unstable for a narrower setting. A second consideration for the inner characteristic is that it should be set inside any swing for which the system could recover. The 150 degree unstable point is usually the limiting case.

The reason for setting the inner characteristic as narrow as possible is so that an adequate separation-angle differential between the outer and inner characteristics can be selected allowing reasonable TL62, TL63 and TL64 timer settings for possible fast swings. The setting of the outer characteristic is now determined from system swing studies and a consideration of breaker operating capability. The outer characteristic should be set large enough so that when it resets, the breaker that is tripped will not have to interrupt an out-of-phase condition of greater than 90 degrees between the two systems. Considering only the breaker interrupting capability, the optimum setting of the outer characteristic for the simple system of Fig. 4 would be:

(forward reach) LOB = B

(reverse reach) LOB* = A

4.167/5 timer setting

The forward and reverse reaches are exactly at the respective ends of the system. This surrounds the system with a circle of diameter AB which is the loci of the 90 degree separation angles for all ratios of E_A/E_B. The angles of maximum reach of LOB and LOB* are the same as the system reach angle. On the basis of system swing studies, the known setting of the inner characteristic, the range of settings on the TL62, TL63 and TL64 timers, and the included angle of the outer characteristic must be selected to permit reasonable TL62, TL63 and TL64 timer settings. If the swing is fast, the outer characteristic must have a smaller included angle (larger setting) as compared to a slower swing setting. If the swing study indicates an included angle of greater than 90 degrees, the breaker interrupting duty should become the limiting factor and a 90 degree characteristic would result. If the swing study indicates an included angle less than 90 degrees, then this criteria becomes the limiting factor. However, the outer characteristic should not be set so large that it picks up on maximum load transfer across the line. The middle characteristic setting is between the inner and outer, and if TL62 and TL63 pickup time allow, it should be set outside the largest tripping element for which out-of-step blocking is desired.

With all the characteristics determined, the TL61, TL62, TL63 and TL64 pickup times may be set. The actual timer pickup values have already been considered in selecting characteristic sizes in conjunction with system swing studies. These timer settings are graduated to some extent, since as the swing enters the outer characteristic, its speed will probably be increasing.

Considering the simplified system of Fig. 5, the sequential procedure is as follows:

(a) Establish LOB and LOB* reaches

For the example assume that the best values of LOB and LOB* on a per-unit basis are:

LOB = 15

LOB* = 5

(b) This establishes the reach settings as close as possible to the end points of the system. Determine the value of the included angle, β_3, of the inner characteristic. For this example the stability limit criteria of $\beta_3 = 150^o$ is selected.

$$\beta_3 = 150^o$$

(c) Set the inner characteristic 2-7/5 timer pickup time to:

$$P.U. = (\beta_3/360^o)\ (16.67\ ms)$$

$$P.U. = 6.95\ ms$$

(NOTE: The pickup times calculated are approximate values. To determine accurately that the desired included angle has been achieved with a particular pickup setting, the characteristic should be plotted and a graphical verification of the angle made.)

(d) Determine the value of the included angle, β_1, of the outer characteristic. Here it is assumed that system swing studies and load considerations have dictated an angle of

$$\beta_1 = 70^o$$

(e) Set the outer characteristic 2-7/5 timer pickup time to:

$$P.U. = (\beta_1/360^o)\ (16.67\ ms)$$

$$P.U. = 3.24\ ms$$

(f) Determine the value of the included angle, β_2, of the middle characteristic. Here the angle β_2 is chosen as 100 degrees to position the middle characteristic approximately half way between the inner and outer characteristics.

$$\beta_2 = 100^o$$

(g) Set the middle characteristic 2-7/5 timer pickup time to:

$$P.U. = (\beta_2/360^o)\ (16.67\ ms)$$

$$P.U. = 4.63\ ms$$

(h) Set the pickup times of the TL61, TL62, TL63 and TL64 timers based on system swing studies.

TESTS AND ADJUSTMENTS REQUIRED

The SLLP52A relay is usually supplied from the factory mounted and wired as part of a complete static relay equipment. The relay includes the following adjustments, some of these have been preset at the factory, others must be set by the user. The factory adjustments should be rechecked by the user per the procedures under DETAILED TESTING INSTRUCTIONS to insure that no shipping damage has occurred. The steps must be performed in the order shown.

1) Basic minimum ohmic tap setting (user setting)
2) Voltage restraint tap setting (LOB and LOB* reach) (user setting)
3) Network general calibration check (user check).

NOTE: If this step does not give the results indicated, four additional checks are necessary before proceeding. These checks will enable the user to determine which part of the networks require readjustment. The checks are:

a. Voltage sequence network balance and output
b. Current sequence network balance and output
c. Current sequence network output magnitude adjustment (P5)
d. Relay system reach angle adjustment (P6).

4) Positioning of links (user setting)
5) Current level detector setting (user setting)
6) LOB characteristic plotting on an R-X diagram (user check)
7) Timer settings (user setting)

DETAILED TESTING INSTRUCTIONS

Basic Minimum Ohmic Tap Setting

The arrangement of the basic ohmic taps is described under CONSTRUCTION, and the choice of tap setting is discussed in separate write-up entitled OVERALL LOGIC DESCRIPTION. The reach at the relay system angle is given by the following relationship:

$$Z = \frac{1.33\ T_B}{T} \times 100$$

$$Z^* = 1.33\ T_B \times \frac{100}{T^*}$$

where:

T = Voltage restraint tap setting expressed in percent, FWD

T_B = Basic minimum ohmic tap setting

Z = Relay reach in the forward direction

T^* = Voltage restraint tap setting expressed in percent, REV

Z^* = Relay reach in the reverse direction

Voltage Restraint Tap Setting

The arrangement of the voltage restraint tap blocks is described under CONSTRUCTION, and the choice of tap setting is discussed in a separate write-up entitled OVERALL LOGIC DESCRIPTION. The pickup voltage at the relay system angle is given by the following relationship:

$$V_1 = \frac{I_1 \times 1.33 \times T_B \times 100}{T}$$

where:

T = Voltage restraint tap setting expressed in percent

T_B = Basic minimum ohmic tap setting

I_1 = Positive sequence current

Tap setting of LOB adjusts forward reach and LOB* adjusts reverse reach.

General Network Calibration Check

Be sure the DC power supply to the SLLP is turned on. This is a check of both the voltage and current network balances and network output calibration. Perform the checks as outlined in Fig. 13. If the required outputs cannot be obtained, it is an indication that the original network adjustments have been disturbed. The following four checks are required only if the network adjustments have been disturbed.

1. Voltage Sequence Network Balance

   This test, described in Fig. 14, consists of two parts, V_1 null and V_1 output checks. It should be noted that this test requires a three-phase test source of equal voltages (within one to two percent). Alternate readjustment of pots P1 and P2 is required to obtain the 60 or 50 hertz null since the pots are interdependent. When the fundamental frequency has been completely nulled, it is normal for some harmonic voltage to be evident at the test jack, V_1. The magnitude of the harmonic voltage depends on the harmonic content of the test source, but usually is less than 0.2 V_{p-p}.

   When performing the V_1 output tests, the exact value of voltage obtained will vary from relay to relay depending on component tolerances, but will be approximately as shown in Fig. 14. This value should be noted very precisely since it is the reference for making another setting in this relay equipment.

2. Current Sequence Network Balance

   This test, described in Fig. 15, consists of two parts, I_1Z null and I_1Z output checks. Ammeters used in this test should first be calibrated in series to insure that the current used in each phase of the test circuit is equal. Alternate readjustment of pots P3 and P4 is required since they are interdependent. Adjust for 60 or 50 hertz null leaving only harmonic voltage at the I_1Z test jack. Also check that the I_1Z output is approximately as shown in Fig. 15. The exact value will be set in the next step.

3. Current Sequence Network Output Magnitude Adjustment

   NOTE: The DC power supply to the SLLP relay must be on for this test and adjustment. Use the test circuits of Fig. 16 and adjust P5 until the I_1Z magnitude is equal to the V_1 magnitude. Pot P5 is the I_1Z magnitude adjustment.

4. Relay System Reach Angle Adjustment.

   The DC power supply must be turned on for this test. Use test Fig. 16 and adjust P6 until the I_1Z and V_1 quantities are exactly in phase. Pot P6 is the I_1Z angle adjustment. Since there is some interaction between P5 and P6, it may be necessary to readjust P5 at this time to maintain an I_1Z magnitude equal to V_1. The magnitude should be recorded at this time for use later in rechecking this relay.

Positioning of Links

The arrangement of the links is described under **CONSTRUCTION** and the choice of link settings is described in the section **CIRCUIT DESCRIPTION.**

Current Level Detector Setting

The current level detector is a supervisory input to the out-of-step tripping logic. The level detector is on the D101 card in position AJ. The pickup level of D101 is adjusted by adjustment of the associated P1 pot. Turning P1 clockwise increases pickup level, counterclockwise decreases pickup level.

To set D101 pickup level use the test #2 circuit of Fig. 15. D101 pickup can be monitored by an oscilloscope with channel A pickup connected to TP19 of the SLLP. Connect scope reference to TP1 of the SLLP.

LOB Characteristic Plotting

Each of the relay characteristics may be checked over its entire range by using the test circuit of Fig. 16. By setting the current in each branch for constant relay rated current, the reach at any angle becomes a function of the calculated settings of both the base reach and the voltage restraint taps. Rotating the phase shifter provides a means of checking the reach on any point of the characteristic.

To obtain any points on the relay characteristic, observe the following procedure:

1. Set up the test circuit of Fig. 12.

2. Set currents to relay rated current (five amperes/or one ampere RMS).

3. Connect the instrumentation (preferably an oscilloscope) between the characteristic output test point (TP_) and reference TP1.

   The test points for the characteristics are as follows: TP3 (outer), TP5 (middle), TP6 (inner).

4. Set phase angle meter at the specific angle of interest by rotating the phase shifter.

5. Adjust the gang variac until the characteristic function output fully picks up. Note that the point just at the verge of pickup, as read on the voltmeter (V), defines the characteristic.

All necessary points can be obtained by simply repeating Steps 4 and 5 until the characteristic is clearly defined.

TIMER ADJUSTMENTS AND TESTS

LOB Time-delay Cards

These cards should not be adjusted unless a plot of the mho characteristic indicates an improper pickup time or if the reset time is too short to produce a continuous logic signal.

In the SLLP52A relay, the pickup time of each of the three LOB timers (positions C, D and E) is adjustable between two and seven milliseconds. The setting determines the shape of the mho characteristic. Increasing the timer pickup setting tends to narrow the characteristic; decreasing the setting widens the characteristic. The reset time delay (drop-out time) of the timer provides an overlap of the next half-cycle measurement and produces a continuous logic signal.

The following procedure may be used to set characteristic timers for six milliseconds or less; for timer settings greater than six milliseconds the procedure outlined under Logic Time-delay Cards must be used.

Connect current and voltage inputs as described in Fig. 16. Place appropriate timer card in a card adapter. Reduce the applied voltage until the swing condition applied to the relay is within the relay characteristic. Connect timer card input (pin 3) to one channel of the oscilloscope and the timer card output (pin 8) to the second channel.

Input to the timer card should be blocked slightly longer than the desired pickup delay (if necessary, adjust the applied AC voltage to obtain this). In order to observe the operating delay time, the reset time must be reduced (turn P3 counter-clockwise so that the timer resets each half-cycle). The operating delay time can now be measured on the oscilloscope. Adjust P2 to obtain the desired pickup delay time (turn P2 clockwise to increase pickup time). The reset time should then be adjusted until the output becomes continuous. P2 should be adjusted one full turn clockwise after the output becomes continuous. The mho characteristic should be plotted and compared to the desired characteristic. Readjust the timer if necessary to obtain the desired characteristic.

Logic Time-delay Cards

Time-delay cards are provided in the logic circuit to coordinate the operation of the SLLP52A. In order to test the timer cards, it is necessary to remove the card previous to the timer and to place the timer card in a card adapter. The timer test circuit is shown in Fig. 11. Opening the normally closed contact causes the output to step up to plus 15 volts DC after the pickup delay of the timer. To increase the pickup time turn the upper potentiometer on the timer card clockwise. Closing the contact causes the timer output to drop out after the reset time-delay setting of the card. If

the timer card is provided with a variable reset delay, it can be adjusted by the lower potentiometer on the timer card (clockwise increases reset time).

TABLE II

TIMER	POSITION	REMOVE CARD IN POSITION
TL61	N	J
TL62	P	K
TL63	S	L
TL64	R	F

PERIODIC CHECKS AND ROUTINE MAINTENANCE

PERIODIC TESTS

All functions included in the SLLP52A relay may be checked at periodic intervals using the procedures described in the section covering DETAILED TESTING INSTRUCTIONS. Cable connections between the SLLP52A relay and the associated Type SLAT relay can be checked by observing the SLLP52A outputs at test points in the SLAT relay.

The following checks are suggested as periodic checks/routine maintenance.

1. Network General Calibration Check - See detailed testing instruction - General Network Calibration Check.

2. MHO Characteristic Plotting on R-X Diagram - See detailed testing instruction - MHO Characteristic Plotting

3. Current Level Detector Pickup Setting - See detailed testing instruction - Current Level Detector Adjustment.

TROUBLESHOOTING

In any troubleshooting of equipment, it should first be established which unit is functioning incorrectly. The overall logic diagram supplied with the equipment shows the combined logic of the complete equipment and the various test points in each unit. By signal tracing, using the overall logic diagram and the various test points, it should be possible to quickly isolate the trouble.

A test adapter card (0149C7259G2) is supplied with each static relay equipment to supplement the prewired test points on the test cards. Use of the adapter card is described in the card instruction book, GEK-34158.

A dual-trace oscilloscope is a valuable aid to detailed troubleshooting, since it can be used to determine phase shift, operate and reset times, as well as input and output levels. A portable dual-trace oscilloscope with a calibrated sweep and trigger facility is recommended.

SPARE PARTS

To minimize possible outage time, it is recommended that a complete maintenance program should include the stocking of at least one spare card of each type. It is possible to replace damaged or defective components on the printed circuit cards, but great care should be taken in soldering so as not to damage or bridge-over the printed circuit buses, or overheat the semiconductor components. The repaired area should be recovered with a suitable high-dielectric plastic coating to prevent possible breakdowns across the printed buses due to moisture and dust. The wiring diagrams for the cards in the SLLP52A relay are included in the card book, GEK-34158; the card types are shown on the component location diagram, Fig. 3.

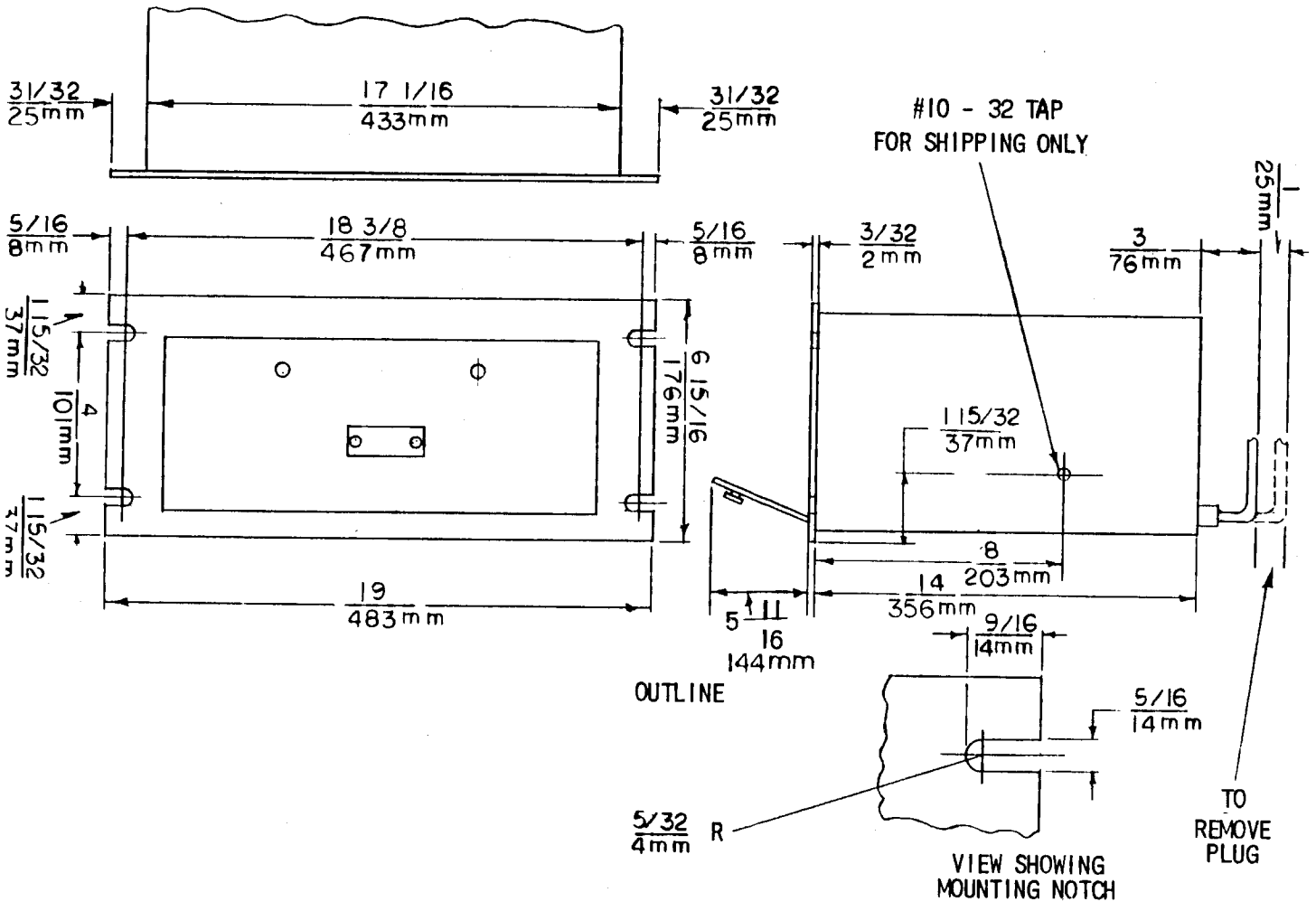


Fig. 1 (0227A2037-0) Outline and Mounting Dimensions for the Type SLLP52A Relay

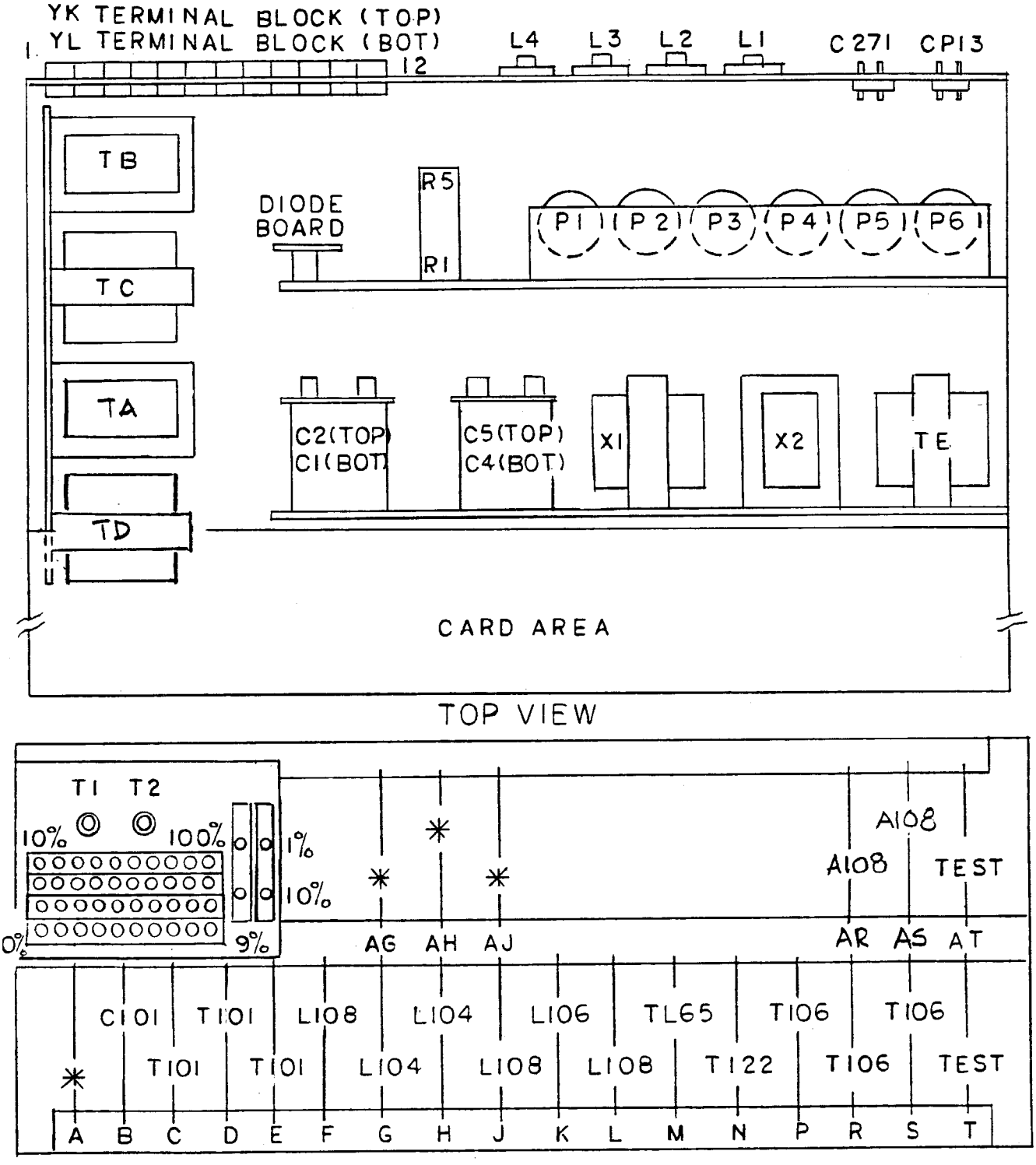
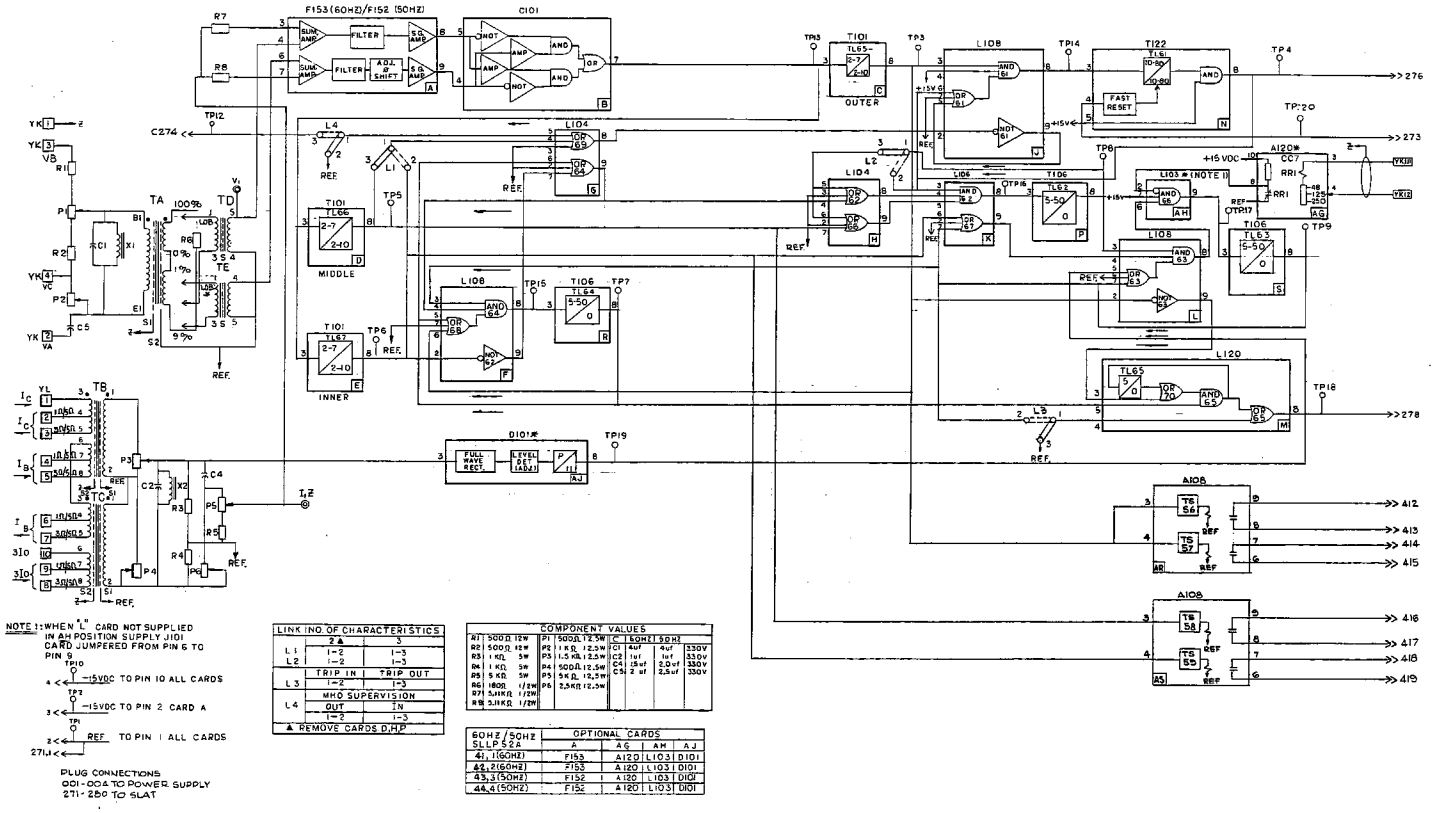


Fig. 2 (0285A5783-0) Component and Card Locations for the Type SLLP52A Relay



NOTE 1: WHEN "L" CARD NOT SUPPLIED IN AH POSITION SUPPLY J101 CARD JUMPERED FROM PIN 6 TO PIN 9

TP10 —15VDC TO PIN 10 ALL CARDS

TP2 —15VDC TO PIN 2 CARD A

TP1 REF TO PIN 1 ALL CARDS

271,1

PLUG CONNECTIONS
001-004 TO POWER SUPPLY
271-280 TO SLAT

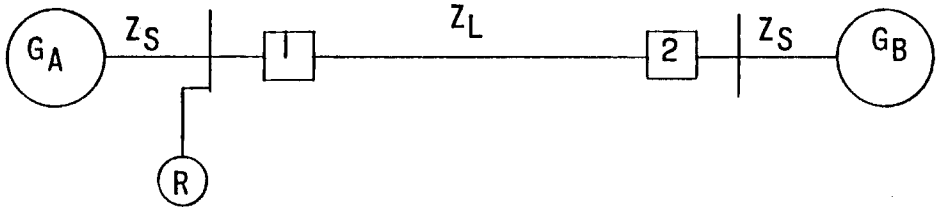
LINK INO OF CHARACTERISTICS		
	2 ▲	3
L1	1-2	1-3
L2	1-2	1-3
	TRIP IN	TRIP OUT
L3	1-2	1-3
	MHO SUPERVISION	
L4	OUT	IN
	1-2	1-3

▲ REMOVE CARDS D,H,P

COMPONENT VALUES						
R1	500Ω 12W	P1	500Ω 12.5W	C	50HZ	50HZ
R2	500Ω 12W	P2	1 KΩ 12.5W	C1	4uf	4uf 330V
R3	1 KΩ 5W	P3	1.5 KΩ 12.5W	C2	1uf	1uf 330V
R4	1 KΩ 5W	P4	500Ω 12.5W	C4	.15uf	2.0uf 330V
R5	5 KΩ 5W	P5	5KΩ 12.5W	C5	2 uf	2.5uf 330V
R6	180Ω 1/2W	P6	2.5KΩ 12.5W			
R7	5.1KΩ 1/2W					
R8	5.1KΩ 1/2W					

60HZ/50HZ SLLP52A	OPTIONAL CARDS			
	A	AG	AM	AJ
41,1(60HZ)	F153	A120	L103	D101
42,2(60HZ)	F153	A120	L103	D101
43,3(50HZ)	F152	A120	L103	D101
44,4(50HZ)	F152	A120	L103	D101

Fig. 3 (0145D8011-1) Internal Connections for the Type SLLP52A Relay



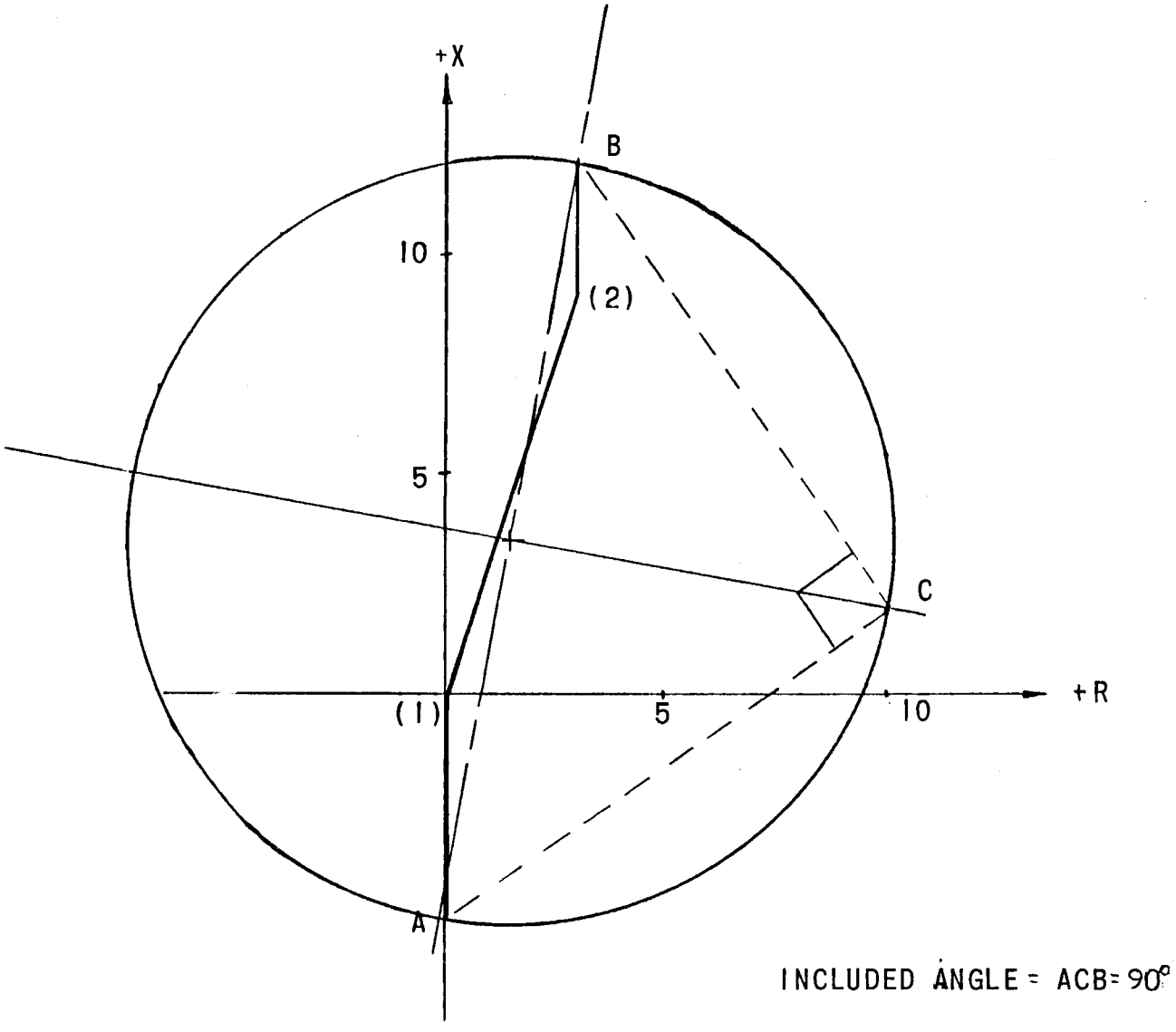


Fig. 4 (0227A2452-0) Optimal Setting for System Shown

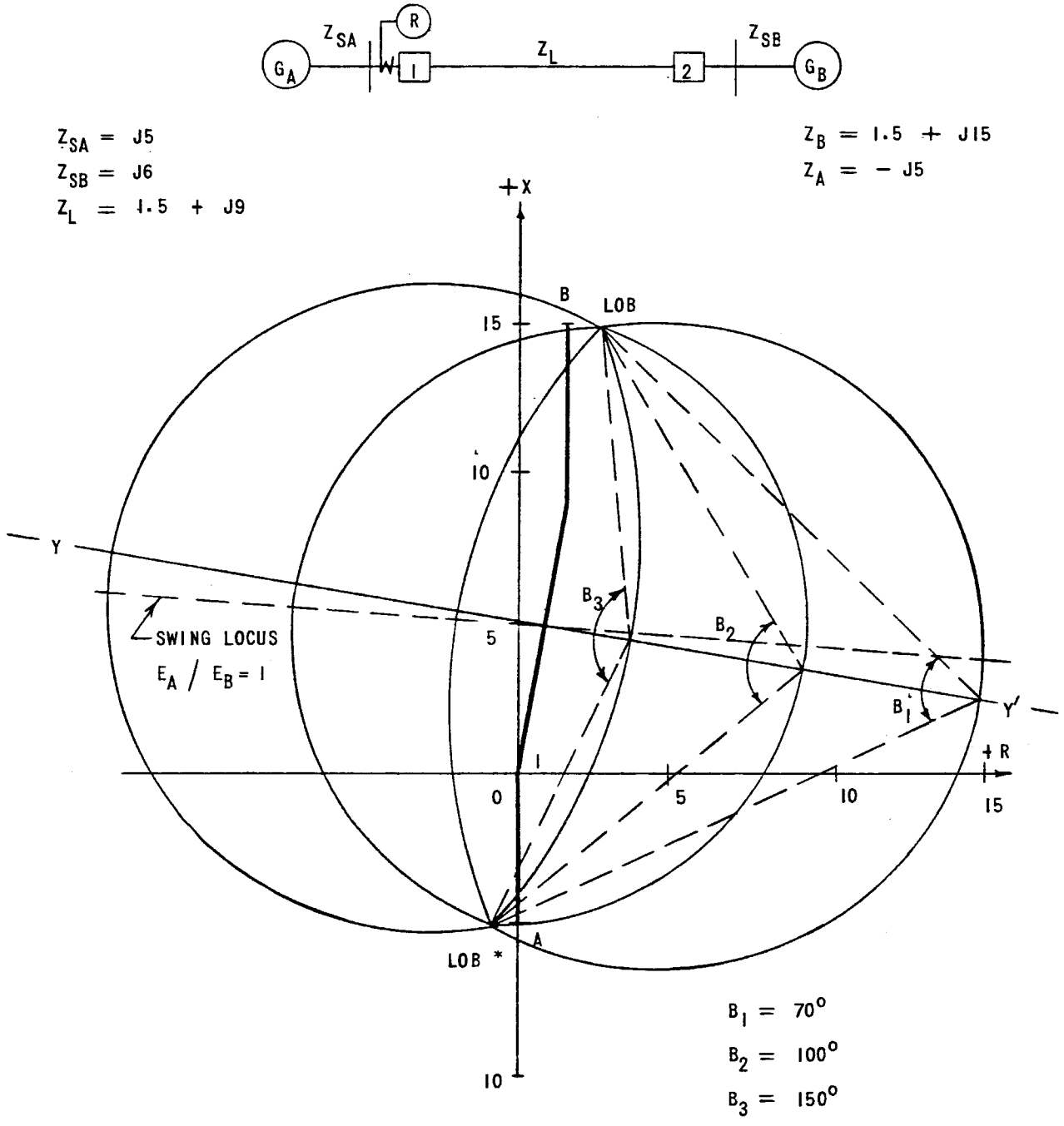


Fig. 5 (0246A7983-0) Practical SLLP52A Setting for System Shown

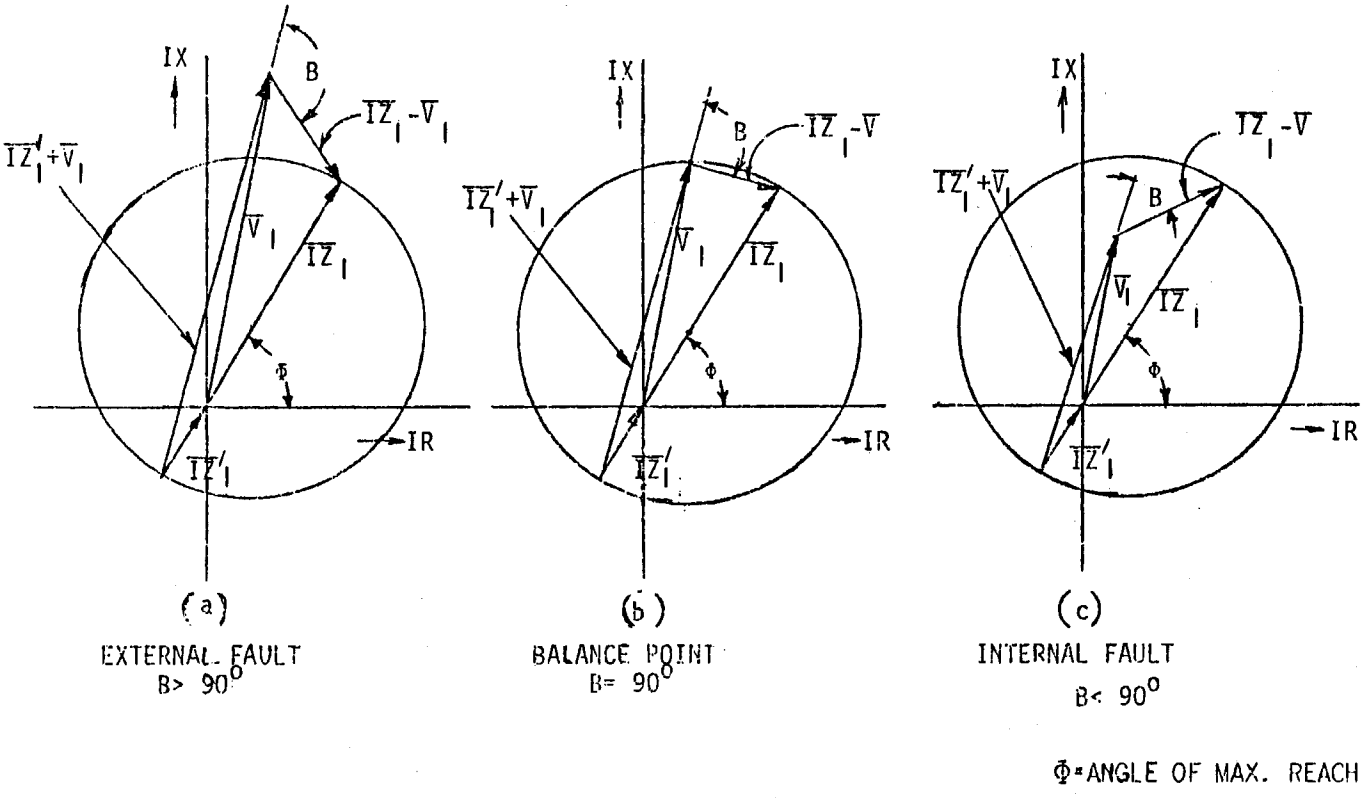


Fig. 6 (0246A7984-0) Offset Mho Characteristic by Phase Angle Measurement

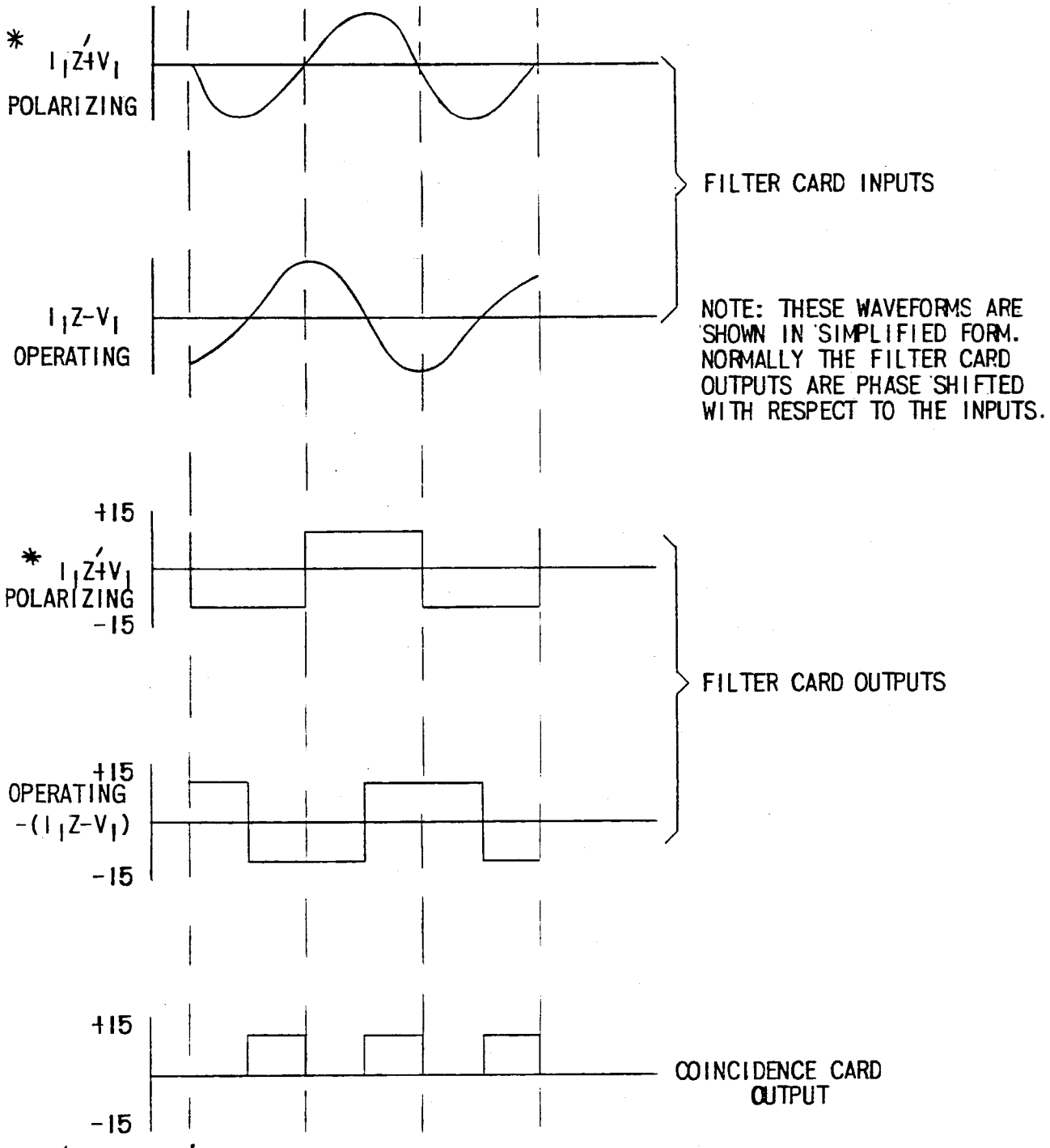


Fig. 7 (0246A7985-2) SLLP Operating Quantity Waveforms

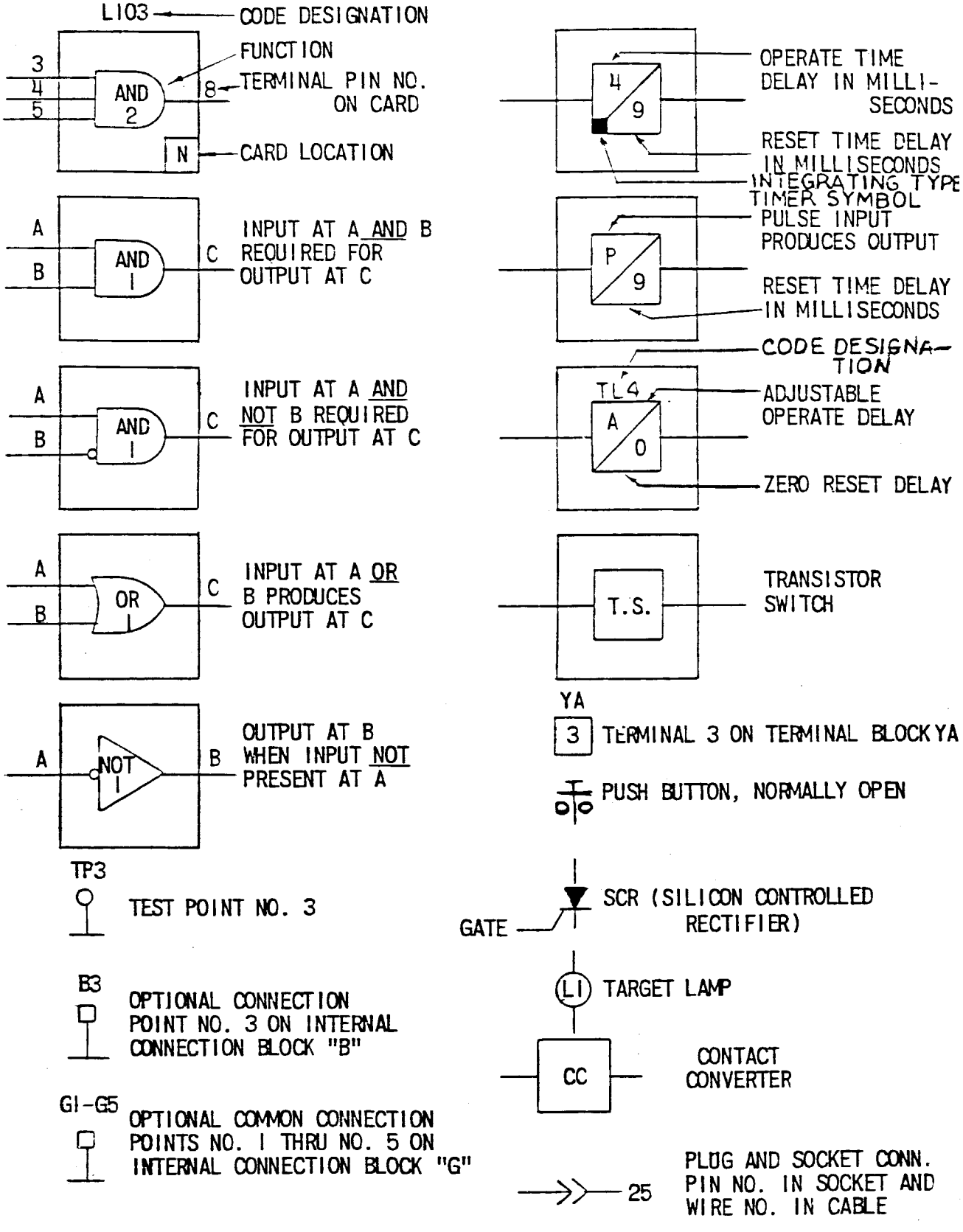


Fig . 8 (0227A2047-1) Logic and Internal Diagram Legend

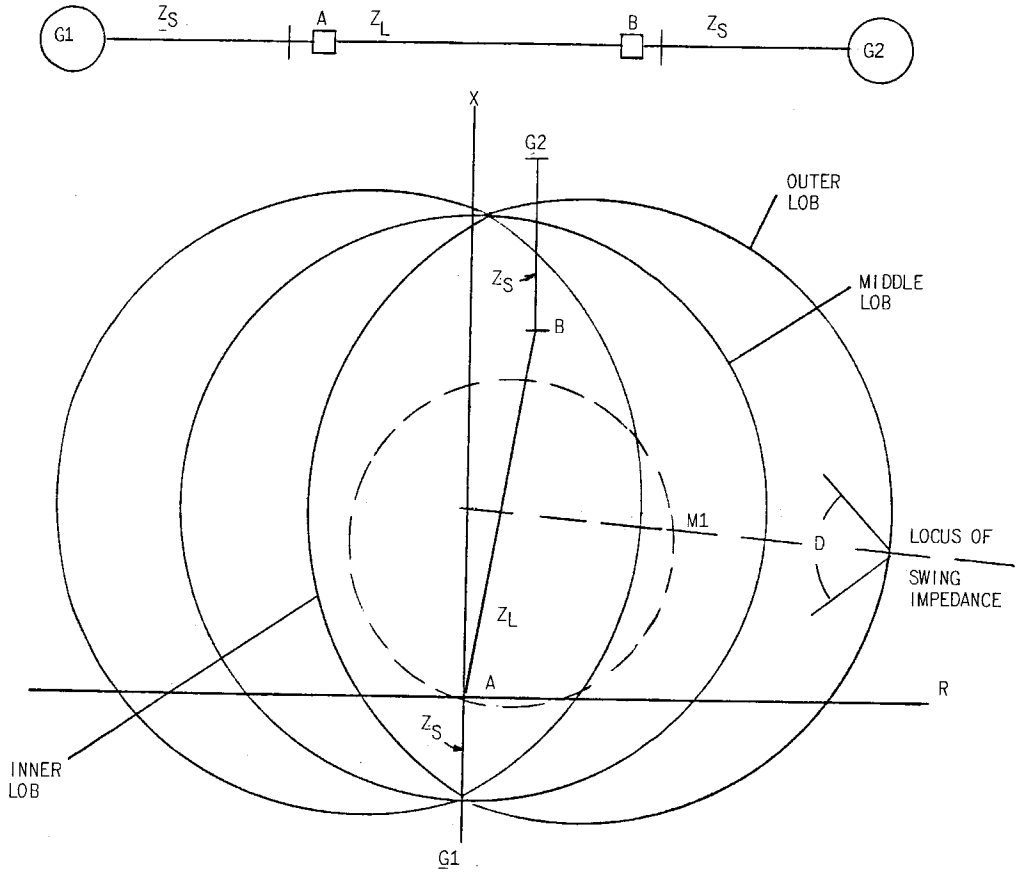
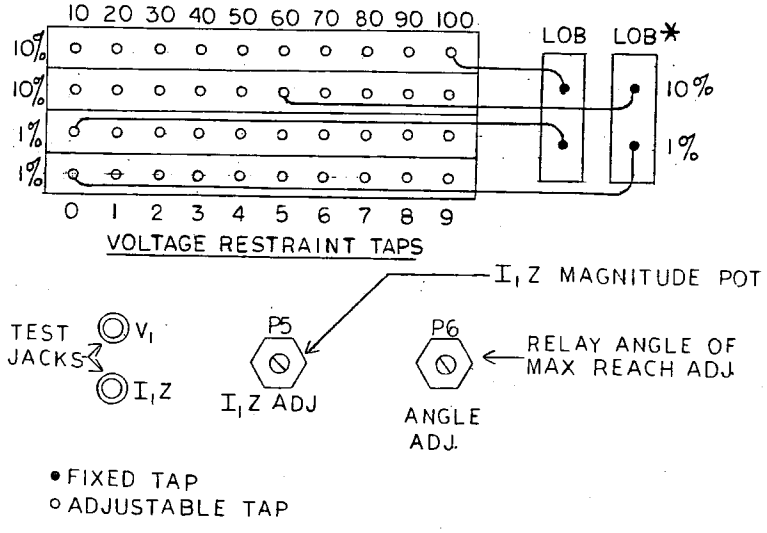


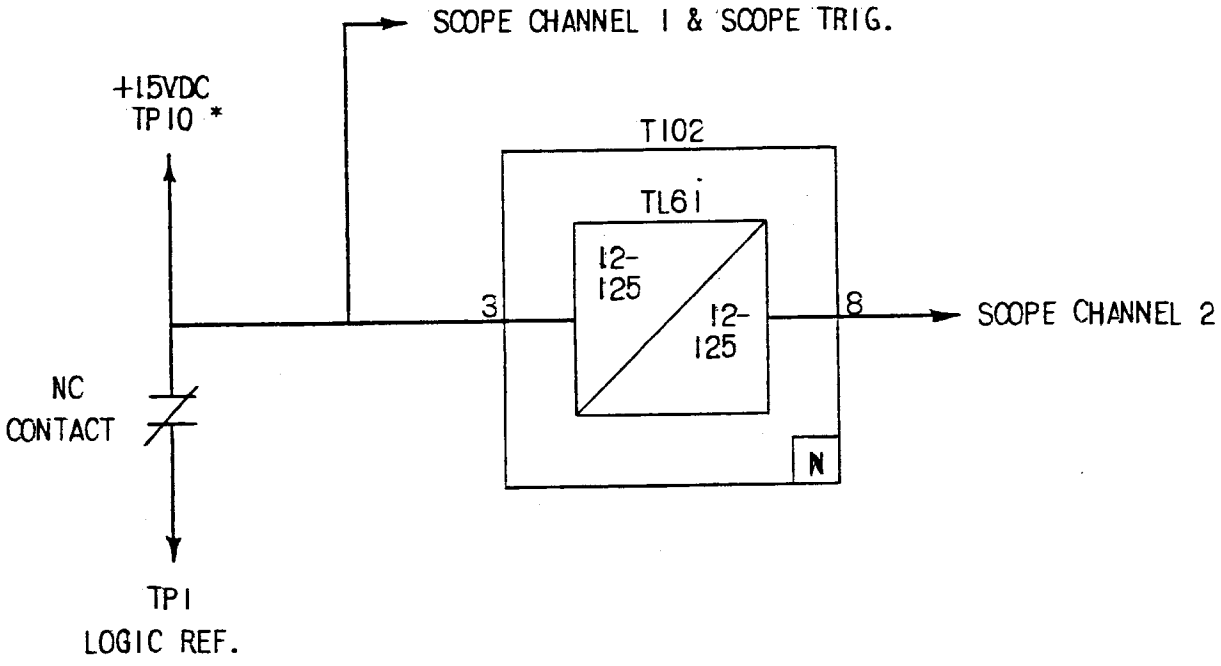
Fig. 9 (0227A2518-1) Typical SLLP Relay Settings on a System



LOB 100% VOLTAGE RESTRAINT TAP ILLUSTRATED
REACH = 1.33 x 1.00 TB
LOB * 60% VOLTAGE RESTRAINT TAP ILLUSTRATED
REACH = 1.33 x 1.67 TB

TB = BASIC MINIMUM OHMIC TAP SETTING

Fig. 10 (0285A6243-0) Typical SLLP Tap Block Connections



* THE 15VDC SIGNAL AT PIN 10 HAS A CURRENT LIMITING RESISTOR MOUNTED ON THE TEST CARD.

Fig. 11 (0246A7987-0) Logic Timer Test Circuit

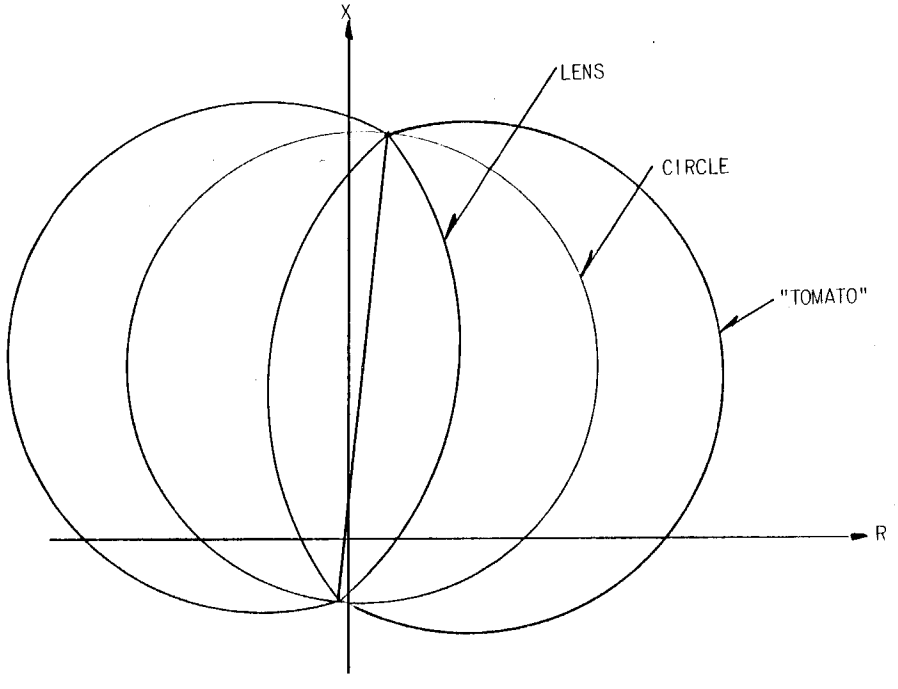
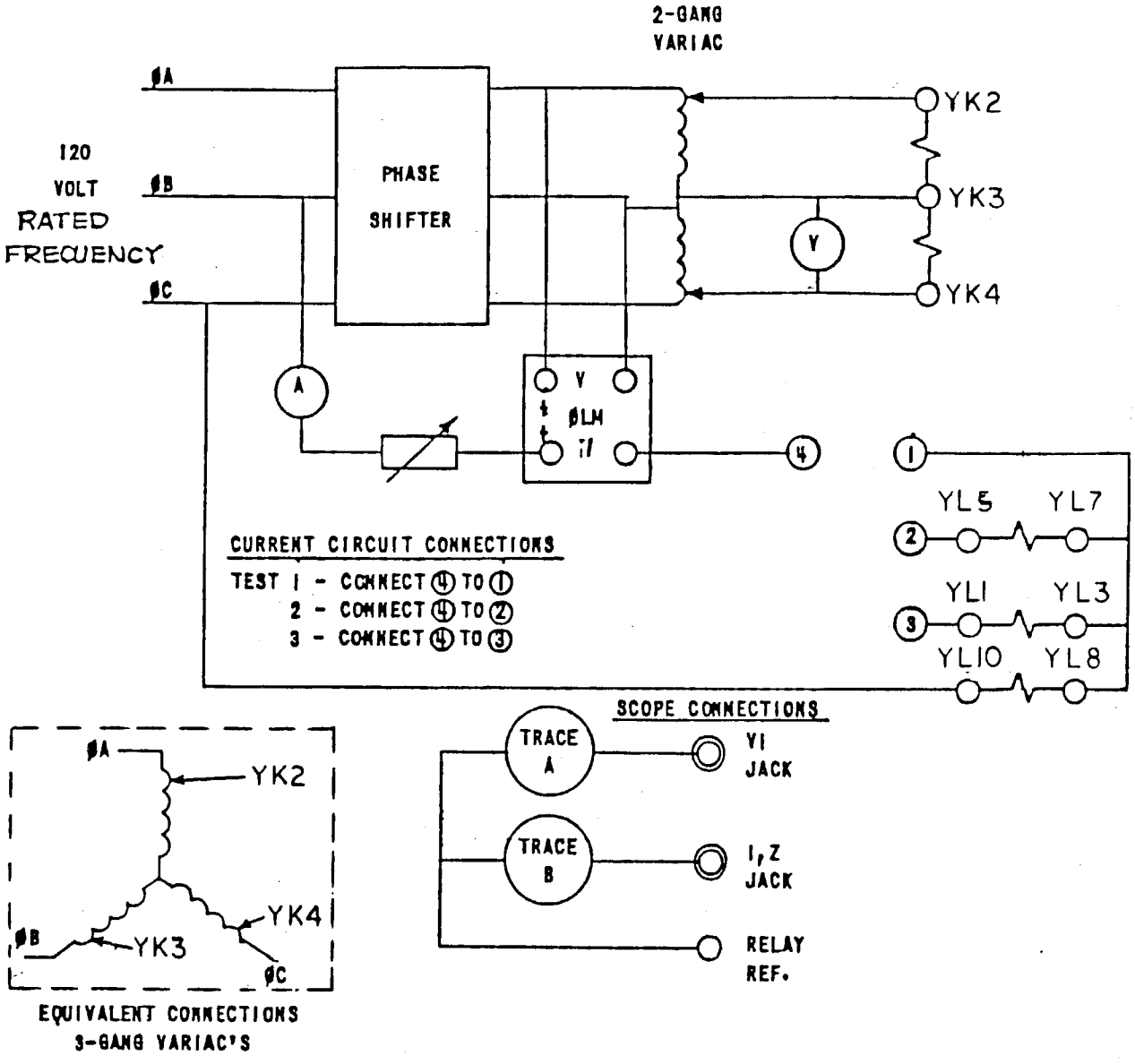


Fig. 12 (0227A2515-0) Mho Characteristics for the Type SLLP52A Relay



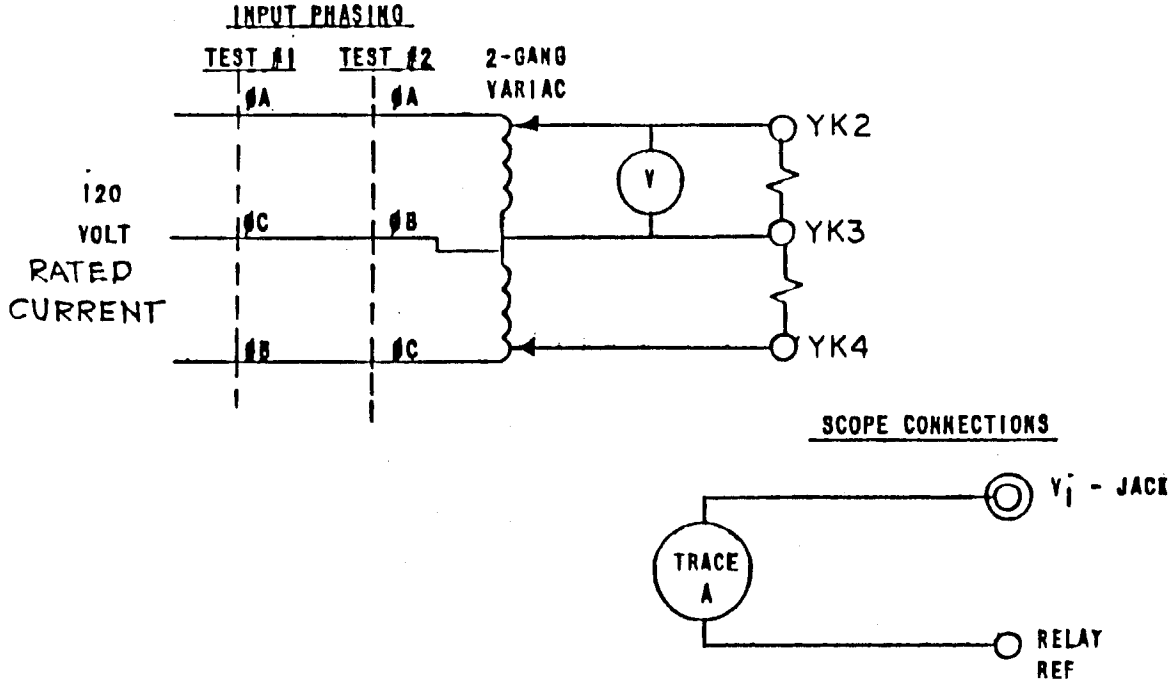
EQUIVALENT CONNECTIONS
3-GANG VARIAC'S

	BALANCED 3Ø RELAY INPUT VOLTS	INPUT AMPS	PHASE ANGLE *	OUTPUT INDICATION	REMARKS **
TEST 1	8.66 VOLT RMS	RATED CURRENT	TEST ANGLE	CHECK $\dot{V}_I = \dot{I}_I . Z$ (±.05V)	AØ TO GRD. NETWORK CHECK
TEST 2	8.66 VOLT RMS	RATED CURRENT	TEST ANGLE +120°	$\dot{V}_I \cong 1.2$ VOLTS P-P	BØ TO GRD. NETWORK CHECK
TEST 3	8.66 VOLT RMS	RATED CURRENT	TEST ANGLE +240°	$\dot{V}_I$ & $\dot{I}_I$ Z IN PHASE (± 0.2MS)	CØ TO GRD. NETWORK CHECK

* TEST ANGLE = RELAY ANGLE PLUS (+) 30°

** RELAY VOLTAGE RESTRAINT TAP SETTING = 100% FOR ALL TESTS

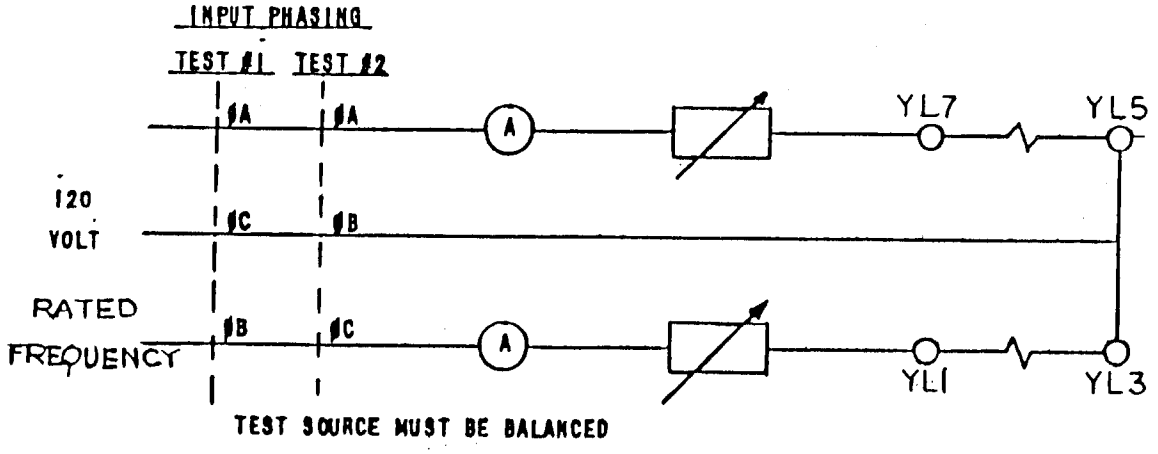
Fig. 13 (0285A6244-0) SLLP Sequence Network Check Test Circuit

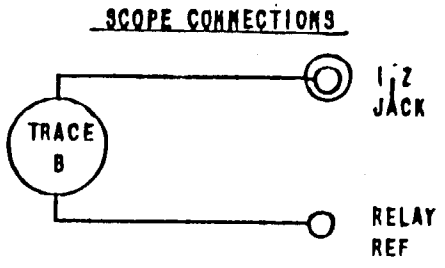


TEST	BALANCED 3Ø RELAY INPUT VOLTS	OUTPUT INDICATION	ADJUST	REMARKS *
#1 Vi - NULL	120 VOLTS R.M.S.	LESS THAN 0.2 VOLT P-P RIPPLE	P2 & P1 ALTERNATELY FOR MINIMUM FUNDAMENTAL OUTPUT	VOLTAGE RESTRAINT TAP SETTING = 100% START P2 & P1 ADJUSTMENT FROM MIDPOINT OF POTS
#2 Vi OUTPUT	26 VOLTS R.M.S.	APPROX. 8.4 VOLTS P-P	NONE	VOLTAGE RESTRAINT TAP SETTING = 100% RECORD VOLTAGE VALUE FOR I_1Z CALIBRATION

* OBSERVE INPUT PHASING

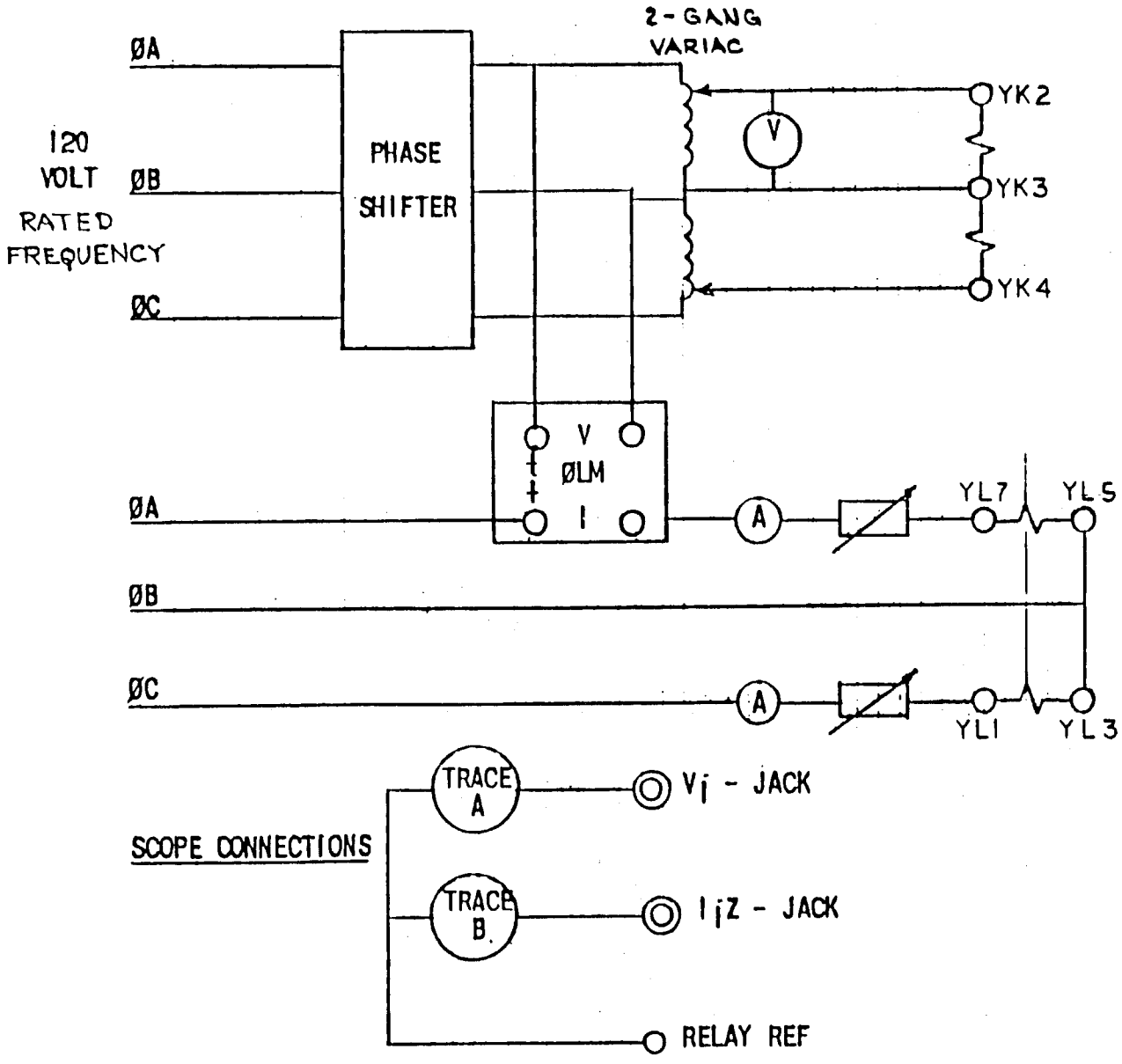
Fig. 14 (0285A6245-0) SLLP Voltage Sequence Null Test





	INPUT AMPS	OUTPUT INDICATION	ADJUST	REMARKS
TEST #1 I_1Z NULL	RATED CURRENT PER PHASE	LESS THAN 0.2 VOLT P-P RIPPLE	P4 & P3 ALTERNATELY FOR MINIMUM FUNDAMENTAL OUTPUT	OBSERVE INPUT PHASING, START P4 & P3 ADJUSTMENT FROM MIDPOINT OF POTS
TEST #2 I_1Z OUTPUT	RATED CURRENT PER PHASE	APPROXIMATELY 8.4 VOLTS P-P	P5 TO OBTAIN VALUE EQUAL TO V_1 OUTPUT	OBSERVE INPUT PHASING

Fig. 15 (0285A6246-0) SLLP Current Sequence Null Test



BALANCED 3Ø RELAY INPUT VOLTS	INPUT AMPS	PHASE ANGLE	OUTPUT INDICATION	ADJUST	REMARKS
26 VOLTS RMS	RATED CURRENT PER PHASE	TEST ANGLE	V_j & I_jZ EQUAL MAGNITUDE AND IN PHASE (TRACES A & B)	ADJUST P6 TO BRING I_jZ IN PHASE WITH V_j READJUST P5 TO MAINTAIN MAGNITUDE EQUAL TO V_j	OBSERVE INPUT PHASING RELAY VOLTAGE RESTRAINT TAP SETTING = 100%

* TEST ANGLE = RELAY ANGLE MINUS (-) 30°

Fig. 16 (0285A6247-0) SLLP Angle of Maximum Reach Setting

GENERAL ELECTRIC COMPANY
POWER SYSTEMS MANAGEMENT BUSINESS DEPT.
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