INSTRUCTIONS

GEK-41952

STATIC DIRECTIONAL OVERCURRENT

GROUND RELAY

TYPE SLPG51A

POWER SYSTEMS MANAGEMENT DEPARTMENT

GENERAL ELECTRIC

PHILADELPHIA, PA.

CONTENTS

STATIC DIRECTIONAL OVERCURRENT

GROUND RELAY

TYPE SLPG51A

DESCRIPTION

The Type SLPG51A relay is a directional overcurrent ground relay that was specifically designed to provide high speed ground fault protection in a directional comparison carrier blocking pilot relaying scheme or in a permissive overreaching transferred tripping scheme.

This relay is packaged in one case, two rack units in height as shown in Figure 1. The component location diagram for the relay is shown in Figure 2 and the internal connection diagram is shown in Figure 3. A typical external connection diagram for this relay is shown in Figure 4. A complete terminal of equipment requires, in addition to the SLPG relay, a suitable phase relay, an overcurrent relay SLC, an SLA auxiliary logic relay, an SLAT output relay, an SSA power supply, a test panel and a communication channel.

The measuring functions included in the SLPG51A relay are as follows:

DOF - zero sequence directional unit which operates for faults in the forward or tripping direction

DOR - zero sequence directional unit which operates for faults in the reverse or blocking direction

G3 - non-directional zero sequence overcurrent unit for high current level tripping function

For proper transmission line protection this relay is applied with other overcurrent functions contained in a Type SLC relay. Two units that are necessary for a directional comparison protection scheme are:

G2 - non-directional zero sequence overcurrent unit for low current level tripping function

G1 - non-directional zero sequence overcurrent unit for supervision of DOF and DOR or for carrier starting.

APPLICATION

The Type SLPG51A relay is applied as a zero sequence directional overcurrent ground relay in a directional comparison carrier blocking scheme. The SLPG51A relay is supplemented by G1 and G2 overcurrent units in this application. The settings of these units affect the coordination of the relaying scheme and this is discussed below.

DOR and DOF

DOF is a directional unit looking in the forward (tripping) direction. If its measuring quantities meet minimum pick up values, DOF will pick up when the operating current and polarizing quantities indicate zero sequence current flowing in the tripping direction. In general this unit requires no adjustment, but care should be exercised to insure the polarizing quantities are sufficient so the DOF will be picked up for all internal faults.

DOR is a directional unit looking in the reverse (blocking) direction. If its measuring quantities meet minimum pick up values, the DOR will pick up when the operating current and polarizing quantities indicate zero sequence current flowing in the blocking direction. In general this unit requires no adjustment, but care must be exercised to insure that DOR has enough polarizing quantity to insure it will pick up for all external faults when G2 and DOF at the remote terminal are picked up.

The sensitivity levels of these directional units are as follows:
I- polarizing (3Io) must be greater than 0.4 amperes
V- polarizing (3Vo) must be greater than 5 volts
I- operating (3Io) must be greater than 0.4 amperes

The DOF and DOR directional units may be current polarized, voltage polarized or dual polarized. No matter what polarization is used the polarizing quantity must exceed a certain magnitude. This is defined by the following equation:

$$3Vo + 3Io\ (12.5) \geq 5 \qquad (1)$$

In addition to the polarizing quantity requirement defined by equation (1),it is separately required that the operating current, 3Io, derived from the protected line currents exceeds 0.4 ampere in order for the directional units to operate to provide an output.

In this scheme, the zero sequence overcurrent function G1 and the DOR directional function are used to start carrier blocking only for external faults. Tripping is accomplished thru zero sequence overcurrent functions G2 and G3 supervised by the DOF directional function. Coordination must be established between blocking functions at one end of the line with the tripping functions at the opposite end of the line.

G1 and G2 PICKUP

Set the G2 pickup no higher than 75% of the minimum single-phase-to-ground fault current in the relay with the remote breaker closed.

$$G2 \leq \frac{3}{4}\left(I \text{ fault minimum}\right) \qquad (2)$$

The G1 pickup setting at the remote end of the line should be no greater than as indicated by the following equation.

$$G1 \leq \frac{3}{4}\ (G2 - 3I_{co}) \qquad (3)$$

where G1 = pick up setting of G1 unit
G2 = pick up setting of G2 unit
I_{co} = zero sequence charging current in the protected line during an external single-phase-to-ground fault near the G1 terminal of the line.

Equation (3) indicates the minimum permissible margin between G1 and G2 settings. Also this margin must be satisfied for external faults near both ends of the protected line. Larger margins will provide for greater security against false tripping on external faults. As a general rule, G1 may be set for the lowest pick up that will still not result in a continuous blocking signal during full load conditions as a result of system unbalance or harmonics. The G2 pickup, however, should be set as high as possible but with a sensitivity that provides at least 1.5 times and preferably 2-3 times pick up for the minimum internal fault.

The $3I_{co}$ term in equation (3) results from the fact that during ground faults external to the protected line the current entering the terminal farthest from the fault (G2 end) is greater than the current leaving the terminal nearest the fault (G1 end). This difference current is the line zero sequence charging current.

The value of $3I_{co}$ will depend on many factors including the following:

a. system configuration and impedance values
b. fault location, maximum $3I_{co}$ will occur when the fault is just beyond the protected live section
c. length of the protected line
d. whether or not shunt reactors are in use

The attached memorandum suggests a means of approximating the value of $3I_{co}$ line charging current.

G3 PICKUP

The G3 pickup setting must be high enough so that it does not pick up on the zero sequence current flow produced by unequal breaker pole closing when picking up load across the line. The magnitude of $3I_{co}$ that will flow in the line during this condition depends upon a number of factors, including the following:

a. system positive, negative and zero sequence impedances
b. magnitude of the voltage appearing across the open poles of the breaker before closing any poles
c. sequence of pole closing
d. instantaneous angle of closing

In most applications a pick up setting for G3 in the range of $3I_o$ equal to 3 to 5 amperes should suffice. If possible the unequal pole closing current should be determined by test upon installation.

The G3 unit supervised by DOF provides high speed tripping of the line terminal for heavy ground faults producing fault currents above the G3 setting.

COORDINATION

The zero sequence polarizing voltage, $3V_o$, that exists on the system during a fault is highest at the point of fault. This voltage decreases as one moves away from the point of fault and toward the source of the zero sequence current. Thus, for an external fault, the $3V_o$ polarizing voltage will be higher at the terminal closest to the fault than it will be at the far terminal. This provides for a natural coordination between the DOR blocking unit at one end of the line with the DOF tripping unit at the other end of the line. This is true only if the potential transformer ratios are the same at both ends of the line and if the line is of sufficient length to provide a significant voltage difference from one end to the other.

When current polarization is used, it may be difficult to coordinate sensitivities between DOR at one end and DOF at the other end. This is due to the variation in the distribution of zero sequence currents in the polarizing sources at the two ends of the line for differing system conditions. When dual polarization is used both of the effects of potential polarization and current potential must be considered. This is indicated in equation (1), discussed previously. It is even more difficult, generally, to coordinate current polarization at one end with potential polarization at the other end. This combination is not recommended.

Polarization considerations are:

1. when potential polarization alone is used, a natural coordination is attained between DOF at one end of the line and DOR at the other end of the line
2. if the system is such that current polarization alone is safe to use, then dual polarization is safer and better to use
3. on short lines where current polarization is least apt to be safe to use, potential polarization alone should suffice.

Tripping is initiated by DOF and G2 and blocking is initiated by DOR and G1. Coordination is necessary so that for any external single-phase-to-ground fault for which both DOF and G2 operate, it also causes DOR and G1 at the other end to operate more sensitively. Two approaches may be considered to obtain this coordination. These are:

a. set G2 at one end of the line to be less sensitive than both G1 and DOR at the other end.

OR

b. set G2 at one end of the line to be less sensitive than G1 at the other end and insure that DOF at one end of the line is less sensitive than DOR at the other end.

Potential polarization only

Set G2 pickup

$$G2 \geq \frac{4}{3}\ (0.4) + 3I_{co} \qquad (4)$$

The 0.4 is the $3I_o$ sensitivity of the operating circuit of the DOR function. Set G1 with a $3I_o$ pickup that is less than 0.4 amperes but not so low that it picks up on the normal system unbalance due to load flow. Usually a 0.2 ampere pickup setting for G1 will be satisfactory.

Potential polarization provides a natural coordination between the DOR blocking unit at one end of the line with the DOF tripping unit at the opposite end of the line as discussed previously. For all internal single-phase-to-ground faults the zero sequence polarizing voltage $3V_o$ should exceed 5 volts at both ends of the line in order to insure high speed tripping.

Current polarization only

Set pickup of G2 and G1 the same as specified for potential polarization in the previous section.

Select the polarizing current transformers at both ends of the line to satisfy both the following requirements:

a. for all internal faults the secondary polarizing current, $3I_0$, must not be less than 0.4 amperes.

b. for all external faults that will cause G2 at the tripping end to pick up, the secondary polarizing current supplied to the blocking terminal should be at least equal to the secondary polarizing current supplied to the tripping terminal.

Dual polarization

Set the pickup of G1 the same as specified for potential polarization described previously.

The requirements for setting G2 depend upon whether the choice is made to coordinate G2 with G1 alone and to coordinate DOF with DOR separately; or to coordinate G2 with both G1 and DOR.

To coordinate G2 with G1 and DOR with DOF:

a. set G2 with a pickup determined by equation (4) above

b. select the polarizing current transformers at both ends of the line so that for all external ground faults that will cause G2 at the tripping end to pick up, the polarizing current supplied to the blocking end will be at least as great as that supplied to the tripping end.

c. for all internal faults determine that the polarizing quantities at both ends of the line satisfy equation (1), this is required in order to trip.

To coordinate G2 at one end with both G1 and DOR at the opposite end:

a. set G2 with a pickup that is at least equal to the higher of the two values determined from equations (4) and (5) below

$$G2 \geq \frac{4}{3}\ (0.4) + 3I_{co} \qquad (4)$$

$$G2 \geq \frac{4}{3}\ \frac{5}{Z_{01}} + 3I_{co} \qquad (5)$$

where: Z_{01} is the secondary zero sequence ohms of the protected line section calculated from the primary zero sequence impedance, the line CT ratio and the ratio of the potential transformers used to provide the zero sequence potential polarization.

the 5 is the 5 volt sensitivity of DOR polarizing circuit

Equation (5) is based on the fact that the magnitude of $3V_0$ at the blocking end of a line for an external single-phase-to-ground fault beyond the blocking end must be greater than the zero sequence impedance of the protected line times the $3I_0$ flowing through the protected line.

The setting thus selected for G2 must still permit tripping for all internal faults. This criteria is defined by equation (2) discussed previously.

TIMER SETTINGS

The characteristic timers are those timers that are usually a part of a measuring function and are not intended for field adjustment unless they are found to be misadjusted. In the SLPG51A relay the 6,4/5 timer after AND112 and DOF is not intended for field adjustment. The actual timer settings which are shown on the internal connection diagram are 5.8 ms, 4.16 ms / 5ms. This type of timer will provide an output on an initial input pulse of 5.8 ms or more or it will provide an output on two or more consecutive input pulses of 4.16 ms.

The characteristic 3/50 timer following AND113 and DOR is not intended for field adjustment. This timer setting provides a speed advantage for the DOR blocking unit over the slower DOF tripping. This does not eliminate any of the other coordination requirements given in the previous portions of this discussion.

The logic timer 8/0 following DOF and the 6,4/5 timer provides a delay to prevent false tripping via G2 on the zero sequence current produced by unequal breaker pole closing. In some extreme conditions of unequal breaker pole closing it may be necessary to increase the time delay to something greater than 8 ms. This should be checked by actual field tests. It is not recommended that this timer be set for any pickup delay any less than 8 ms.

RANGES

G3 - GROUND OVERCURRENT UNIT, ONE TO TEN AMPERES

The operation of the directional unit (DOF, DOR) is supervised by the G1 function in the associated SLC relay. Current in the operating circuit must therefore be above the G1 pickup setting to produce operation. The polarizing source should be greater than 0.4 amperes if current polarized, or greater than 5 volts if potential polarized. The operating current which is the residual current of the protected line must also be greater than 0.4 amperes.

RATINGS

The Type SLPG51A relay is designed for use in an environment where the air temperature outside the relay case is between $-20^{\circ}C$ and $+65^{\circ}C$.

The Type SLPG51A relay requires a ±15VDC power source which can be obtained from a Type SSA50 power supply.

The current circuits of the Type SLPG51A are rated 5 amperes, rated frequency, for continuous duty and have a one second rating of 300 amperes. The potential circuits are rated 120 volts, rated frequency.

OPERATING PRINCIPLES AND CHARACTERISTICS

The directional characteristics, DOF and DOR, of the SLPG51A are shown in Figures 5 and 6 for current polarization and Figures 7 and 8 for voltage polarization respectively. The input operating current ($3I_0$) and polarizing current ($3I_0$) and / or voltage ($3V_0$) supplied to the transactors or transformer produce proportional voltage signals which are filtered and phase compensated then squared (shaped) to enable a time comparison or coincidental measurement of the input phase angle relationship. Allowing the term "coincidence" to describe both in phase and out of phase comparisons, the forward looking function, DOF, produces an output based upon each half cycle of in phase coincidence, whereas the reverse looking function, DOR, operates on the out of phase coincidence of the same derived voltage signals. The amount of coincidence required and therefore the included angle of the operating characteristic is determined by the timer settings on the "P" position card for DOF and the "N" position card for DOR. Since the output from either directional function requires the operation of the G1 overcurrent function in the SLC51, the area around the origin equivalent to the G1 setting is not included in the operating characteristics.

The combination of filtering and timer settings utilized in the SLPG51 is designed to overcome unwanted operations on zero sequence inrush and unequal pole closures as well as proper coordination between the forward and reverse direction functions. The DOF characteristic timer produces an output (at TP5) for a single input block of 5.8 milliseconds or two input blocks of 4.16 milliseconds which is equivalent to operating and polarizing input quantity coincidence for 120 degrees and 90 degrees respectively. The DOR characteristic timer is an intergrating timer which produces an output for a single 3 millisecond input signal or repetitive 2 ms input blocks (one each half cycle) resulting in an overlap of the DOF and DOR characteristics.

The G3 function in the SLPG51 is an adjustable non-directional overcurrent function which operates on residual current. The current is routed through a transactor of which the output voltage is controlled by secondary loading set at the factory. The voltage is filtered, full wave rectified and fed to the customer adjustable level detector. The detector output pulses are stretched to provide continuous logic output signals.

CALCULATION OF SETTINGS

Refer to the APPLICATION section for a discussion of the considerations involved in setting this

relay. It is usually necessary to have the results of a system short circuit study available in order to make and verify the settings of the various relay functions being used.

CONSTRUCTION

The SLPG51A relay is packaged in a two rack unit (1 R.U.= 1 3/4") enclosed metal case with hinged front cover and removable top cover. The case is suitable for mounting on a standard 19 inch rack. The outline and mounting dimensions of the case and the physical location of the components are shown in Figures 1 and 2 respectively.

Current and potential enter the SLPG51A on a twelve point terminal strip located on the rear of the relay case. The terminal strip is labled GA.

A potentiometer (P1) for adjusting G3 is located on the front panel of the unit. This pot is factory set, G3 pickup level is adjusted by means of a pot located on the level detector card. The SLPG51A contains printed circuit cards identified by a code number such as D102, F105, L111, and T103 where D designates detector, F designates filter, L designates logic and T designates time delay. The printed circuit cards plug in from the front of the unit. The sockets are marked with letter "addresses" which appear on guide strips in front of each socket, on the component location diagram and on the internal connection diagram. The test points (TP1, TP2, etc) shown on the internal connection diagram are connected to instrument jacks on a test card in position T with TP1 at the top of the card. The internal connections of the printed circuit cards are shown in the Printed Circuit Card Instruction Book GEK-34158.

Pin number 1 on the test card in position T is connected to relay reference, number 2 to -15VDC, and pin number 10 to +15VDC. Output signals are measured with respect to the reference bus on the test card (TP1). Logic signals are approximately +15 VDC for the ON or LOGIC ONE condition, and less than 1 VDC for the OFF or LOGIC ZERO condition. Filter card outputs are either +15VDC or -15VDC for the ON condition.

These outputs can be monitored with an oscilloscope, a portable high impedance DC voltmeter, or the test panel voltmeter if available. When the test panel meter is supplied, it will normally be connected to the reference bus. Placing the relay test lead in the proper test point pin jack will connect the meter for testing. When time delay cards are to be adjusted or checked, an oscilloscope which can display two traces simultaneously and which has a calibrated horizontal sweep should be used.

RECEIVING, HANDLING AND STORAGE

These relays will normally be supplied as a part of a static relay equipment, mounted in a rack or cabinet with other static relays and test equipment. Immediately upon receipt of the static relay equipment, it should be unpacked and examined for any damage sustained in transit. If injury or damage resulting from rough handling is evident, file a damage claim at once with the transportation company and promptly notify the nearest GENERAL ELECTRIC SALES OFFICE.

Reasonable care should be exercised in unpacking the equipment. If the equipment is not to be installed immediately, it should be stored indoors in a location that is free from moisture, dust, metallic chips, and severe atmospheric contaminants.

Just prior to final installation the shipping support bolt should be removed from each side of all relay units to facilitate possible future unit removal for maintenance. These shipping support bolts are approximately eight inches back from the relay unit front panel. WARNING: STATIC RELAY EQUIPMENT, WHEN SUPPLIED IN SWING RACK CABINETS, SHOULD BE SECURELY ANCHORED TO THE FLOOR OR TO THE SHIPPING PALLET TO PREVENT THE EQUIPMENT FROM TIPPING OVER WHEN THE SWING RACK IS OPENED.

INSTALLATION TESTS

CAUTION

THE LOGIC SYSTEM SIDE OF THE DC POWER SUPPLY USED WITH MOD III STATIC RELAY EQUIPMENT IS ISOLATED FROM GROUND. IT IS A DESIGN CHARACTERISTIC OF MOST ELECTRONIC INSTRUMENTS THAT ONE OF THE SIGNAL INPUT TERMINALS IS CONNECTED TO INSTRUMENT CHASSIS. IF THE INSTRUMENT USED TO TEST THE RELAY EQUIPMENT IS ISOLATED FROM GROUND, ITS CHASSIS MAY HAVE AN ELECTRICAL POTENTIAL WITH RESPECT TO GROUND. THE USE OF A CONNECTION TO THE EQUIPMENT, SUCH AS A TEST LEAD INADVERTANTLY DROPPING AGAINST THE RELAY CASE, MAY CAUSE DAMAGE TO THE LOGIC CIRCUITRY. NO EXTERNAL TEST EQUIPMENT SHOULD BE LEFT CONNECTED TO THE STATIC RELAYS WHEN THEY ARE IN PROTECTIVE SERVICE, SINCE TEST EQUIPMENT GROUNDING REDUCES THE EFFECTIVENESS OF THE ISOLATION PROVIDED.

The Type SLPG51A relay is usually supplied from the factory mounted and wired in a static relay equipment. The following checks and adjustments should be made by the user in accordance with the procedures given under DETAILED TESTING INSTRUCTIONS before the relays are put into service.

1. G3 Level detector pickup setting
2. Timer pickup and dropout settings
3. DOF/DOR directional unit operation

DETAILED TESTING INSTRUCTIONS

G3

The G3 overcurrent function may be set by applying a variable single phase test source to GA5 - GA6 connections A and B as shown in Figure 9 and monitoring the pickup at TP8 (voltage steps from less than 1 VDC to more than 10 VDC). Momentarily apply test current and monitor the output. Adjust the K card potentimoter for the desired operating point (closkwise pot rotation raises the operating point).
CAUTION: THIS RELAY IS RATED AT 5 AMPERES CONTINUOUS DUTY. TO SET FOR HIGHER CURRENT LEVELS, APPLY TEST CURRENT TO THE RELAY ON MOMENTARY BASIS (APPROXIMATELY ONE SECOND).

DIRECTIONAL FUNCTIONS DOF,DOR

The operation of the directional functions in the SLPG51A may be checked using the test circuit of Figure 10 and connections per Table 1. G1 supervision input can be simulated by removal of the CG211 connector at the rear of the unit. The test circuits supply inputs at approximately the MID-RANGE ANGLE of the operating characteristics.

TABLE 1

FUNCTION	CONNECTIONS A B	MONITOR OUTPUT AT	VOLTAGE
DOF/DOR CURRENT POLARIZED	GA7 GA8	TP5,TP7	15VDC
		TP6	0
		TP8,TP9*	15VDC
	GA8 GA7	TP5,TP7	0
		TP6	15VDC
		TP8	15VDC
		TP9	0
DOF/DOR POTENTIAL POLARIZED	GA9 GA10	TP5,TP7	15VDC
		TP6	0
		TP8,TP9*	15VDC
	GA10 GA9	TP5,TP7	0
		TP6	15VDC
		TP8*	15VDC
		TP9	0

* IF TEST CURRENT IS ABOVE G3 PICKUP SETTING

G3 CALIBRATION

The PI potentiometer on the front of the SLPG51A is factory set to provide the specified 1 to 10 amps pick up adjustment range for the card pickup potentiometer. A check of the calibration may be made using the above G3 testing procedure and a card adapter in position K to gain access to the input signal. With 5 amps applied and an AC voltmeter connected between "K" card pins 3 and 1, measure 3.0 volts RMS.

TIMER ADJUSTMENTS AND TESTS

The T107 card contains three potentiometers P1, P2 and P3 which have been factory set and should not be adjusted unless a plot of the operating characteristics indicates an improper time setting. Potentiometer P2 must be set before P1 adjustment can be checked since the single pulse operating time (5.8 ms) is a combination of both potentiometer settings. Potentiometer P2 is set for 4.16 milliseconds pickup time providing ±90 degree operating area about the Mid-range Angle. Timer settings greater than 4.16 milliseconds decrease the DOF operating area whereas shorter times increase the operating area. Potentiometer P3 is set for five millisecond dropout delay. Clockwise rotation of the potentiometers increases the operating delay. The T103 contains a single potentiometer, P1, for adjustment of pickup delay.

The T123 DOF characteristic timer is set to produce an output for a single Logic 1 input signal of greater than 3 milliseconds duration or consecutive half cycle input pulses of more than two milliseconds.

The timer settings may be tested using the test circuit of Figure 11 and a dual trace oscilloscope to compare input and output signals. Remove the printed circuit card preceding the timer under test and monitor signals per the following Table II. The card extender is required for access to PIN 7 the "P" position T107 card.

TABLE II

TIMER	FUNCTION	REMOVE CARD	INPUT & CHANNEL "A"	CHANNEL "B"	ADJUSTMENT
T107	4.16 ms P.U.	M	TP3	"P" PIN 7	P2
	5.8 ms P.U.	M	TP3	TP5	(PI FACTORY SET)
	5 ms D.O.	M	TP3	TP5	P3
T103	8 ms P.U.	P	TP5	TP7	P1
T123	3 ms P.U.	M	TP4	TP6	P1
	50 ms D.O.	M	TP4	TP6	P2

OPERATING CHARACTERISTICS

The DOF and DOR characteristics may be checked using the test circuit of Figure 12. This figure gives the test circuit to check the potential polarizing circuit and the current polarizing circuit. DOF operation can be monitored at TP5 and DOR operation can be monitored at TP6.

To check DOF and DOR using potential polarization, apply five amperes and 120 volts to the relay as indicated in Figure 12. Adjust the phase shifter to where the current lags the voltage by 80 degrees. At this point DOF should be operated (10 to 15VDC signal at TP5) and DOR should not (0 to 1VDC at TP6). Adjust the phase shifter in both directions from this point and determine the two end points of the DOF characteristic. The end point is the angle at which DOF just operates; that is, the signal at TP5 steps from less than 1VDC to greater than 10VDC. The DOF characteristic should be operated for all angles between the two end points. The center of this operating area (Mid-Range Angle) should be where the current lags the voltage by 80 degrees ±10 degrees. The end points should be greater than 60 degrees but less than 120 degrees from the Mid-range Angle. In other words, one end point should occur in the region where the current leads the voltage by 40 degrees to where it lags by 20 degrees. The other end point should occur in the region where the current lags the voltage by 140 to 200 degrees. Check that there is a region on both sides of the DOF Mid-range Angle where both DOF and DOR operate.

To check the DOR characteristic using potential polarization adjust the phase shifter to where the current leads the voltage by 100 degrees. At this point DOR should be operated and DOF should not. Determine the end points of the DOR characteristic in a similar manner as was used in the DOF characteristic. The Mid-range Angle of the DOR characteristic should be where the current leads the voltage by 100 degrees, ±10 degrees, or approximately 180 degrees out of phase with the DOF Mid-range Angle. The end points of DOR should fall within 110 degrees to 150 degrees of the Mid-range Angle. In other words, one end point should occur in the region where the current lags the voltage by 10 degrees to 50 degrees. The other end point should occur in the region where the current lags the voltage by 110 degrees to 150 degrees.

If the end points of either DOF or DOR do not fall within the specified regions, touch up the pickup setting of the characteristic timers. The T107 in Position P is for DOF and the T123 in Position N is for DOR. A clockwise rotation of the pickup potentiometer adjustment increases the pickup delay but decreases the distance between the Mid-range Angle and the end points. A counterclockwise rotation decreases the pickup delay but increases this operating area.

To check the DOF and DOR characteristics using current polarization, apply five amperes to the operating and the polarizing circuit as indicated in Figure 12. Adjust the phase shifter to where the two currents are in phase. At this point DOF should be operated (10 to 15VDC signal at TP5) and DOR should not (0 to 1VDC signal at TP6). Adjust the phase shifter in both directions from this point and determine the two end points of the DOF characteristic. The end point is the angle at which DOF just operates; that is, the signal at TP5 steps from less than 1VDC to greater than 10VDC. The DOF should be operated for all angles between the Mid-range Angle and the end points. The Mid-range Angle or center of the DOF characteristic should be where the two currents are in phase ±10 degrees. The end points should be greater than 60 degrees, but less than 120 degrees from the Mid-range Angle. In other words, one end point occurs in the region where the operating current leads the polarizing current by 60 to 120 degrees. The other end point occurs in the region where the operating current lags the polarizing current by 60 to 120 degrees. Check that there is a region on each side of the Mid-range Angle where both DOF and DOR operate.

To check the DOR characteristic using current polarization adjust the phase shifter until the two currents are 180 degrees out of phase. At this point DOR should be operated and DOF should not. Determine the two end points of the DOF characteristic. The Mid-range Angle should be where the operating current and polarizing current are 180 degrees out of phase, ±10 degrees. The end points should occur greater than 110 degrees but less than 150 degrees from the Mid-range Angle. In other words, one end point should occur in the region where the operating current leads the polarizing current by 30 degrees to 70 degrees. The other end point should occur in the region where the operating current lags the polarizing current by 30 degrees to 70 degrees.

CHECKING DIRECTIONAL ACTION WITH LOAD CURRENT

The polarity of the external connections to the SLPG51 may be checked using load current if it is potential polarized. The test connections are shown in Figure 13. The procedure is to supply to the relay phase-to-neutral voltage from one phase, and phase current from the next lagging phase. This will give a correct indication of the directional action of the relay. If the balanced three-phase load current is flowing into the protected line section and is in the range of lagging by less than 20 degrees to leading by less than 90 degrees, then the DOF function should operate. If the balanced three-phase load current is flowing out of the protected line zone and is leading or lagging by any angle up to 90 degrees, then the DOR function should operate. For this test load current must be greater than G1 pickup.

The phase 1 voltage for this test can be obtained by disconnecting phase 1 voltage from the primary of the wye-broken-delta transformer and shorting the phase 1 primary winding on this transformer. Phase 2 current can be obtained by shorting the current transformer secondaries in phases 1 and 3 opening their circuits to the relay.

As a further check, a phase angle meter can be connected to read the angle between the current and voltage being supplied to the relay. For the most definite indication for load current flow into the protected line section, the test current should be within ±60 degrees of the Mid-range Angle of the DOF characteristic. In other words, the test current should lag the test voltage by 20 degrees to 140 degrees. For load current flow out of the protected line section, the test current should be within ±90 degrees of the Mid-range Angle of the DOR characteristic. In other words, the test current should be in the region of leading the test voltage by 150 degrees to lagging by 30 degrees.

If the directional unit is current polarized from a current transformer in a power transformer neutral, it is not possible to check the polarity of this connection with a simple test using load current as described above.

MAINTENANCE

PERIODIC CHECKS

For any periodic testing of the type SLPG51A relay the trip coil circuit of the circuit breaker should be opened by opening the disconnect switches or other test switches provided for this purpose.

TROUBLE-SHOOTING

Test points are provided at selected points in the Type SLPG51A relay to observe outputs if trouble-shooting is necessary. The use of a card adapter will make the pins on any on card available for testing.

For the physical location of components and cards refer to Figure 2, the component location diagram.

SPARE CARDS

The number of spare cards to carry in stock would depend on the total number of static relays, using similar cards, at the same location or serviced by the same test group. For each type of card (different code designation) a suggested minimum number of spare cards would be:

1	spare	for	1 to	25 cards
2	spares	for	26 to	75 cards
3	spares	for	76 to	125 cards

CARD DRAWINGS

Details of the circuits of the printed circuit cards can be obtained in the printed circuit card book GEK-34158.

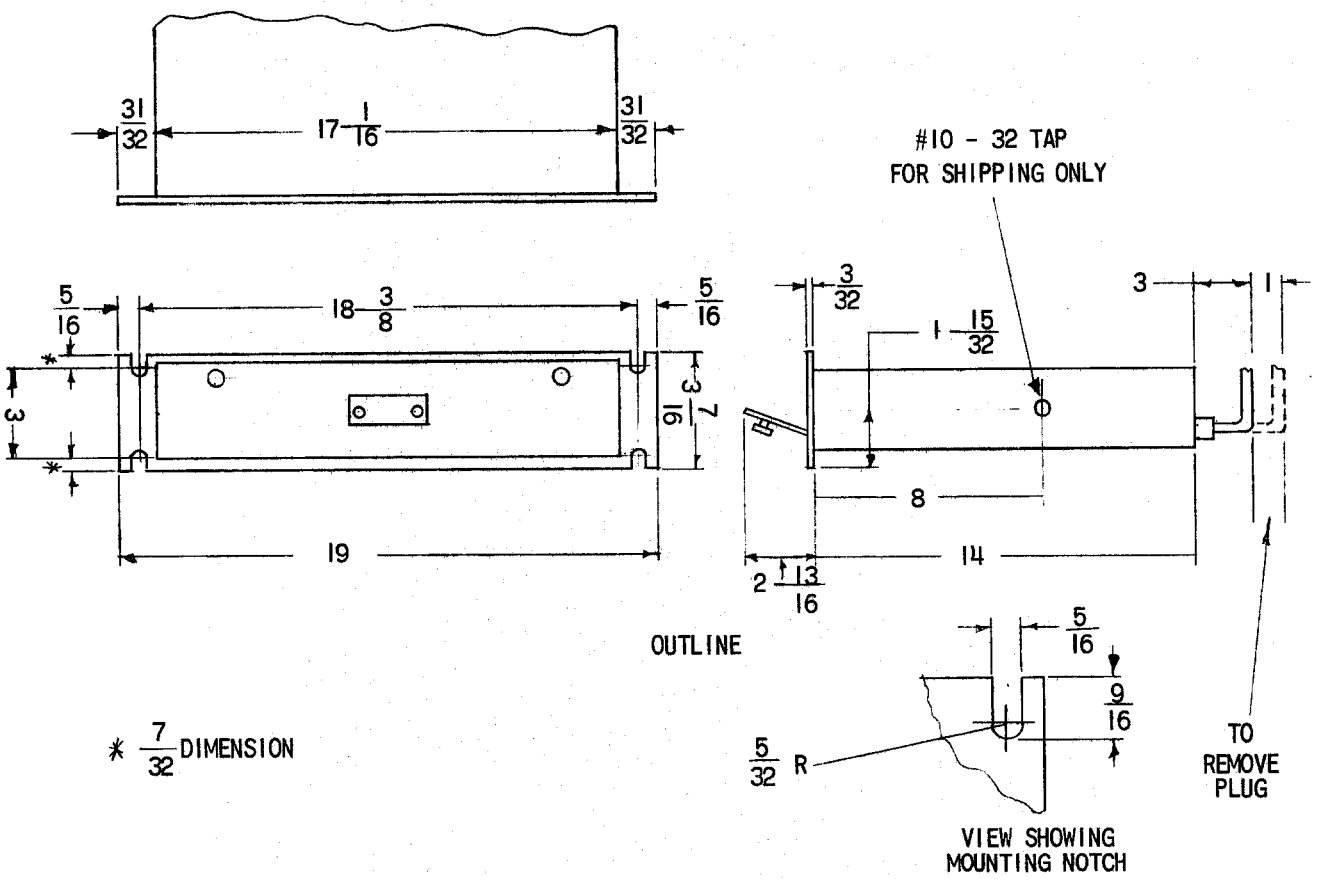
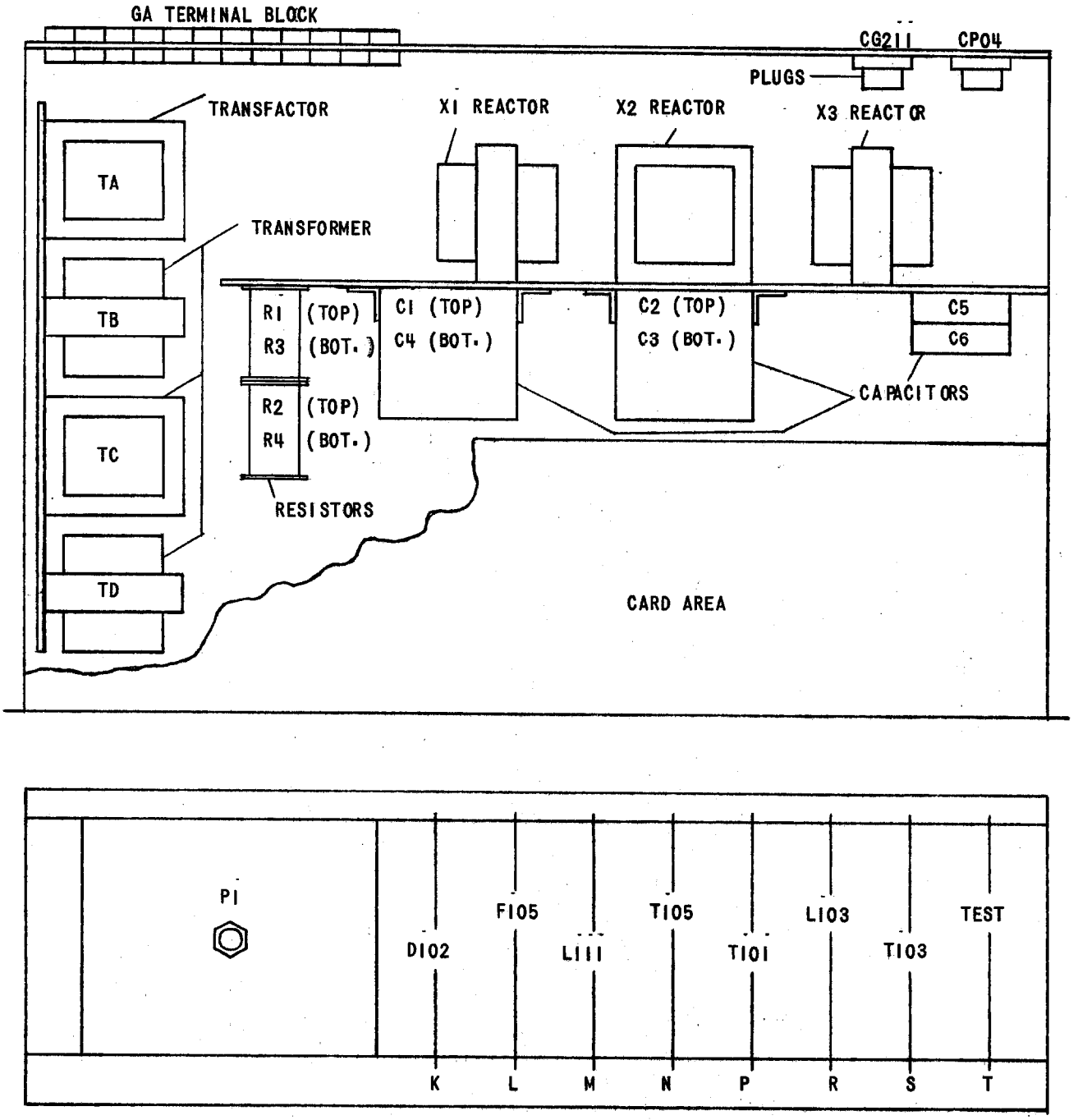


Figure 1 (0227A2036-0). Outline and Mounting Dimensions for the Type SLPG51A Relay



P.C. CARD 0277A2032 GR-9

Figure 2 (0257A3222-0). Component Location Diagram for the Type SLPG51A Relay

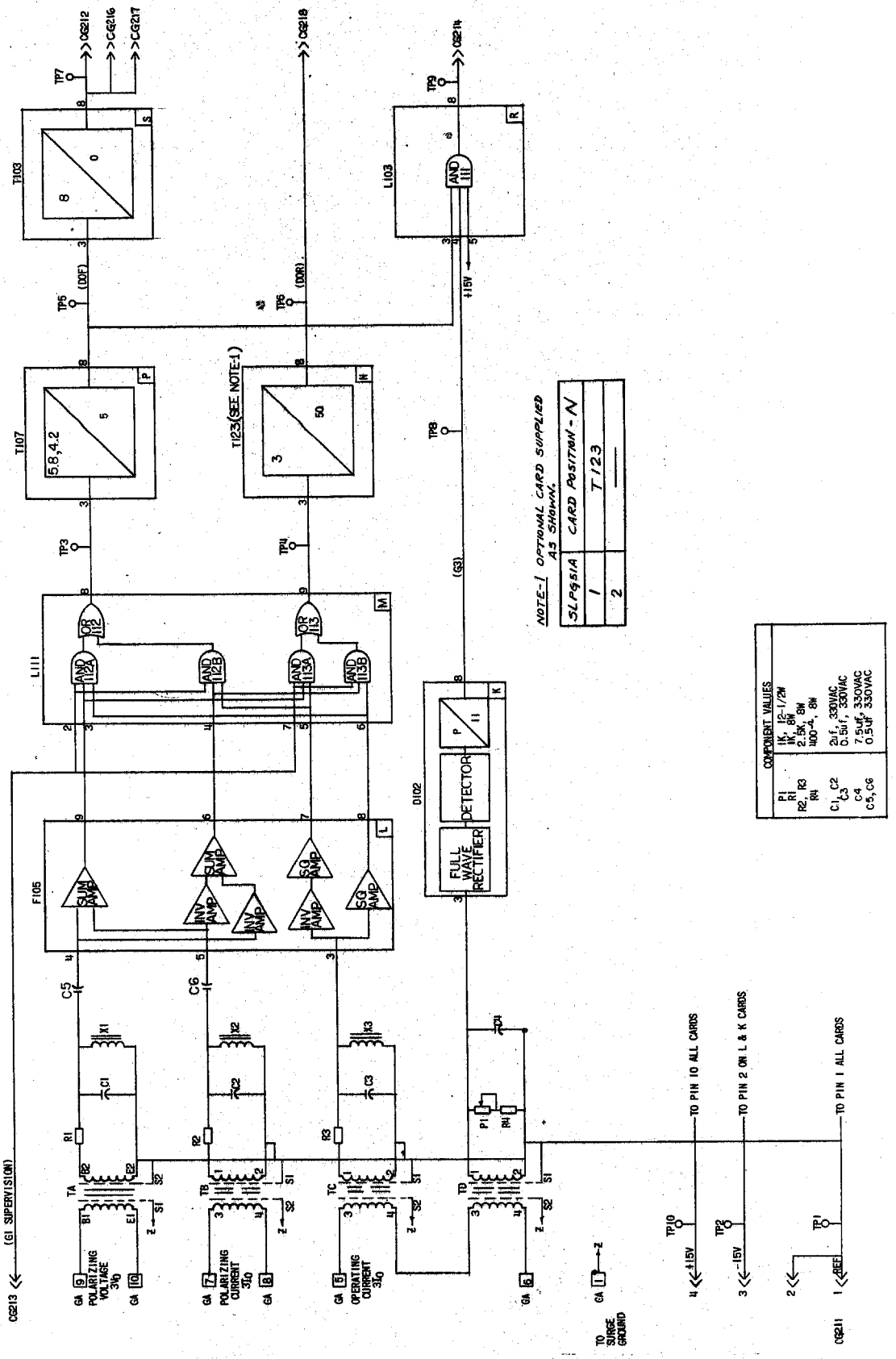


Figure 3 (0149C7222-3). Internal Connections Diagram of the SLPG51A Relay

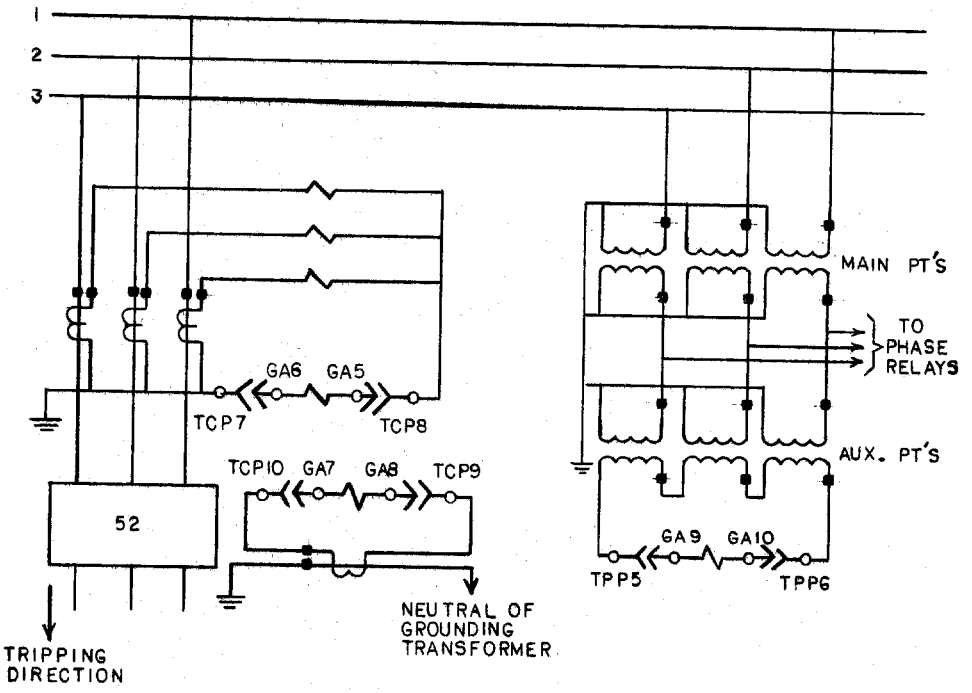


Figure 4 (0257A6231-1). Typical External Connections for the SLPG51A Relay

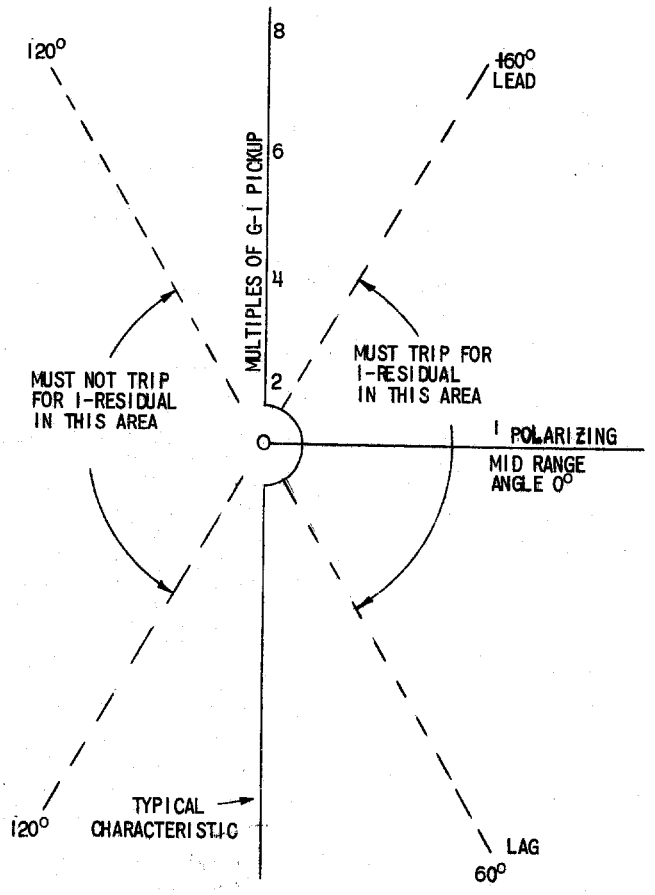


Figure 5 (0257A6225-0). Typical SLPG51 DOF Characteristic Current Polarized

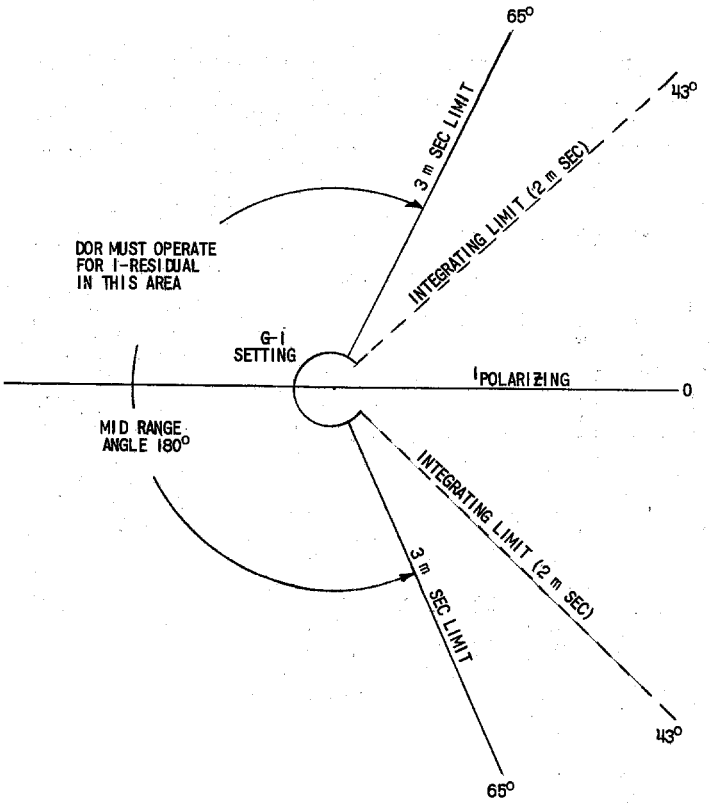


Figure 6 (0257A6224-0). Typical SLPG51 DOR Characteristic Current Polarized

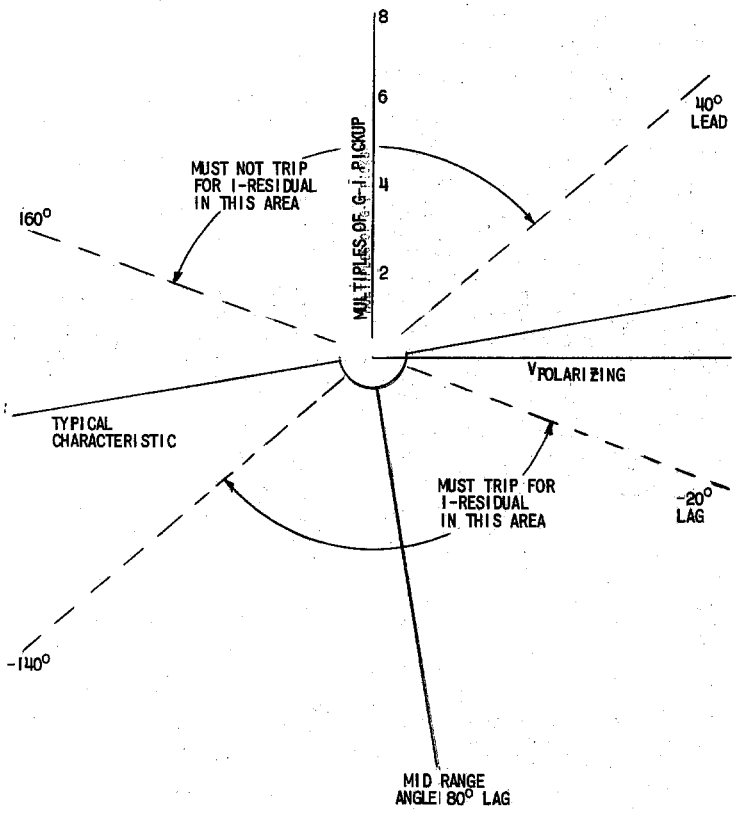


Figure 7 (0257A6223-0). Typical SLPG51 DOF Characteristic Potential Polarized

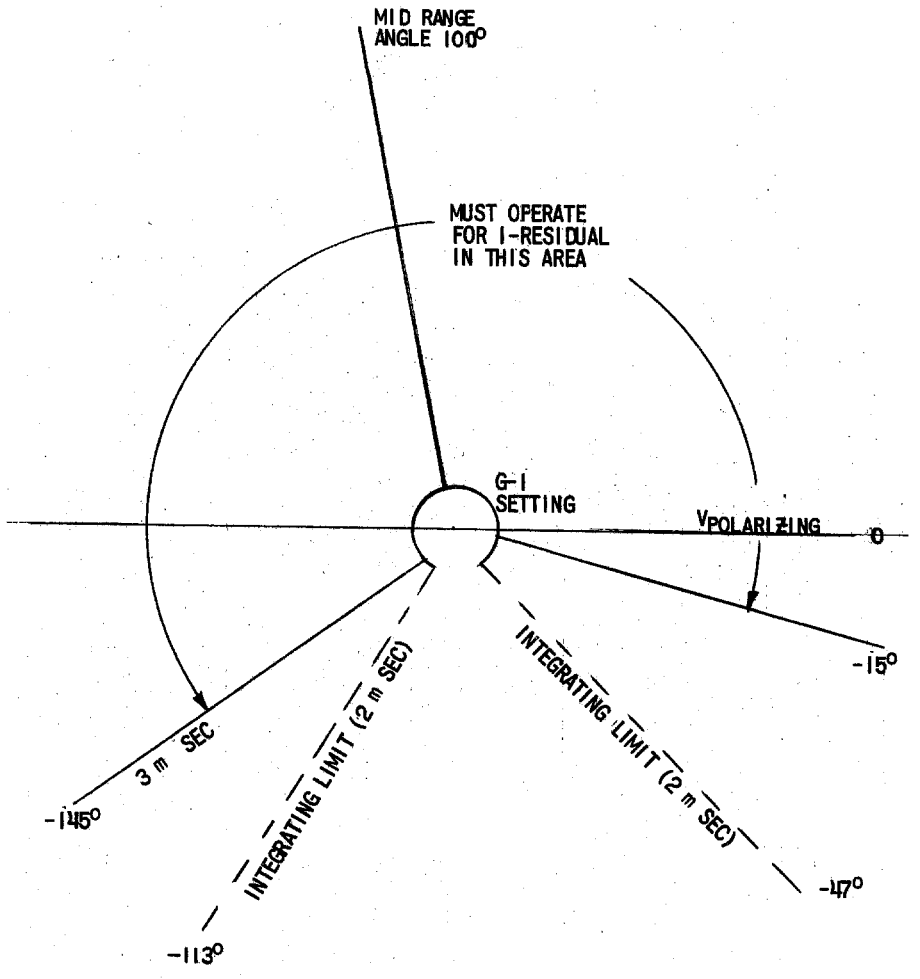
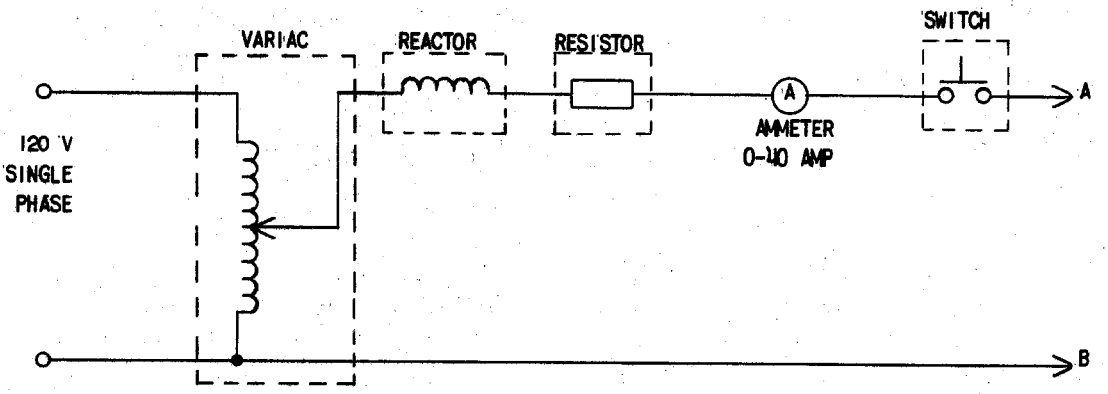


Figure 8 (0257A6227-0). Typical SLPG51 DOR Characteristic Potential Polarized



TEST CIRCUIT FOR NON-DIRECTIONAL
OVER CURRENT FUNCTIONS.

Figure 9 (0246A3681-1). G1 Overcurrent Function Test Circuit

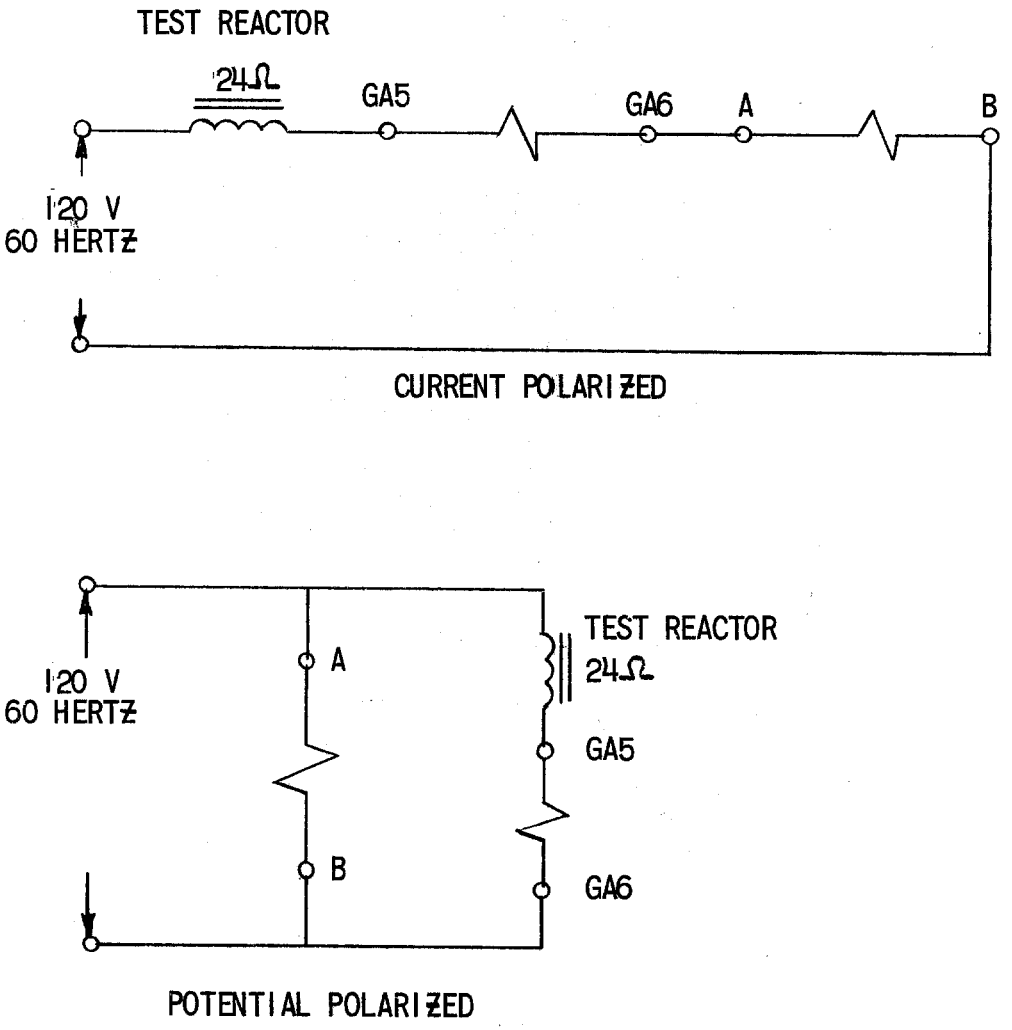


Figure 10 (0257A6222-0). SLPG51A Directional Function Test Circuits

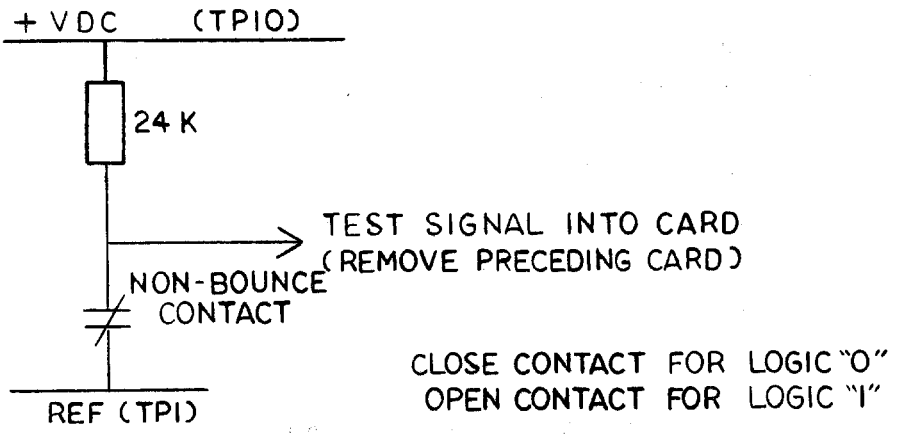
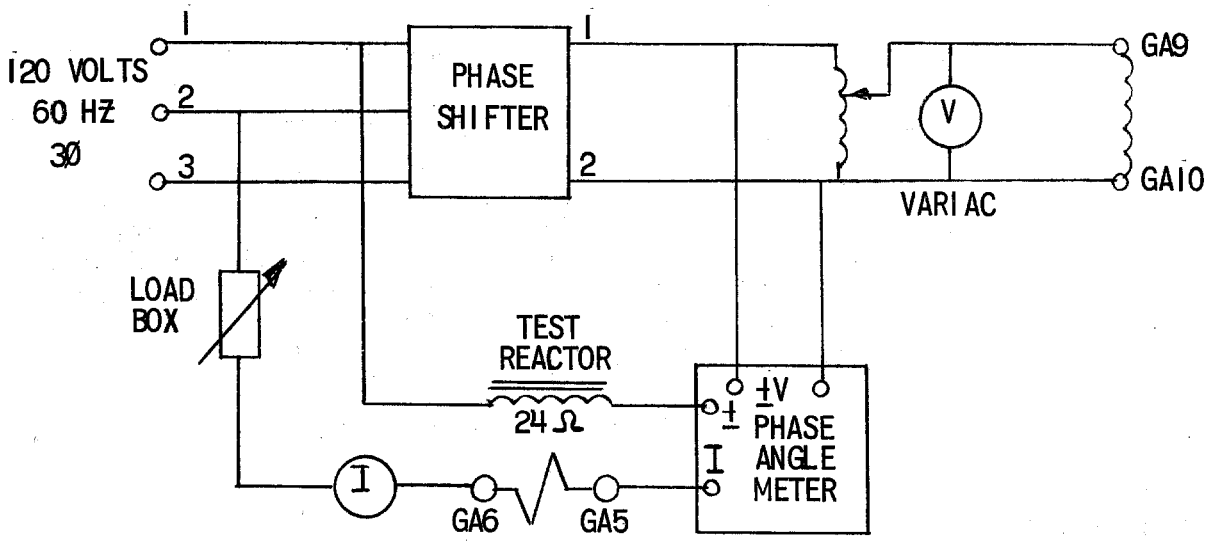
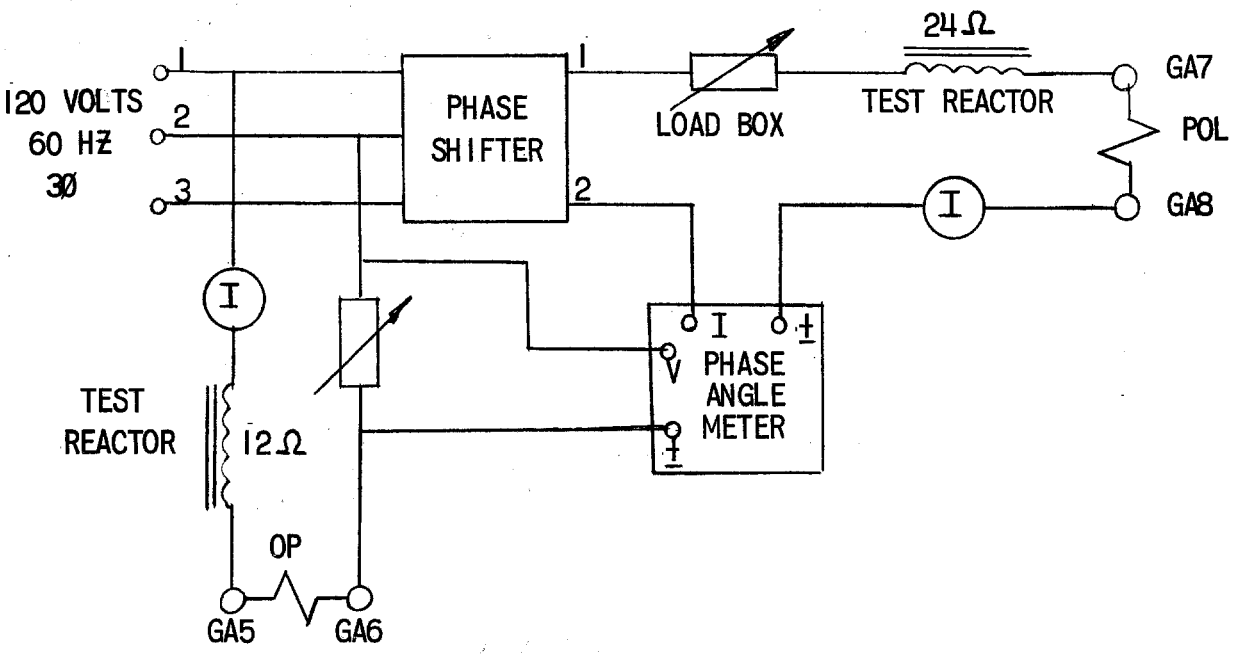


Figure 11 (0227A2153-0). Timer Test Circuit



POTENTIAL POLARIZATION



CURRENT POLARIZATION

Figure 12 (0257A6226-0). SLPG51A Directional Characteristics Test Circuit

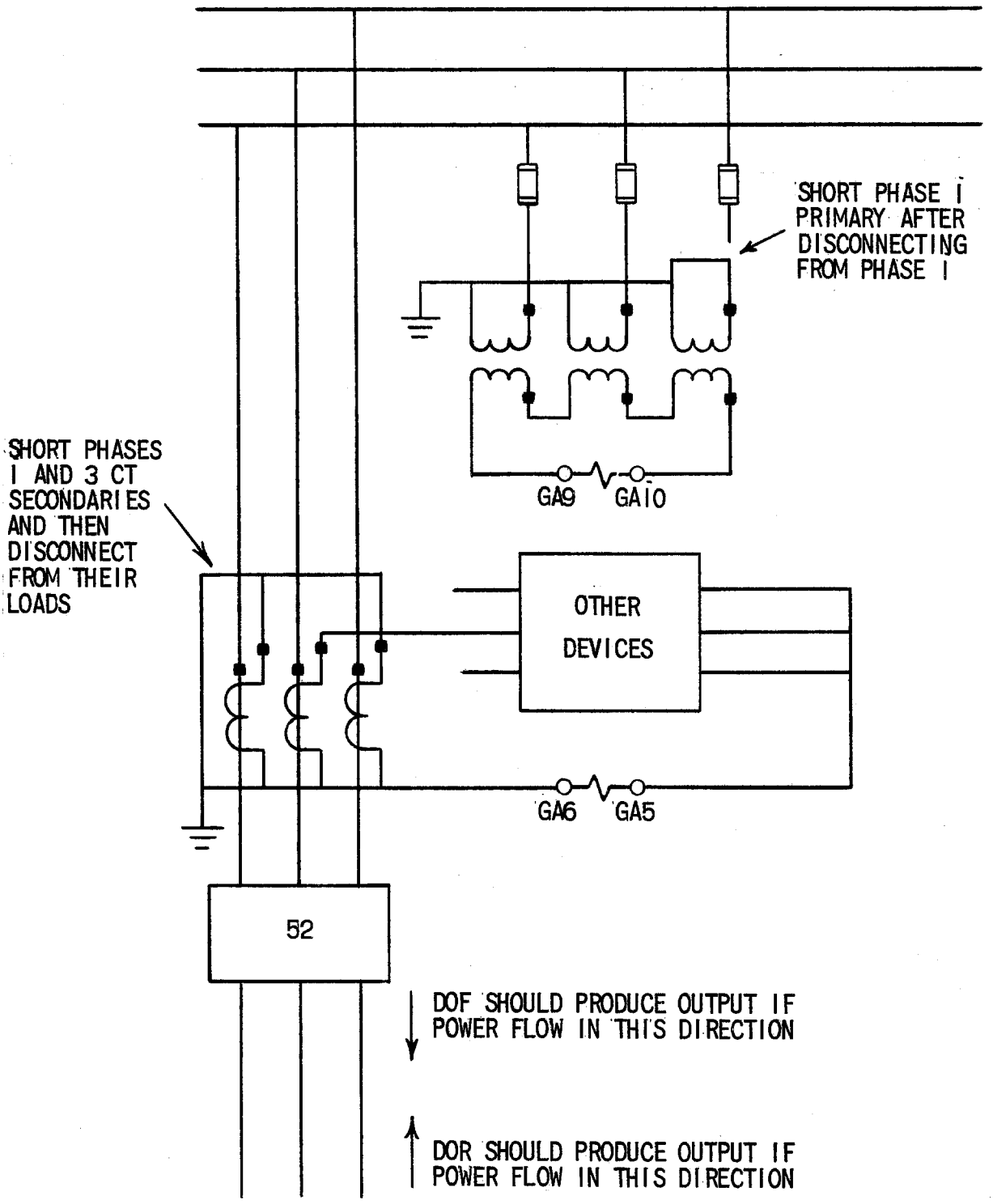


Figure 13 (0257A8506-0). Load Current Polarity Test