INSTRUCTIONS

GEK-45413

STATIC PHASE SELECTOR

TYPE SLS51A

POWER SYSTEMS MANAGEMENT DEPARTMENT

GENERAL ELECTRIC

PHILADELPHIA, PA.

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STATIC PHASE SELECTOR

TYPE SLS51A

DESCRIPTION

The type SLS51A relay is used in single pole tripping and reclosing schemes to select the appropro-ate pole or poles of the breaker(s) to be tripped. The single pole phase selector circuits provide phase selection for single line to ground faults. The phase A selector compares the phase co-incidence between I_{A2} and I_{AO}. I_{A2} and I_{AO} are essentially in phase for A to ground faults and 120° out of phase for B to ground and C to ground faults. Hence the phase relation between I_{A2} and I_{AO} provides a reliable method of selecting phase A for A to ground faults. Similarly, the phase B selector uses I_{B2} and I_{BO}, and the phase C selector uses I_{C2} and I_{CO} for phase selection.

The SLS51A relay is packaged in a four rock unit (one rock unit =1.75 in) case whose out line and mounting dimensions are shown in Fig 2. Component locations are shown in Fig 3. The internal connections are shown in Fig 1.

The sequence quantities referred to phase A are illustrated in Fig 4 for single line to ground faults and double line to ground faults.

On double line to ground faults the single pole phase selectors select the unfaulted phase, that is for a BC to ground fault, the phase A selector operates.

The three pole phase selector circuits consists of two functions, a positive sequence undervoltage function that measures the positive sequence voltage of the relay location and a compensated positive sequence undervoltage function that is intended to measure the positive sequence voltage at or near the remote and of the line. The compensated positive sequence undervoltage function has a zero sequence restraint signal to prevent operation on single line to ground faults at the near end of the line. The compensated undervoltage function operates in accordance with the equation

$$|V_{1R} - I_1 Z_R| + |I_0 Z_R| < 0.5\, V_1 \text{ per unit}$$

Where V_{1R} is the positive sequence voltage at the relay and Z_R is an adjustable reach setting.

APPLICATION

Reference should be made to the appropriate logic description for application information for the particular application considered.

Typically the single pole phase selectors have a co-incidence timer setting of 120° electrical degrees.

The uncompensated undervoltage function is typically set at one half the minimum positive sequence voltage that occurs under load (but not fault) conditions on the power syster. If line side potential is used, this setting should be checked to ensure it is above the positive sequence voltage occuring when one phase is open on the line after a single pole trip.

The compensated undervoltage function typically has the same undervoltage setting as the uncompensated undervoltage function. The positive and zero sequence reach settings (Z_R) are typically the same and equal to 125° of the positive sequence impendance of the line. However, on series compensated lines a different reach setting may be appropriate depending on the locations of the series capacitors.

RATINGS

The Type SLS51A relay is designed for use in an environment where the ambient temperature around the relay case is between - 20°C and +65°C.

The Type SLS51A relay requires a ±15VDC power source which can be obtained from a Type SSAS0/51 power supply.

These instructions do not purport to cover all details or variations in equipment nor to provide for every possible contingency to be met in connection with installation, operation or maintenance. Should further information be desired or should particular problems arise which are not covered sufficiently for the purchaser's purposes, the matter should be referred to the General Electric Company.

To the extent required the products described herein meet applicable ANSI, IEEE and NEMA standards; but no such assurance is given with respect to local codes and ordinances because they vary greatly.

The current circuits of the Type SLS51A relay are rated for 1 Ampere, 50 Hertz for continuous duty and have a one second rating of 50 Amperes.
The potential circuits are rated for 120 VAC.

BURDENS

The Type SLS51A relay presents a maximum burden to the Type SSA Power supply of:

150 ma from the +15VDC supply
75 ma from the -15VDC supply

The burden presented by the current circuits at 1A is.

The burden presented by the potential circuits at 120 VAC is

RANGES

Each single phase selector has the following sensitivity:

0.03 Ampere negative sequence
0.06 Ampere $3I_0$

The V_1 function has a pickup range of 40 to 80 VRMS
The positive and zero sequence reaches (Z_1 & Z_0) have a range of 5 to 150 ohms

The V_1X function has a pickup range of 40-80 VRMS.

OPERATING PRINCIPLES

A. Introduction

The SLS51A relay uses signals derived from the secondary currents and voltages as operating quantities for the various measuring functions included in the unit. Signals proportional to positive sequence voltage and current, negative sequence current and zero sequence current are derived in the relay.

B. Positive Sequence Voltage Network

The positive sequence voltage network is shown on the internal connection diagram of figure 1. The positive sequence voltage network consists of 3 phase to phase voltage transformers (TA, TB, TC) and an active (using operational amplifiers) sequence network which is contained on the F144 card in card location H. The voltage at the V_1 test jack is given by the expression:

$$V_1 \text{ test jack} = 0.10 \times V_{1A}$$

where: V_{1A} is the positive sequence input voltage referenced to phase A
Potentiometers P1 and P2 are used to cancel small errors due to the potential source which supplies the relay.

C. Positive Sequence Current Network

The positive sequence current network is shown on the internal connection diagram of figure 1. The positive sequence current network consists of three phase to phase current transformers (TD,TE, TF), three loading reactors (X1, X2, X3) and an active sequence network on the F143 card in card location G. The output of the card may be measured at pin 9 of the G card. The voltage at this point is given by the expression:

$$\text{Voltage at pin 9, G card} = 1.1 \times I_{A1} \angle 0°$$

where: I_{A1} is the positive sequence component of the input current referenced to phase A.

D. NEGATIVE SEQUENCE CURRENT NETWORK

The negative sequence current networks are shown on the internal connections diagram of figure 1. The negative sequence current networks use the same current transformers and reactors as the positive sequence current network. Active Sequence networks are located on the F140 cards in positions D,E, and F. The network output may be observed at pin 9 of these cards. Its magnitude is given by:

$$\text{Pin 9 output} = 5.4\ I_Z$$

where I_Z is the magnitude of the negative sequence current in the input.

The outputs of the three cards are 120° out of phase because each network is referenced to a different phase.

E. ZERO SEQUENCE CURRENT NETWORK

The zero sequence current network is shown on the internal connection diagram of figure 1. It consists of a current transformer TG and a loading reactor X4. The input to the CT is the secondary $3I_o$ current, the output is a voltage proportional to the zero sequence current.

RECEIVING, HANDLING AND STORAGE

These relays will normally be supplied as a part of a static relay equipment, mounted in a rack or cabinet with other static relays and test equipment. Immediately upon receipt of a static relay equipment, it should be unpacked and examined for any damage sustained in transit. If injury or damage resulting from rough handling is evident, file a damage claim at once with the transportation company and promptly notify the nearest General Electric Sales Office.

Reasonable care should be exercised in unpacking the equipment. If the equipment is not to be installed immediately, it should be stored indoors in a location that is free from moisture, dust, and metallic chips, and severe atmospheric contaminants.

Just prior to final installation the shipping support bolt should be removed from each side of all relay units, to facilitate possible future unit removal for maintenance. These shipping support bolts are approximately 8 inches back from the relay unit front panel. Static relay equipment, when supplied in swing rack cabinets, should be securely anchored to the floor or to the shipping pallet to prevent the equipment from tipping over when the swing rack is opened.

INSTALLATION TESTS

CAUTION

THE LOGIC SYSTEM SIDE OF THE DC POWER SUPPLY USED WITH MOD III STATIC RELAY EQUIPMENT IS ISOLATED FROM GROUND. IT IS A DESIGN CHARACTERISTIC OF MOST ELECTRONIC INSTRUMENTS THAT ONE OF THE SIGNAL INPUT TERMINALS IS CONNECTED TO INSTRUMENT CHASSIS. IF THE INSTRUMENT USED TO TEST THE RELAY EQUIPMENT IS ISOLATED ROM GROUND, ITS CHASSIS MAY HAVE AN ELECTRICAL POTENTIAL WITH RESPECT TO GROUND. THE USE OF A CONNECTION TO THE EQUIPMENT, SUCH AS A TEST LEAD INADVERTANTLY DROPPING AGAINST THE RELAY CASE, MAY CAUSE DAMAGE TO THE LOGIC CIRCUITRY.

NO EXTERNAL TEST EQUIPMENT SHOULD BE LEFT CONNECTED TO THE STATIC RELAYS WHEN THEY ARE IN PROTECTIVE SERVICE, SINCE TEST EQUIPMENT GROUNDING REDUCES THE EFFECTIVENESS OF THE ISOLATION PROVIDED.

A. CONSTRUCTION

The SLS51A relay is packaged in an enclosed metal case with hinged front cover and removable top cover. The case is suitable for mounting on a standard 19 inch rack. The outline and mounting dimensions and the physical location of the components are shown in figures 2 & 3 respectively. The current and potential quantities enter the SLS51A relay on twelve point terminal strips located on the rear of the relay case. The potential connections are made on the RD terminal strip, the current on the RE terminal strip.

The various test jacks are located on the front of the unit. The positive sequence voltage network trimmer potentiometers (P1 & P2) are located on the rear of the unit.

The SLS51A relay also contains printed circuit cards identified by a code number such as F140, C104, T133 where F designates filter, C designates coincidence and T designates time delay.

The printed circuit cards plug in from the front of the unit. The card sockets are identified by letter designations or "addresses"(D,E,AD etc) which appear ont the guide strips in front of each socket, on the component location diagram on the internal connection diagram, and on the printed circuit card itself. The test points (TP1, TP2 etc) shown on the internal connection diagram are connected to instrument test jacks on a test card in position T or AT. The jacks are numbered from top to bottom with T_{P1} to T_{P10} on the AT card and T_{P11} to T_{P20} on the T card. T_{P1} is connected to relay reference, T_{P2} is connected to -15VDC and T_{P10} to +15VDC. Output signals are measured with respect to relay reference. Logic signals are approximately +15VDC for the ON or "logic one" condition and less than /VDC for the OFF or "logic zero" condition. The output of the filter cards may be analog signals with a range of -15V to +15V. The internal connections of the printed circuit cards along with information on design and testing may be found in the Printed Circiut Card Instruction Book GEK-34158.

Relay signals can be monitored with an oscilloscope, a portable high impedance voltmeter, or the equipment test panel meter. When time delay cards are to be adjusted or checked, an oscilloscope which can display two traces simultaneously and which has a calibrated horizontal sweep should be used.

When the SLS51A relay is supplied mounted in a static relay equipment, the incoming potential and current circuits pass through test receptacles on the equipment test panel. The potential test plug is labled TPP, the current TCP. These plugs may be replaced with Type XLA test plugs which allow test voltages and currents to be supplied to the relay while maintaining a continuous path for the secondary current.

B. REQUIRED TESTS AND ADJUSTMENTS

The SLS51A relay is usually supplied from the factory mounted and wired as part of a complete static relay equipment. All units in an equipment are tested together and all unit nameplates carry the equipment summary number. The necessary tests and adjustments are listed below those marked with an asterisk must be set by the user. All steps should be performed per the procedures under Detailed Testing Instructions to insure that no shipping damage has occurred. The steps should be performed in the order shown.

1. Positive sequence voltage network balance setting*
2. Positive negative sequence current network balance checks.
3. Single pole selector checks
4. Three pole selector checks and settings*
   a) Positive & zero sequence reach setting
   b) Positive sequence voltage phase shift setting
   c) V_{1X} pickup setting
   d) V_1 pickup setting

C. DETAILED TESTING INSTRUCTIONS

1. Positive Sequence Voltage Balance Setting

The purpose of this test is to adjust the trimmer potentiometers P_1 and P_2. Because these potentiometers are intended to correct small errors due to unbalance in the potential source, it is necessary to set these potentiometers with the equipment connected to the system. For preliminary tests before installation, these potentiometers may be left at the factory setting.

When the SLS51A is mounted in a static relay equipment, the incoming potential circuits pass through the potential test plug (TPP) on the ewuipment test panel. The plug may be replaced with an Type XLA test plug, and the phase rotation of the source voltage may be reversed on the plug connections. This simulates negative sequence voltage being supplied to the relay. Refer to figure 5.

With only negative sequence voltage applied, observe the voltage at the V_1 test jack with an oscilloscope. This voltage should be less than 0.3V peak to peak and consist primarily of third harmonic. Potentiometers P_1 and P_2 may be alternately adjusted to lower the magnitude of the V_1 test jack.

2. Positive/Negative Sequence Current Network Balance Checks

There are no adjustments in the positive or negative sequence current networks. The precision components used for these networks eliminates the need for adjustments. The following procedure will ascertain that the networks are functioning properly.

i) Use the negative sequence connections of figure 6. Set the current in each phase to one ampere. Check for ±15V square waves at the I_{A2}, I_{B2}, and I_{C2} test jacks. Set the X option plug on the G card to position A, adjust potentiometer P_1 on the G card fully clockwise; check for less than 5 volts peak to peak at the I_2Z test jack.

ii) Use the positive sequence connections of figure 6. Set the current in each phase to one ampere. Check for less than 10 volts peak to peak at the I_{A2}, I_{B2}, and I_{C2} test jacks. Note that the currents may be adjusted ±.02 ampere to achieve this null. A different current adjustment may be needed to achieve the null at each test jack.

Set the X option plug on the G card in position 4, adjust P_1 on the G card fully counter clockwise, set the current for 0.2 ampere per phase. Check that the voltage at the I,Z test jack is greater than 7.4 VRMS.

3. Single Pole Phase Selector Checks

i) Timer D.C. Pickup and Dropout Setting

The D.C. pickup and dropout of the characteristic timers (T133 cards in positions AE, AG and AJ) can be set using the circuit of figure 7. The integrated pickup will be set in section 4.
Openning the contact causes the output to step to +15 VDC after the pickup delay of the timer. Turning potentiometer P_1 (upper pot on card) clockwise increases the pickup delay. Closing the contact causes the output to drop from 15VDC to less than 1VDC after the dropout delay of the timer.

ii) Functional Tests

Connect the phase A to ground test circuit of figure B. Set the current for one ampere. Check that the logic signal at $+P_{14}$, T_{P15}, & T_{P16}, is at 15VDC; if it is at reference, remove the appropriate card in the associated Type SLA unit to produce a logic one at T_{P14}, T_{P15}, & T_{P16}. Check for continuous output at T_{P3} (A phase selector)and no output at T_{P4} and T_{P5} (B & C phase selectors). Repeat for the B to ground and C to ground tests of figure G.

4. Three Pole Selector Checks and Settings

i) Positive and Zero Sequence Reach Setting

Connect the phase A to ground test circuit of figure 8. Set the current for 2 amperes. For the positive sequence reach, set the X option plug on the F143 card in position G per the following table. For the zero sequence reach set the X option plug on the F142 card in position K per the following table

X option tap	Z_0/Z_1 reach (R)
1	60 to 150 Ω
2	25 to 60 Ω
3	10 to 25 Ω
4	5 to 10 Ω

NOTE: Use the highest numerical tap possible for the desired setting

Use potentiometer P_1 on the F142 card in position K to adjust the voltage at the I_0Z test jack to a value given by the expression

$$I_0Z \text{ TEST JACK} = 0.135\ XZ_0$$

where Z_0 is the desired zero sequence reach setting

Use potentiometer P_1 on the F143 card in position G to adjust the voltage at the I_1Z test jack to a value given by the expression:

$$I_1Z \text{ Test jack} = 0.135\ X\ Z_1$$

where Z_1 is the desired positive sequence reach setting

ii) Positive Sequence Voltage Level and Phase Shift Setting.

The V_1 phase shift is set by means of the W option plug on the F144 card in position H. The available phase shifts are listed in the following table

W option tap	V_1 leading phase shift
0	0°
1	10°
2	20°
3	30°

Connect the positive sequence voltage circuit of figure 9. Disconnect all current inputs. Set the voltage for 120 VRMS phase to phase. Check that the voltage at the V_1 test jack is between 6.85 and 7.15 VRMS. If the voltage is outside this range, adjust potentiometer P_1 on the F144 card in position H to obtain 7.0 VRMS at the V_1 test jack.

Set the test voltage for the desired V_1 pickup. Adjust potentiometer P_1 on the D117 card in position AM to just obtain pickup. Note that due to the NOT output of the D117 card, T_{P7} is at reference when the applied voltage is greater than the pickup setting and at +15VDC when the applied voltage is less than the pickup setting.

Set the test voltage for the desired V_{1X} pickup. Adjust potentiometer P_2 on the F135 card in position AK to just obtain pickup at T_{P6}. Note that the signal at T_{P6} is at reference when the applied voltage is greater than the V_{1X} pickup setting and at +15VDC when the applied voltage is less than the pickup setting.

iii) Timer Integration Setting and Three Pole Selector Check

Use the Test I connections of figure 10. Adjust the current magnitude to obtain blocks at T_{P13} which are 5 ms wide. Adjust P_3 on the T133 card in position AL to just obtain output at T_{P6}. Readjust the current to obtain 6.5 ms blocks at T_{P13}. Replace the AL timer with a T133 from position AE, AG or AJ. Adjust P_3 on the card to just obtain pickup at T_{P6}. Return all cards to their original locations.

Use the Test II connections of figure 10. Set the phase shifter for an angle of 85°-$\emptyset$ is the positive sequence voltage phase shift set in step ii.

The value of I_A test current depends upon the positive sequence reach of the unit (Z_1). The test current to be used is given in the following table.

Z_1(R)	X-TAP	I_A (AMP)
5 - 60	2,3,4	2
60 - 150	1	1

Set the applied voltage to a value given by the expression:

$$V = \frac{I_A Z_1}{3} \times \sqrt{3} \equiv \frac{I_A Z_1}{\sqrt{3}} \text{ (VRMS } \emptyset\text{-}\emptyset)$$

The operating point of the V_{1X} function (measured at T_{P6}) should be within 10% of the I_B test current level given by the expression:

$$I_B = \frac{V_{1X} \text{ (pick up)} \quad \sqrt{3}}{Z_0}$$

where V_{1X} (pick up) is the RMS phase to phase voltage set previously
Z_0 is the zero sequence impedence set previously
I_B is the test current of figure 10.

NOTE: Currents greater than 2 amperes should not be continuously applied to the relay.

Periodic Checks and Routine Maintenance

1. Periodic Tests

All of the functions included in the SLS51A relay may be checked at periodic intervals using the procedures described in Installation Tests. Cable connections between the SLS51A relay and the associated Type SLA logic unit may be checked by observing the test points is the SLA relay.

2. Trouble Shooting

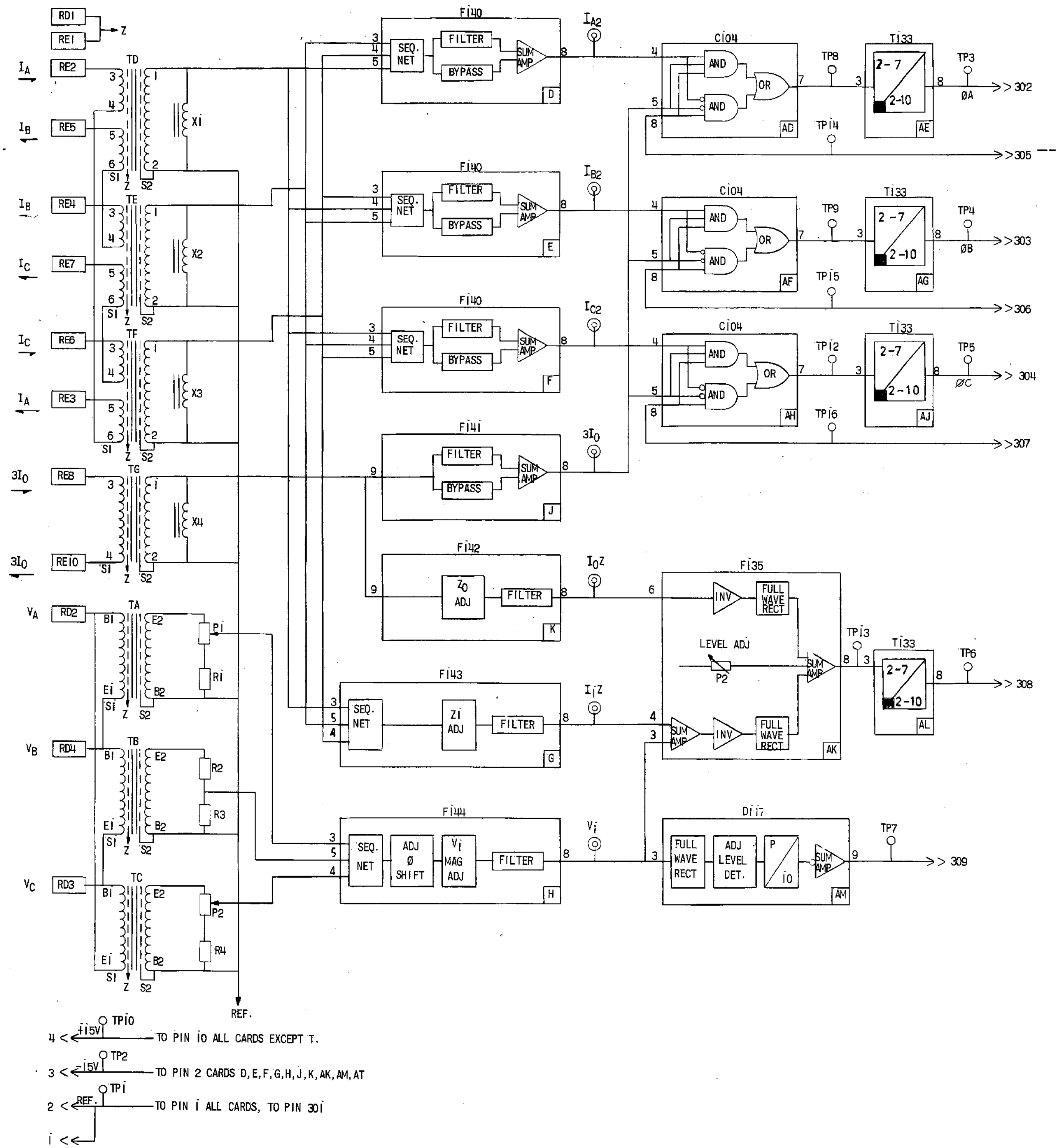
In any trouble shooting of equipment, it should first be established which unit is functioning incorrectly. The overall logic diagram supplied with the equipment shows the combined logic of the complete equipment and the various test points in each unit. By signal tracing, using the overall logic diagram and the various test points, it should be possible to quickly isolate the trouble.

A test adapater card is supplied with each static relay equipment to supplement the pre-wired test points on the test cards. Use of the adapter card is described in the card instruction book GEK-34158.

A dual-trace oscilloscope is a valuable aid to detailed trouble shooting, since it can be used to determine phase shift, operate and reset times as well as input and output levels. A portable dual-trace oscilloscope with a calibrated sweep and trigger facility is recommended.

3. Spare Parts

To minimize possible outage time, it is recommended that a complete maintenance program should include the stocking of at least one spare card of each type. It is possible to replace damaged or defective components on the printed circuit cards, but great care should be taken in soldering so as not to damage or bridge-over the printed circuit buses, or overheat the semi-conductor components. The repaired area should be recovered with a suitable high-dielectric plastic coating to prevent possible breakdowns across the printed buses due to moisture and dust. The wiring diagrams for the cards in the SLCN51B relay are included in the card book GEK-34158; the card types are shown on the component location diagram (Figure 3).



COMPONENT VALUES	
R1,R3,R4	500Ω,5 1/4W
R2	24Ω,5 1/4W
P1,P2	50Ω,12 1/2W

FIGURE 1 (0167C8727-1) INTERNAL CONNECTIONS DIAGRAM FOR THE TYPE SLS51A RELAY.

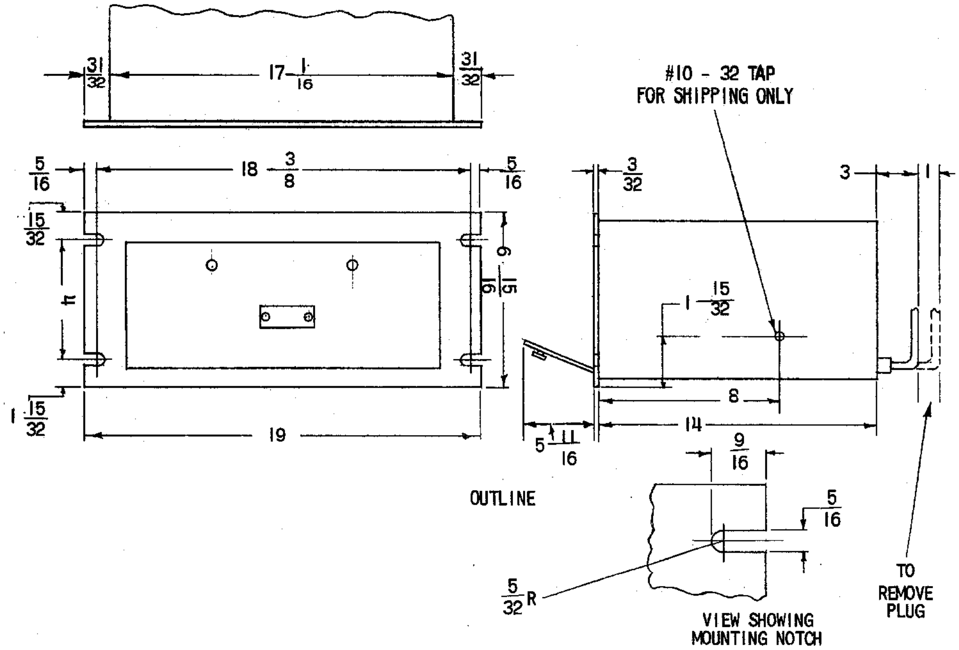


FIGURE 2 (0227A2037-0) OUTLINE AND MOUNTING DIMENSIONS FOR THE SLS51A

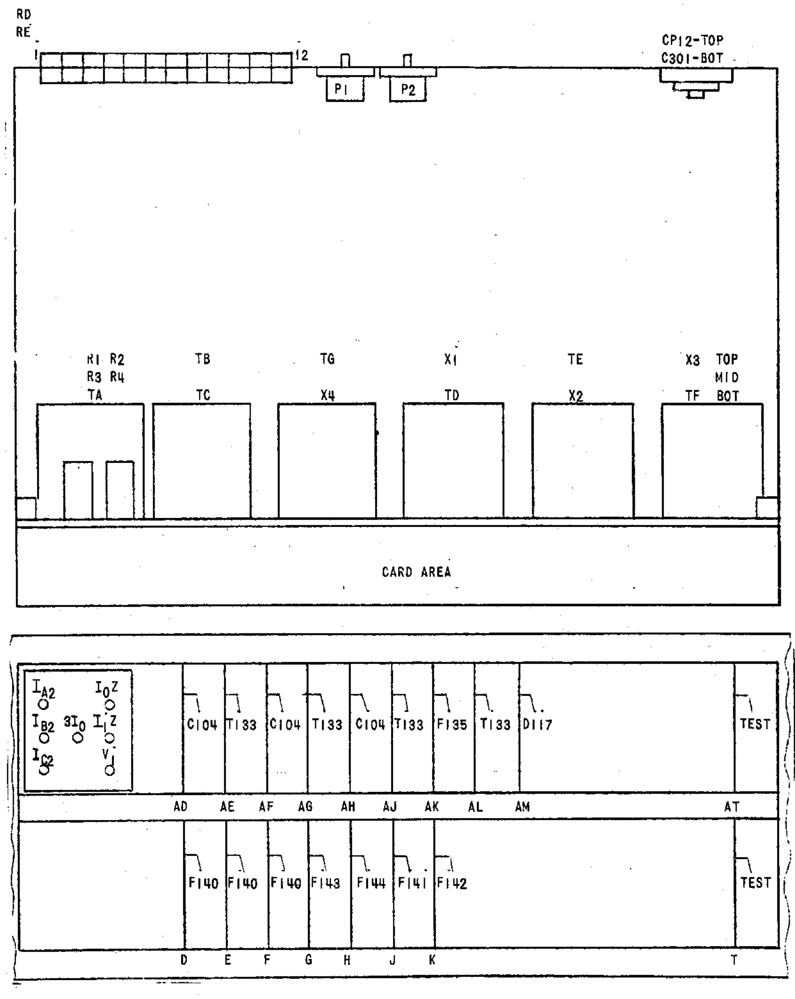


FIGURE 3 (0257A6271-0) COMPONENT LOCATION DIAGRAM FOR THE TYPE SLS51A.

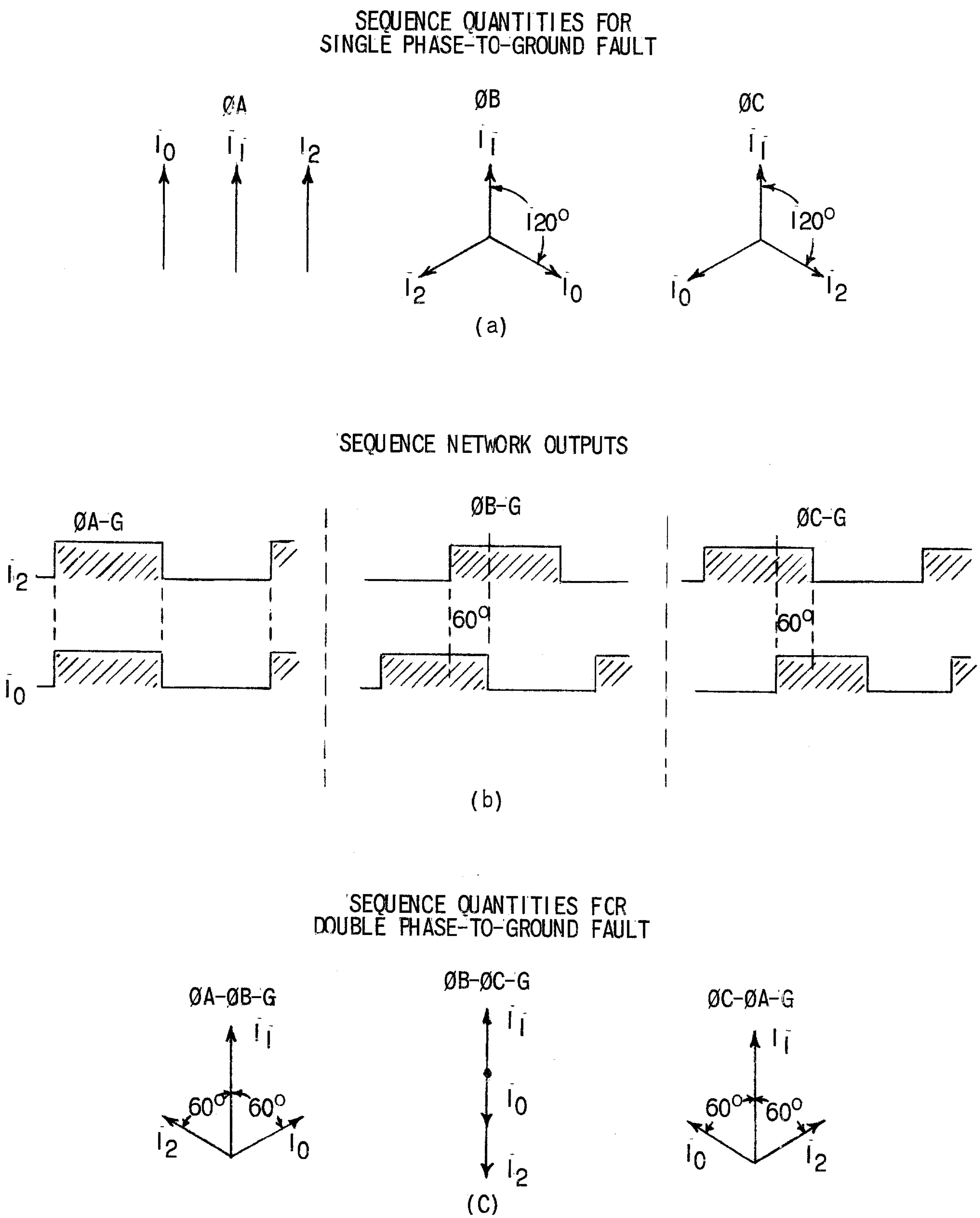


FIGURE 4 (0257A6249-0) SEQUENCE NETWORK INPUTS AND OUTPUTS.

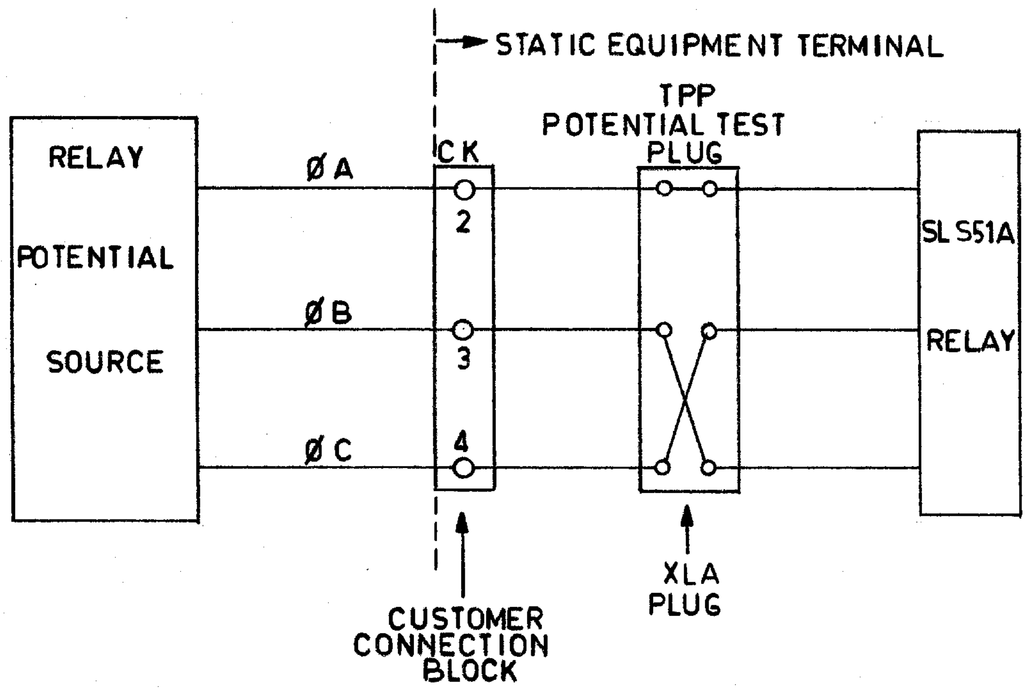


FIGURE 5 (0257A8737-0) CONNECTIONS FOR POSITIVE SEQUENCE VOLTAGE NETWORK BALANCE CHECK.

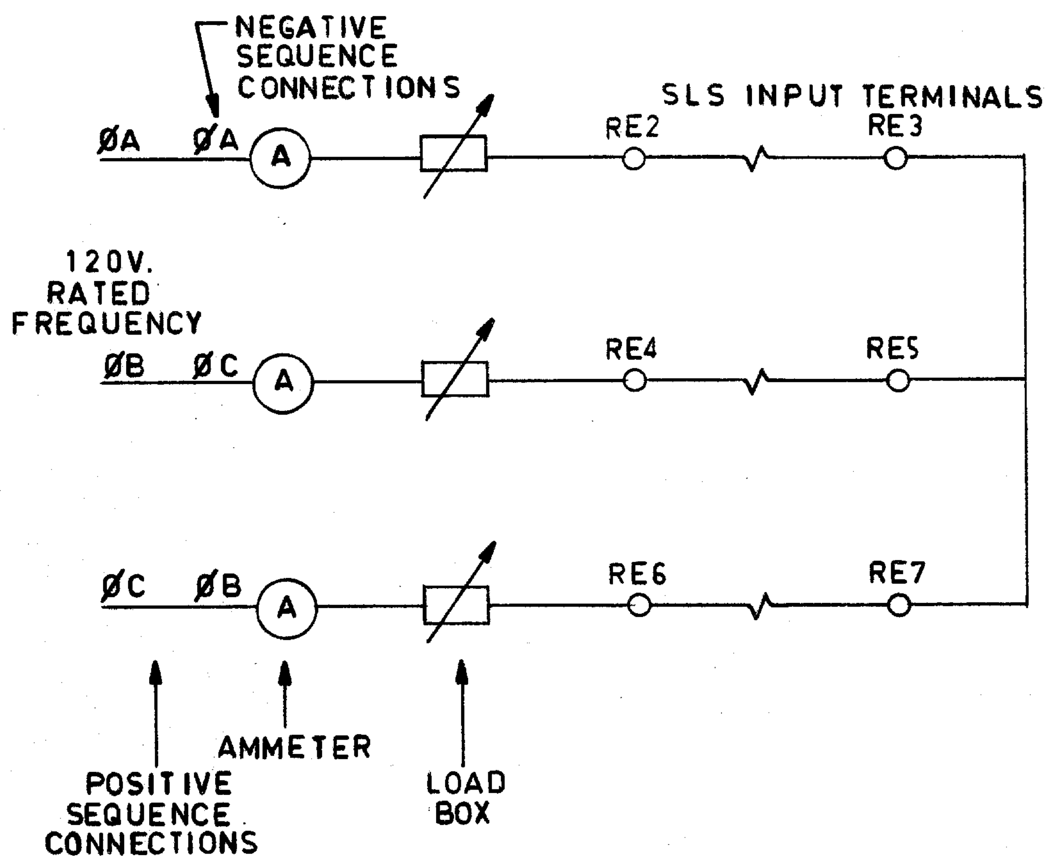
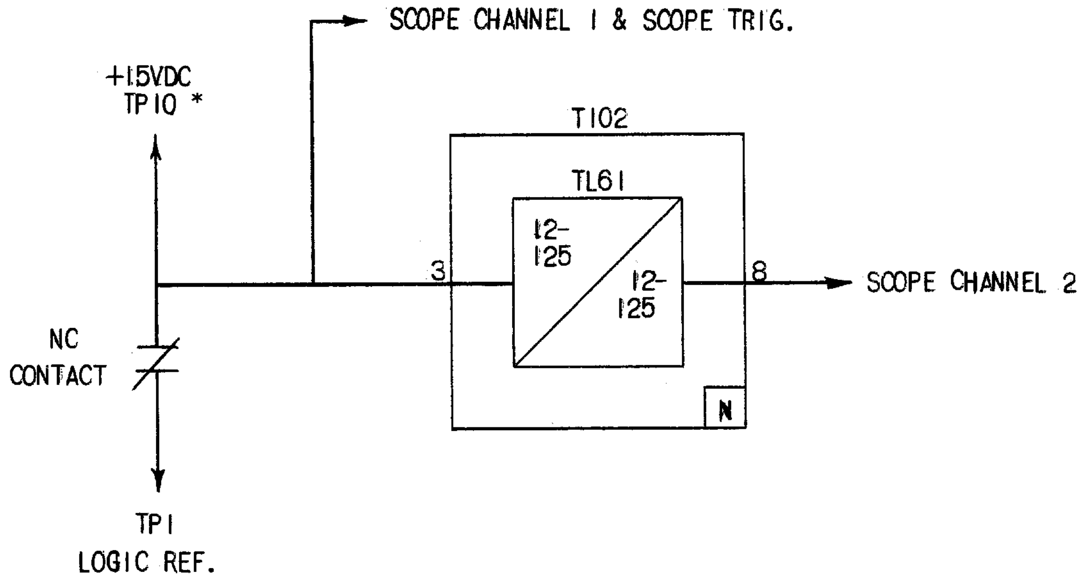
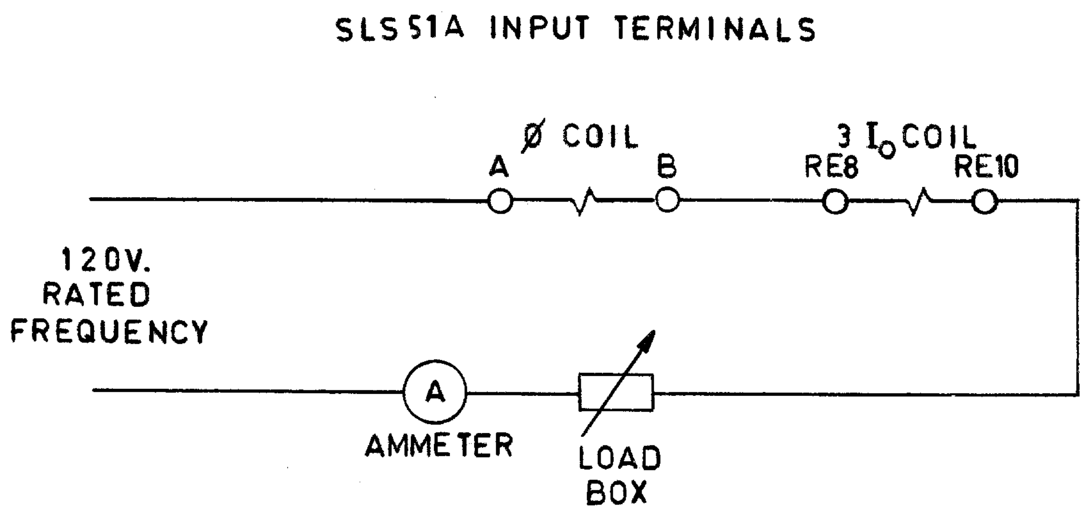


FIGURE 6 (0257A8738-0) CONNECTIONS FOR SEQUENCE CURRENT NETWORK BALANCE CHECK.



* THE 15VDC SIGNAL AT PIN 10 HAS A CURRENT LIMITING RESISTOR MOUNTED ON THE TEST CARD.

FIGURE 7 (0246A7987-0) TIMER TEST CIRCUIT



TEST	A	B
A–G	RE 2	RE 3
B–G	RE 4	RE 5
C–G	RE 6	RE 7

FIGURE 8 (0257A8740-0) CONNECTIONS FOR SINGLE POLE PHASE SELECTOR CHECKS

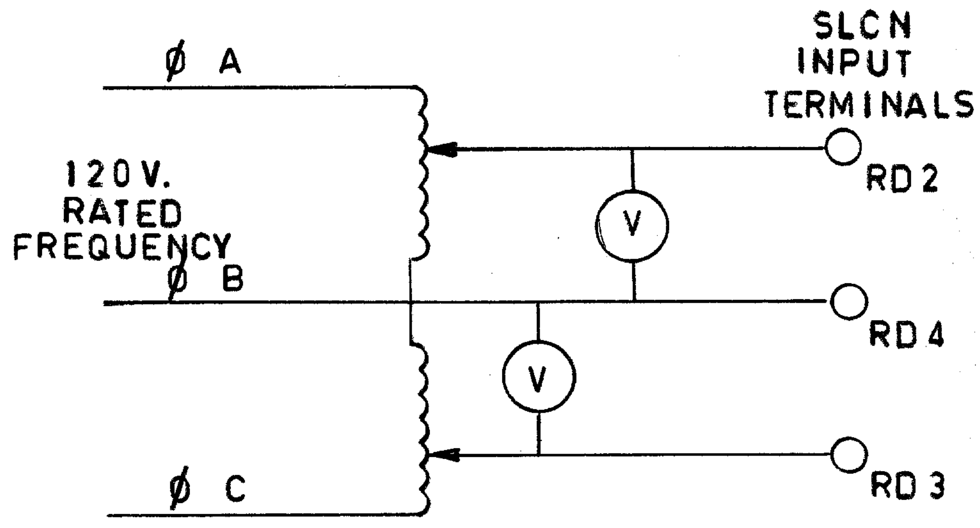
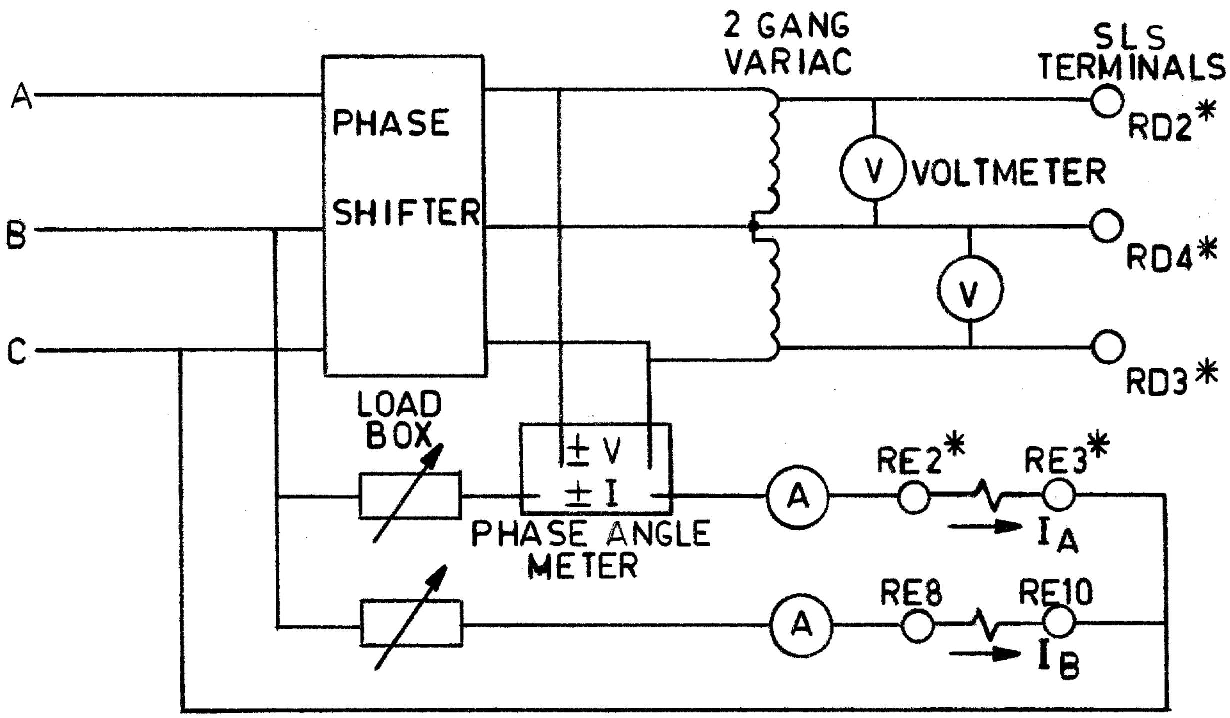


FIGURE 9 (0257A8739-0) CONNECTIONS FOR POSITIVE SEQUENCE VOLTAGE LEVEL DETECTOR TESTS



* DO NOT MAKE THESE CONNECTIONS FOR TEST I

FIGURE 10 (0257A8736-0) CONNECTIONS FOR THREE POLE SELECTOR OPERATIONAL CHECK

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