INSTRUCTIONS

GEK- 34079A

NEGATIVE SEQUENCE DISTANCE RELAY

TYPE SLYN51A

GENERAL ELECTRIC

CONTENTS

DESCRIPTION

The SLYN51A is a solid state negative sequence distance relay that is packaged in one 2 rack unit case the outline and mounting dimensions of which are illustrated in Figure 1.

This relay is not intended for use by itself. Rather it was designed to be employed in conjunction with other solid state measuring and logic relays to provide protection against all types of faults on series compensated lines and on uncompensated lines that are adjacent to series compensated lines. The total complement of functions that may be included in the SLYN51A are noted below.

M_2T - First zone negative sequence directional distance tripping function.

L_2T - Negative sequence directional distance pilot tripping function.

M_2B - Negative sequence directional distance blocking function.

D_2F - Negative sequence directional function operates in the tripping direction.

D_2R - Negative sequence directional function operated in the blocking direction.

In general, the M_2T function is not provided unless specifically requested since it is not an essential element in the protective scheme. When it is employed it will provide first zone direct tripping for all phase-to-phase and most double phase-to-ground faults within its reach setting. However, all SLYN51A relays include facilities for adding the M_2T function in the field by obtaining the proper printed circuit cards and plugging them into available sockets. However, in order to utilize the function, the proper logic is required in other relays that comprise the total scheme.

Please refer to the overall logic diagram and the associated description for the specific job involved to determine whether or not the M_2T function is included. This information may also be obtained from the nameplate mounted on the SLYN51A relay since the nameplate lists the range of all the included measuring functions.

The internal connections for the SLYN51A are shown in Figure 3. While the location of all the components including printed circuit cards is included in Figure 2.

APPLICATION

The SLYN51A is a negative sequence relay including both distance and directional functions that is intended to be an integral part of a pilot relaying scheme for use in the protection of series compensated lines and lines adjacent to series compensated lines. It is suitable for use in schemes that employ carrier channels as well as microwave channels.

All of the functions in the SLYN51A with the exception of the M_2T are essential to the total scheme of protection. The M_2T is an optional first zone direct tripping function that is not normally required. When used it will provide first zone distance protection for all phase-to-phase and most double phase-to-ground faults on the protected line within its setting. However, it is only suitable for use on very long lines. For information on the application of the M_2T function please refer to the Local Sales Office of the General Electric Company. While all SLYN51A relays include the wiring and card sockets to accommodate the M_2T function, the proper logic is required in the other relays that comprise the total scheme if M_2T is to be used.

The basic protective scheme of which the SLYN51A is a part may be routinely applied to all lines up to 200 miles in length where:

a) The source of ac potential to the relays is located on the line side of the series capacitors in the protected line.

b) The compensation in the line does not exceed 80 percent.

These instructions do not purport to cover all details or variations in equipment nor to provide for every possible contingency to be met in connection with installation, operation or maintenance. Should further information be desired or should particular problems arise which are not covered sufficiently for the purchaser's purposes, the matter should be referred to the General Electric Company.

c) The series capacitor protective gaps are set to flash at an instantaneous value of voltage that is equal to, or lower than, the peak value of the rated phase-to-neutral voltage of the line.

For the proper external connections for the SLYN51A relay please refer to the elementary diagrams furnished with the overall equipment.

RANGES

The SLYN51A relay has an adjustable system reach of 1 to 30 ohms in the forward (tripping) direction

The reach of each measuring function in the SLYN51A is fixed at a specific percentage of the relay system reach. For example, if the relay system reach has been set at 4.0 ohms and the relay nameplate indicated the M_2T reach is 75%, then the reach of the M_2T is 75% x (4) = 3 ohms.

All fixed reaches are listed on the relay nameplate. Typical values are shown here.

M_2T operate	90%
M_2T restraint	90%
L_2T operate	100%
L_2T restraint	150%
M_2B operate	125%
M_2B restraint	150%

The SLYN51A has an angle of maximum reach which is adjustable between 60 and 90 degrees.

All adjustment ranges are listed on the relay nameplate. Typical ranges are shown here.

D_2R and D_2F offset 20-100%

RATINGS

The Type SLYN51A relay is designed for use in an environment where the air temperature outside the case is between $-20^{o}C$ and $+65^{o}C$.

The Type SLYN51A relay requires a ±15 VDC power source which can be obtained from a Type SSA power supply.

The current circuits of the SLYN51A relay are rated at 5 amperes rated frequency, for continuous duty and have a one second rating of 300 amperes. The potential circuits are rated at 120V, rated frequency.

CHARACTERISTICS

Operating Principles

The SLYN51A relay uses negative sequence voltage and current networks to obtain the V_2 and I_2Z signals which are used as the operating quantities for the various measuring functions. Some functions also require positive sequence operating quantities (V_1, I_1Z). The positive sequence quantities are supplied from a type SLYP relay. The operating theory of the relay networks which derive the negative sequence quantities is explained in the following paragraphs.

A. Negative Sequence Voltage Network

The negative sequence voltage network is shown in Figure 4. The network consists of a variable resistor and capacitor phase-shift circuit plus a resistor divider circuit. These circuits are adjusted to phase shift a voltage and adjust the voltage magnitude until the output is equal in phase angle and magnitude of V_{AN}, since $V_{AN} = V_2$ for a balanced negative sequence input.

The derivation of the output voltage is described below.

$$V_{OUT} = V_{C-B} \frac{kP1 + R2}{R1+R2+P1} + V_{B-A} \frac{m\,P2}{mP2 + 1/jwc}$$

where K and m are the fraction of P1 and P2 used.

By design,

$$\frac{k\,P1 + R2}{R1 + R2 + P1} = 1/2$$

$$\frac{m\,P2}{mP2 + 1/jwc} = 1/2\ \underline{/60^o}$$

Therefore,

$$V_{OUT} = 1/2\ V_{C-B} + 1/2\ V_{B-A}\ \underline{/60^o}$$

$$V_A = V_{A0} + V_{A1} + V_{A2}$$

$$V_B = V_{A0} + a^2\ V_{A1} + a\ V_{A2}$$

$$V_C = V_{A0} + a\ V_{A1} + a^2\ V_{A2}$$

$$V_{OUT} = 1/2 \left[(V_{A0} + a\ V_{A1} + a^2\ V_{A2}) - (V_{A0} + a^2\ V_{A1} + a\ V_{A2}) \right] + 1/2\ \underline{/60^o} \left[(V_{A0} + a^2\ V_{A1} + aV_{A2}) - (V_{A0} + V_A + V_{A2}) \right]$$

$$= 1/2 \left[(a-a^2)\ V_{A1} + (a^2-a)\ V_{A2}\right] + 1/2\ \underline{/60^o} \left[(a^2-1)\ V_{A1} + (a-1)\ V_{A2}\right]$$

$$= .866 \left[V_{A1}\ \underline{/90^o} + V_{A2}\ \underline{/-90^o} + V_{A1}\ \underline{/-90^o} + V_{A2}\ \underline{/210^o} \right]$$

$$V_{OUT} = 1.5\ V_{A2}\ \underline{/240^o}$$

For a pure negative sequence input:

$$V_{OUT} = .866\ V_{B-A}\ \underline{/90^o}$$

B. Negative Sequence Current Network

The negative sequence current network used in the SLYN51A relay is shown in Figure 5. The network consists of two transactors (marked TB and TC in Figure 5), each with two primary windings plus an adjustable resistive load across the secondary of each transactor. The output is obtained by vectorially adding the secondary voltage of the two transactors when each adjustable resistor has been set to obtain a very specific phase angle between the two secondary windings.

The term "transactor" is a contraction of transformer - reactor. It is essentially an air-gap current transformer with secondary current (and therefore, secondary voltage across the loading resistor) proportional to the vector sum of the input currents. The performance of a transactor in a circuit is described by its transfer impedance and the associated angle.

$$Z_T = \frac{V_{OUT}}{I_{IN}}\ \underline{/\theta T}$$

Where: V_{OUT} = Secondary output voltage

I_{IN} = Vector sum of the input currents

θ_T = Angle by which V_{OUT} leads I_{IN}

The derivation of the negative sequence current network output voltage is given below.

By design:

$$Z_{TC} = .85\ \sqrt{3}\ Z_{TB}$$

$$\theta_{TB} = 75^{o}$$

$$\theta_{TC} = 45^{o}$$

$$V_{OUT} = k\left[\ Z_{TB}\ (I_B - I_C)\ \underline{/75^{o}}\ \right] + Z_{TC}\ (I_C - 1/3\ I_N)\ \underline{/45^{o}}$$

where k is the percentage of P3 used

Let k = .85

$$V_{OUT} = .85\ Z_{TB}\ (I_B - I_C)\ \underline{/75^{o}} + .85\ \sqrt{3}\ Z_{TB}\ (I_C - 1/3\ I_N)\ \underline{/45^{o}}$$

$$I_B = I_{A0} + a^2\ I_{A1} + a\ I_{A2}$$

$$I_C = I_{A0} + a\ I_{A1} + a^2\ I_{A2}$$

$$V_{OUT} = .85\ Z_{TB}\left[\ (I_{A0} + a^2\ I_{A1} + a\ I_{A2}) - (I_{A0} + a\ I_{A1} + a^2\ I_{A2})\ \right]\ \underline{/75^{o}}$$

$$+ .85\ \sqrt{3}\ Z_{TB}\left[\ I_{A0} + a\ I_{A1} + a^2\ I_{A2} - 1/3\ \ (3\ I_{A0})\ \right]\ \underline{/45^{o}}$$

$$= .85\ Z_{TB}\left[\ (a^2 - a)\ I_{A1} + (a - a^2)\ I_{A2}\right]\ \underline{/75^{o}} + 85\ \sqrt{3}\ Z_{TB}\ \left[a\ I_{A1} + a - I_{A2}\right]\ \underline{/45^{o}}$$

$$= .85\ \sqrt{3}\ Z_{TB}\ (I_{A1}\ \underline{/-15^{o}} + I_{A2}\ \underline{/165^{o}} + I_{A1}\ \underline{/165^{o}} + I_{A2}\ \underline{/285^{o}})$$

$$V_{OUT} = .85\ \sqrt{3}\ Z_{TB}\ I_{A2}\ \underline{/225^{o}}$$

By means of similar manipulations it may be shown that the negative sequence networks of the SLYN51A produce no output when pure positive sequence quantities are applied.

C. Negative Sequence Distance Elements

The M_2T, L_2T, and M_2B elements use an amplitude comparator as the basic discriminating unit. Refer to card locations G, H, and J in Figure 3.

The amplitude comparator cards are used to determine when the operating quantity is greater than the restraint quantity. The operating quantity is the vector sum of the signals at pins 3 and 4. For the M_2T function this is $(-V_2 + I_2Z)$. The restraint quantity is the vector sum of the signals at pins 6 and 7. For the M_2T function this is $(-V_1 + I_1Z)$.

The operating and restraint quantities are AC signals which are rectified on the card. An output signal is produced when the operating quantity is greater than the restraint quantity. When this output lasts longer than the pickup setting of the function timer, an M_2T output is produced.

The reaches of the negative sequence functions are expressed as a percentage of the relay reach. Thi percentage is determined by the fixed resistors mounted on the N102 and N103 cards through which the operating and restraint quantities must pass.

The reach of the operating quantity in percent is given by the relationship:

$$\text{Reach} = \frac{R_{V2} + 10K}{R_{I2Z} + 10K} \times 100\%$$

where R_{V2} and R_{I2Z} are the fixed resistors mounted on the N102 and N103 cards through which the V_2 and I_2Z signals pass. The reach of the restraint quantity in percent is given by the relationship:

$$\text{Reach} = \frac{R_{V1} + 10K}{R_{I1Z} + 10K} \times 100\%$$

where R_{V1} and R_{I1Z} are the fixed resistors mounted on the N102 and N103 cards through which the V_1 and I_1Z signals pass.

In some functions a capacitor in series with the resistor provides a phase shift in that signal. The reach must then be calculated using the series impedance of the resistor and capacitor.

D. Negative Sequence Directional Elements

The D_2R and D_2F elements use a coincidence logic circuit to sense direction. Refer to card locations N, P, R, and S in Figure 3. The input quantities are V_2 and I_2Z from the sequence networks. If the input quantities are in phase long enough to operate the associated timer, a logic signal will be produced indicating the reverse direction. Likewise, if the input quantities are out of phase long enough to operate the associated timer, a logic signal will be produced indicating the forward direction.

Operating Characteristics

The operate and reset times of each distance and direction element is basically determined by the characteristic timer, the type of fault and the incidence angle. There is no significant time delay in the circuitry ahead of the timer.

The sensitivity of each directional element is 0.2 Amperes I_2.

For the distance elements, a phase current of one ampere on a three phase fault will cause the distance units to pull back to no less than 90% of nominal reach, with a basic ohmic tap setting (T_B) of 3Ω.

DC Burden

The Type SLYN51A relay presents a burden to the Type SSA power supply of:

200 ma from the +15 VDC supply
60 ma from the -15 VDC supply

AC Burden

Potential Circuits at 120V Ø-Ø.

	PHASE A		PHASE B		PHASE C	
RESTRAINT	100%	0%	100%	0%	100%	0%
VOLT-AMP	7.0		5.5			
WATTS						
VARS						

Current Circuits at 5A Ø-N.

	PHASE A		PHASE B		PHASE C	
BASE TAP	3Ω	1Ω	3Ω	1Ω	3Ω	1Ω
R	0.0	0.0	.040		.013	
X	0.0	0.0	.023		.013	
Z	0.0	0.0	.046		.018	

CALCULATION OF SETTINGS

The proper settings for the measuring functions in the SLYN51A relay will depend to some degree on the specific application. For this reason, it is recommended that the application information supplied with the description of the overall logic diagram of the total scheme be consulted for the proper considerations and settings. There are a number of adjustments available in this relay but only some of them are intended for field settings. These are itemized below.

The reach settings for L_2T, M_2B, and M_2T (when used) functions are all made by one common adjustment. This is done in two parts.

a) Selection of basic tap (T_B) on the back of the relay.

b) Selection of percent tap (T) on the front of the relay.

With this common setting, the relative reaches of all these functions are fixed at the factory for the specific application of long line (100-200) miles or for a short line (100 miles or less) as the case may be. If for any reason the intended application changes it is suggested that the local General Electric Company Sales Office be consulted for any required information.

The negative sequence polarizing voltages for the negative sequence directional units are compensated. The amount of compensation must be set in the field depending on system line conditions. This setting is accomplished by two potentiometers. One potentiometer affects both D_2F and D_2R during the negative half cycle of current. The second potentiometer also affects both D_2F and D_2R but during the positive half cycle of current. In addition to these two potentiometers, there is one link that is associated with both D_2F and D_2R. This link should always be in the "B" position.

Please refer to the INSTALLATION TESTS section of this instruction book for information on how to make the desired settings on this relay.

RECEIVING, HANDLING AND STORAGE

These relays will normally be supplied as a part of a static relay equipment, mounted in a rack or cabinet with other static relays and test equipment. Immediately upon receipt of a static relay equipment, it should be unpacked and examined for any damage sustained in transit. If injury or damage resulting from rough handling is evident, file a damage claim at once with the transportation company and promptly notify the nearest General Electric Sales Office.

Reasonable care should be exercised in unpacking the equipment. If the equipment is not to be installed immediately, it should be stored indoors in a location that is free from moisture, dust, and metalli chips, and severe atmospheric contaminants.

Just prior to final installation the shipping support bolt should be removed from each side of all relay units, to facilitate possible future unit removal for maintenance. These shipping support bolts are approximately 8 inches back from the relay unit front panel. Static relay equipment, when supplied in swing rack cabinets, should be securely anchored to the floor or to the shipping pallet to prevent the equipment from tripping over when the swing rack is opened.

INSTALLATION TESTS

CAUTION

THE LOGIC SYSTEM SIDE OF THE DC POWER SUPPLY USED WITH MOD III STATIC RELAY EQUIPMENT IS ISOLATED FROM GROUND. IT IS A DESIGN CHARACTERISTIC OF MOST ELECTRONIC INSTRUMENTS THAT ONE OF THE SIGNAL INPUT TERMINALS IS CONNECTED TO INSTRUMENT CHASSIS. IF THE INSTRUMENT USED TO TEST THE RELAY EQUIPMENT IS ISOLATED FROM GROUND, ITS CHASSIS MAY HAVE AN ELECTRICAL POTENTIAL WITH RESPECT TO GROUND. THE USE OF A TEST INSTRUMENT WITH A GROUNDED CHASSIS WILL NOT AFFECT THE TESTING OF THE EQUIPMENT. A SECOND GROUND CONNECTION TO THE EQUIPMENT, SUCH AS A TEST LEAD INADVERTANTLY DROPPING AGAINST THE RELAY CASE, MAY CAUSE DAMAGE TO THE LOGIC CIRCUITRY. NO EXTERNAL TEST EQUIPMENT SHOULD BE LEFT CONNECTED TO THE STATIC RELAYS WHEN THEY ARE IN PROTECTIVE SERVICE, SINCE TEST EQUIPMENT GROUNDING REDUCES THE EFFECTIVENESS OF THE ISOLATION PROVIDED.

The Type SLYN51A relay is usually supplied from the factory mounted and wired in a static relay equipment. The following checks and adjustments should be made by the user in accordance with the procedures given under DETAILED TESTING INSTRUCTIONS before the relays are put into service:

1. Negative sequence voltage network balance check*
2. Negative sequence current network balance check*
3. V_2 magnitude setting*
4. Relay angle of maximum reach setting
5. I_2Z magnitude setting*
6. Voltage restraint tap setting
7. Basic minimum ohmic tap setting
8. Function timer setting*
9. Amplitude comparator card checks*
10. D_2F and D_2R K factor setting

* Factory Settings

Construction

The SLYN51A relay is packaged in an enclosed metal case with hinged front cover and removable top cover. The case is suitable for mounting on a standard 19 inch rack. The outline and mounting dimensions of the case and the physical location of the components are shown in Figures 1 and 2 respectively.

The tap blocks for making the voltage restraint settings are located on the front panel of the unit. The method of making restraint tap settings is illustrated in Figure 6. The connections are made by means of taper pin connectors; special tools are supplied with each equipment for the removal and insertion of these pin connectors.

The current and potential enter the SLYN51A on twelve point terminal strips location on the rear of the relay case. The potential connections are made on the YG terminal strip, the current connections on the YH terminal strip.

The basic minimum ohmic tap (T_B) setting is accomplished on the YH terminal strip on the rear panel of the unit. The current connections for the 1Ω and 3Ω taps are shown in Table I.

TABLE I

	I_B		I_C		$3I_o$	
	IN	OUT	IN	OUT	IN	OUT
1Ω BASE REACH	YH1	YH2	YH4	YH6	YH9	YH10
3Ω BASE REACH	YH1	YH3	YH5	YH7	YH8	YH10

The V_2 and I_2Z test jacks, the I_2Z magnitude pot (P5) and the relay angle of maximum reach pot (P6) are located on the front of the unit below the voltage restraint taps. The negative sequence filter potentiometers (P1, P2, P3, P4) are located inside the relay case as shown in Figure 2. The V_2 magnitude potentiometer (P7) is located on the rear of the unit.

The SLYN51A relay also contains printed circuit cards identified by a code number such as F110, L111, N102, T101, where F designates filter or comparator, L designates logic, T designates time delay, and N designates network. The printed circuit cards plug in from the front of the unit. The sockets are identified by letter designations or "addresses" (D, E, F, etc.) which appear on the guide strips in front of each socket, on the component location diagram, on the internal connections diagram and on the printed circuit card itself. The test points (TP1, TP2, etc.) shown on the internal connection diagram are connected to instrument jacks on a test card in position T with TP1 at the top of the card. The internal connections of the printed circuit cards are shown in the Printed Circuit Card Instruction Book GEK-34158.

Pin number 1 on the test card in position T is connected to relay reference, pin number 2 to -15 VDC, and pin number 10 to +15 VDC. Output signals are measured with respect to the reference bus on the test card (TP1). Logic signals are approximately +15 VDC for the ON or LOGIC ONE condition, and less than 1 VDC for the OFF or LOGIC ZERO condition. Filter card outputs are either +15 VDC or -15 VDC for the ON condition.

These outputs can be monitored with an oscilloscope, a portable high impedance DC voltmeter, or the test panel voltmeter if available. When the test panel meter is supplied, it will normally be connected to the reference bus. Placing the relay test lead in the proper test point pin jack will connect the meter for testing. When time delay cards are to be adjusted or checked, an oscilloscope which can display two traces simultaneously and which has a calibrated horizontal sweep should be used.

Detailed Testing Instructions

Before proceeding with the following test program, be sure that the tripping circuits in the associated Type SLAT relay are open.

A. Negative Sequence Network Balance Checks

The voltage and current sequence networks have been accurately preset at the factory to obtain positive sequence cancellation. No further adjustments should be required in the field. It is recommended, however, that the networks be checked at the time of installation to insure that nothing has occurred during shipment to unbalance the networks.

Negative Sequence Voltage Network

To check the null of the sequence voltage network, use the test circuit of Figure 7 and the connections of Table II. The three phase-phase voltages should be exactly equal in magnitude and 120° apart. For best resolution, use a voltage near the rated value. If the source voltages are not balanced (within a few percent) a single phase variac should be used to correct the unbalanced phase.

TABLE II

TEST FIGURE POINT	A	B	C
SLYN51A TERMINAL	YG2	YG4	YG3

The voltage at the V_2 test jack should consist solely of harmonics with no fundamental present. The peak to peak value of the network output will depend on the system, but should be on the order of a few tenths of a volt.

If the network needs readjustment to eliminate the 60 Hz fundamental, set P1 and P2 at midrange. Alternately make small adjustments in P1 and P2 until the desired level is achieved.

Negative Sequence Current Network

Method I - Three Phase Test Source

To check the null of the sequence current network, use the test circuit of Figure 8 and the connection of Table III. The three currents should be exactly equal in magnitude and 120° apart. Rated current (5A) will provide best resolution. If the source voltages are not balanced (within a few percent) a single phase variac should be used to correct the unbalanced phase.

TABLE III

TEST FIGURE POINT	D	E	F	G
SLYN51A TERMINAL	YH7	YH5	YH3	YH1

Jumper H to I.

The voltage at the I_2Z test jack should consist solely of harmonics with no fundamental present. The peak to peak value of the network output will depend on the system, but should be on the order of a few tenths of a volt.

If the network needs readjustment to eliminate the 60 Hz fundamental, set P3 and P4 at midrange. Alternately make small adjustments to P3 and P4 until the desired level is achieved.

Method II - Single Phase Test Source

The basic circuit used in checking the network is shown in Figure 9. This arrangement provides the means of obtaining two test currents of equal magnitude but separate by 60°. Then by appropriate connections to the network it is possible to simulate a balanced positive sequence current (Table IV). During the following tests the basic current level in each branch will be 5 amps, and since these currents will add at a 60° angle, the total load in the variac will be about 8.7 amps. It is desirable that the 110 volt scale of the phase angle meter be used to minimize the effect of this potential circuit on the relation between the two test currents. It is further desirable that the variac be set near its maximum voltage output and that the load boxes be set to obtain approximately 5 amps as a preliminary step, since this will provide the greatest possible voltage to the phase angle meter and will insure the best possible accuracy.

The negative sequence current is simulated by setting branch "A" current to lag an equal current in branch "B" by 60° and by reversing the branch "B" current at the relay. Branch "A" current now leads the reversed branch "B" current by 120°.

The following procedure is suggested.

1. Make connections per Figure 9 and Table IV.
2. Adjust the branch "B" load box to obtain approximately 5 amps when the variac is set for 110 volts.
3. Adjust the branch "A" load box until the phase angle meter indicates a 60° lag of current with respect to voltage.
4. Readjust the branch "B" load box until branch "A" and "B" currents are equal.
5. Adjust the variac until both currents are 5 amps.
6. Touch up branch "A" load box for angle trimming and branch "B" load box for magnitude trimming.

TABLE IV

TEST FIGURE POINT	A	B	C
SLYN51A TERMINAL	YH1	YH7	YH3, YH5

The voltage at the I_2Z jack may be a distorted wave at system frequency. With perfectly balanced currents and a network which has been perfectly adjusted, the waveform observed at the I_2Z jack should consist solely of harminics (primarily third and fifth).

Since perfection is seldom realized, the branch "A" and branch "B" load boxes should now be touched up until the waveform contains no fundamental component, and then the variac readjusted until the branch "B" current is again 5 amps. Branch "A" current should be 5 amps ± 0.5 amps, and the angle between the "A" and "B" currents should be 60° ± 3°. The peak-to-peak value of the network output, which now will consist solely of harmonics, will depend on the system, but should be on the order of a few tenths of a volt.

If the network needs readjustment to eliminate the 60 Hz fundamental, follow steps 1 through 6 above. Set P3 and P4 at mid-range. Alternately make small adjustments to P3 and P4 until the desired level is achieved.

B. V_2 Magnitude Adjustment

The magnitude of the V_2 test jack voltage must be set equal to the magnitude of the V_1 test jack voltage in the associated SLYP relay with the same level of voltage applied.

Apply balanced positive sequence voltage (near rated) to the associated SLYP relay. Measure the voltage at the V_1 test jack (RMS).

Apply balanced negative sequence voltage of the same magnitude to the SLYN51A using the test circuit of Figure 7 and the connections of Table V.

TABLE V

TEST FIGURE POINT	A	B	C
SLYN51A TERMINAL	YG2	YG3	YG4

Adjust the P7 potentiometer (on rear of unit) until the voltage measured at the V_2 test jack (RMS) is equal to that measured at the V_1 test jack.

C. I_2Z Magnitude Adjustment And Relay Angle Of Maximum Reach Adjustment

Since there is some interdependence between these two adjustments, if either one is changed the other should be checked.

Method I - Three Phase Test Current Source

Use the test circuit of Figure 10 and the connections of Table VI. Set the voltage restraint taps at 100%.

TABLE VI

TEST FIGURE POINT	A	B	C	D	E	F	G
SLYN51A TERMINAL	YG2	YG3	YG4	YH1	YH3	YH5	YH7

Jumper H to K and J to I.

It is the nature of this test circuit that the relay angle of maximum reach lags the measured or apparent, line angle by 30°. Thus, if an angle of maximum reach of 85° is desired, the apparent angle (measured on the phase angle meter) will be 115°.

The test procedure is outlined below:

1. Set $V_{\phi-\phi}$ equal to 26 VRMS and the current equal to 5 amperes (each phase). For testing at restraint taps other then 100%, the phase to phase voltage should equal:

$$V_{\phi-\phi} = \frac{26 \text{ VRMS}}{\% \text{ RESTRAINT}} \times 100$$

2. Adjust phase shifter to obtain the apparent line angle on the phase angle meter (30° leading the desired angle of maximum reach).

3. Adjust P6 until the voltage at the I_2Z test jack is exactly 180° out of phase with the voltage at the V_2 test jack.

4. Adjust P5 until the voltage (RMS) at the I_2Z test jack exactly equals that at the V_2 test jack.

5. Repeat steps 3 and 4 if necessary.

Method II - Single Phase Test Current Source

Use the test circuit of Figure 11 and the connections of Table VII. This table gives a BC current connection, and a balanced negative sequence voltage connection. Set voltage restraint taps at 100%.

TABLE VII

TEST FIGURE POINT	A	B	C	D	E	F	G
SLYN51A TERMINAL	YG2	YG3	YG4	YH1	YH3	YH7	YH5

It is the nature of this test circuit that the relay angle of maximum reach leads the measured or apparent, line angle by 60°. Thus, if an angle of maximum reach of 85° is desired, the apparent angle will be 25°.

The test procedure is outlined below.

1. Set $V_{\phi-\phi}$ equal to 15 VRMS ($26/\sqrt{3}$), and the current equal to 5 amperes.

2. Adjust the phase shifter to obtain the apparent line angle on the phase angle meter (the relay angle of maximum reach leads the apparent angle by 60°).

3. Adjust P6 until the voltage at the I_2Z test jack is exactly 180° out of phase with the voltage at the V_2 test jack.

4. Adjust P5 until the voltage (RMS) at the I_2Z test jack exactly equals that at the V_2 test jack.

5. Repeat steps 3 and 4 if necessary.

3Io Circuit Check

Apply 5 amperes to the relay per the test circuit of Figure 12 and the connections of Table VIII. Check that the voltage (RMS) at the I_2Z test jack is one third of that obtained by Method I or $1/\sqrt{3}$ times that obtained by Method II.

TABLE VIII

TEST FIGURE POINT	A	B
SLYN51A TERMINAL	YH8	YH10

D. Voltage Restraint Tap Setting

The arrangement of the voltage restraint tap blocks is described under CONSTRUCTION, and the choice of tap settings is discussed in the section on CALCULATION OF SETTINGS. The pickup voltage at the relay angle of maximum reach is given by the relationship:

$$V_2 = \frac{I_2 \times T_B \times 100}{T}$$

where: T = Voltage restraint tap setting in percent
T_B = Basic minimum ohmic tap setting
I_2 = Negative sequence test current

E. Basic Minimum Ohmic Tap Setting

The arrangement of the basic ohmic taps is described under CONSTRUCTION, and the choice of tap settings is discussed in the section on CALCULATION OF SETTINGS. The reach at the relay angle of maximum reach is given by the relationship:

$$Z_{MAX} = \frac{T_B \times 100}{T}$$

where: T = Voltage restraint tap setting in percent
T_B = Basic minimum ohmic tap setting

F. Timer Card Adjustments And Tests

The settings for the SLYN51A functions are discussed in the section on CALCULATION OF SETTINGS.

In order to test the timer cards it is necessary to remove the card which supplies the timer input and to place the timer card under test in a card adapter. The timer test circuit is shown in Figure 13. Opening the N.C. contact causes the output to step up to +15 VDC after the pickup delay of the timer. To increase the pickup time, turn the upper potentiometer (on the T101 and T107 cards adjust P2) on the timer card clockwise. Closing the contact causes the timer output to drop out after the reset delay setting of the card. To increase the reset time, turn the lower potentiometer (on the T101 and T107 cards adjust P3) on the card clockwise.

The shorter of the two pickup times of the T107 card can be observed at pin 7 of the card. The longer of the two pickup times is factory adjusted by P1 for a pickup time of 1.2 ms longer than the shorter time. This output must be observed at pin 8.

G. Amplitude Comparator Card Tests

In order to test the amplitude comparator functions in the SLYN51A, it is necessary to energize both the SLYN51A and the associated SLYP. The test connections are shown in Figure 14. The comparator card under test should be placed in a card adapter so that the card inputs may be observed. The outputs of the SLYN51A functions should be observed at the test point following the associated timer. The following procedure should be used for checking the balance point of the SLYN51A amplitude comparator functions:

1. Adjust the three phase variac of Figure 14 for approximately 120V phase to phase.

2. Adjust the 2-gang variac until the voltage (RMS) at the V_2 test jack is exactly twice the voltage (RMS) at the V_1 test jack. The voltmeter of Figure 14 should read approximately 40V in the counter clockwise direction from the zero position.

3. Jumper the I_1Z test jack to reference.

4. Adjust the phase shifter until the quantities at pin 3 and pin 4 of the card under test are 180° out of phase.

5. Increase the current until the associated timer output goes from a logic one to a logic zero. At this balance point the I_2Z test jack voltage will be equal to the value given by this expression:

$$I_2Z = \left[\frac{Z_2}{Z_1} - \frac{1}{2}\,\frac{Z_2}{Z_3}\right] V_2$$

where:

1/2 is the ratio $\frac{V_1}{V_2}$ set in step 2.

V_2 is the voltage at the V_2 test jack.

Z_1 is the magnitude of the series impedance in the V_2 circuit.

Z_2 is the magnitude of the series impedance in the I_2Z circuit.

Z_3 is the magnitude of the series impedance in the V_1 circuit.

The input current required is approximately 7 amperes for each volt of signal at the I_2Z test jack. The impedances, Z_1, Z_2, Z_3 are calculated from the impedance on the "N" network card plus the input resistor on the amplitude comparator card. If the input current required is high (above 10A), a lower value may be calculated by setting $V_1 = V_2$ in step 2, and modifying the equation above with a $\frac{V_1}{V_2}$ ratio of 1.

6. For the functions with a timer pickup setting of less than 4.16 ms., the operating point occurs for a higher value of I_2Z than calculated. This is to provide better transient response. For a pickup of 3.5 MS, the I_2Z voltage at the balance point should be approximately 15% higher than calculated.

7. Remove I_1Z jumper.

8. Jumper the I_2Z test jack to reference.

9. Adjust the phase shifter until the quantities at pin 6 and pin 7 of the card under test are in phase.

10. Increase the current until the associated timer output goes from a logic one to a logic zero. At this balance point the I_1Z test jack voltage will be equal to the value given by the expression:

$$I_1Z = \left[\frac{Z_4}{Z_1} - \frac{1}{2}\,\frac{Z_4}{Z_3}\right] V_2$$

where:

1/2 is the ratio $\frac{V_1}{V_2}$ set in step 2.

V_2 is the voltage at the V_2 test jack.

Z_1 is the magnitude of the series impedance in the V_2 circuit.

Z_3 is the magnitude of the series impedance in the V_1 circuit.

Z_4 is the magnitude of the series impedance in the I_1Z circuit.

As in step 5, the input current required is approximately 7 amperes for each volt of signal at the I_2Z test jack.

11. For the functions with a timer pickup setting of less than 4.16 ms, the operating point occurs for a higher value of I_2Z than calculated. This is to provide better transient response. For a pickup of 3.5 ms the I_2Z voltage at the balance point should be approximately 15% higher then calculated.

Sample Calculation

Table IX lists the N card components for an amplitude comparator function.

TABLE IX

CIRCUIT	N-CARD COMPONENTS
V_2	6.19K, .33 uf
I_2Z	2.1K
V_1	8.25K
I_1Z	4.64K

$Z_4 = 4.64K + 10K = 14.64$
(10K is the input impedance of the amplitude comparator card)
$Z_3 = 8.25K + 10K = 18.25K$
$Z_2 = 2.10K + 10K = 12.10K$
$Z_1 \angle \theta = 6.19K - j\, 1/[2\pi (60) (.33 \times 10^{-6})] + 10K = 18.25K \angle -29^{\circ}$
$Z_1 = 18.25K$

$$I_2Z = \left[\frac{Z_2}{Z_1} - \frac{1}{2} \quad \frac{Z_2}{Z_3} \right] V_2$$

$$= \left[\frac{12.1K}{18.25K} - \frac{1}{2} \quad \frac{12.1K}{18.25K} \right] V_2$$

$$I_2Z = .332\ V_2$$

$$I_1Z = \left[\frac{Z_4}{Z_1} - \frac{1}{2} \quad \frac{Z_4}{Z_3} \right] V_2$$

$$= \left[\frac{14.64K}{18.25K} - \frac{1}{2} \quad \frac{14.64K}{18.25K} \right] V_2$$

$$I_1Z = .40\ V_2$$

H. Negative Sequence Directional Units

Use the test circuit of Figure 11 and the connections of Table VII for the following tests.

1. Adjust the voltage and current to obtain 1.0 VRMS at the V_2 and I_2Z test jacks.
2. Adjust the phase shifter so that the test jack voltages are 180° out of phase.
3. Place the F109 card in position N in a card extender and make the following checks:

   a) The voltage at pin 3 should be .47 - .53 V_{RMS}
   b) The voltage at pin 4 should be .47 - .53 V_{RMS}
   c) Link in the "B" position - voltage at pin 4 leads pin 3 by 35° (1.45 - 1.60 ms)
      Link in the "A" position - voltage at pin 4 in phase with pin 3.

   NOTE: The link is located on the N103 card in card position F.

4. Adjust the phase shifter so that the voltages at pin 3 and pin 4 are in phase.
5. With the I_2Z test jack voltage set at 1.0 V_{RMS}, adjust the applied voltage until the V_2 test jack voltage (RMS) is equal to:

$$V_2 = \frac{k}{100} \quad V_{RMS}$$

where k is the desired offset in percent.

6. Observe the output at pin 6 on an oscilloscope. Adjust P1 for no output blocks. Observe the output at pin 9 and adjust P2 for no output.

7. Test per Table X.

TABLE X

TEST JACK PIN 3 AND PIN 4 VOLTAGES PHASE RELATIONSHIP			OUTPUT	
			TP7	TP9
V_2	I_2Z			
0	1.0	-----	+15V	0V
1.0	0	-----	0V	0V
1.0	1.0	IN PHASE	0V	+15V
1.0	1.0	180^o OUT OF PHASE	+15V	0V

PERIODIC CHECKS AND ROUTINE MAINTENANCE

Periodic Tests

All functions included in the SLYN51A relay may be checked at periodic intervals using the procedures described in INSTALLATION TESTS. Cable connections between the SLYN51A and the associated Type SLA relay may be checked by observing the test points in the SLA unit.

The following checks should be made during periodic testing:

1. Relay angle of maximum reach setting.

2. Amplitude comparator card checks.

3. D_2F and D_2R K factor setting.

NOTE: Errors in restraint tap setting, ohmic tap setting, timer settings, etc. will appear when the amplitude comparator cards are checked.

Trouble Shooting

In any trouble shooting of equipment, it should first be established which unit is functioning incorrectly. The overall logic diagram supplied with the equipment shows the combined logic of the complete equipment and the various test points in each unit. By signal tracing, using the overall logic diagram and the various test points, it should be possible to quickly isolate the trouble.

A test adapter card is supplied with each static relay equipment to supplement the prewired test points on the test cards. Use of the adapter card is described in the card instruction book GEK-34158.

A dual-trace oscilloscope is a valuable aid to detailed trouble shooting, since it can be used to determine phase shift, operate and reset times as well as input and output levels. A portable dual-trace oscilloscope with a calibrated sweep and trigger facility is recommended.

Spare Parts

To minimize possible outage time, it is recommended that a complete maintenance program should include the stocking of at least one spare card of each type. It is possible to replace damage or defective components on the printed circuit cards, but great care should be taken in soldering so as not to damage or bridge-over the printed circuit busses, or overheat the semi-conductor components. The repaired area should be recovered with a suitable high-dielectric plastic coating to prevent possible breakdowns across the printed buses due to moisture and dust. The wiring diagrams for the cards in the SLYN51A relay are included in the card book GEK-34158; the card types are shown on the component location diagram (Figure 2).

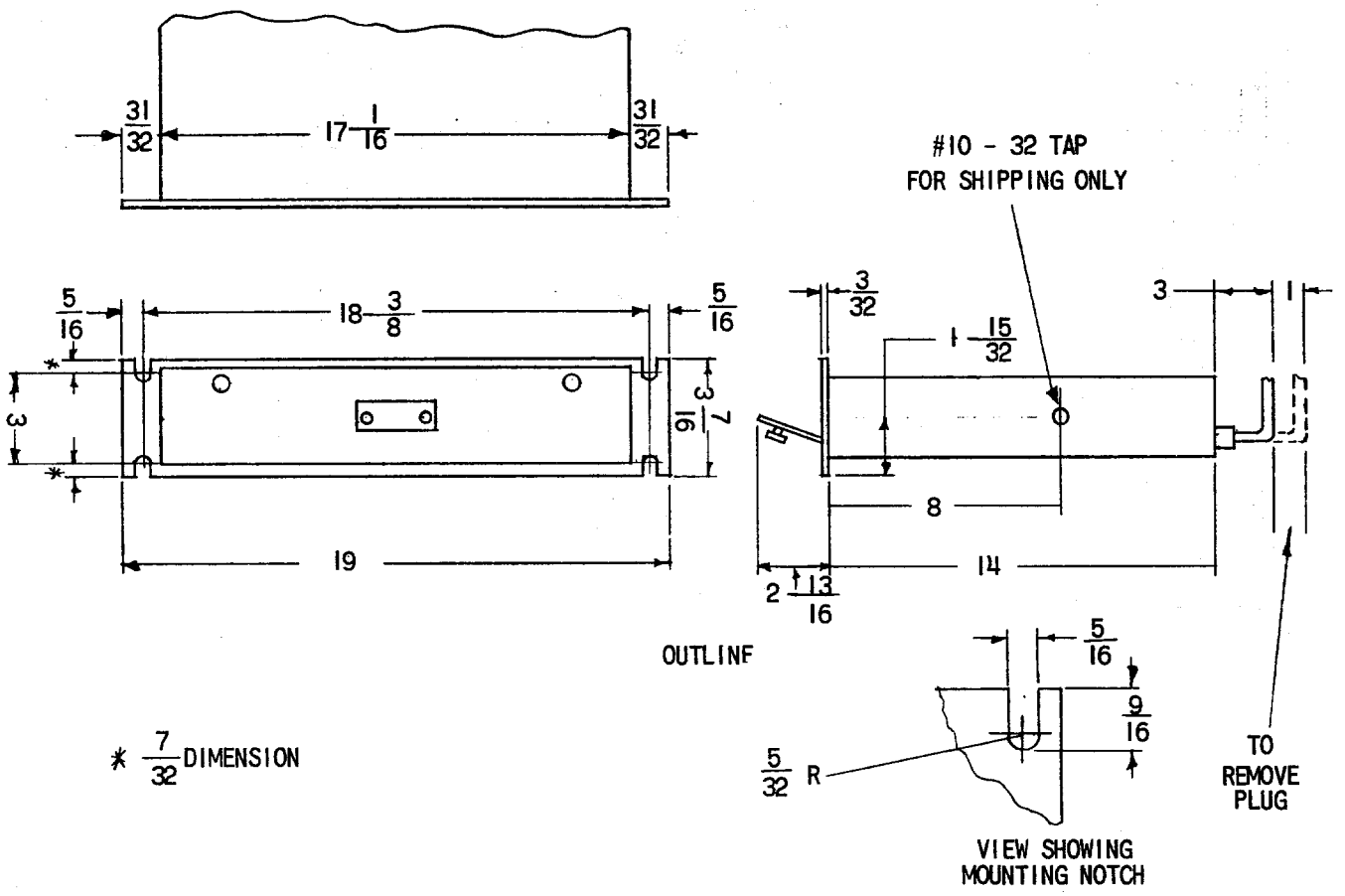
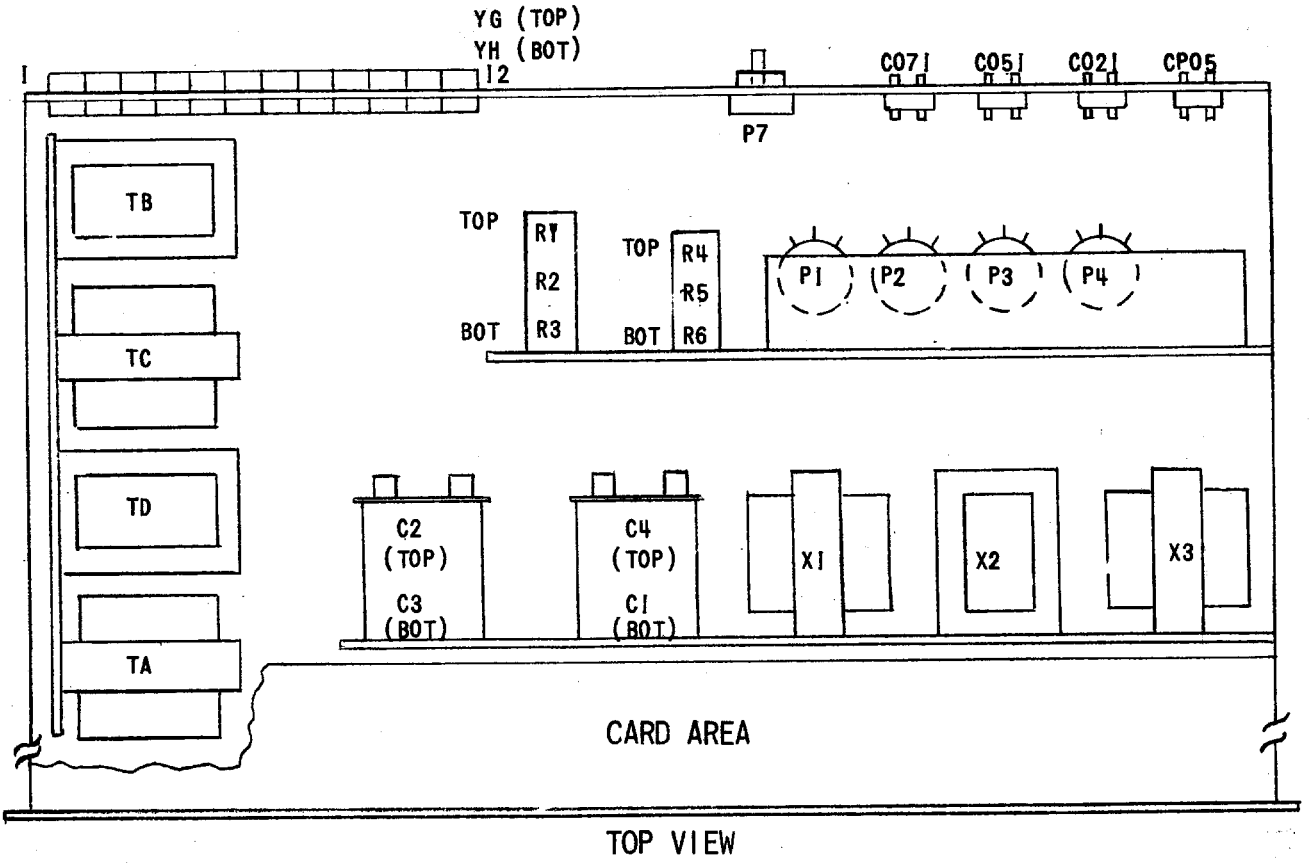


FIG. 1 (0227A2036-0) Outline And Mounting Dimensions For The Type SLYN51A Relay



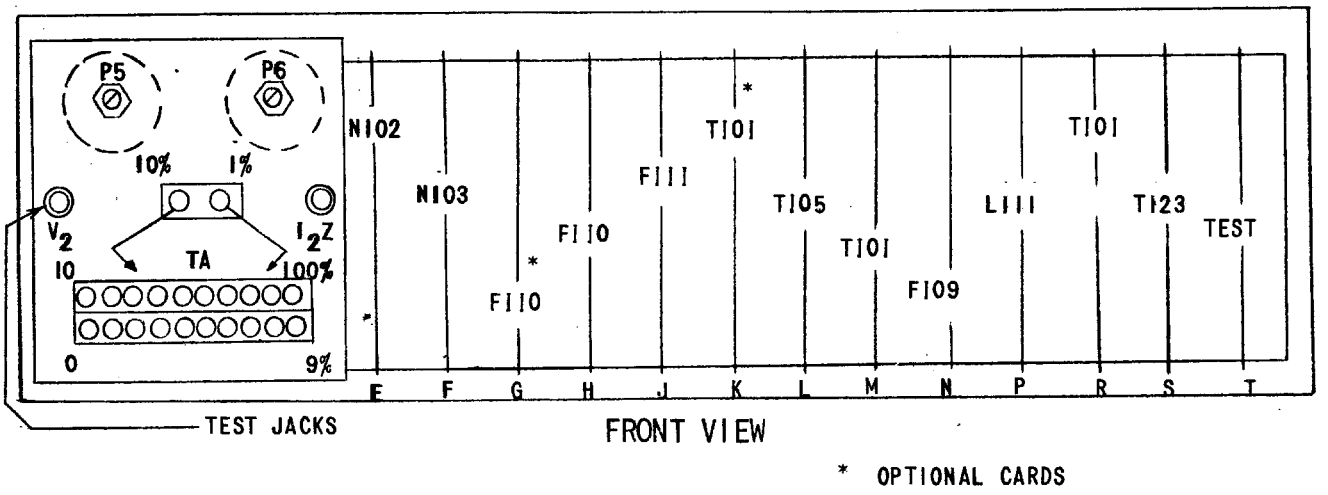


FIG. 2 (0246A2495-2) Component Location Diagram For The Type SLYN51A Relay

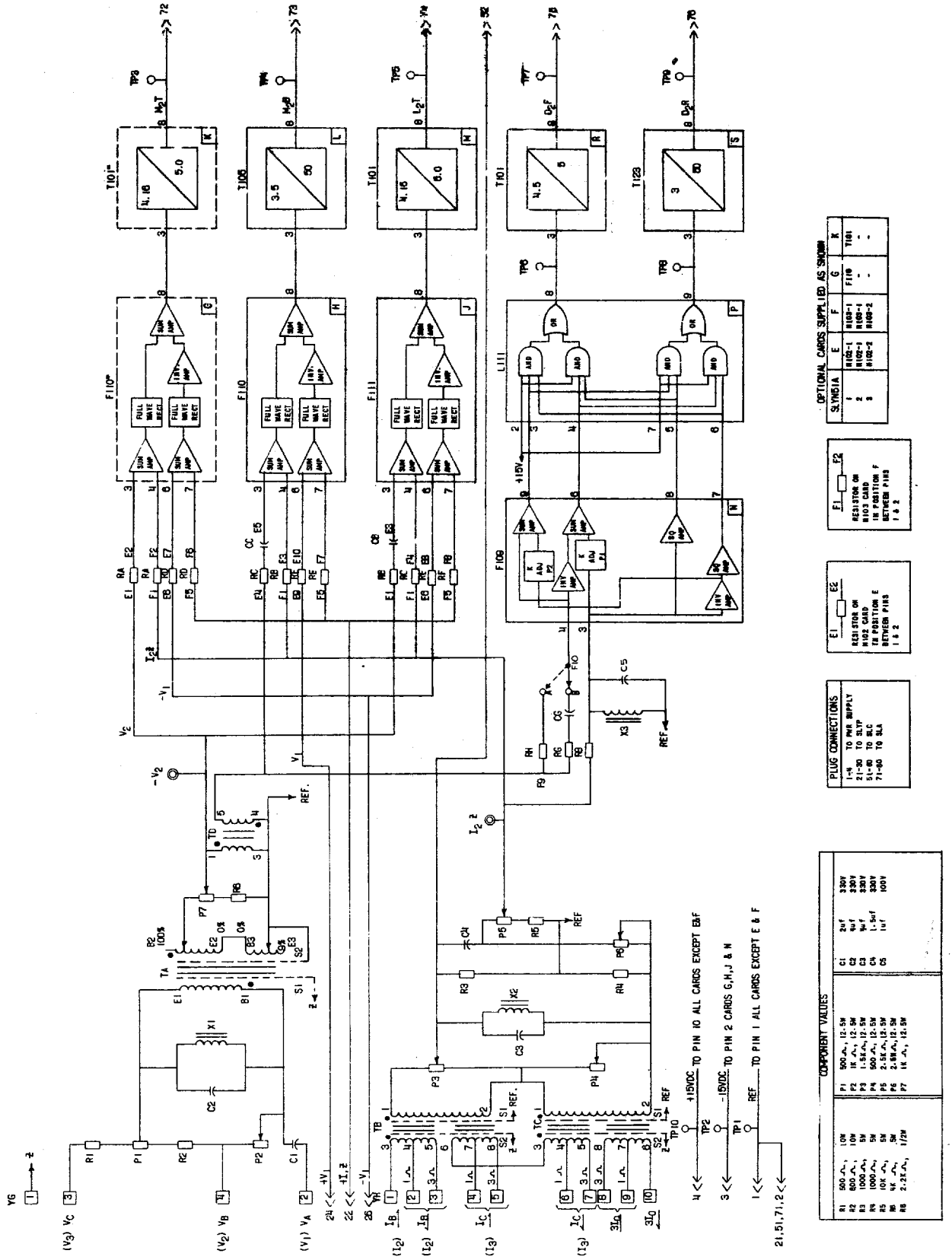


FIG. 3 (0149C7229-10) Internal Connections For The Type SLYN51A Relay

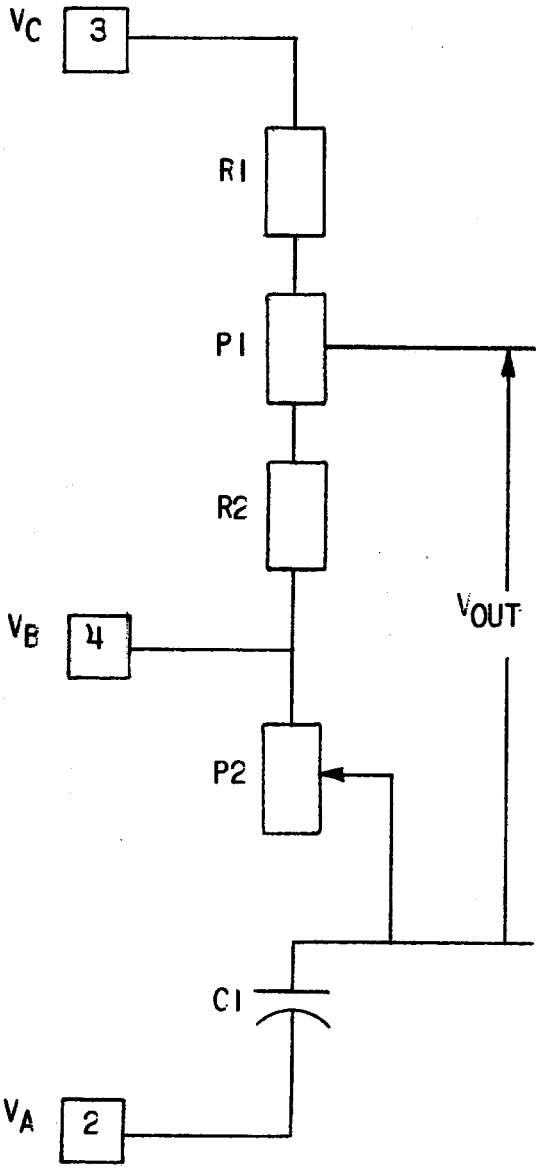


FIG. 4 (0227A2176-0) SLYN Negative Sequence Voltage Network

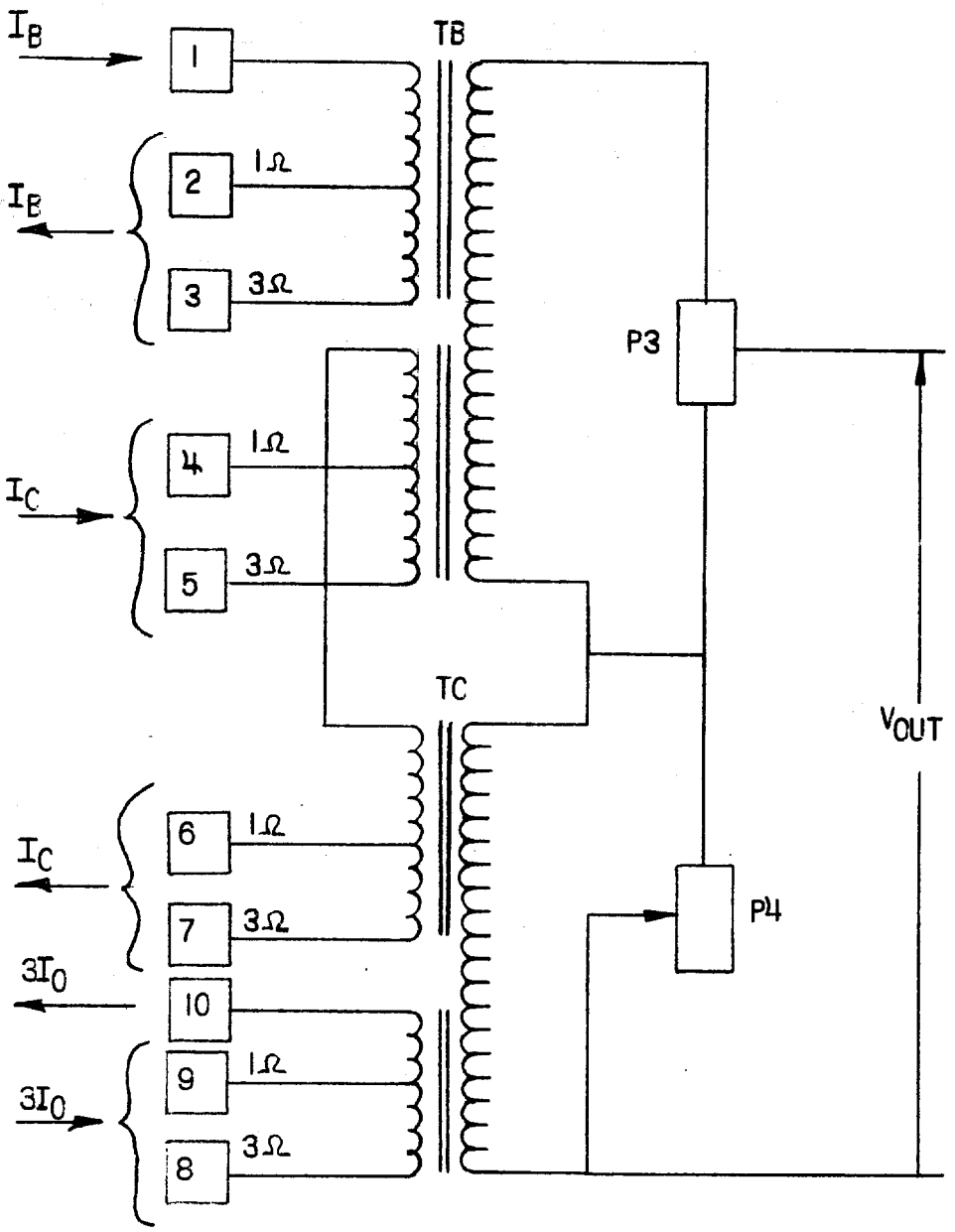
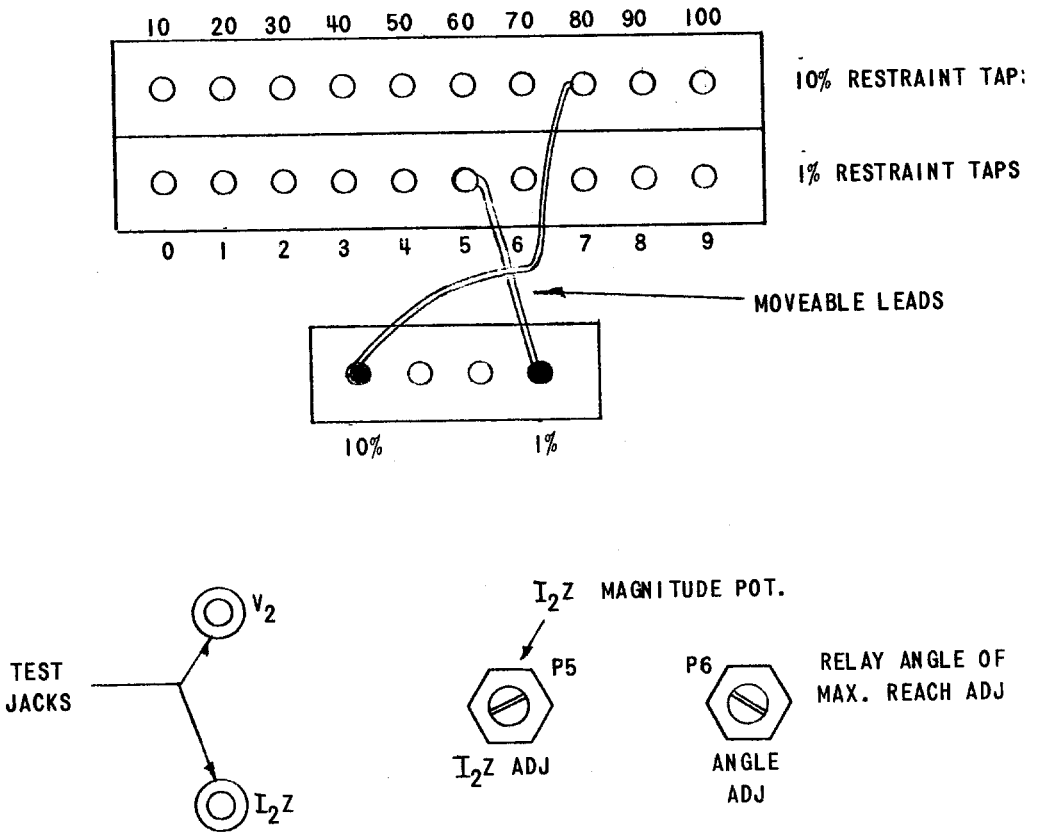


FIG. 5 (0227A2179-0) SLYN Negative Sequence Current Network



● FIXED TAP

○ ADJUSTABLE TAP

85% VOLTAGE RESTRAINT TAP ILLUSTRATED

REACH = 1.18 T_B

T_B = BASIC MINIMUM OHMIC TAP SETTING

FIG. 6 (0227A2178-1) Typical SLYN Voltage Restraint Tap Settings

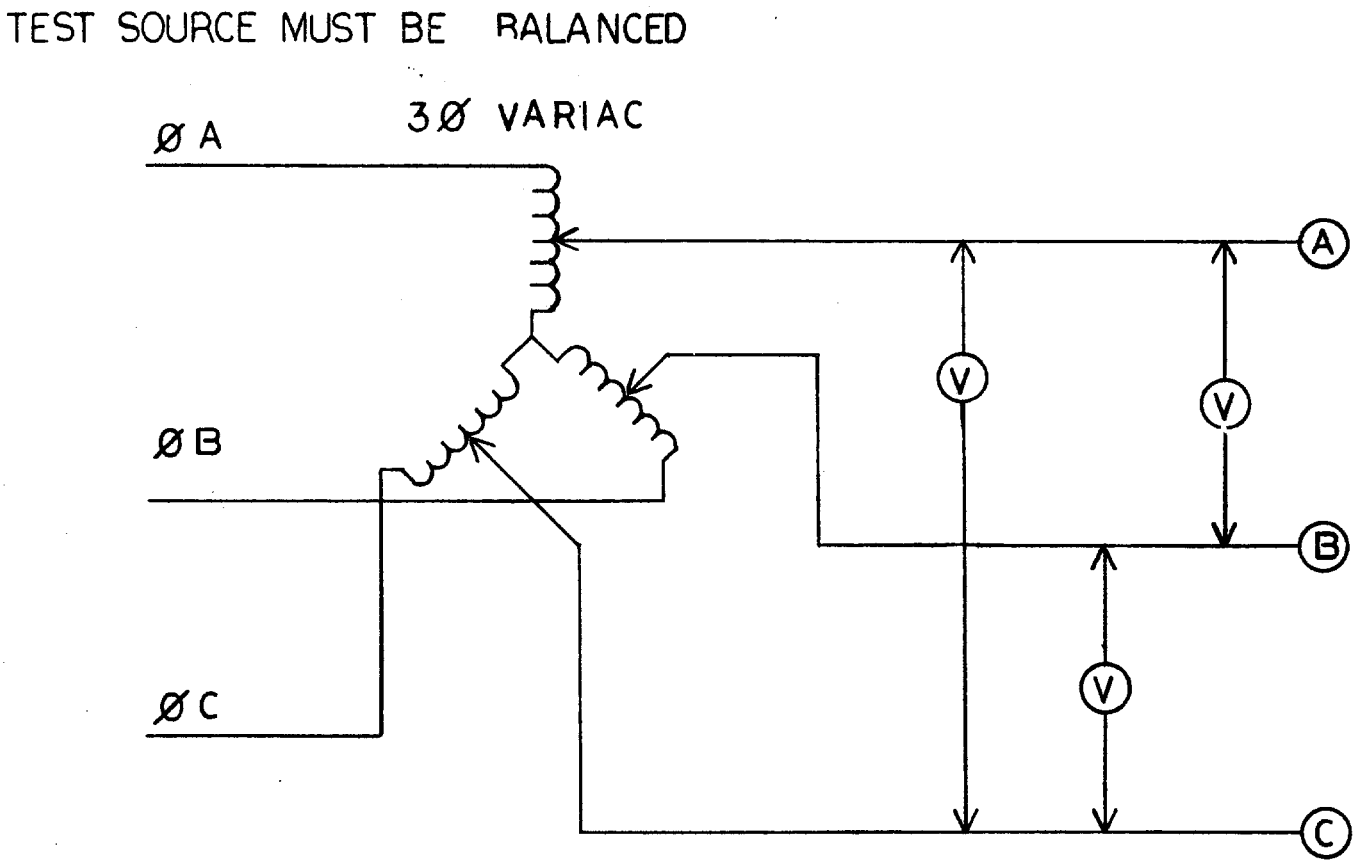


FIG. 7 (0246A6884-1) SLYN Voltage Network Test Connections

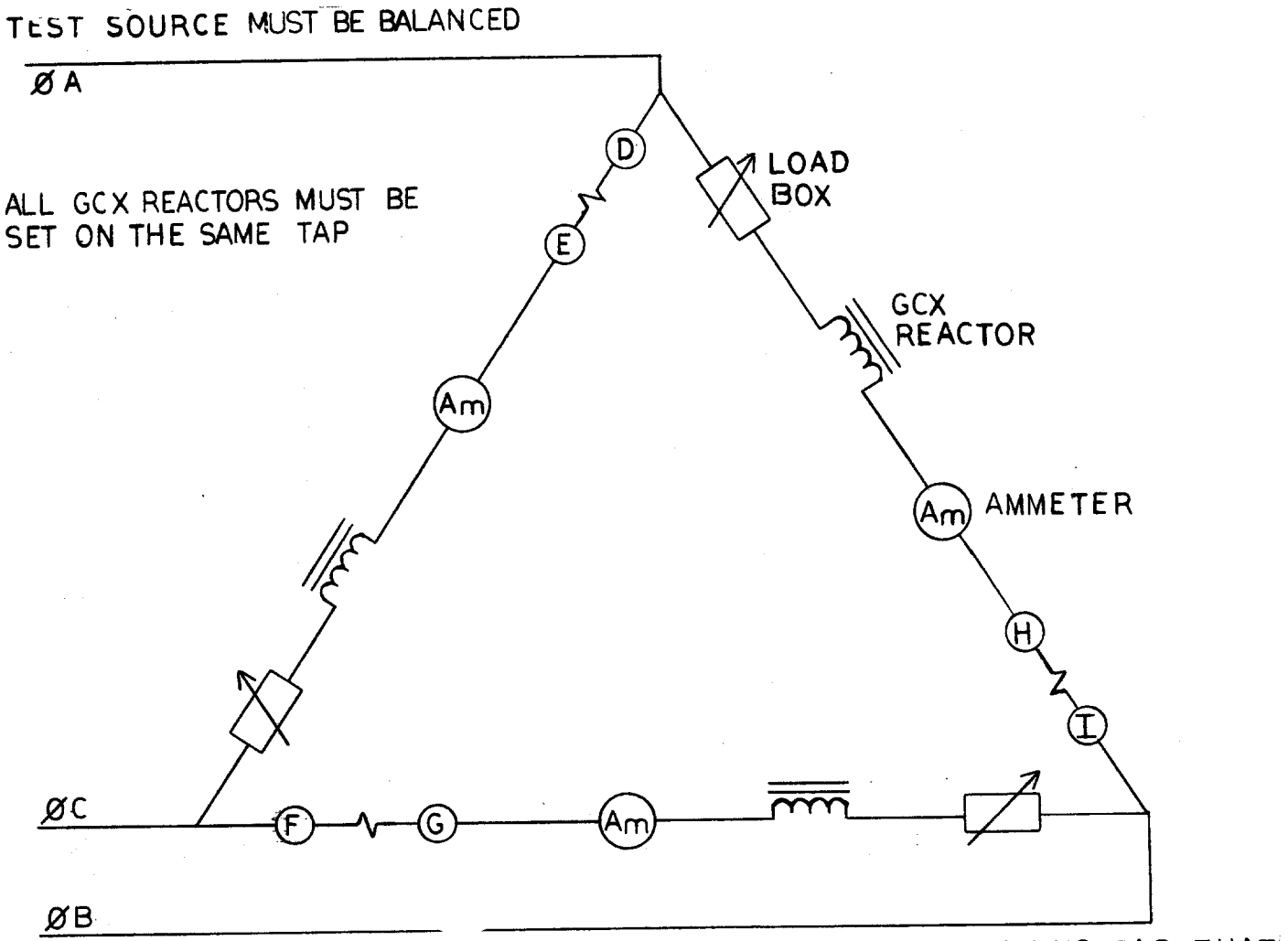


FIG. 8 (0246A6883-1) SLYN Current Network Test Connections-Method I

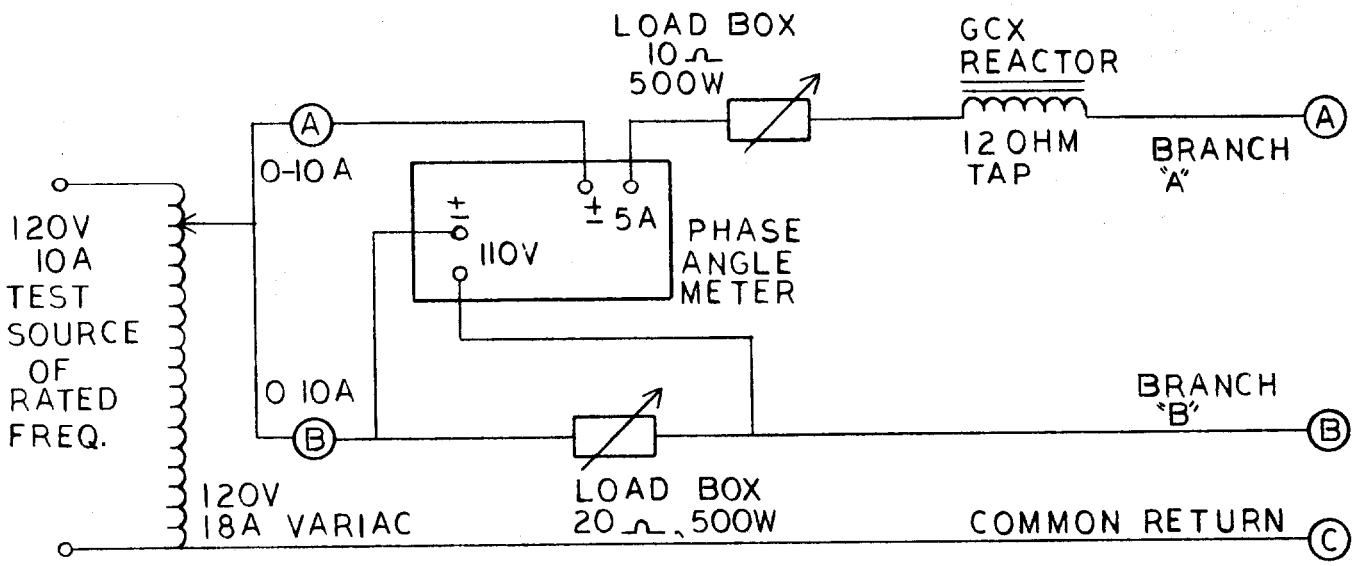


FIG. 9 (0246A6882- 1) SLYN Current Network Test Connections-Method II

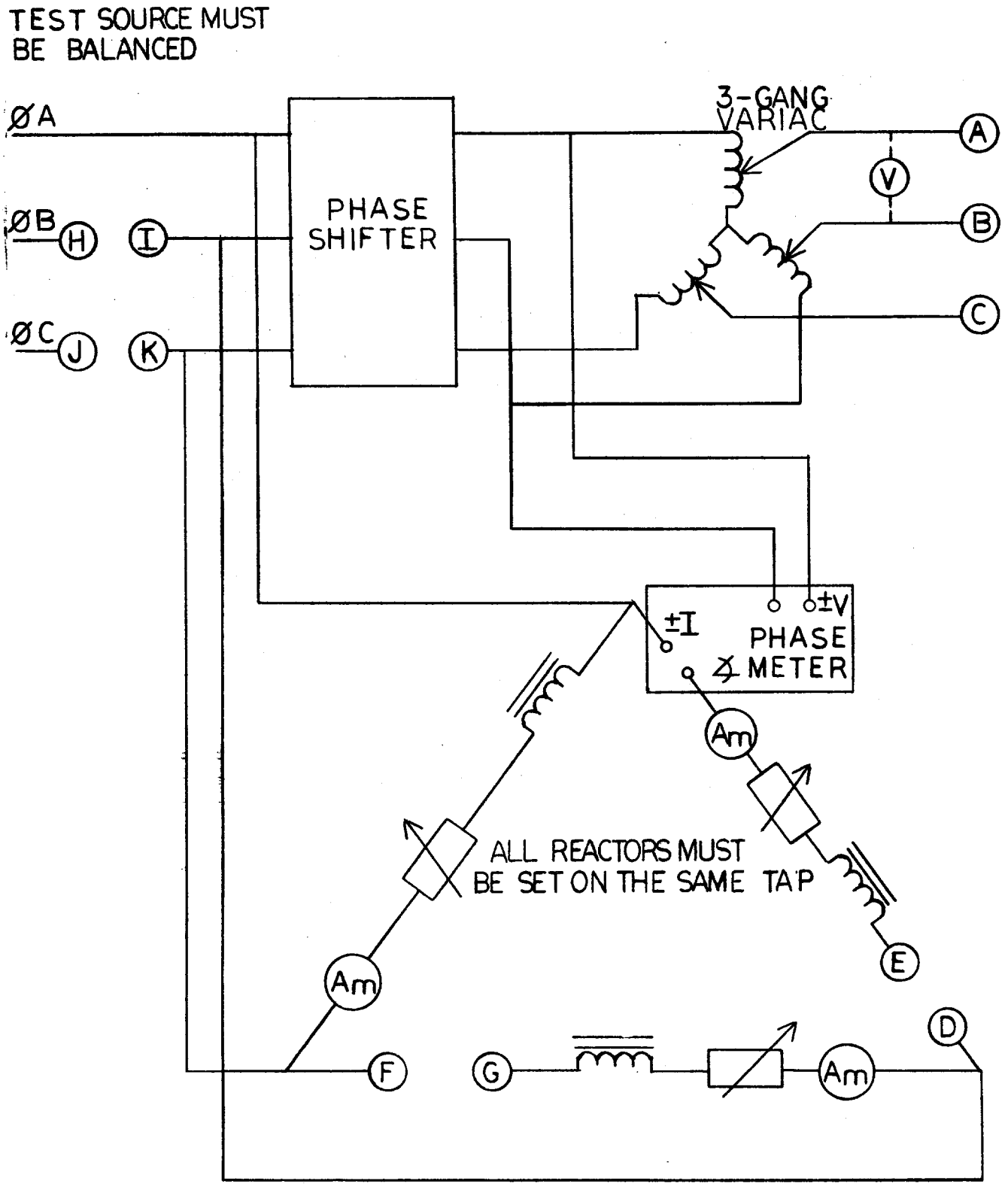


FIG. 10 (0246A6881-1) SLYN Unit Test Circuit-Method I

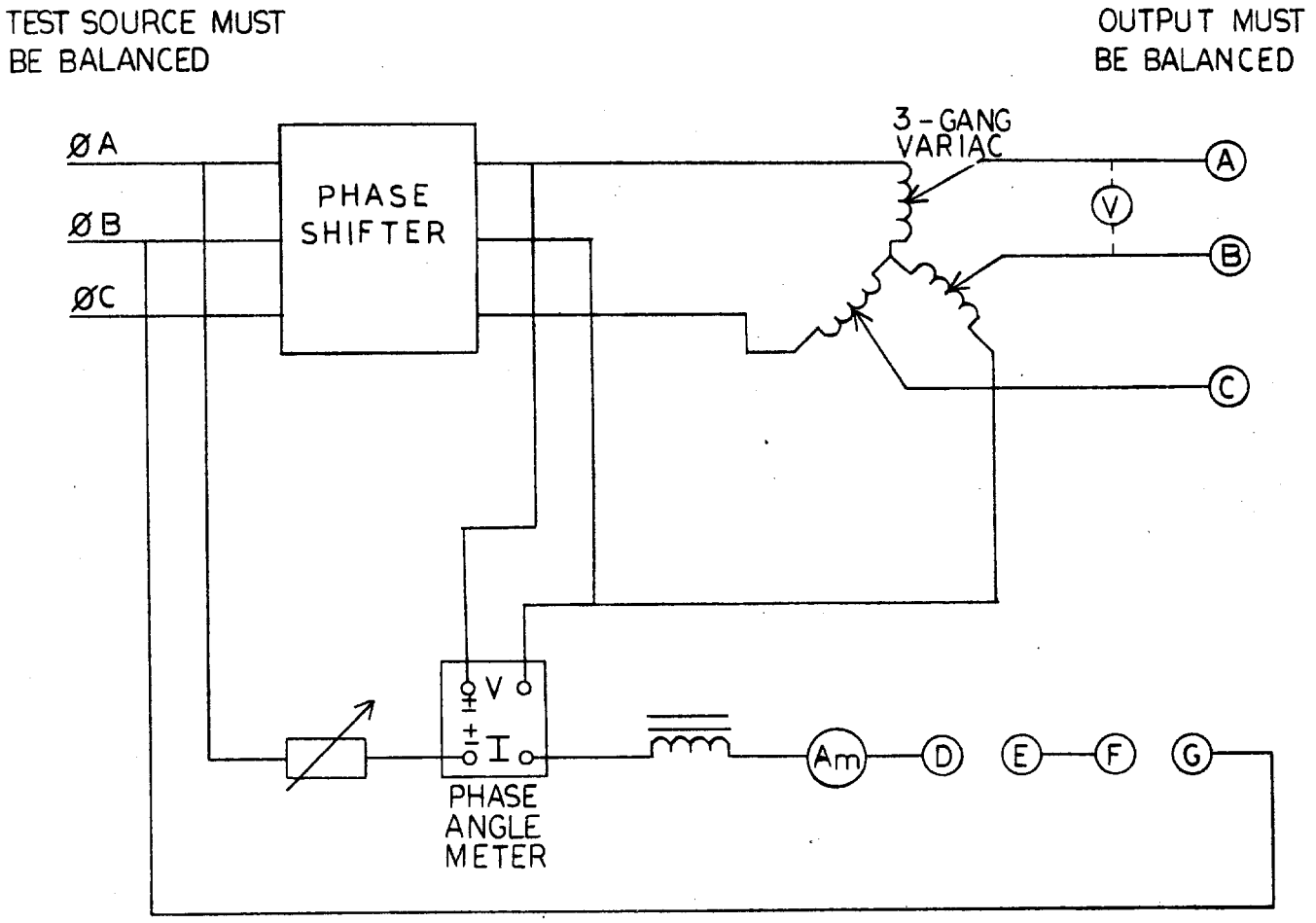


FIG. 11 (0246A6880-1) SLYN Unit Test Circuit-Method II

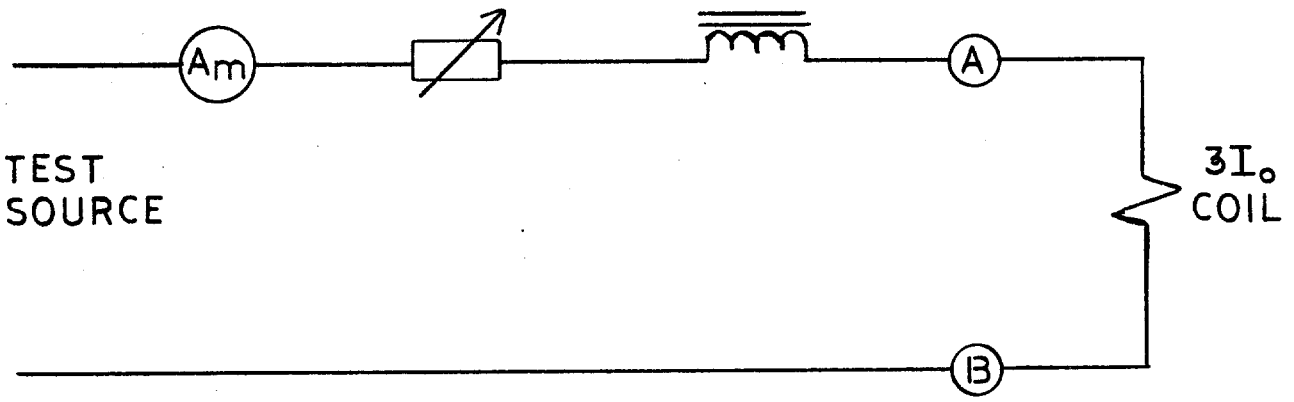
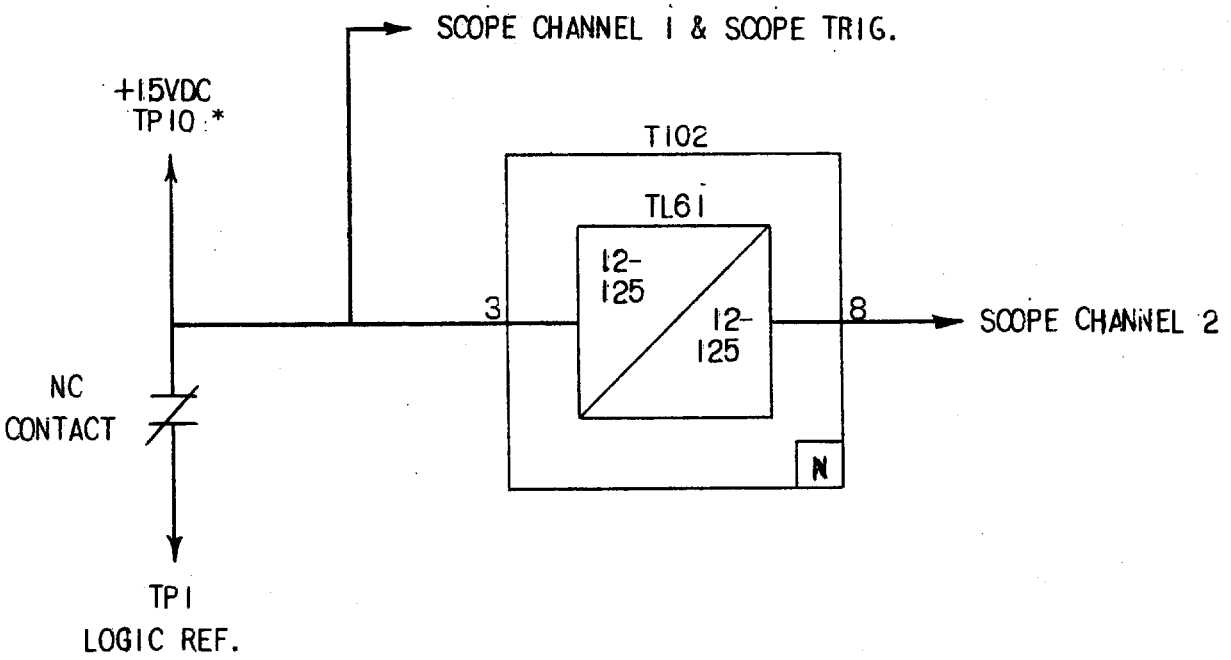


FIG. 12 (0246A6879-0) SLYN 3Io Test Circuit



* THE 15VDC SIGNAL AT PIN 10 HAS A CURRENT LIMITING RESISTOR MOUNTED ON THE TEST CARD.

FIG. 13 (0246A7987-0) Timer Test Circuit

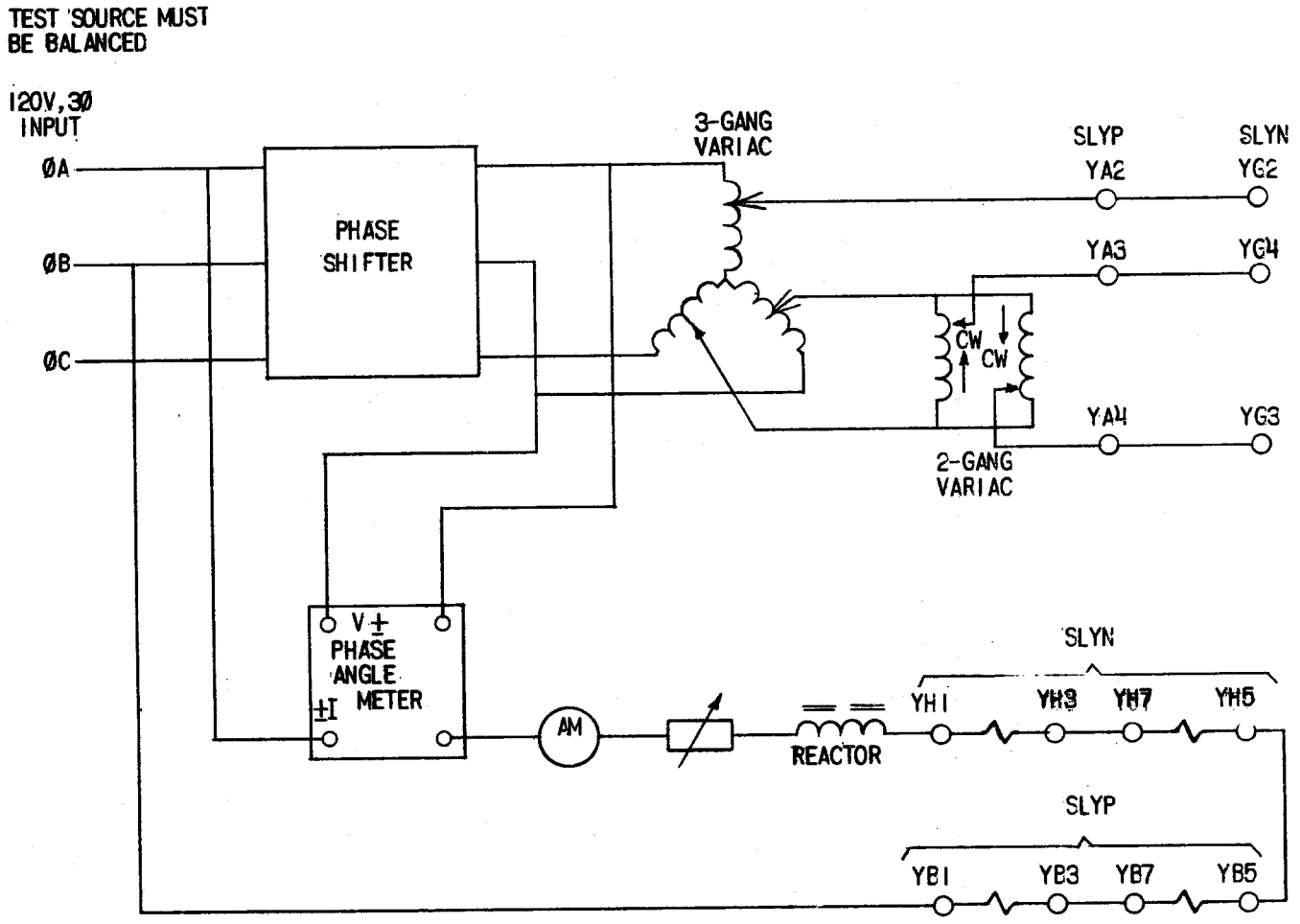


FIG. 14 (0227A2177-1) Amplitude Comparator Test Circuit

GENERAL ELECTRIC COMPANY
POWER SYSTEMS MANAGEMENT BUSINESS DEPT

GENERAL ELECTRIC