INSTRUCTIONS

GEK-45340

STATIC NEGATIVE SEQUENCE DISTANCE RELAY

TYPE SLYN51B

POWER SYSTEMS MANAGEMENT DEPARTMENT

GENERAL ELECTRIC

PHILADELPHIA, PA.

CONTENTS

DESCRIPTION

The SLYN51B is a solid state negative sequence distance relay that is packaged in one 2 rack unit case the outline and mounting dimensions of which are illustrated in Figure 1.

This relay is not intended for use by itself. Rather it was designed to be employed in conjunction with other solid state measuring and logic relays to provide protection against all types of faults on series compensated lines and on uncompensated lines that are adjacent to series compensated lines. The total complement of functions that may be included in the SLYN51B are noted below:

M_2T - First zone negative sequence directional distance tripping function. (optional)

L_2T - Negative sequence directional distance pilot tripping function.

M_2B - Negative sequence directional distance blocking function.

D_2T - Negative sequence directional function operates in the tripping direction.

D_2B - Negative sequence directional function operated in the blocking direction.

Other equipment in a typical terminal would include other fault detecting and measuring relays to respond to balanced three phase faults, a type SLA logic relay, a type SLAT output relay and a type SSA regulated DC power supply.

The overall logic diagram and the relay nameplate indicate which of the optional functions are included in a particular equipment. All SLYN51B relays include the wiring and sockets for all of the above functions. When any optional function is omitted in a particular SLYN51B this function may be added in the field by obtaining the necessary printed circuit cards and inserting them in the proper sockets. However, the addition of optional functions to an existing equipment does require that any associated logic in other relays in the equipment also be present or added at that time.

The internal connections for the SLYN51B is shown in Figure 2, and the component location diagram is shown in Figure 3. Detailed information on the various printed circuit cards is included in GEK-34158.

APPLICATION

The SLYN51B is a negative sequence relay including both distance and directional functions that is intended to be an integral part of a pilot relaying scheme for use in the protection of series compensated lines and lines adjacent to series compensated lines. It is suitable for use in schemes that employ carrier channels as well as microwave channels.

All of the functions in the SLYN51B with the exception of the M_2T are essential to the total scheme of protection. The M_2T is an optional first zone direct tripping function. When used it will provide first zone distance protection for all phase-to-phase and most double phase-to-ground faults on the protected line within its setting. However, it is only suitable for use on uncompensated lines. For information on the application of the M_2T function please refer to the Local Sales Office of the General Electric Company.

There are different types of SLYN51B relays depending on line length and potential device location. Line length may be "short" or "long", with long defined as a line greater than 100 miles in length. These differences as well as specific recommendation for both compensated and uncompensated lines are given in the applicable Logic Description for the particular equipment.

The L_2T and M_2B negative sequence distance function in a particular type of scheme are provided with fixed ratios of ohmic reach to assure optimum coordination. The overall reach of all of these functions may be lengthened or shortened by a common field adjustment which maintains these fixed reach ratios when the required setting is accomplished for a particular line length. This common setting is the negative sequence impedance represented by the ratio of the negative sequence voltage network output to the negative sequence current network output, and it is referred to as the "Relay System Reach".

The required Relay System Reach setting for a particular line is equal to the secondary negative sequence ohms of the line times a margin factor "R" which is related to line length. This "R" margin factor provides Relay System Reach settings that are longer than the line for short lines, and settings that approach the line length for long lines. The Relay System Reach setting is accomplished by the selection of a base reach tap in the SLYN51B negative sequence current network, and a voltage restraint tap in the negative sequence voltage network. Use the same margin factor used in the associated SLYP.

The following table gives typical reaches for the various functions in the SLYP51B. Unless otherwise stipulated, the relays will be shipped with a relay system reach angle of 85^{o} and function timers set as shown on the relay internal connections diagram, figure 2.

	LONG LINE, LINE SIDE PT	SHORT LINE LINE SIDE PT	LONG LINE BUS SIDE PT
FUNCTION	REACH IN % OF RELAY SYSTEM REACH		
M_2T OPERATE	20-90	20-90	20-90
M_2T RESTRAINT	20-90	20-90	20-90
M_2B OPERATE	150	300	150
M_2B RESTRAINT	100	100	100
L_2T OPERATE	150	150	150
L_2T RESTRAINT	125	125	125

The directional functions, D_2B and D_2T, have an adjustable offset of 20-100% of the system reach when supplied for the line side PT application and when supplied for bus side application the offset range is 5-50% of the system reach.

RANGES

The SLYN51B relay has an adjustable system reach of 1.30 ohms in the trip direction, with 1 ohm and 3 ohm base reach taps in the current circuits and 1% taps in the voltage circuits. With the exception of the M_2T function, the reach of each measuring function in the SLYN51B is fixed at a specific percentage of the Relay System Reach. For example, if the Relay System Reach has been set at 4.0 ohms, and the unit nameplate indicates that the M_2 reach is 125%, then the reach of the L_2T function at the relay system angle is 5.0 ohms. The M_2T function is adjustable over a range of 20-90% of the Relay System Reach.

The standard angle setting for the Relay System Reach is 85^{o}. This angle can be adjusted over the range of 60^{o} to 90^{o} for special applications.

The Type SLYN51B relay is designed for use in an environment where the air temperature outside the case is between $-20^{o}C$ and $+65^{o}C$.

The Type SLYN51B relay requires a ± 15 VDC power source which can be obtained from a Type SSA50 and up power supply.

The current circuits of the SLYN51B relay are rated at 5 amperes rated frequency, for continuous duty and have a one second rating of 300 amperes. The potential circuits are rated at 120V, rated frequency.

CHARACTERISTICS

OPERATING PRINCIPLES

The SLYN51B relay uses negative sequence voltage and current networks to obtain the V_2 and I_2Z signals which are used as the operating quantities for the various measuring functions. Some functions also require positive sequence operating quantities (V_1, I_1Z). The positive sequence quantities are supplied from a type SLYP relay. The operating theory of the relay networks which derive the negative sequence quantities is explained in the following paragraphs.

A. Negative Sequence Voltage Network

The negative sequence voltage network is shown in Figure 4. The network consists of a variable resistor and capacitor phase-shift circuit plus a resistor divider circuit. These circuits are adjusted to phase shift a voltage and adjust the voltage magnitude until the output is equal in phase angle and magnitude of V_{AN}, since $V_{AN} = V_2$ for a balanced negative sequence input.

The derivation of the output voltage is described below.

$$V_{OUT} = V_{C-B} \frac{kP1 + R2}{R1+R2+P1} + V_{B-A} \frac{m\ P2}{mP2 + 1/jwc}$$

where K and m are the fraction of P1 and P2 used.

By design,

$$\frac{k\ P1 + R2}{R1 + R2 + P1} = 1/2$$

$$\frac{m\ P2}{P2 + 1/jwc} = 1/2\ \underline{/60^o}$$

Therefore,

$$V_{OUT} = 1/2\ V_{C-B} + 1/2\ V_{B-A}\ \underline{/60^o}$$

$$V_A = V_{A0} + V_{A1} + V_{A2}$$

$$V_B = V_{A0} + a^2\ V_{A1} + a\ V_{A2}$$

$$V_C = V_{A0} + a\ V_{A1} + a^2\ V_{A2}$$

$$V_{OUT} = 1/2 \left[(V_{A0} + a\ V_{A1} + a^2\ V_{A2}) - (V_{A0} + a^2\ V_{A1} + a\ V_{A2}) \right] + 1/2\ \underline{/60^o} \left[(V_{A0} + a^2\ V_{A1} + a\ V_{A2}) - (V_{A0} + V_A + V_{A2}) \right]$$

$$= 1/2 \left[(a-a^2)\ V_{A1} + (a^2-a)\ V_{A2}\right] + 1/2\ \underline{/60^o} \left[(a^2-1)\ V_{A1} + (a-1)\ V_{A2}\right]$$

$$= .866 \left[V_{A1}\ \underline{/90^o} + V_{A2}\ \underline{/-90^o} + V_{A1}\ \underline{/-90^o} + V_{A2}\ \underline{/210^o} \right]$$

$$V_{OUT} = 1.5\ V_{A2}\ \underline{/240^o}$$

For a pre negative sequence input:

$$V_{OUT} = .866\ V_{B-A}\ \underline{/90^o}$$

B. Negative Sequence Current Network

The negative sequence current network used in the SLYN51B relay is shown in Figure 5. The network consists of two transactors (marked TB and TC in Figure 5), each with two primary windings plus an adjustable resistive load across the secondary of each transactor. The output is obtained by vectorially adding the secondary voltage of the two transactors when each adjustable resistor has been set to obtain a very specific phase angle between the two secondary windings.

The term "transactor" is a contraction of transformer - reactor. It is essentially an air-gap current transformer with secondary current (and therefore, secondary voltage across the loading resistor) proportional to the vector sum of the input currents. The performance of a transactor in a circuit is described by its transfer impedance and the associated angle.

$$Z_T = \frac{V_{OUT}}{I_{IN}}\ \underline{/\theta T}$$

Where: V_{OUT} = Secondary output voltage
I_{IN} = Vector sum of the input currents
θ_T = Angle by which V_{OUT} leads I_{IN}

The derivation of the negative sequence current network output voltage is given below.

By design:

$$Z_{TC} = .85 \sqrt{3}\ Z_{TB}$$

$$\theta_{TB} = 75^o$$

$$\theta_{TC} = 45^o$$

$$V_{OUT} = k \left[Z_{TB} (I_B - I_C) \underline{/75^o} \right] + Z_{TC} (I_C - 1/3\ I_N) \underline{/45^o}$$

where k is the percentage of P3 used

Let k = .85

$$V_{OUT} = .85\ Z_{TB} (I_B - I_C) \underline{/75^o} + .86 \sqrt{3}\ Z_{TB} (I_C - 1/3\ I_N) \underline{/45^o}$$

$$I_B = I_{A0} + a^2\ I_{A1} + a\ I_{A2}$$

$$I_C = I_{A0} + a\ I_{A1} + a^2\ I_{A2}$$

$$V_{OUT} = .85\ Z_{TB} \left[(I_{A0} + a^2\ I_{A1} + a\ I_{A2}) - (I_{A0} + a\ I_{A1} + a^2\ I_{A2}) \right] \underline{/75^o}$$

$$+ .85 \sqrt{3}\ Z_{TB} \left[I_{A0} + a\ I_{A1} + a^2\ I_{A2} - 1/3\ \ (3\ I_{A0}) \right] \underline{/45^o}$$

$$= .85\ Z_{TB} \left[(a^2 - a)\ I_{A1} + (a - a^2)\ I_{A2} \right] \underline{/75^o} + 85\ /\overline{3}\ Z_{TB} \left[a\ I_{A1} + a - I_{A2} \right] \underline{/45^o}$$

$$= .85 \sqrt{3}\ Z_{TB} (I_{A1} \underline{/-15^o} + I_{A2} \underline{/165^o} + I_{A1} \underline{/165^o} + I_{A2} \underline{/285^o})$$

$$V_{OUT} = .85 \sqrt{3}\ Z_{TB}\ I_{A2} \underline{/255^o}$$

By means of similar manipulations it may be shown that the negative sequence networks of the SLYN51B produce no output when pure negative Sequence quantities are applied.

C. Negative Sequence Distance Elements

The M_2T, L_2T, and M_2B elements use an amplitude comparator as the basic discriminating unit. Refer to card locations G, H, and J in Figure 3.

The amplitude comparator cards are used to determine when the operating quantity is greater than the restraint quantity. The operating quantity is the vector sum of the signals at pins 3 and 4. For the M_2T function this is $(-V_2 + I_2Z)$. The restraint quantity is the vector sum of the signals at pins 6 and 7. For the M_2T function this is $(-V_1 + I_1Z)$.

The operating and restraint quantities are AC signals which are rectified on the card. An output signal is produced when the operating quantity is greater than the restraint quantity. When this output lasts longer than the pickup setting of the function timer, an M_2T output is produced.

The reaches of the negative sequence functions are expressed as a percentage of the relay reach. This percentage is determined by impedance components mounted on the N102 and N103 cards through which the operating and restraint quantities must pass.

The reach of the operating quantity is given by the relationship:

$$\text{Reach} = \frac{R_{V2} + 10K}{R_{I2Z} + 10K} \times 100\%$$

where R_{V2} and R_{I2Z} are the impedance components mounted on the N102 and N103 cards through which the V_2 and I_2Z signals pass.

The reach of the restraint quantity in percent is given by the relationship:

$$\text{Reach} = \frac{R_{V1} + 10K}{R_{I1Z} + 10K} \times 100\%$$

where R_{V1} and R_{I1Z} are the impedance components mounted on the N102 and N103 cards through which the V_1 and I_1Z signals pass.

In some functions a capacitor in series with a resistor provides a phase shift in that signal. The reach must then be calculated using the series impedance of the resistor and capacitor.

D. Negative Sequence Directional Elements

The D_2T and D_2B elements use a coincidence logic circuit to sense direction. Refer to card locations N, P, R, and S in Figure 3. The input quantities are V_2 and I_2Z from the sequence networks. If the input quantities are in phase long enough to operate the associated timer, a logic signal will be produced indicating the reverse direction. Likewise, if the input quantities are out of phase long enough to operate the associated timer, a logic signal will be produced indicating the forward direction.

OPERATING CHARACTERISTICS

The operate and reset times of each distance and direction element is basically determined by the characteristic timer, the type of fault and the incidence angle. There is no significant time delay in the circuitry ahead of the timer.

The sensitivity of each directional element is 0.2 Amperes I_2.

For the distance elements, a phase current of one ampere on a three phase fault will cause the distance units to pull back to no less than 90% of nominal reach, with a basic ohmic tap setting (T_B) of 3Ω.

DC BURDEN

The Type SLYN51B relay presents a burden to the Type SSA power supply of:

200 ma from the +15 VDC supply
60 ma from the -15 VDC supply

AC BURDEN

Potential Circuits at 120V Ø-Ø.

	PHASE A		PHASE B		PHASE C	
RESTRAINT	100%	0%	100%	0%	100%	0%
VOLT-AMP	7.0		5.5		11.5	
WATTS						
VARS						

Current Circuits at 5A Ø-N.

	PHASE A		PHASE B		PHASE C	
BASE TAP	3Ω	1Ω	3Ω	1Ω	3Ω	1Ω
R	0.0	0.0	.040		.013	
X	0.0	0.0	.023		.013	
Z	0.0	0.0	.046		.018	

CALCULATION OF SETTINGS

The proper settings for the measuring functions in the SLYN51B relay will depend to some degree on the specific application. For this reason, it is recommended that the application information supplied with the description of the overall logic diagram of the total scheme be consulted for the proper considerations and settings. There are a number of adjustments available in this relay but only some of them are intended for field settings. These are itemized below.

1. The system reach setting.
   This is made in two parts:

   a) Selection of basic tap (T_B) on the back of the relay.

   b) Selection of percent tap (T) on the front of the relay.

2. The individual reach setting for the M_2T.

3. The percent compensation for the D_2B and D_2T functions.

The system reach setting for the SLYN51B is normally set equal to the system reach setting of the associated SLYP relay. Refer to the Calculation of Settings section of the associated SLYP instruction book for an explanation on determining the system reach setting. Also refer to the description supplied with the overall logic diagram of the total scheme for application information on the system reach setting as well as information on the proper setting for the M_2T, D_2B, and D_2T functions.

RECEIVING, HANDLING AND STORAGE

These relays will normally be supplied as a part of a static relay equipment, mounted in a rack or cabinet with other static relays and test equipment. Immediately upon receipt of a static relay equipment, it should be unpacked and examined for any damage sustained in transit. If injury or damage resulting from rough handling is evident, file a damage claim at once with the transporation company and promptly notify the nearest General Electric Sales Office.

Reasonable care should be exercised in unpacking the equipment. If the equipment is not to be installed immediately, it should be stored indoors in a location that is free from moisture, dust, and metallic chips, and severe atmospheric contaminants.

Just prior to final installation the shipping support bolt should be removed from each side of all relay units, to facilitate possible future unit removal for maintenance. These shipping support bolts are approximately 8 inches back from the relay unit front panel. Static relay equipment, when supplied in swing rack cabinets, should be securely anchored to the floor or to the shipping pallet to prevent the equipment from tipping over when the swing rack is opened.

INSTALLATION TESTS

CAUTION

THE LOGIC SYSTEM SIDE OF THE DC POWER SUPPLY USED WITH MOD III STATIC RELAY EQUIPMENT IS ISOLATED FROM GROUND. IT IS A DESIGN CHARACTERISTIC OF MOST ELECTRONIC INSTRUMENTS THAT ONE OF THE SIGNAL INPUT TERMINALS IS CONNECTED TO INSTRUMENT CHASSIS. IF THE INSTRUMENT USED TO TEST THE RELAY EQUIPMENT IS ISOLATED FROM GROUND, ITS CHASSIS MAY HAVE AN ELECTRICAL POTENTIAL WITH RESPECT TO GROUND. THE USE OF A TEST INSTRUMENT WITH A GROUNDED CHASSIS WILL NOT AFFECT THE TESTING OF THE EQUIPMENT. HOWEVER, A SECOND GROUND CONNECTION TO THE EQUIPMENT, SUCH AS A TEST LEAD INADVERTENTLY DROPPING AGAINST THE RELAY CASE, MAY CAUSE DAMAGE TO THE LOGIC CIRCUITRY. NO EXTERNAL TEST EQUIPMENT SHOULD BE LEFT CONNECTED TO THE STATIC RELAYS WHEN THEY ARE IN PROTECTIVE SERVICE, SINCE TEST EQUIPMENT GROUNDING REDUCES THE EFFECTIVENESS OF THE ISOLATION PROVIDED.

CONSTRUCTION

The SLYN51B relay is packaged in an enclosed metal case with hinged front cover and removable top cover. The case is suitable for mounting on a standard 19 inch rack. The outline and mounting dimensions of the case and the physical location of the components are shown in Figures 1 and 3 respectively.

The tap blocks for making the voltage restraint settings are located on the front panel of the unit. The method of making restraint tap settings is illustrated in Figure 6. The connections are made by means of taper pin connectors; special tools are supplied with each equipment for the removal and insertion of these pin connectors.

The current and potential enter the SLYN51B on twelve point terminal strips located on the rear of the relay case. The potential connections are made on the YG terminals strip, the current connections on the YH terminal strip.

The basic minimum ohmic tap (T_B) setting is accomplished on the YH terminal strip on the rear panel of the unit. The current connections for the 1 Ω and 3 Ω taps are shown in Table I.

TABLE I

	I_B		I_C		$3I_0$	
	IN	OUT	IN	OUT	IN	OUT
1 BASE REACH	YH1	YH2	YH4	YH6	YH9	YH10
3 BASE REACH	YH1	YH3	YH5	YH7	YH8	YH10

The V_2 and I_2Z test jacks, the I_2Z magnitude pot (P5) and the relay angle of maximum reach pot (P6) are located on the front of the unit above the voltage restraint taps. The negative sequence filter potentiometers (P1, P2, P3, P4) are located inside the relay case as shown in Figure 3. The V_2 magnitude potentiometer (P7) is located on the rear of the unit.

The SLYN51B relay also contains printed circuit cards identified by a code number such as F110, L111, N102, T101, where F designates filter or comparator, L designates logic, T designates time delay, and N designates network. The printed circuit cards plug in from the front of the unit. The sockets are identified by letter designations or "addresses" (D, E, F, etc.) which appear on the guide strips in front of each socket, on the component location diagram, on the internal connections diagram and on the printed circuit card itself. The test points (TP1, TP2, etc.) shown on the internal connection diagram are connected to instrument jacks on a test card in position T with TP1 at the top of the card. The internal connections of the printed circuit cards are shown in the Printed Circuit Card Instruction Book GEK-34158.

Pin number 1 on the test card in position T is connected to relay reference, pin number 2 to -15 VDC, and pin number 10 to +15 VDC. Output signals are measured with respect to the reference bus on the test card (TP1). Logic signals are approximately +15 VDC for the ON or LOGIC ONE condition, and less than 1 VDC for the OFF or LOGIC ZERO condition. Filter card outputs are either +15 VDC or -15 VDC for the ON condition.

These outputs can be monitored with an oscilloscope, a portable high impedance DC voltmeter, or the test panel voltmeter if available. When the test panel meter is supplied, it will normally be connected to the reference bus. Placing the relay test lead in the proper test point pin jack will connect the meter for testing. When time delay cards are to be adjusted or checked, an oscillscope which can display two traces simultaneously and which has a calibrated horizontal sweep should be used.

TEST AND ADJUSTMENTS REQUIRED

The SLYN51B relay is usually supplied from the factory, mounted and wired as part of a complete static relay equipment. The relay includes the following adjustments, some of these have been preset at the factory, others must be set by the user. The factory adjustments should be rechecked by the user per the procedures under Detailed Testing Instructions to insure that no shipping damage has occurred. The steps must be performed in the order shown.

1) Basic minimum ohmic tap setting (user setting).
2) Voltage restraint tap setting (user setting).
3) Network General Calibration Check (user check).
   NOTE: If this step does not give the results indicated, four additional checks are necessary before proceeding. These checks will enable the user to determine which part of the networks require adjustment. The checks are:
   a) Voltage Sequence Network Balance and Output (P7)
   b) Current Sequence Network Balance and Output
   c) Current Sequence Network Output Magnitude Adjustment (P5)
   d) Relay System Reach Angle Adjustment (P6).
4) Timer card adjustments and tests (user check).
5) M2T reach setting (user setting).
6) Amplitude comparator card checks (user check).
7) D_2T and D_2B settings (user setting).

DETAILED TESTING INSTRUCTIONS

A. BASIC MINIMUM OHMIC TAP SETTING

The arrnagement of the basic ohmic tap is described under Construction, and the choice of tap setting is discussed in separate write-up titled Overall Logic Description. The reach at the Relay System Angle is given by the following relationship:

$$Z = \frac{T_B \times 100}{T}$$

where:

T = Voltage restraint tap setting in percent.

T_B = Basic minimum ohmic tap setting.

B. VOLTAGE RESTRAINT TAP SETTING

The arrangement of the voltage restraint tap blocks is described under construction, and the choice of tap settings is discussed in the section on calculations of settings and a separate write-up titled Overall Logic Description. The pickup voltage at the Relay System Angle given by the following relationship:

$$V_2 = \frac{I_2 \times T_B \times 100}{T}$$

where: V_2 = Negative sequence voltage
T = Voltage restraint tap setting in percent
T_B = Basic minimum ohmic tap setting
I_2 = Negative sequence current

C. GENERAL NETWORK CALIBRATION CHECK

Be sure the DC power supply to the SLYN is turned on. This is a check of both the voltage and current network balances and network output calibration. Perform the checks as outlined in Figure 7. If the required outputs cannot be obtained, it is an indication that the original network adjustments have been disturbed. The following four checks are required only if the network adjustments have been disturbed.

1) Voltage Sequence Network Balance

This test, described in Figure 8 consists of two parts, V_2 null and V_2 output checks. It should be noted that this test requires a 3-phase test source of equal voltages (within 1-2%). Alternate readjustment of pots P1 and P2 is required to obtain the 60 Hz null since the pots are interdependent. When the fundamental frequency has been completely nulled, it is normal for some harmonic voltage to be evident at the test jack, V_2. The magnitude of the harmonic voltage depends on the harmonic content of the test source but usually is less than 0.2 V_{P-P}.

The magnitude of the V_2 test jack voltage must be set equal to the magnitude of the V_1 test jack voltage in the associated SLYP relay with the same level of voltage applied.

Adjust the P7 potentiometer (on rear of unit) until the voltage measured at the V_2 test jack (RMS) is equal to that measured at the V_1 test jack.

2) Current Sequence Network Balance

This test, described in Figure 9, consists of two parts, I_2Z null and I_2Z output checks. Ammeters used in this test should first be calibrated in series to insure that the current used in each phase of the test circuit is equal. Alternate readjustment of pots P3 and P4 is required since they are interdependent. Adjust for 60 Hertz null leaving only harmonic voltage at the I_2Z test jack.

3) Current Sequence Network Output Magnitude Adjustment

NOTE: The DC power supply to the SLYN relay must be on for this test and adjustment. Use the test circuits of Figure 9 and adjust P5 until the I_2Z magnitude is equal to the V_2 magnitude. Pot P5 is located on the front of the relay and is identified as I_2Z magnitude adjustment.

4) Relay System Reach Angle Adjustment

The DC power supply must be turned on for this test. Use test Figure 10 and adjust P6 until the I_2Z and V_2 quantities are exactly 180^o out of phase. Pot P6 is located on the front of the relay and is identified as angle adjustment. Since there is some interaction between P5 and P6, it may be necessary to readjust P5 at this time to maintain an I_2Z magnitude equal to V_2. The magnitude should be recorded at this time for use later in rechecking this relay.

D. TIMER CARD ADJUSTMENTS AND TESTS

The pickup setting determines the amount of coincidence that must occur between the operate and restraint signals before a logic signal output occurs. The reset time delay (dropout time) of the timer provides an overlap of the next half cycle measurement and in some cases provides an intentional time delay before resetting. Timer outputs are DC logic signals. Timer settings are discussed in separate instructions titled Overall Logic Description.

First it is necessary to remove the card before the timer and to place the timer card in a card adapter. The timer test circuit is shown in Figure 11. Opening the N.C. contact causes the output to step up to +15 VDC after the pickup delay of the timer. To increase the pickup time, turn the upper potentiometer (T101 cards adjust P2) on the timer card clockwise. Closing the contact causes the timer output to dropout after the reset delay setting of the card. To increase the reset time, turn the lower potentiometer (on T101 card adjust P3) on the card clockwise.

E. M_2T REACH SETTING

The M_2T function has separate reach adjustments for the operating quantity and the restraint quantity. These adjustments are located on the type N103 card in position F. Potentiometer PA is the adjustment for the operating quantity, I_2Z, and potentiometer PD is the adjustment for the restraint quantity, I_1Z. The range is 20%-100% for both the operate and restraint quantity.

The pot setting corresponding to the desired operating reach can be calculated from the following expression:

$$PA + RA = \frac{(RV_2 + 10K)}{\%\ Reach} 100\% - 10K = R_{I2Z}$$

Note that the PA + RA in the above expression is also equal to R_{I2Z} in the expression in the section on Characteristics - negative sequence distance elements.

In order to set the potentiometer, remove the N103 card from the relay and connect an accurate ohmmeter across the PA and RA combination, card pins 1 and 2. Adjust PA for the ohmmeter reading given by the expression above.

The pot setting corresponding to the desired restraint reach can be calculated from the following expression:

$$PD + RD = \frac{(R_{V1} + 10K)}{\%\ Reach} 100\% - 10K = R_{I1Z}$$

Note that the PD + RD in the above expression is also equal to R_{I1Z} in the expression in the section on characteristics - negative sequence distance elements.

In order to set the potentometer, remove the N103 card from the relay and connect an accurate ohmmeter across the PD and RD combination, card pins 5 and 6. Adjust PD for the ohmmeter reading given by the expression above.

Replace the N103 card in the relay. The M_2T function should be given an operational check per the instruction below titled "Amplitude Comparator Card Tests".

F. AMPLITUDE COMPARATOR CARD TESTS

The following is a two step procedure for checking the balance point of each amplitude comparator function: M_2T, L_2T, M_2B. The first step (items 1-7) checks the amount of I_2Z needed to balance a preset ratio of voltages and the second step (items 8-11) checks the amount of I_1Z needed to balance a preset ratio of voltages.

In order to test the amplitude comparator functions in the SLYN51B, it is necessary to energize both the SLYN51B and the associated SLYP. The test connections are shown in Figure 12. The comparator card under test should be placed in a card adapter so that the card inputs may be observed. The outputs of the SLYN51B functions should be observed at the test point following the associated timer.

1. Adjust the three phase variac of Figure 12 for approximately 120V phase to phase.

2. Adjust the 2-gang variac until the voltage (RMS) at the V_2 test jack is exactly twice the voltage (RMS) at the V_1 test jack. The voltmeter of Figure 14 should read approximately 40V in the counter clockwise direction from the zero position.

3. Jumper the I_1Z test jack to reference.

4. Adjust the phase shifter until the quantities at pin 3 and pin 4 of the card under test are 180^o out of phase.

5. Increase the current until the associated timer output goes From a logic one to a logic zero. At this balance point the I_2Z test jack voltage will be equal to the value given by this expression: ($\pm$5%).

$$I_2Z = \left[\frac{Z_2}{Z_1} - \frac{1}{2} \frac{Z_2}{Z_3} \right] V_2$$

where:

$1/2$ is the ratio $\frac{V_1}{V_2}$ set in step 2.

V_2 is the voltage at the V_2 test jack.

Z_1 is the magnitude of the series impedance in the V_2 circuit.

Z_2 is the magnitude of the series impedance in the I_2Z circuit.

Z_3 is the magnitude of the series impedance in the V_1 circuit.

In the 3 Ω base reach tap, the input current required is approximately 7 amperes for each volt of signal at the I_2Z test jack. The impedances, Z_1, Z_2, Z_3 are calculated from the impedance on the "N" network card plus the input resistor on the amplitude comparator card. If the input current required is high (above 10A), a lower value may be calculated by setting $V_1 = V_2$ in step 2, and modifying the equation above with a $\frac{V_1}{V_2}$ ratio of 1.

6. The equation above is exact only if the associated timer is set for 4.16 MS. For the functions with a timer pickup setting of less than 4.16 ms, the operating point occurs for a higher value of I_2Z than calculated. This is to provide better transient response. For a pickup of 3.5 MS, the I_2Z voltage at the balance point should be approximately 15% higher than calculated.

7. Remove I_1Z jumper.

8. Jumper the I_2Z test jack to reference.

9. Adjust the phase shifter until the quantities at pin 6 and pin 7 of the card under test are in phase.

10. Increase the current until the associated timer output goes from a logic one to a logic zero. At this balance point the I_1Z test jack voltage will be equal to the value given by the expression:

$$I_1Z = \left[\frac{Z_4}{Z_1} - \frac{1}{2}\frac{Z_4}{Z_3}\right] V_2$$

where:

1/2 is the ratio $\frac{V_1}{V_2}$ set in step 2.

V_2 is the voltage at the V_2 test jack.

Z_1 is the magnitude of the series impedance in the V_2 circuit.

Z_3 is the magnitude of the series impedance in the V_1 circuit.

Z_4 is the magnitude of the series impedance in the I_1Z circuit.

As in step 5, the input current required is approximately 7 amperes for each volt of signal at the I_2Z test jack. (for the 3.0 base reach tap)

11. For the functions with a timer pickup setting of less than 4.16 ms, the operating point occurs for a higher value of I_2Z than calculated. This is to provide better transient response. For a pickup of 3.5 ms the I_2Z voltage at the balance point should be approximately 15% higher than calculated.

SAMPLE CALCULATION

Table IX lists the N card components for an amplitude comparator function.

TABLE IX

CIRCUIT	N-CARD COMPONENTS
V_2	6.19K, .33 uf
I_2Z	2.1K
V_1	8.25K
I_1Z	4.64K

Z_4 = 4.64K + 10K = 14.64
(10K is the input impedance of the amplitude comparator card)
Z_3 = 8.25K + 10K = 18.25K
Z_2 = 2.10K + 10K = 12.10K
$Z_1 \,\underline{/\,\theta} = 6.19K - j\,1/[2\pi\,(60)\,(.33 \times 10^{-6})] + 10K = 18.25K \,\underline{/-29^0}$
Z_1 = 18.25K

$$I_2Z = \left[\frac{Z_2}{Z_1} - \frac{1}{2}\frac{Z_2}{Z_3}\right] V_2$$

$$= \left[\frac{12.1K}{18.25K} - \frac{1}{2}\frac{12.1K}{18.25K}\right] V_2$$

$$I_2Z = .332\ V_2$$

$$I_1Z = \left[\frac{Z_4}{Z_1} - \frac{1}{2}\frac{Z_4}{Z_3}\right] V_2$$

$$= \left[\frac{14.64K}{18.25K} - \frac{1}{2}\frac{14.64K}{18.25K}\right] V_2$$

$$I_1Z = .40\ V_2$$

G. D_2B AND D_2T OFFSET SETTINGS AND OPERATIONAL CHECKS

The following is a three step testing procedure for the negative sequence directional element. The first step, items 1-3 below, checks the signal dropping impedances ahead of the directional comparator card, position N. The second step, item 4-6, sets the amount of offset desired and the third step, item 7, is an overall functional check.

Refer to the test circuit shown in Figure 13.

1. Adjust the voltage and current to obtain 1.0 VRMS at the V_2 and I_2Z test jacks.

2. Adjust the phase shifter so that the test jack voltages are 180^0 out of phase.

3. Place the F109 card in position N in a card extender and make the following checks:

   a) The voltage at pin 3 should be .47 - .53 V_{RMS}
   b) The voltage at pin 4 should be .47 - .53 V_{RMS}
   c) Link in the "B" position - voltage at pin 4 leads pin 3 by 35^0 (1.45 - 1.60 ms)
   Link in the "A" position - voltage at pin 4 in phase with pin 3. ($\pm$ .10 ms)

NOTE: The link is located on the N103 card in card position F.

4. Adjust the phase shifter so that the voltages at pin 3 and pin 4 are exactly in phase.

5. With the I_2Z test jack voltage set at 1.0 V_{RMS}, adjust the applied voltage until the V_2 test jack voltage (RMS) is equal to:

$$V_2 = \frac{k}{100} \quad V_{RMS}$$

where k is the desired offset in percent.

6. Observe the output at pin 6, position N, on an oscilloscope. Adjust P1 for no output blocks. Observe the output at pin 9 and adjust P2 for no output.

7. Test per Table III.

TABLE III

TEST JACK VOLTAGES		PIN 3 AND PIN 4 PHASE RELATIONSHIP	OUTPUT	
V_2	I_2Z		TP7	TP9
0	1.0	-----	+15V	0V
1.0	0	-----	0V	0V
1.0	1.0	IN PHASE	0V	+15V
1.0	1.0	180^0 OUT OF PHASE	+15V	0V

PERIODIC CHECKS AND ROUTINE MAINTENANCE

PERIODIC TESTS

All functions included in the SLYN51B relay may be checked at periodic intervals using the procedures described in the section covering Detailed Testing Instructions. Cable connection between the SLYN51B relay and the associated type SLA relay can be checked by observing the SLYN51B outputs at test points in the SLA relay.

The following checks are suggested as periodic checks/routine maintenance.

1) Network General Calibration Check - See Detailed Testing Instruction.

2) Amplitude comparator card checks - See Detailed Testing Instruction.

3) D_2T and D_2B operational checks - See Detailed Testing Instruction.

TROUBLE SHOOTING

In any trouble shooting equipment, it should first be established which unit is functioning incorrectly. The overall logic diagram supplied with the equipment shows the combined logic of the complete equipment and the various test points in each unit. By signal tracing, using the overall logic diagram and the various test points, it should be possible to quickly isolate the trouble.

A test adapter card (0149C7259G-2) is supplied with each static relay equipment to supplement the prewired test points on the test cards. Use of the adapter card is described in the card Instruction Book GEK-34158.

A dual-trace oscilloscope is a valuable aid to detailed trouble shooting, since it can be used to determine phase shift, operate and reset times as well as input and output levels. A portable dual-trace oscilloscope with a calibrated sweep and trigger facility is recommended.

SPARE PARTS

To minimize possible outage time, it is recommended that a complete maintenance program should include the stocking of at least one spare card of each type. It is possible to replace damaged or defective components on the printed circuit cards, but great care should be taken in soldering so as not to damage or bridge-over the printed circuit busses, or overheat the semi-conductor components. The repaired area should be recovered with a suitable high-dielectric plastic coating to prevent possible breakdowns across the printed busses due to moisture and dust. The wiring diagrams for the cards in the SLYN51B relay are included in the card book GEK-34158; the card types are shown on the component location diagram, Figure 3.

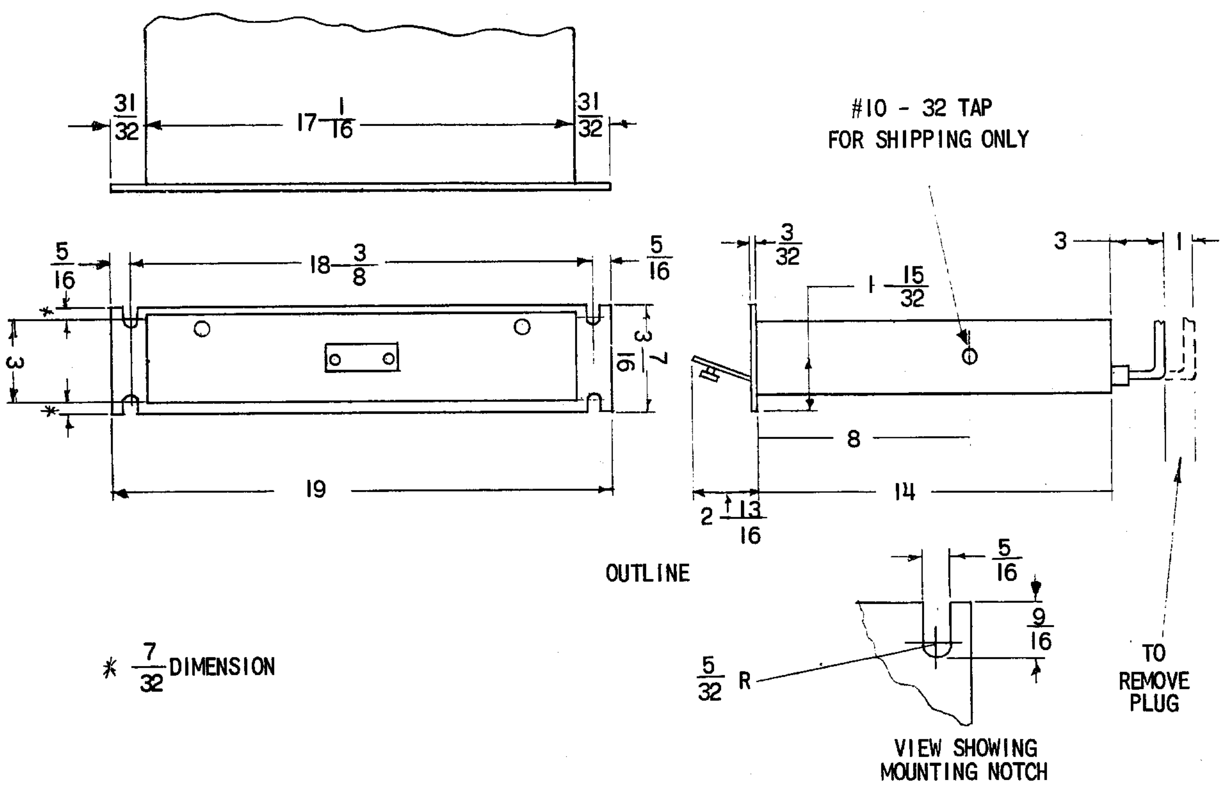


FIG. 1 (227A2036-0) OUTLINE AND MOUNTING DIMENSIONS FOR THE TYPE SLYN51B RELAY

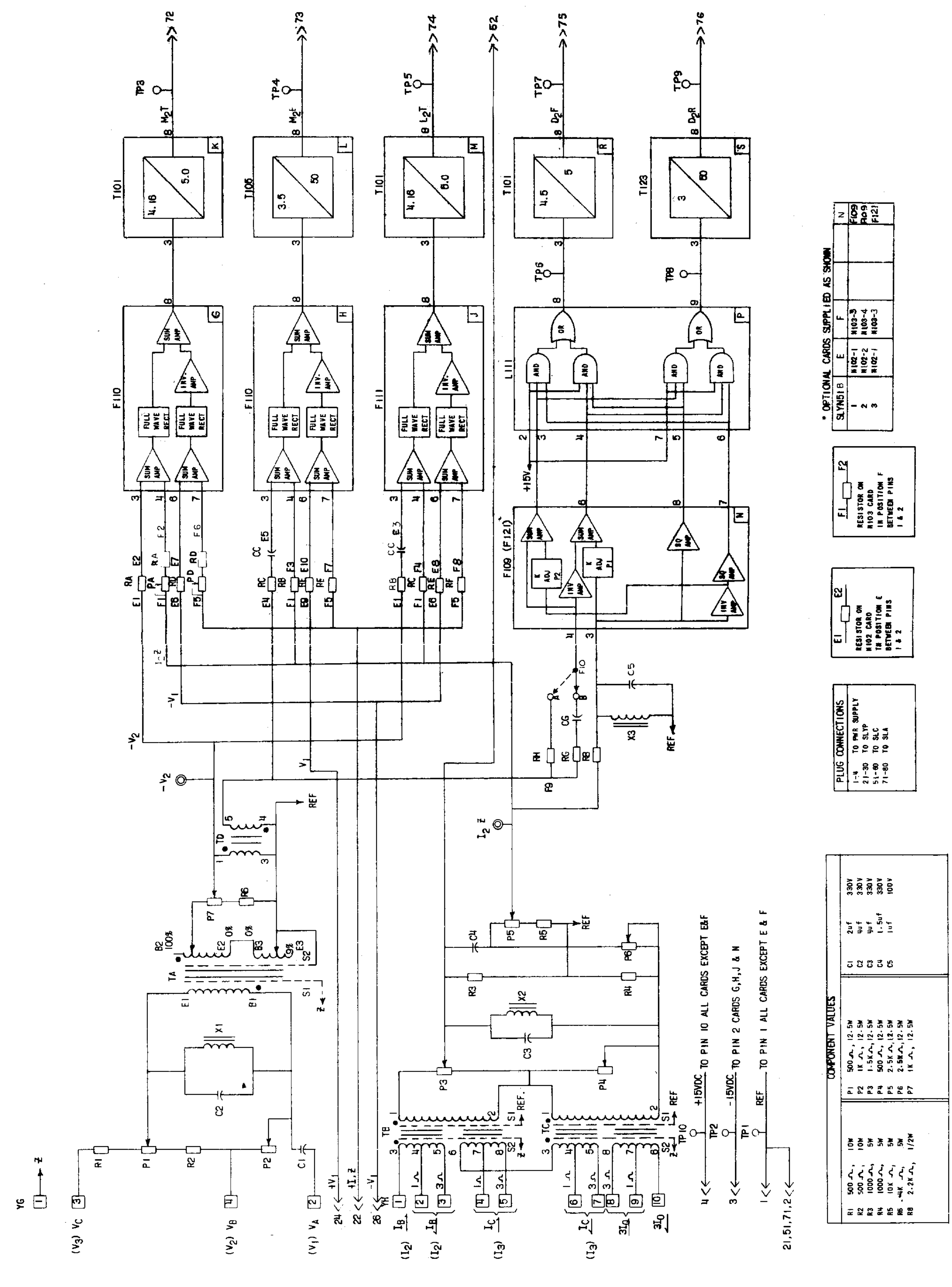
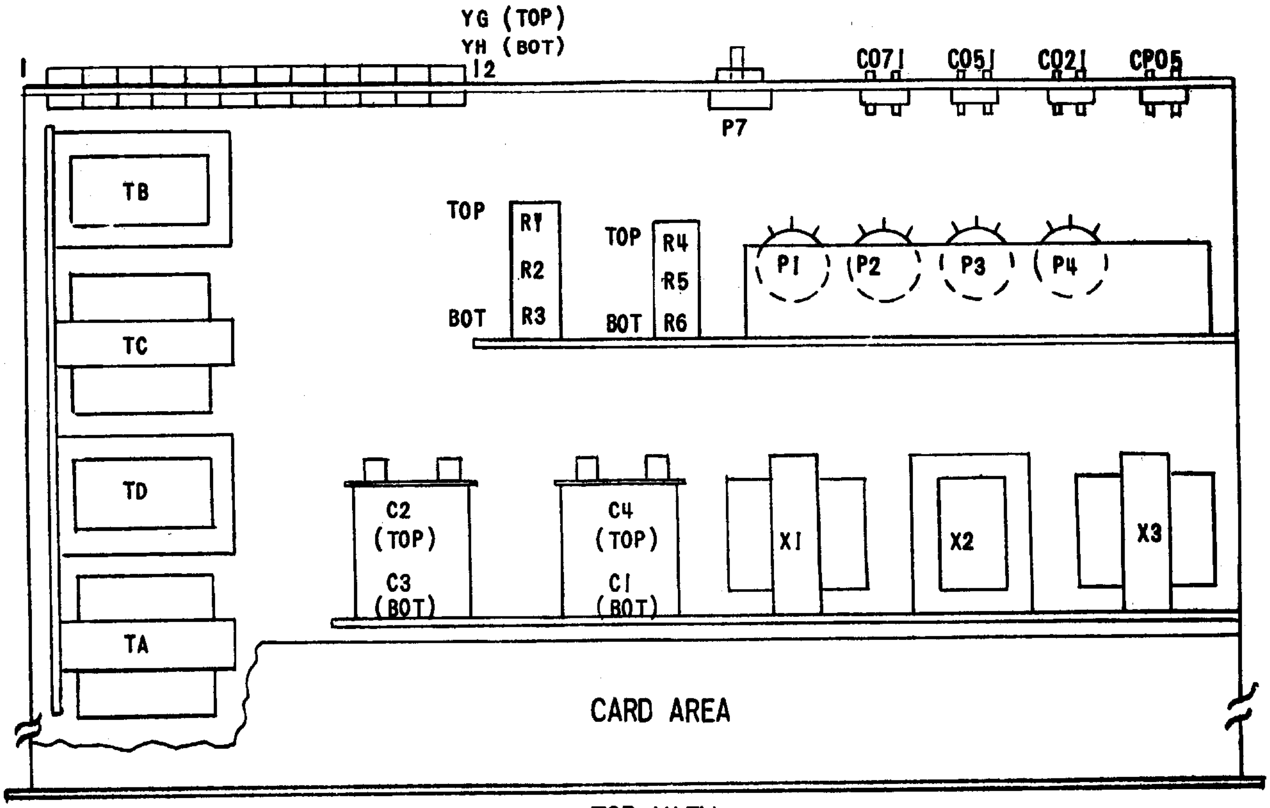
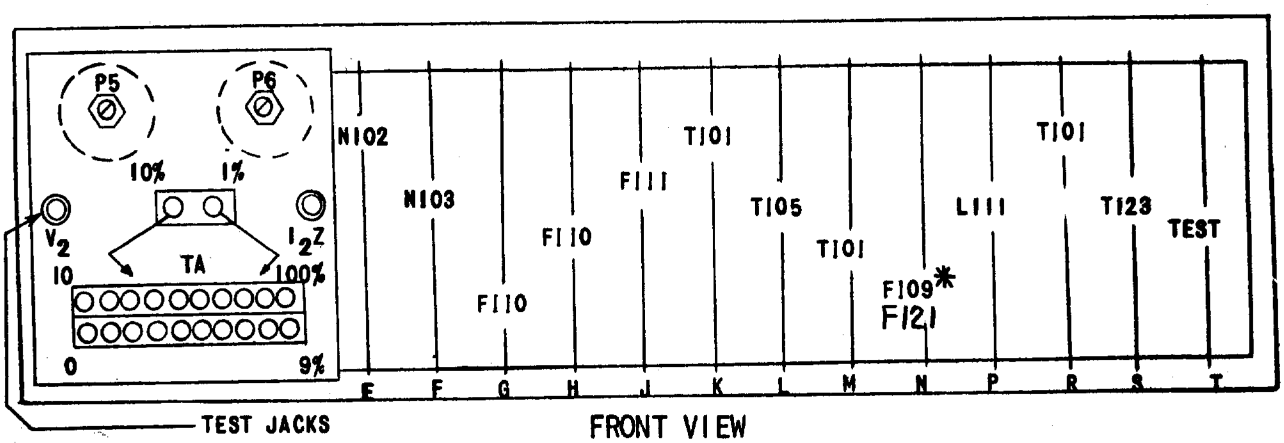


FIG. 2 (149C7376-1) INTERNAL CONNECTIONS FOR THE TYPE SLYN51B RELAY



TOP VIEW



FRONT VIEW

* OPTIONAL CARDS

FIG. 3 (227A2198-0) COMPONENT LOCATION DIAGRAM FOR THE TYPE SLYN51B RELAY

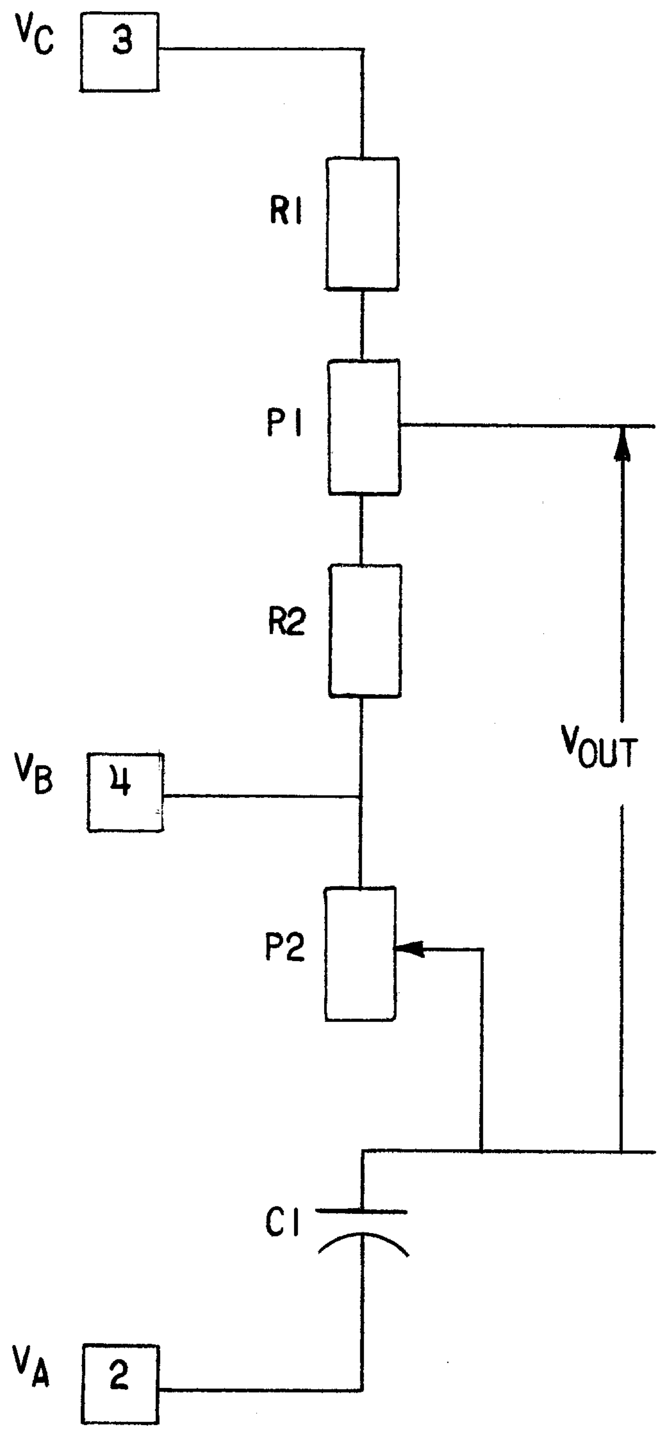


FIG. 4 (227A2176-0) SLYN NEGATIVE SEQUENCE VOLTAGE NETWORK

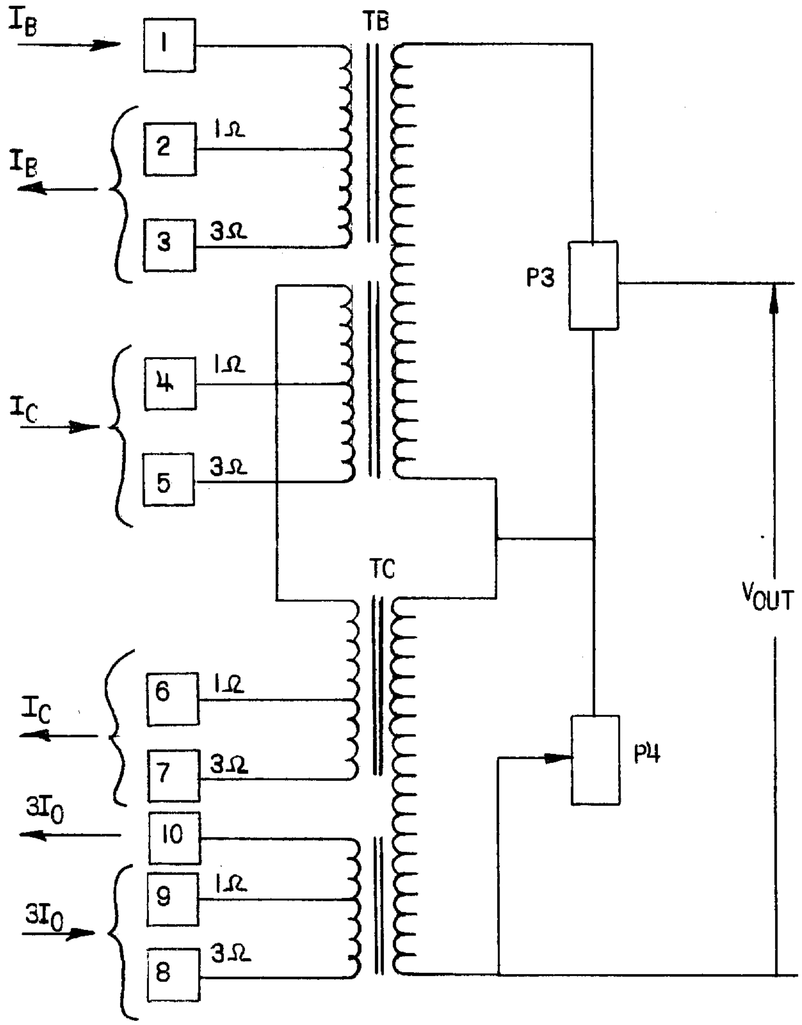
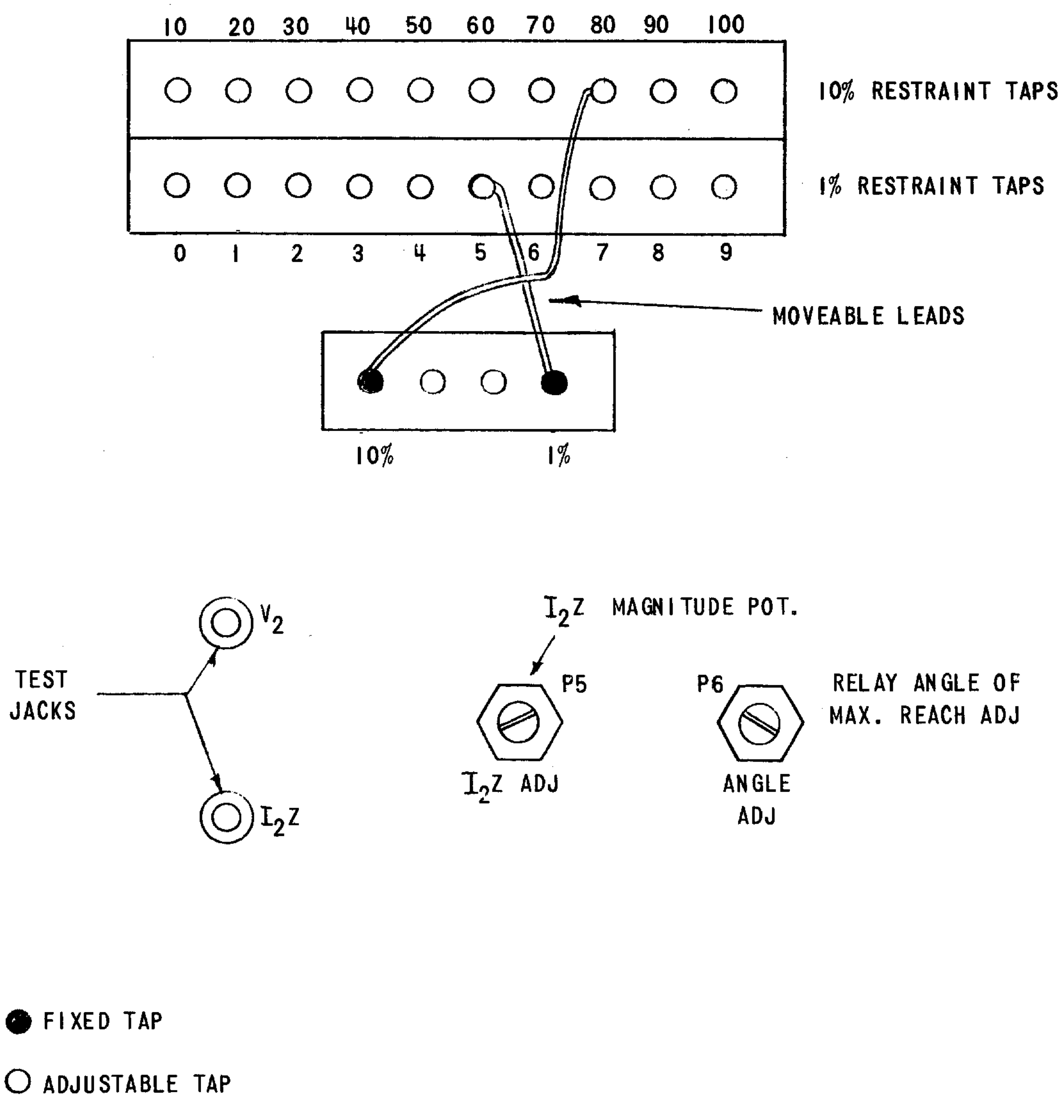


FIG. 5 (227A2179-0) SLYN NEGATIVE SEQUENCE CURRENT NETWORK

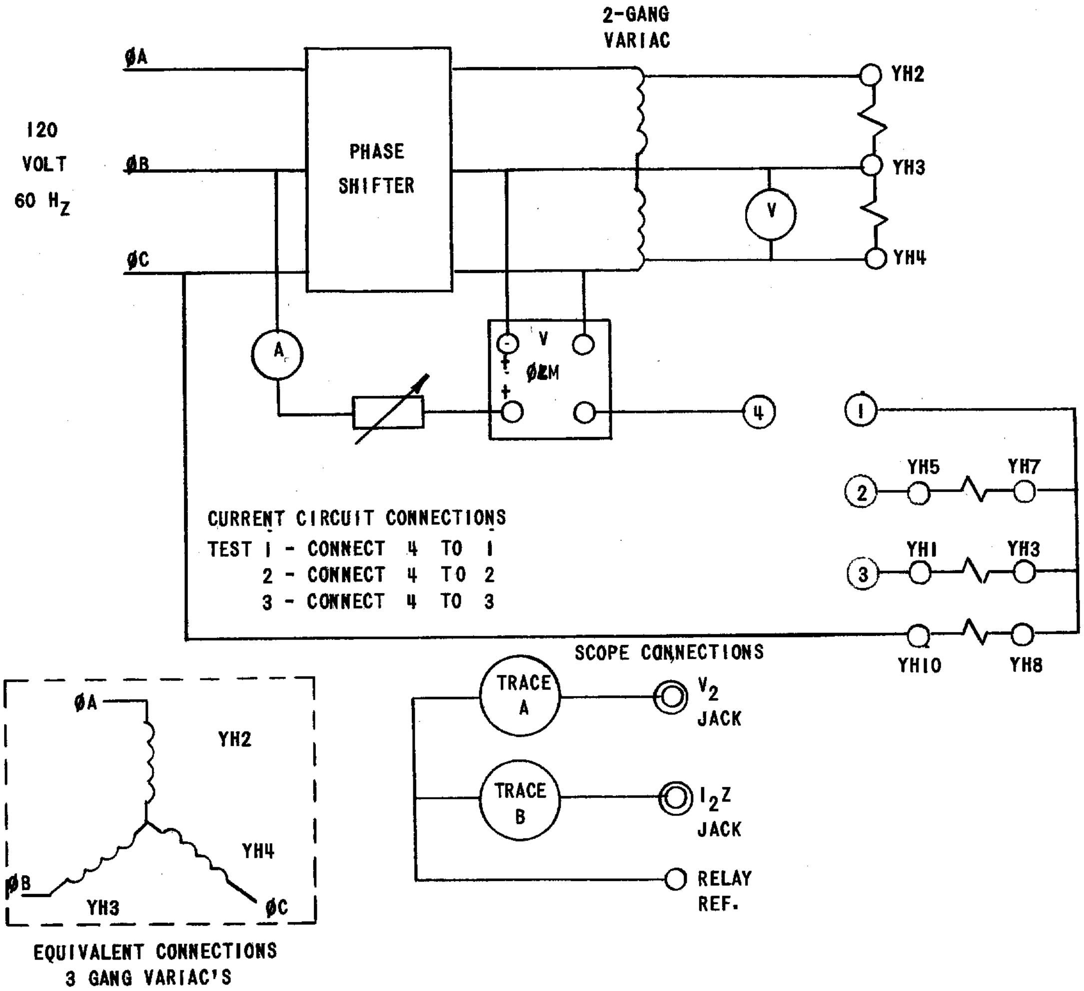


85% VOLTAGE RESTRAINT TAP ILLUSTRATED

REACH $\simeq$ 1.18 T_B

T_B = BASIC MINIMUM OHMIC TAP SETTING

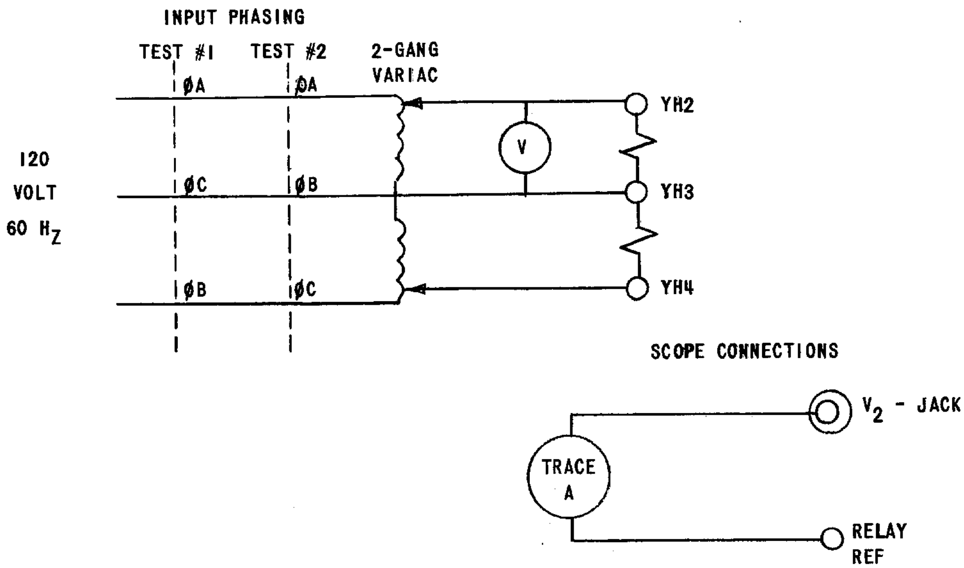
FIG. 6 (227A2178-1) ~~TYPICAL~~ SYLN VOLTAGE RESTRAINT TAP SETTING



	BALANCED 3Ø RELAY INPUT VOLTS	INPUT AMPS	PHASE ANGLE *	OUTPUT INDICATION	REMARKS **
TEST 1	8.66 VOLT RMS	5 AMP	TEST ANGLE	CHECK $V_2 = I_2Z$ (±.05V) V ≅ 1.2 VOLTS P-P V_2 & I_2Z 180° OUT OF PHASE (±0.[illegible]MS)	AØ TO GRD. NETWORK CHECK
TEST 2	8.66 VOLT RMS	5 AMP	TEST ANGLE +120°		BØ TO GRD. NETWORK CHECK
TEST 3	8.66 VOLT RMS	5 AMP	TEST ANGLE +240°		CØ TO GRD. NETWORK CHECK

* TEST ANGLE RELAY ANGLE PLUS +30°
** RELAY VOLTAGE RESTRAINT TAP SETTING 100% FOR ALL TESTS

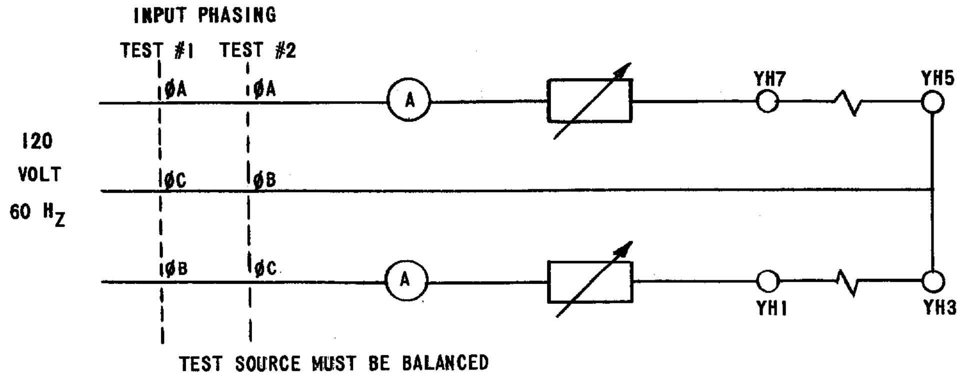
FIG. 7 (257A6215-0) NEGATIVE SEQUENCE NETWORK CHECK 1 Ø CURRENT

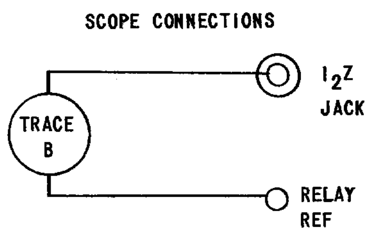


TEST	BALANCED 3Ø RELAY INPUT VOLTS	OUTPUT INDICATION	ADJUST	REMARKS *
#1 V_2-NULL	120 VOLTS R.M.S.	LESS THAN 0.2 VOLT P-P RIPPLE	P2 & P1 ALTERNATELY FOR MINIMUM FUNDAMENTAL OUTPUT	VOLTAGE RESTRAINT TAP SETTING 100% START P2 & P1 ADJUSTMENT FROM MIDPOINT OF POTS
#2 V_2 OUTPUT	26 VOLTS R.M.S.	APPROX. 3.4 VOLTS P-P	P7	VOLTAGE RESTRAINT TAP SETTING 100% SET VOLTAGE EQUAL TO V_1 RECORD VOLTAGE VALUE FOR I_2Z CALIBRATION

* OBSERVE INPUT PHASING

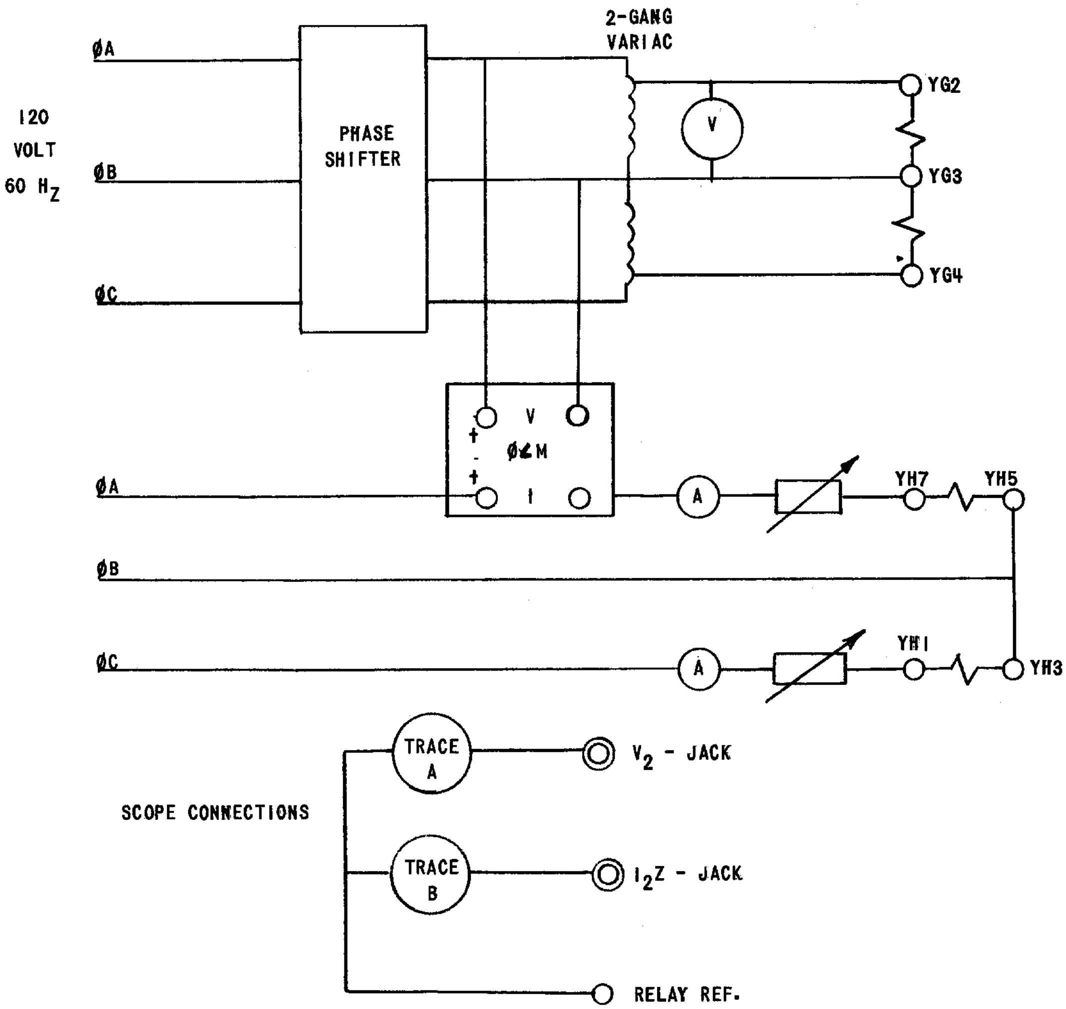
FIG. 8 (257A6217-0) VOLTAGE SEQUENCE NETWORK TEST





	INPUT AMPS	OUTPUT INDICATION	ADJUST	REMARKS
TEST #1 I_2Z NULL	5 AMPS PER PHASE	LESS THAN 0.2 VOLT P-P RIPPLE	P4 & P3 ALTERNATELY FOR MINIMUM FUNDAMENTAL OUTPUT	OBSERVE INPUT PHASING, START P4 & P3 ADJUSTMENT FROM MIDPOINT OF POTS
TEST #2 I_2Z OUTPUT	5 AMPS PER PHASE	APPROXIMATELY 3.4 VOLTS P-P	P5 TO OBTAIN VALUE EQUAL TO V_2 OUTPUT	OBSERVE INPUT PHASING

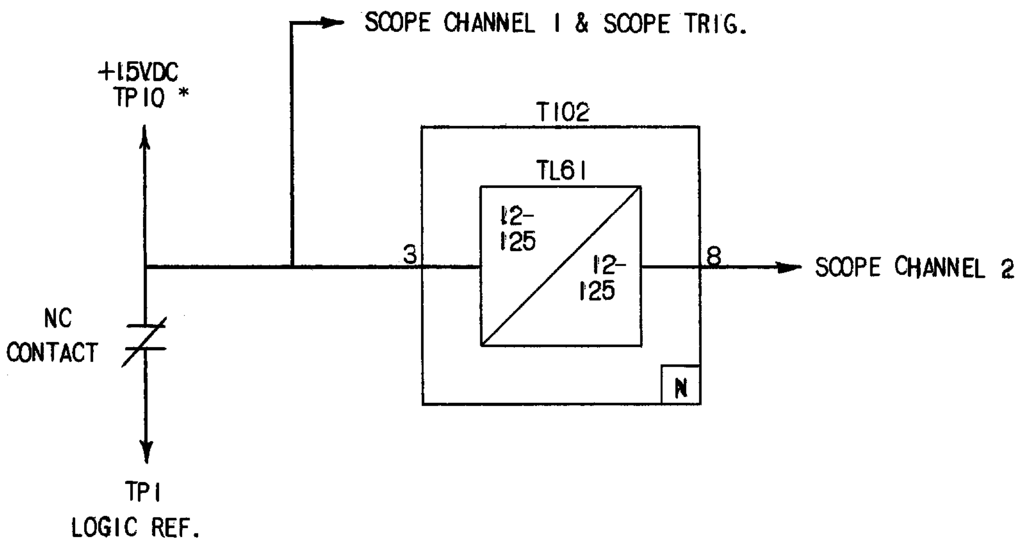
FIG. 9 (257A6216-0) CURRENT SEQUENCE NETWORK TEST



* TEST ANGLE RELAY ANGLE (+) 30°

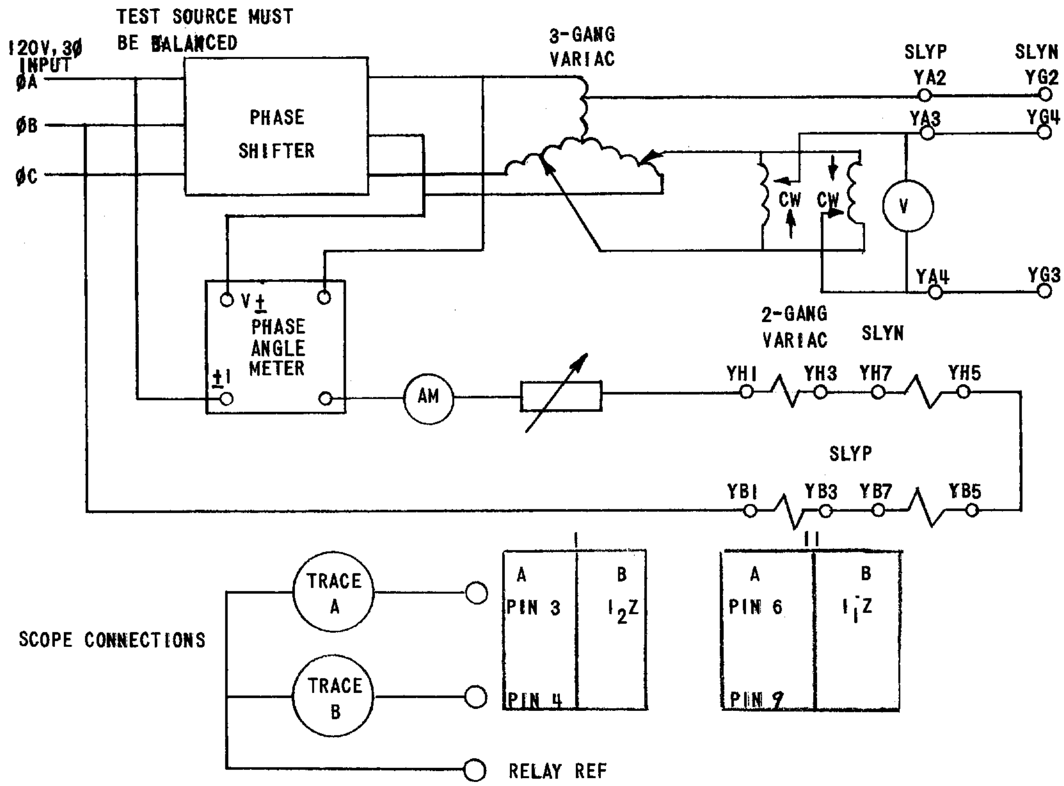
BALANCED 3Ø RELAY INPUT VOLTS	INPUT AMPS	PHASE ANGLE *	OUTPUT INDICATION	ADJUST	REMARKS
26 VOLTS RMS	5 AMPS PER PHASE	TEST ANGLE	V_2 & I_2Z EQUAL MAGNITUDE AND 180° OUT OF PHASE (TRACES A & B)	ADJUST P6 TO BRING I_2Z 180° OUT OF PHASE WITH V_2 READJUST P5 TO MAINTAIN MAGNITUDE EQUAL TO V_2	OBSERVE INPUT PHASING RELAY VOLTAGE RESTRAINT TAP SETTING 100%

FIG. 10 (257A6214-0) RELAY SYSTEM REACH ANGLE



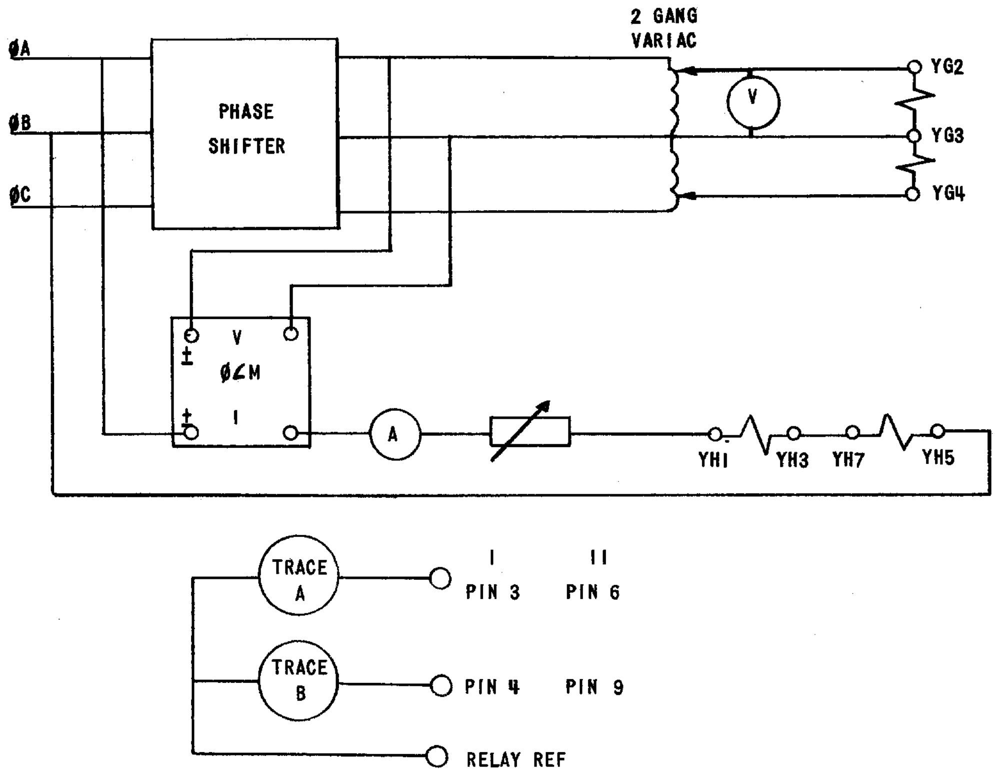
* THE 15VDC SIGNAL AT PIN 10 HAS A CURRENT LIMITING RESISTOR MOUNTED ON THE TEST CARD.

FIG. 11 (246A7987-0) TIMER TEST CIRCUIT



BALANCED 3Ø RELAY INPUT VOLTS	INPUT AMPS	ADJUST	REMARKS
I 120V	INCREASE UNTIL REQUIRED OUTPUT IS NOTED	1) 2 GANG VARIAC FOR V_2 TEST JACK VOLTAGE TWICE* V_1 TEST JACK (*SEE TEXT) 2) PHASE SHIFTER UNTIL PIN 3 AND 4 OF CARD UNDER TEST ARE 180° OUT OF PHASE (SEE I-A)	JUMPER I_1Z TO REFERENCE INCREASE CURRENT UNTIL TIMER OUTPUT GOES FROM LOGIC ONE TO LOGIC 0 RECORD I_2Z VOLTAGE FOR COMPUTATION (SEE I-B)
II 120V	INCREASE UNTIL REQUIRED OUTPUT IS NOTED	1) 2 GANG VARIAC FOR V_2 TEST JACK VOLTAGE TWICE * V_1 TEST JACK (*SEE TEXT) 2) PHASE SHIFTER UNTIL PIN 6 AND 9 OF CARD UNDER TEST ARE IN PHASE (SEE II-A)	REMOVE I_1Z JUMPER AND JUMPER I_2Z TO REFERENCE INCREASE CURRENT UNTIL TIMER OUTPUT GOES FROM LOGIC ONE TO LOGIC 0 RECORD I_1Z VOLTAGE FOR COMPUTATION (SEE II-B)

FIG. 12 (257A6218-0) AMPLITUDE COMPARATOR TEST CIRCUIT



BALANCED 3Ø RELAY INPUT VOLTS	INPUT AMPS	ADJUST	OUTPUT INDICATION
I ADJUST FOR 1.0V RMS AT V_2 TEST JACK	ADJUST FOR 1.0V RMS AT I_2Z TEST JACK	PHASE SHIFTER FOR V_2 180° OUT OF PHASE WITH I_2Z	VOLTAGE AT PIN 3 AND PIN 4 F109 CARD POSITION N .47-.53 VRMS "A" LINK POSITION PEN 3 AND PEN 4 VOLTAGE IN PHASE (±.1OMS) "B" LINK POSITION PEN 4 LEADS PEN 3 VOLTAGE BY 35° (1.45-1.60MS)
II SET TO OBTAIN THE REQUIRED V_2 TEST JACK VOLTAGE CORRESPONDING TO THE OFFSET DESIRED	ADJUST FOR 1.0VRMS AT I_2Z TEST JACK	ADJUST P1 ON F109 CARD FOR ZERO OUTPUT AT PIN 6 ADJUST P2 ON F109 CARD FOR ZERO OUTPUT AT PIN 9.	PIN 6 OF F109 CARD PIN 9 OF F109 CARD

FIG. 13 (257A6219-0) DIRECTIONAL ELEMENT OFFSET SETTING.

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- • * New Orleans 70114 . . . . 1115 DeArmas St.

MARYLAND
- • * Baltimore 21230. . . . . . . 920 E. Fort Ave.

MASSACHUSETTS
- • * Δ (Boston) Medford 02155 . . . . 3960 Mystic Valley Pkwy.

MICHIGAN
- • * Δ (Detroit) Riverview. . . . 18075 Krause Ave.
- • Flint 48505 . . . . 1506 E. Carpenter Rd.

MINNESOTA
- • Duluth 55807 . . . 50th Ave. W & St.Louis Bay
- • * Minneapolis 55430 . . . . 2025 49th Ave., N.

MISSOURI
- • * Kansas City 64120. . . . . 3525 Gardner Ave.
- • * St. Louis 63110 . . . . 1115 East Rd.

NEW JERSEY
- • New Brunswick 08902 . . . . . 3 Lawrence St.

NEW MEXICO
- • Albuquerque 87109 . . . 4420 McLeod Rd. NE

NEW YORK
- • Albany 12205 . . . . 1097 Central Ave.
- • * (Buffalo) Tonawanda 14150 . . 175 Milens Rd.
- • (Long Island) Old Bethpage 11804 . . . . 183 Bethpage-Sweet Hollow Rd.
- • (New York City) North Bergen, N. J. 07012 . . . . 6001 Tonnelle Ave.
- * (New York City) Clifton, N. J. 07012 . . . . 9 Brighton Rd.
- * Δ Schenectady 12305 . . . . 1 River Rd.
- • Syracuse 13208. . . . 1015 E. Hiawatha Blvd.

NORTH CAROLINA
- • * Charlotte 28208 . . . . 2328 Thrift Rd.

OHIO
- • Akron (Canton) 44720 . . . . 7900 Whipple Ave. N. W.
- • * Cincinnati 45202. . . . . . . .444 West 3rd St.
- • * Δ Cleveland 44125 . . . . . . 4477 East 49th St.
- • Columbus 43229 . . . . 6660 Huntley Rd.
- • * Toledo 43605 . . . . 405 Dearborn Ave.
- • Youngstown 44507. . . . 272 E. Indianola Ave.

OKLAHOMA
- • Tulsa 74145. . . . . . 5220 S. 100th East Ave.

OREGON
- • Eugene 97402 . . . . 570 Wilson St.
- • * Portland 97210 . . . . . . 2727 NW 29th Ave.

PENNSYLVANIA
- • Allentown 18103 . . . . . . 668 E. Highland St.
- * (Delaware Valley) Cherry Hill, N. J., 08034 . . . . 1790 E. Marlton Pike
- • Johnstown 15802 . . . . 841 Oak St.
- • Philadelphia 19124 . . . 1040 East Erie Ave.
- • * (Pittsburgh) West Mifflin 15122 . . . . 4930 Buttermilk Hollow Rd.
- • York 17403 . . . . .54 N. Harrison St.

SOUTH CAROLINA
- • (Charleston) No. Charleston 29401 . . . . 2490 Debonair St.

TENNESSEE
- • Knoxville 37914 . . . . 2621 Governor John Sevier Hwy.
- • Memphis 38107. . . . . . . 708 North Main St.

TEXAS
- • Beaumont 77705 . . . . . 1490 W. Cardinal Dr.
- • Corpus Christi 78401 . . . . . . 115 Waco St.
- • * Dallas 75235 . . . . .3202 Manor Way
- • Houston 77036 . . . . .5534 Harvey Wilson Dr.
- * Houston 77036 . . . . .6916 Harwin Dr.
- • Midland 79701 . . . . 704 S. Johnston St.

UTAH
- • * Salt Lake City 84110 . . . 301 S. 7th West St.

VIRGINIA
- • * Richmond 23224 . . . . 1403 Ingram Ave.
- • Roanoke 24013 . . . . . . 1004 River Ave., SE

WASHINGTON
- • * Seattle 98134 . . . . . 3422 First Ave., South
- • Spokane 99211 . . . . E. 4323 Mission St.

WEST VIRGINIA
- • * Charleston 25328 . . 306 MacCorkle Ave., SE

WISCONSIN
- • (Appleton) Menasha 54910 . . 1725 Racine St.
- • Milwaukee 53207 . . . 235 W. Oklahoma Ave.

• Electrical/Mechanical Service Shop * Instrumentation Shop Δ Special Manufacturing Shop