ST—100*ADJUSTABLE FREQUENCY AC DRIVE
3S7506FV300 TO 3S7506FV319

THEORY OF OPERATION

A brief description of circuit operation for the basic power unit will be presented in this section. In order to simplify the description, the complete circuit will be divided according to the function performed. A partial elementary diagram for each division will be used to describe that portion of the circuit. The complete circuit is shown on the elementary diagram supplied with the equipment.

It is the purpose of this section to provide a basic understanding of circuit operation which should be helpful in the operation and maintenance of ST-100 drives.

POWER UNIT BLOCK DIAGRAM (Figure 1)

The ST-100 power unit will convert 3Ø AC line power to adjustable DC and invert the DC to adjustable frequency AC power. The simplified block diagram of Figure 1 shows the major circuit sections required to perform this function.

Input AC is converted to adjustable DC by half-wave phase controlled rectifiers. This DC is then converted to adjustable frequency AC by controlled switching of the rectifiers in a 3Ø inverter bridge. A single speed reference signal is supplied through a timed acceleration and deceleration circuit to both the voltage regulator and frequency control circuits. The voltage regulator controls the DC voltage supplied to the inverter and the frequency control circuit sets the inverter SCR switching sequence, thus controlling the volts, per hertz ratio of power supplied to the load. A separate commutation circuit controlled by the frequency control circuit will turn off the inverter SCR's at the proper time.

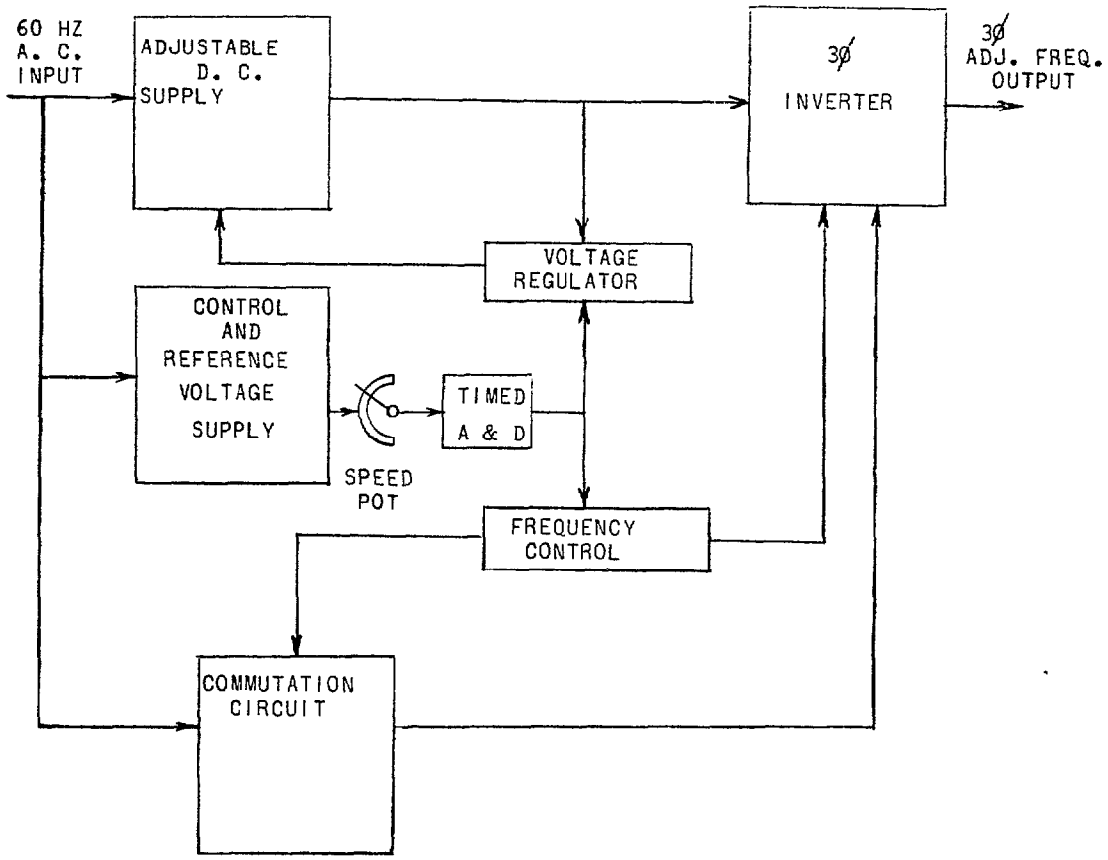

Figure 1. Power Unit Block Diagram

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START-UP CIRCUIT (Figure 2)

The normally closed contact of relay 1CR performs the dual function of discharging capacitor 1C through 29D and 3R and essentially shorting the 47 volt supply to zero through 16D and 52R. When AC input power is applied, relay 1CR will pick up after a delay of approximately 6 cycles determined by resistor 7R and capacitor 18C. This short delay in releasing the 47 volt supply is necessary to prevent the firing circuits from operating until the voltage regulator has stablized.

Pressing the start button will cause relay 2CR to pick up and seal in. This will release the reference voltage set by the speed potentiometer and the power unit output frequency and voltage will start to increase.

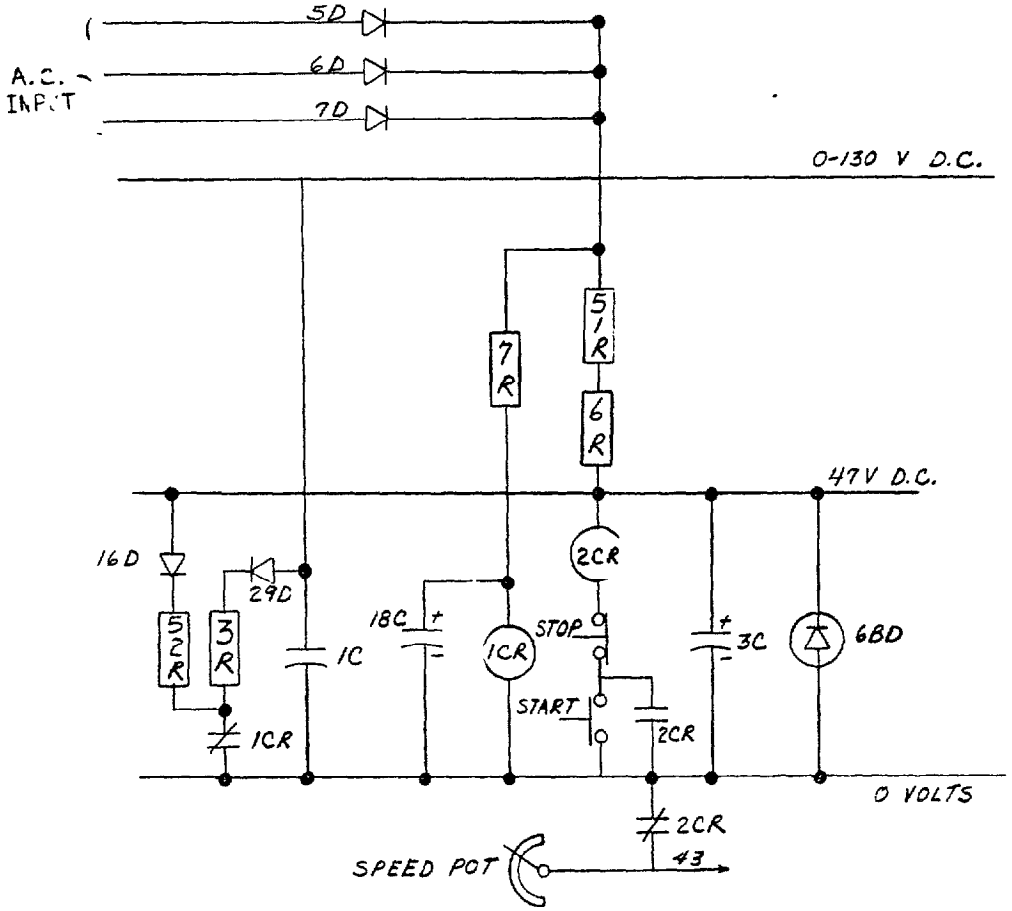

Figure 2. Start-Up Circuit

CONTROL POWER SUPPLY AND REFERENCE INPUT CIRCUIT (Figure 3)

Voltage for the control circuitry is zener regulated at 24.8 volts DC ± 10% by 1, 2, 3, and 4BD. Power is obtained directly from the input lines through half-wave rectifiers 5D, 6D, and 7D. Initial filtering is provided by capacitor 2C and final filtering by capacitor 4C. The voltage dropping resistor 39R limits the current in the zener diodes, and resistor 5R limits the initial surge current in capacitor 2C. Rectifier 8D provides isolation from other circuits supplied by rectifiers 5D, 6D, and 7D.

The input reference voltage at circuit point 43, which controls both output frequency and voltage, can be adjusted between 0 and 12 volts by changing the slider position on potentiometer 2P. Resistor 9R forms a divider circuit with 2P so that the reference voltage across the potentiometer will be approximately 12 volts. The normally closed contact of relay 2CR holds the input voltage at zero, regardless of the setting of potentiometer 2P, until relay 2CR is energized by pressing the start button. Diode 9D and resistor 10R provide a fixed diode drop so that the voltage at 44 will be slightly positive when the voltage at 43 is zero. This is necessary to insure that the inverter starts with a minimum delay after the start button is pressed.

The 47 volt DC supply provides power for all firing circuits and for the start up relay. This supply is zener regulated at 47 volts ± 10% by 6BD and filtered by capacitor 3C. Resistors 51R and 6R limit the current in the zener diode.

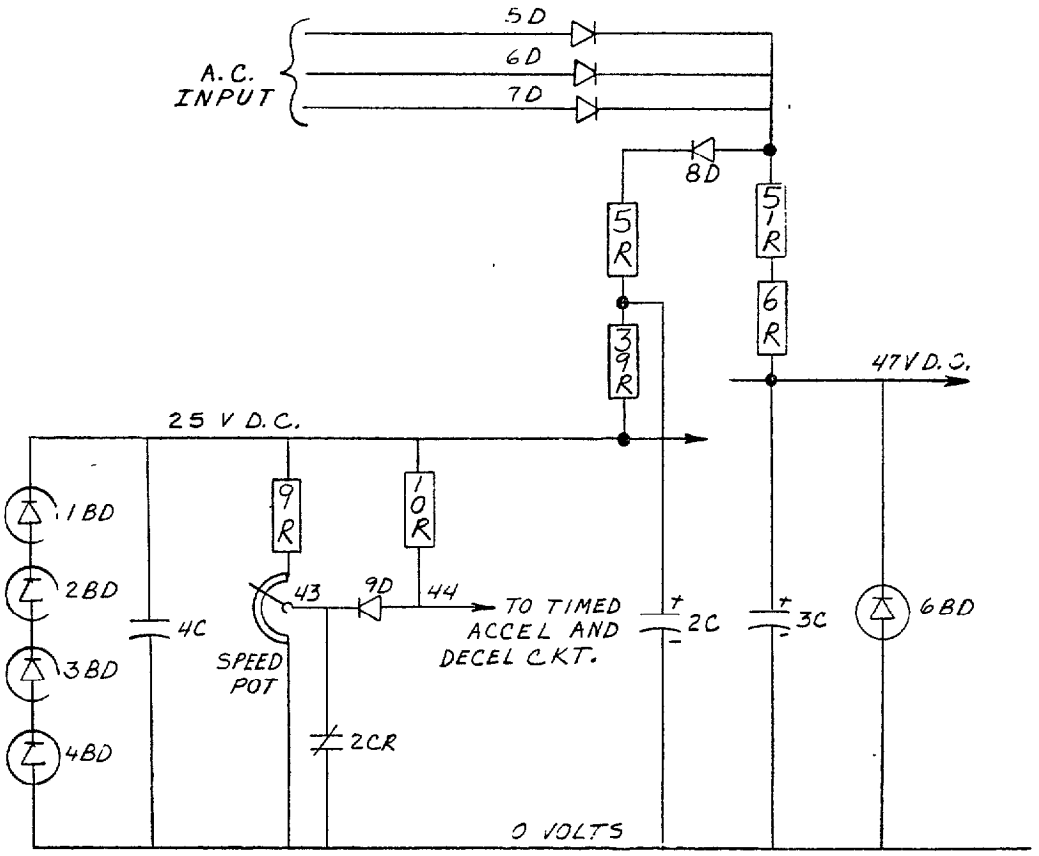

Figure 3. Control Power Supply and Reference Input Circuit

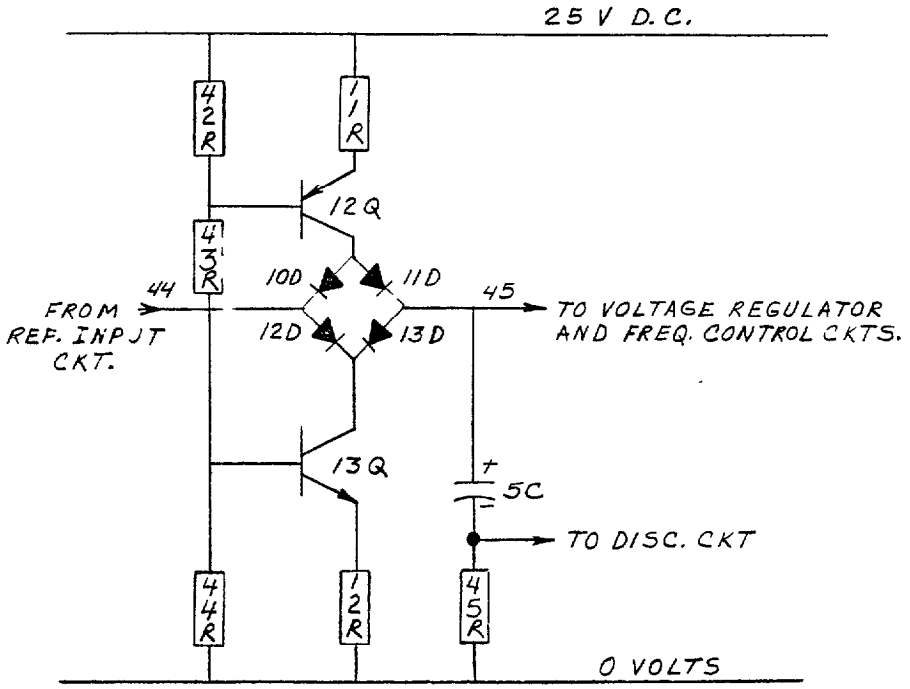

Figure 4. Timed Acceleration and Deceleration Control Circuit

TIMED ACCELERATION AND DECELERATION CONTROL CIRCUIT (Figure 4)

The DC voltage level at circuit point 45 will control both the DC power buss level and the output frequency. This voltage will be the same as the voltage at point 44 which was set by potentiometer 2P. However, the voltage at point 45 will increase and decrease at a linear timed rate determined by the constant current charging and decharging of capacitor 5C through transistors 12Q and 13Q. The current in 12Q and 13Q is set by the voltage across divider resistors 42R and 44R and the value of emitter resistors 11R and 12R. These values of resistance are identical and will be set for approximately 20 seconds. This will be the time required to charge 5C from 0 to 12 volts or discharge from 12 volts to 0, even though the voltage at point 44 may cover this range instantaneously. Other times may be set by changing the value of resistors 11R and 12R. The diode bridge provides decoupling which will allow capacitor 5C to charge through 11R, 12Q and 11D or discharge through 13D, 13Q and 12R depending on whether the voltage at 44 is higher or lower than the voltage at 45.

DC VOLTAGE REGULATOR CIRCUIT (Figure 5)

The reference voltage at point 45 will have the same magnitude as the voltage at point 43 which has been set by potentiometer 2P. Diode 28D is added to match the base to emitter drop of 5Q in the frequency control circuit so that both circuits will start together. Feedback voltage from the DC buss is developed across resistor 14R. The ratio of reference voltage to DC buss voltage is determined by the ratio of 14R to the total resistance of 8R, rheostat 1P, and 14R. This ratio is normally set by adjusting 1P so that 12 volts on the base of 1Q will correspond to 128 volts on the DC buss. The current in transistor 1Q will be proportional to the difference in feedback and reference voltage. This current signal is proportional to the error voltage and will be supplied to the phase control circuits through an emitter follower circuit consisting of transistor 3Q and resistors 46R and 13R. Stablizing is provided by resistor 16R, capacitor 6C, and resistor 13R.

The operation of only one phase control circuit will be covered since these are identical for each of the controlled rectifiers (1SCR, 2SCR, and 3SCR) in the 3Ø

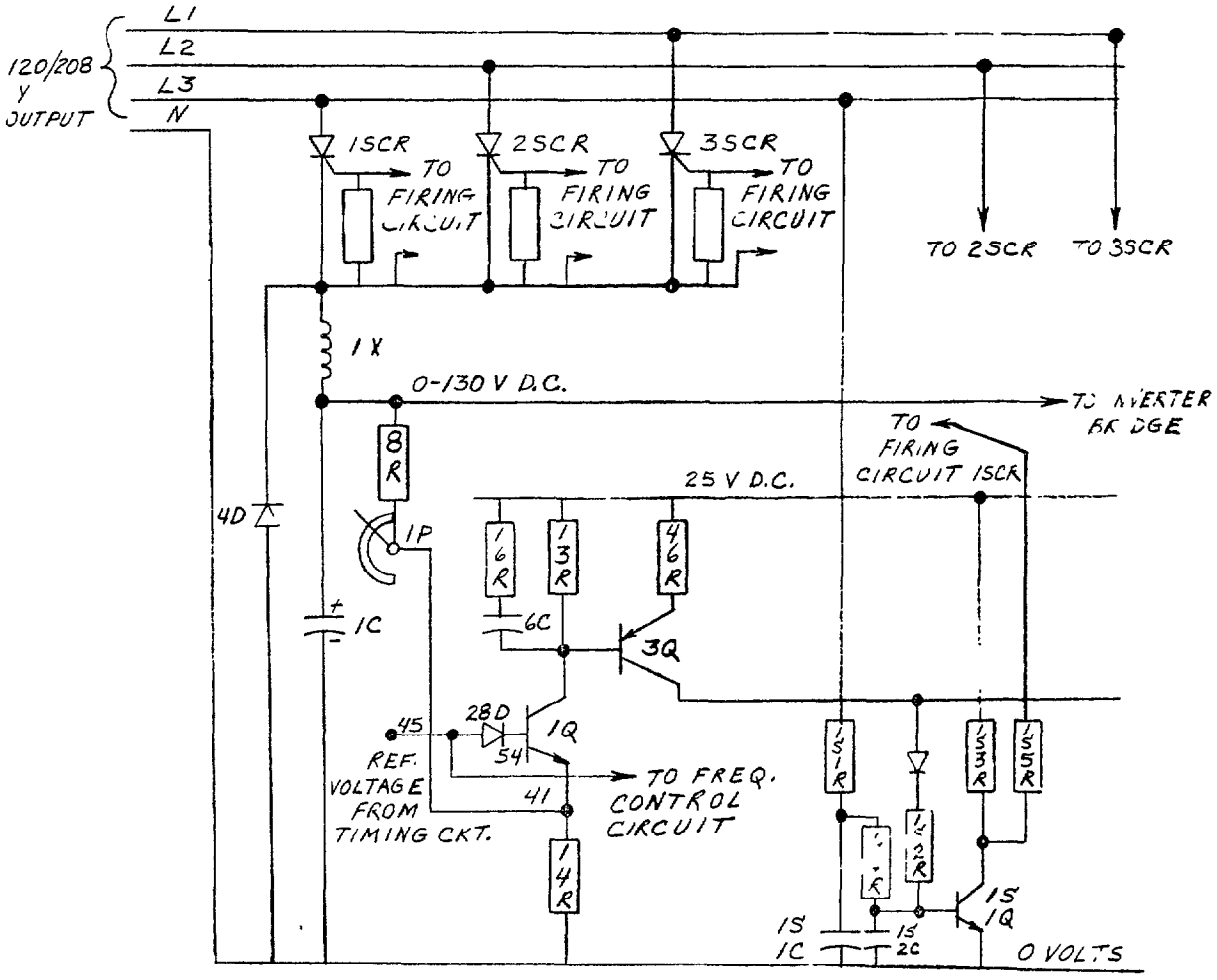

Figure 5. DC Voltage Regulator Circuit

input circuit. Transistor 1S1Q will turn the gating pulses supplied to 1SCR off and on at the proper time during each positive half cycle of the line 1 to neutral voltage. These gating pulses are generated in the firing circuit which will be described later. When transistor 1S1Q turns on, gating pulses will also be turned on. Thus, the point at which 1SCR turns on during each positive half cycle of line to neutral voltage is directly related to the operation of 1S1Q. In order to synchronize the operation of 1S1Q with the line 1 to neutral voltage and provide smooth phase control, a portion of this voltage is shifted approximately 95° leading and supplied to the base. The RC circuit consisting of 1S1R and 1S1C shifts the voltage approximately 5° and the additional 90° shift is provided by 1S4R and 1S2C.

The point that 1S1Q turns on during the half cycle is determined by the amount of current supplied to the base from the voltage regulator circuit. For example, if the reference voltage at point 54 is increased, there will be a proportional increase in current through 1Q and 3Q resulting in more current being supplied to the base of 1S1Q through 1S1D and 1S2R. This increase in current will cause the transistor and 1SCR to turn on earlier in the half cycle increasing the DC buss voltage. A decrease in feedback voltage at point 41 would have the same effect. Of course a decrease in reference voltage or an increase in feedback voltage would have the opposite effect.

The three SCR's will control the current supplied to IC during each positive half cycle of the line 1, 2, and 3 to neutral voltage. Reactor 1X limits the peak current in the capacitor and diode 4D will prevent the SCR cathode voltage from going negative at the low end of the adjustable voltage range and improve the ripple.

FREQUENCY CONTROL CIRCUIT (Figure 6)

Frequency control for the inverter portion of the circuit is provided by the oscillator consisting of 2FL, 20R, 9C, 5Q, 4P, 21R, and 2X. The operation of this oscillator is as follows. Capacitor 9C will charge through 5Q, 4P and 21R until the breakover voltage of 2FL is reached. At this point 2FL will change from the blocking state to a very low impedance conducting state discharging 9C through 20R and 2X. When 9C has discharged, the current in 2X will continue to flow, momentarily reversing the voltage on 9C which causes 2FL to revert back to the blocking state, and the cycle repeats. Each time 2FL conducts, transistor 4Q will turn on causing the voltage at point 74 to drop. The negative going pulses produced at this point are supplied to the ring counter which will be discussed later.

The rate at which pulses occur depends upon the charging current for 9C which is controlled by 5Q. This current is governed by the voltage signal delivered to the

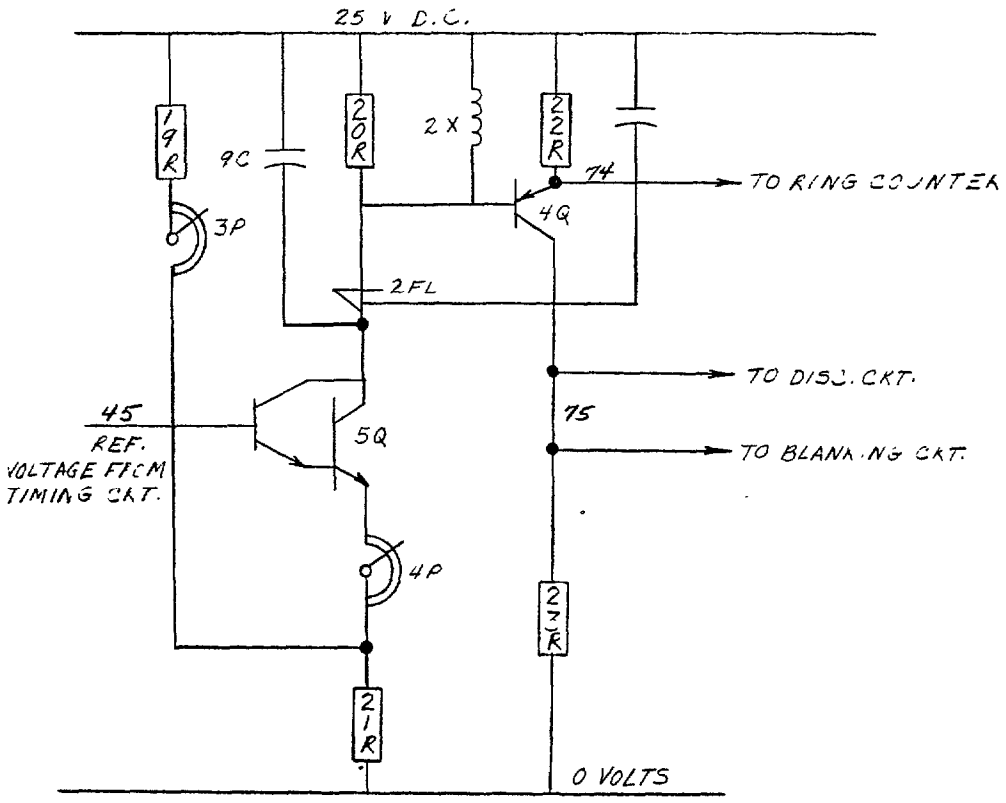

Figure 6. Frequency Control Circuit

base of the darlington amplifier 5Q which converts this voltage signal into a proportional current. The 5Q base voltage signal is in turn obtained from the same basic reference voltage which establishes the level of the DC voltage buss. The charging current for 9C is therefore directly proportional to the DC buss voltage. This provides a constant ratio of volts to frequency as the reference voltage is increased and decreased. Such a constant "volts per hertz" ratio is required in the operation of AC motors.

Rheostat 4P provides a means of adjusting the volts per cycle ratio to match the motor design. Rheostat 3P with 19R is used to boost the voltage at low frequency which is normally required with most AC motors. If the resistance of 3P is reduced the voltage drop across 21R will increase which will in turn reduce the oscillator frequency at the same level of reference voltage. This adjustment is effective mainly at the low frequency end of the constant volts per hertz curve.

FIRING CIRCUIT (Figure 7)

The firing circuits used on ST-100 drives produce a train of steep wave front high energy pulses suitable for firing conventional and inverter type SCR's. Circuit operation will be as follows.

When power is initially applied, current flows from the 47 volt bus through FC2R into the base of transistor FC1Q, thereby causing FC1Q to conduct and to apply voltage to the primary winding of transformer FC1T. Voltage appearing at secondary winding S1 is positive at terminal 3 with respect to terminal 4. This voltage will cause more base current to flow in FC1Q turning it fully on. It can be seen that the connection of secondary winding S1 of FC1T in the circuit is regenerative and causes FC1Q to switch on.

The voltage applied to the primary winding will be the supply voltage minus the voltage across resistor FC1R and the saturated transistor voltage. The voltage across FC1R is caused by the flow of transformer load current and exciting current. With time the voltage across FC1R will increase as exciting current increases. Thus the voltage across the primary winding will decrease, causing a proportional decrease in the voltage developed across secondary S1. Both of these actions are in the direction to eventually cause FC1Q to turn off.

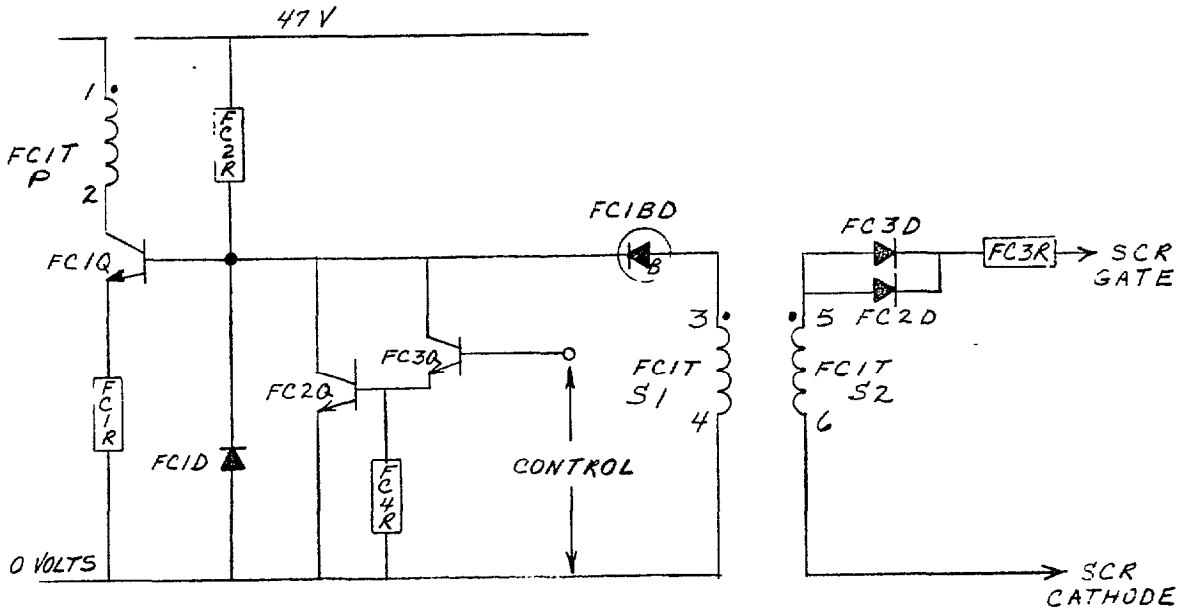

Figure 7. Firing Circuit

Once transistor FC1Q starts to turn off, the process, is regenerative in that direction also. Because of exciting current flowing in the primary winding at the time of turn off, the voltages on all windings will reverse in an attempt to find a path for the ampere turns flowing in the primary. The path is provided by FC1D and FC1BD. The energy trapped in the exciting impedance is eventually delivered at constant voltage (the voltage of zener diode FC1BD) to FC1D and FC1BD. During this time the voltages on all transformer windings are maintained at predetermined values. Also during this time the starting current supplied through FC2R is diverted from the base of FC1Q, thereby providing additional assurance that FC1Q is completely turned off.

After all of the exciting energy has been dissipated, the voltages across all windings go to zero. As a result, the starting current begins to flow through FC2R, into the base of FC1Q and the process starts all over again.

Control of the oscillator is obtained by turning transistors FC2Q and FC3Q on or off. It can be seen that by turning FC2Q and FC3Q on, the feedback path from secondary S1 is shorted out and oscillations will stop even if supply voltage is still present. When transistor FC2Q and FC3Q are turned off, oscillation will start again immediately.

Secondary winding S2 supplies voltage through FC3D, FC2D, and FC3R to the gate of the SCR. Diodes FC2D and FC3D also prevents the gate to cathode of the SCR from being reverse biased when the voltage on winding S2 reverses.

BLANKING CIRCUIT (Figure 8)

The firing pulses supplied to the gates of the six SCR's in the output bridge, will be blanked out for a short period of time following each pulse of the frequency control oscillator. The purpose of this blanking period will be explained in the discussion on operation of the commutation circuit.

Operation of the blanking ciruit is initiated by a voltage pulse from the oscillator at point 75 and supplied to the base of 6Q through 24R, 17D, and 25R. Prior to a pulse from the oscillator, 7Q will be biased on by current through resistor 26R. When voltage is supplied to the base of 6Q it will turn on, thus turning 7Q off. The time period, after each pulse from the oscillator that 6Q remains on and 7Q is held off, will be determined by the values of 10C, 25R, and 60R. This time will be approximately 90 microseconds. While 7Q is off, current will be supplied to the firing circuit control transistors turning off the firing pulses to all SCR's in the output bridge. This current is supplied from the control voltage buss through 27R and 4S1R - 9S1R.

GATING CIRCUIT FOR COMMUTATION SCR'S (Figure 9)

This circuit will supply turn-on pulses alternately at 60° intervals, to commutating SCR's 10SCR and 11SCR. It is

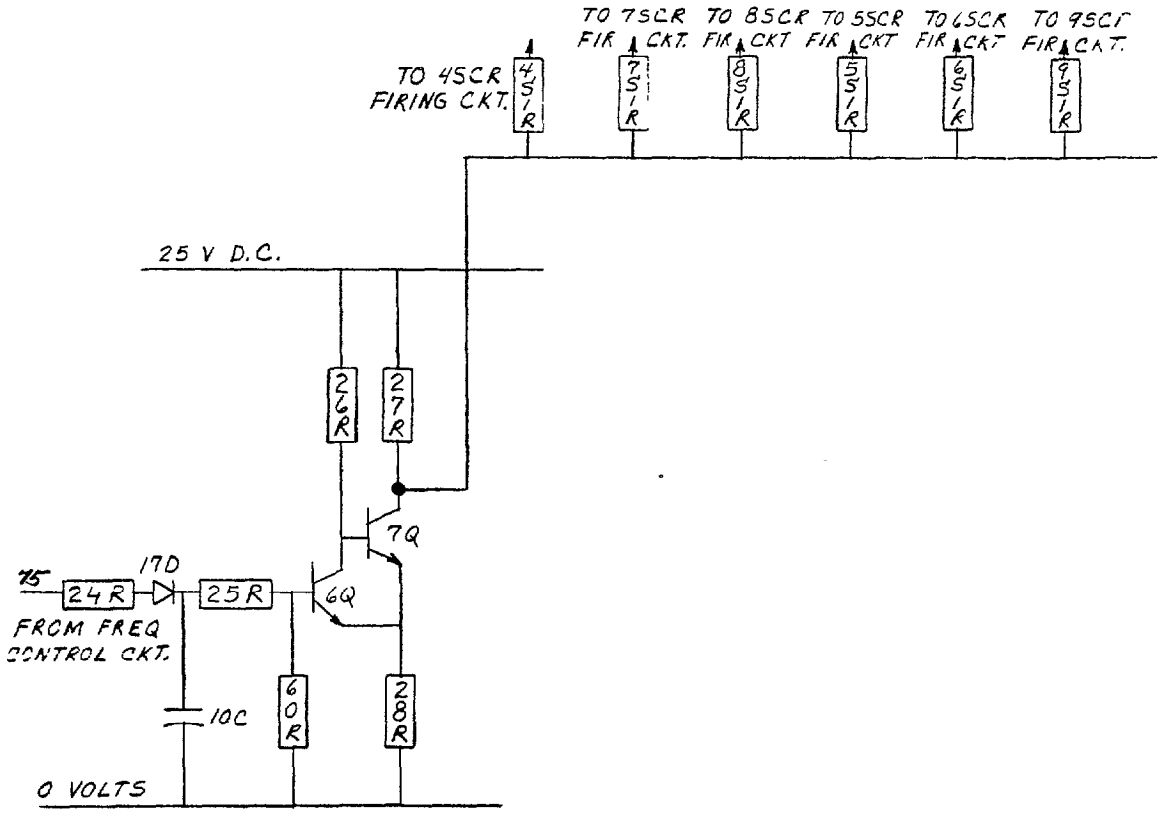

Figure 8. Blanking Circuit

necessary to coordinate the firing of the commutating SCR's with the gating signals supplied to the inverter bridge SCR's. This coordination is provided by the ring counter circuit.

You will note that capacitors 12C and 14C are each connected through a diode and resistor to the collectors of three transistors in the ring counter. The relationships between ring counter collectors and gating pulses at points 31 and 32 are shown graphically in figure 10. It can be seen that there will always be one or two conducting collectors in each group. Also, in each group the number of conducting collectors will alternate at 60° intervals between one conducting and two conducting. In addition, when the number of conducting collectors goes from one to two in the first group, the second group will go from two to one.

Normally 8Q and 11Q are conducting and 9Q and 10Q are non-conducting. When the group of ring counter transistors connected to 12C change from one conducting to two conducting, point 82 will receive a negative increment of voltage. This will cause 8Q to turn off and 9Q to turn on delivering a pulse to the gate of 11SCR. The pulse width is limited by means of the current through 30R which quickly restores the voltage of the right hand side of 12C to its original, slightly positive, level turning 8Q on and 9Q off. The next 60° transition point will cause 10Q to deliver a pulse to the gate of 10SCR. These gating pulses will alternate between the two commutating SCR's every 60° as shown in figure 10.

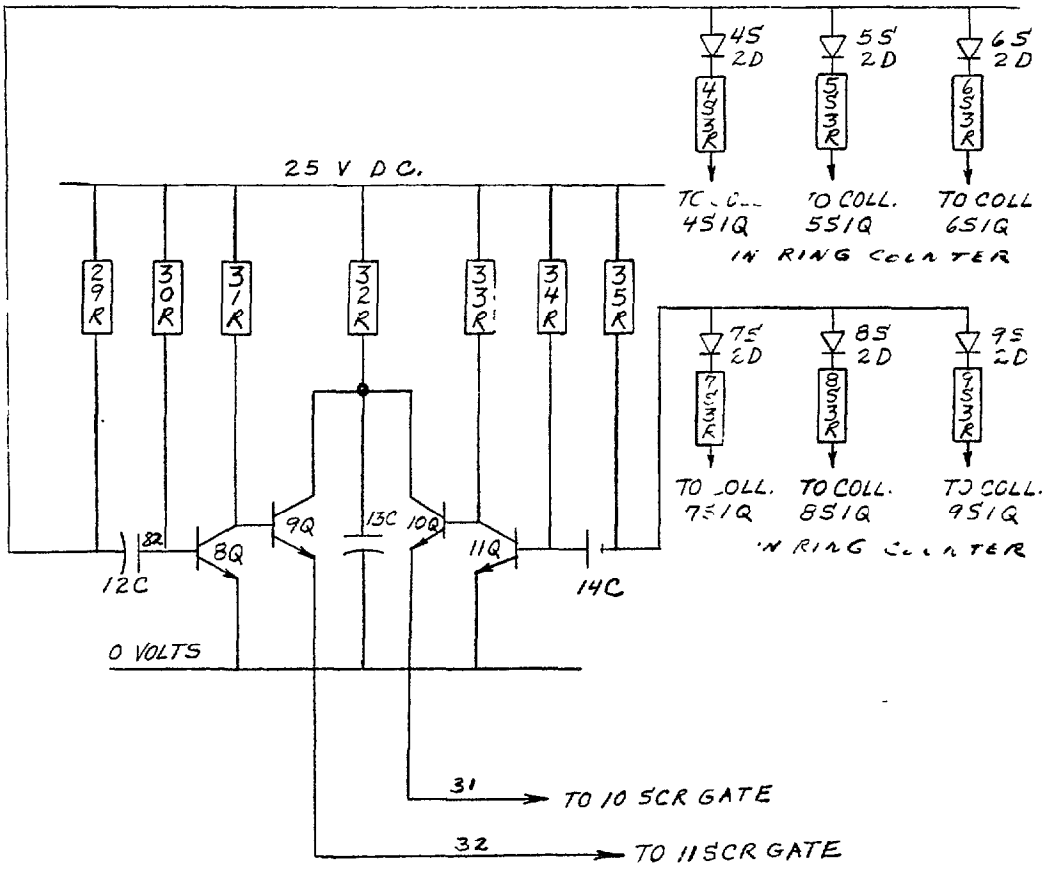

Figure 9. Gating Circuit For Commutation SCR's

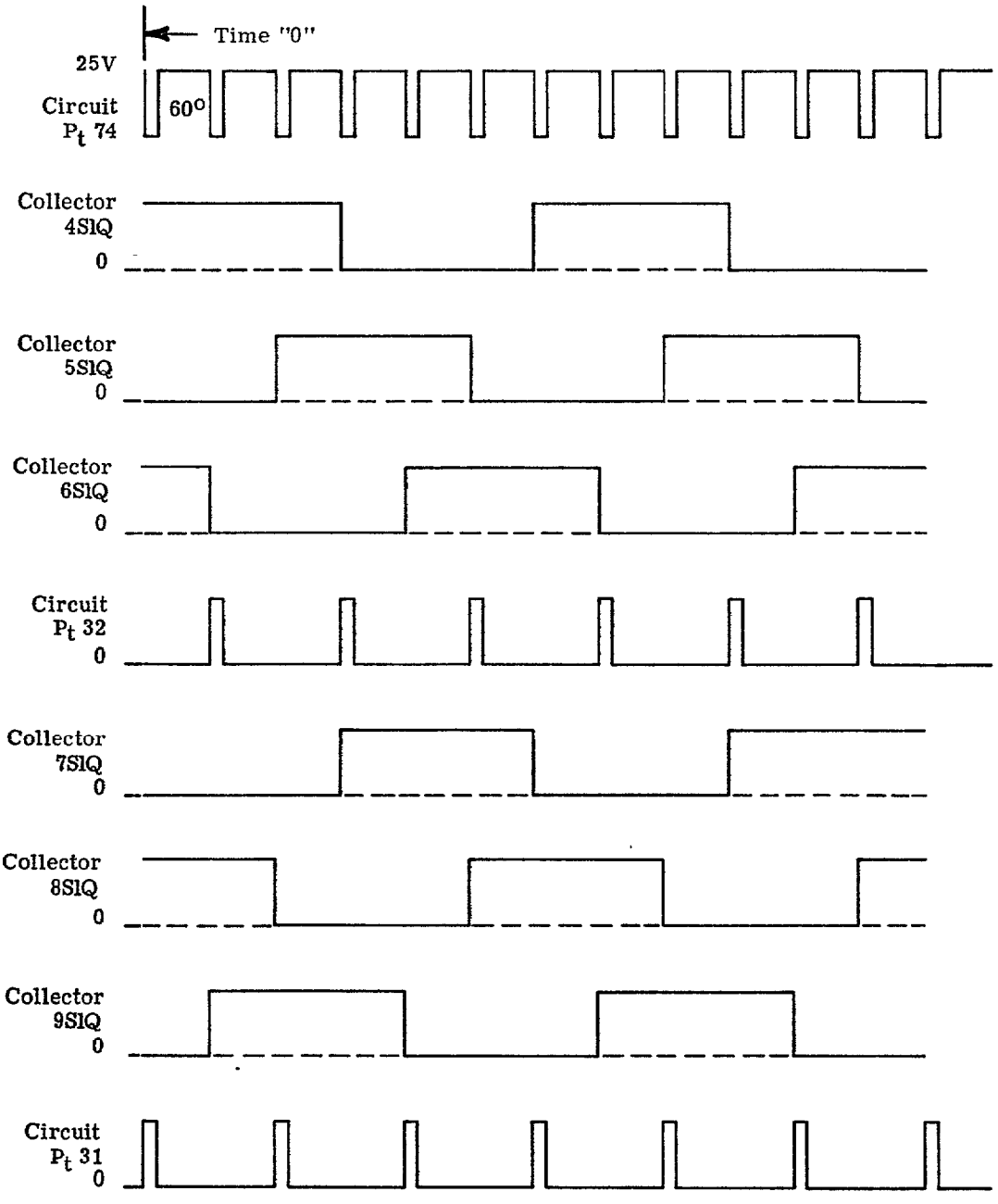

Figure 10. Voltage-Time Relationships

RING COUNTER CIRCUIT (Figure 11)

The ring counter consists of three triggered flip-flops steered from one to another in such a way that successive trigger pulses at circuit point 74 causes the counter to advance from one condition to the next. Steering is such that only six of the eight possible combinations of the flip-flops are used. When each trigger pulse is received, only one of the flip-flops changes state and changes the steering such that when the next pulse is received, another of the flip-flops will change state.

Receipt of six pulses brings the counter back to its starting condition. Trigger pulses arrive every 60° of the desired inverter operating frequency. Components 14D, 26D, 27D, 37R, and 38R are used to prevent the counter from starting in either of the two unwanted combinations. The following table shows the sequence of operation of the six collectors in which a logic 0 designation is applied to a conducting transistor and a logic 1 is applied to a non-conducting transistor. This same relationship is shown graphically in figure 10.

TABLE 1

	TIME	4S1Q	7S1Q	8S1Q	5S1Q	6S1Q	9S1Q
START	0	1	0	1	0	1	0
	60°	1	0	1	0	0	1
	120°	1	0	0	1	0	1
	180°	0	1	0	1	0	1
	240°	0	1	0	1	1	0
	300°	0	1	1	0	1	0
REPEAT	360°	1	0	1	0	1	0

The collectors of the ring counter transistors control the gating signals to the inverter SCR's. Each transistor collector controls one of the SCR's such that when the transistor is conducting, it permits the blocking oscillator firing circuit to supply gating pulses to the SCR it controls.

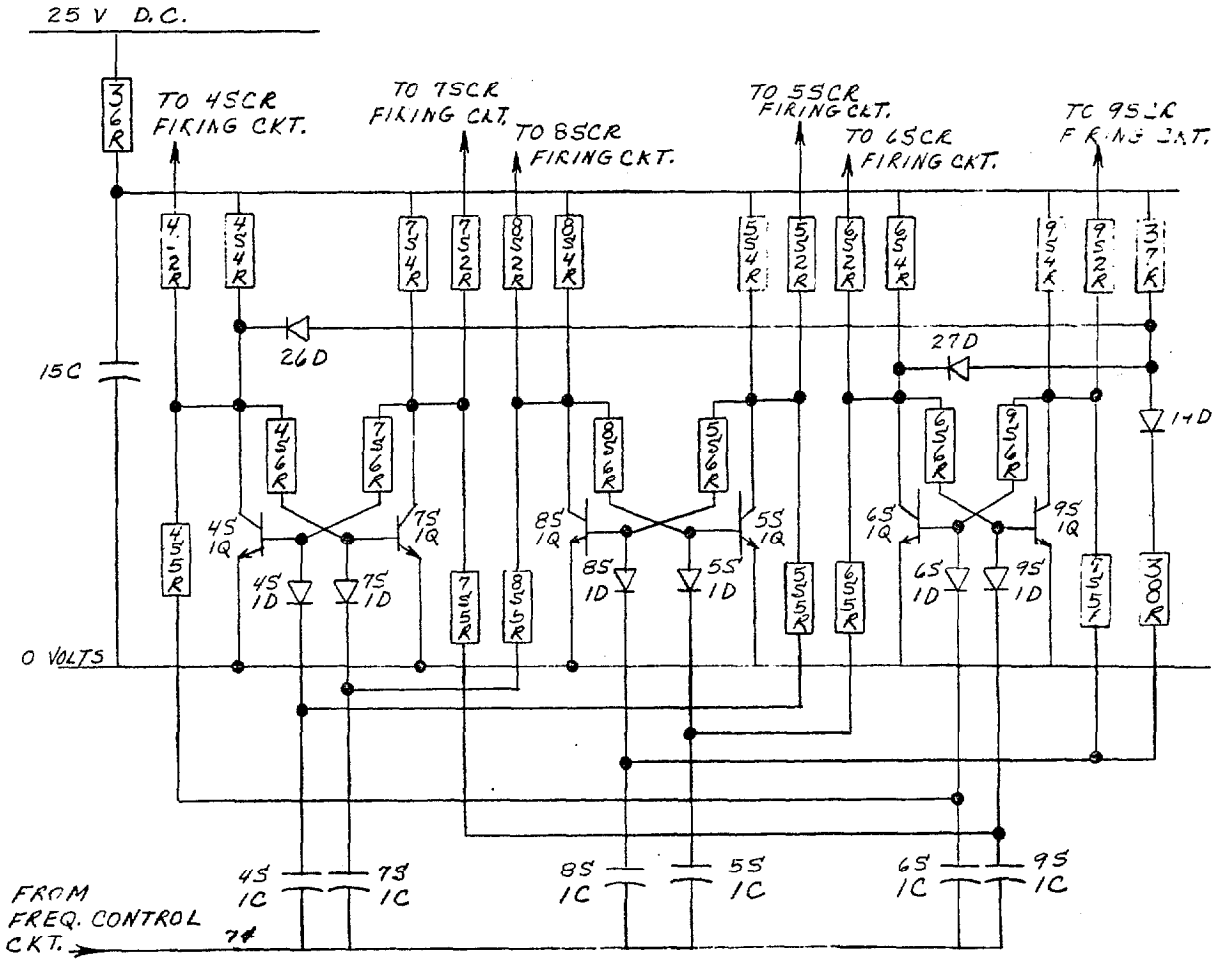

Figure 11. Ring Counter Circuit

INVERTER BRIDGE (Figure 12)

The output power circuit consisting of SCR's 4SCR, 5SCR, 6SCR, 7SCR, 8SCR, and 9SCR, diodes 18D, 19D, 20D, 21D, 22D, and 23D, and secondary windings of commutating transformers 2T and 3T is a three phase inverter bridge operating from an adjustable DC voltage. Power diodes 18D through 23D are connected in inverse parallel with each SCR and make it possible for the inverter to supply lagging loads by providing paths for reverse current flow. Each of the bridge SCR's is operated in synchronism and in phase with its controlling transistor in the ring counter circuit. The following table shows the sequence of SCR operation. It can be seen that this table is consistant with table 1 showing the sequence of transistor operation in the ring counter circuit.

TABLE 2

TIME	4SCR	5SCR	6SCR	7SCR	8SCR	9SCR	TOP ROW	BOTTOM ROW
0	OFF	ON	OFF	ON	OFF	ON	1	2
60°	OFF	ON	ON	ON	OFF	OFF	2	1
120°	OFF	OFF	ON	ON	ON	OFF	1	2
180°	ON	OFF	ON	OFF	ON	OFF	2	1
240°	ON	OFF	OFF	OFF	ON	ON	1	2
300°	ON	ON	OFF	OFF	OFF	ON	2	1
360°	OFF	ON	OFF	ON	OFF	ON	1	2

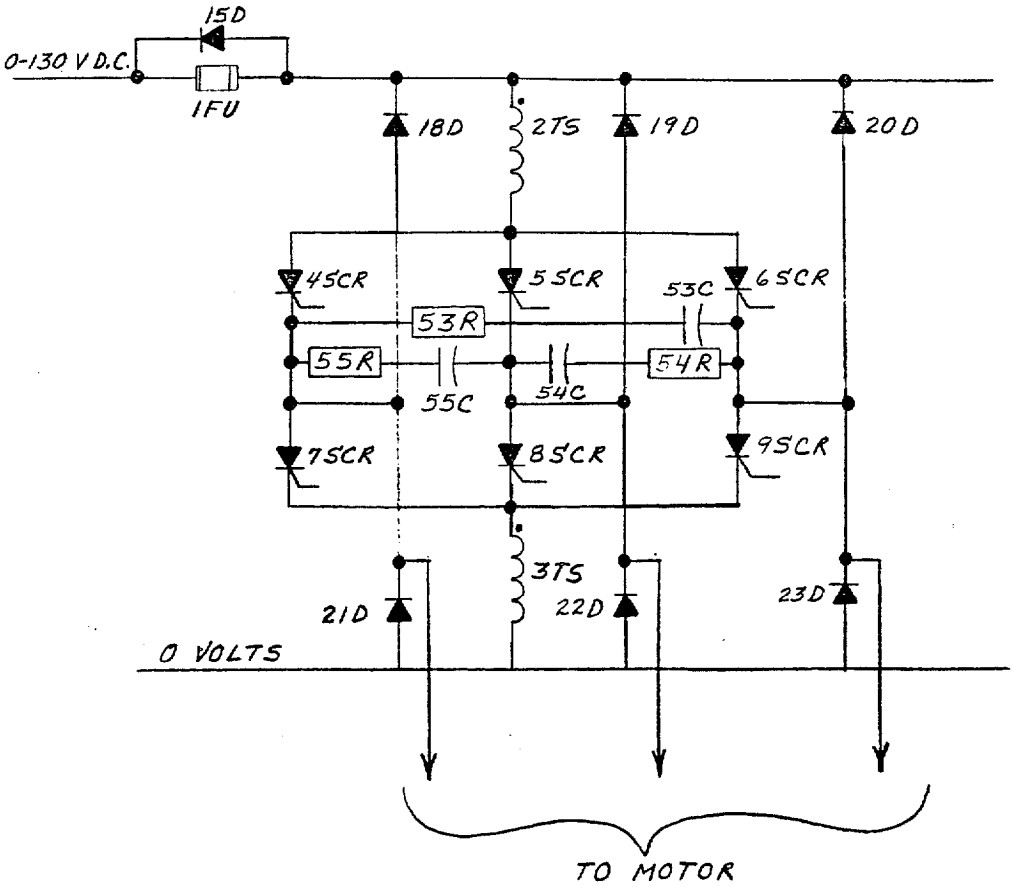

Figure 12. Inverter Bridge

Also shown in Table 2 is the number of SCR's that are conducting at any one time in the top and bottom rows of SCR's. It will be noted that the total number of SCR's conducting at any one time is three and that these SCR's are always so distributed that there are two conducting in one row and one conducting in the other row. The "two-on" condition alternates between the bottom and top rows at successive switching points.

In addition, at each switching point, only one SCR is required to change for conducting to non-conducting and only one from non-conducting to conducting. Also, the SCR that goes from conducting to non-conducting is always one of the two in the same row that have been conducting. Therefore, it is not necessary to turn off all SCR's that are conducting in order to be sure to turn off the one that is actually required to turn off.

It will be necessary to turn off only that row in which two SCR's happen to be conducting. This is accomplished by applying a commutation pulse to only one row of SCR's at one switching point and to the other row of SCR's at the next switching point and so on. These pulses are coordinated with the gating sequence of the SCR's by the ring counter.

The output line to line voltage will be a "quasi-square" wave having a voltage-time relationship as shown in figure 13. Such a wave has no harmonic voltage below the fifth. The R. M. S. fundamental component (superimposed) will be 0.78 times the peak which is determined by the adjustable DC voltage supplied to the inverter.

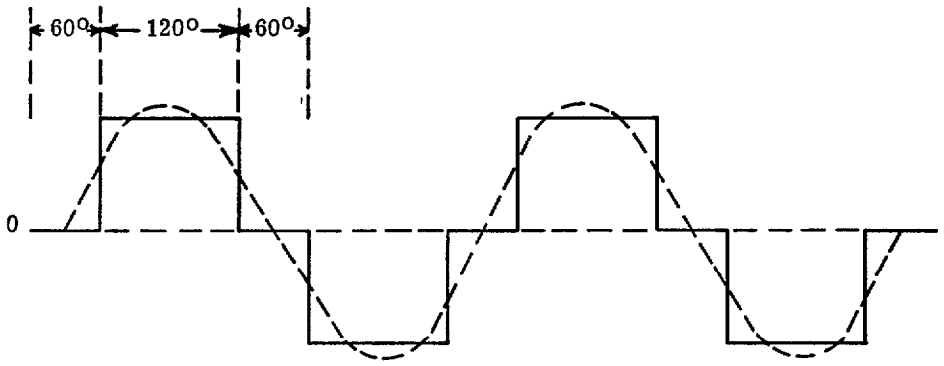

Figure 13. Inverter Output Line to Line Voltage

COMMUTATION CIRCUIT (Figure 14)

Diodes 1D, 2D, and 3D supply current directly from the line through current limiting resistor 48R to charge capacitor 16C. The voltage across 16C will have a magnitude nearly equal to the peak of the input AC voltage. This provides a fixed DC voltage to supply the commutating circuit which consists of 4T, 24D, 2T, 3T, 17C, 25D, 10SCR, and 11SCR. During a typical commutation cycle current will flow through reactor 4T and diode 24D to charge capacitor 17C. With no charge on 17C at the beginning of the charge cycle, the full 150 volts will initially appear across reactor 4T. When capacitor 17C is charged up to 150 volts, the energy stored in reactor 4T will keep the current flowing until the capacitor is charged to approximately 300 volts. Diode 24D prevents the capacitor from discharging back through the reactor.

Capacitor 17C will be discharged through either transformer 2TP and 10SCR or transformer 3TP and 11SCR. You will note in the inverter bridge circuit that secondary windings 2TS connects the top row of SCR's to the top buss and 3TS connects the bottom row of SCR's to the bottom buss. Gating on 10SCR will cause a positive voltage to appear at the dottend ends of the primary and secondary windings of transformer 2T and a negative voltage at the undotted ends. This voltage on winding 2TS will put a reverse voltage on the top row of SCR's. The magnitude of reverse voltage will be 300 volts minus the adjustable DC bus voltage.

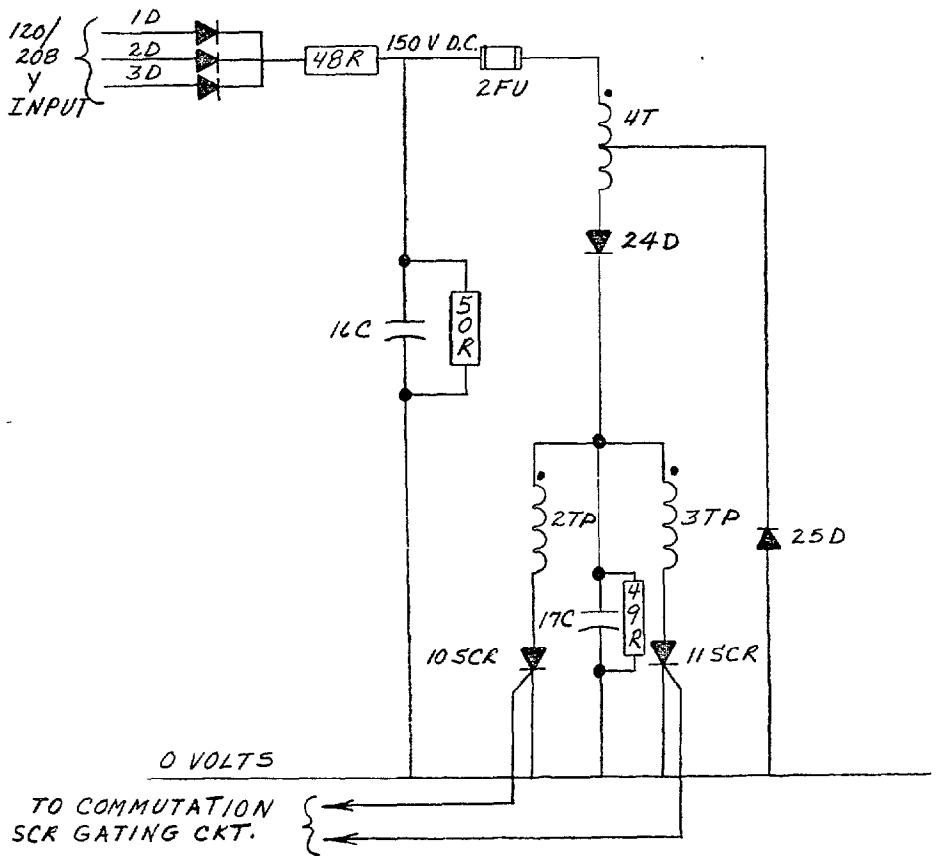

Figure 14. Commutation Circuit

When 11SCR is gated on, the same magnitude of reverse voltage will appear across the bottom row of SCR's. The required sequence for gating on commutation SCR's is given in the description of the inverter bridge circuit.

When commutation is initiated, the load current flowing in secondary winding 2TS is transferred to primary winding 2TP. This initial current in 2TP is replaced by the flow of discharge current from capacitor 17C. As the voltage across 17C decreases, the voltages across windings 2TP and 2TS decrease accordingly. At some point the anode to cathode voltage on the top row of SCR's will become positive again. If gating is withheld from these SCR's at this time, they will not conduct and current will not flow in winding 2TS.

When the voltage across capacitor 17C reaches zero, the voltage across winding 2TP will reverse and charge 17C in the negative direction. This reverse charge on capacitor 17C turns off 10SCR.

Diode 25D limits the negative voltage on 17C to the voltage level at the top of reactor 4T and pumps the excess energy back into the supply. For diode 25D to be effective in returning energy to the supply, it is necessary to prevent the top row of SCR's from being gated on immediately after commutation. This function is provided by the blanking circuit.

When the energy in winding 2TP is exhausted, the current will go to zero and the recharge cycle starts over again. Gating on 11SCR will initiate the next commutation cycle.

COMMUNICATION AND CONTROL DEVICES DEPARTMENT

10-70(100)

GENERAL ELECTRIC

WAYNESBORO, VA.

SUPPLEMENT FOR GEK-14751

ST-100* ADJUSTABLE FREQUENCY AC DRIVE

3S7506FV300 to 3S7506FV319

Voltage Waveforms

The oscilloscope pictures 1 through 18 show typical voltage waveforms found at different circuit points in the power unit. This section will supplement the theory of operation and should be helpful in the maintenance and trouble-shooting of ST-100 drives.

A brief description of the voltages shown in each picture will follow.

1. The top trace shows the line one to neutral voltage and the bottom trace shows the firing pulses supplied to 1SCR. The position of the firing pulses with respect to the AC wave, are such that 1SCR does not fire during the positive half cycle of the line one to neutral voltage.

2. This picture is of the same voltages but with the leading edge of the firing pulse envelope advanced to a firing angle greater than 90°. 1SCR will fire at this point during the positive half cycle of the line one to neutral voltage.

3. The rectified voltage supplied to the DC bus is shown in this picture. At low speed the rectified voltage wave will be clipped at slightly below zero by diode 4D. When the SCR turns off, the voltage at the cathode will immediately jump to the DC bus level.

4. This picture shows the same rectified voltage wave at high speed. The firing angle has increased and the DC bus level is high enough to prevent clipping by diode 4D.

5. The bottom trace shows the phase shifted AC voltage used to synchronize the firing of the SCR with the AC line voltage and to provide smooth phase control. The point at which the phase shifted voltage crosses the zero line is the point that firing pulses are supplied to the SCR.

6. This picture shows the same phase shifted voltage at maximum speed, with the cross over point advanced to increase the firing angle.

7. The negative pulses from the internal oscillator are shown at circuit point 74 with respect to 100. The pulses are used to trigger the ring counter.

8. The voltage waveshape shown here will appear across any transistor (collector to 100) in the three flip-flops of the ring counter. The frequency will be equal to the output frequency.

9. This picture shows the relationship of the oscillator pulses to the voltage across a ring counter transistor. It can be seen that for every cycle of the ring counter voltage, there will be six pulses from the oscillator.

10. The transistor collector voltages of two ajacent flip-flops in the ring counter shows the 120° phase shift necessary to provide the proper switching sequence for SCR's in the inverter bridge.

11. This picture shows the firing pulse envelop supplied to the inverter bridge SCR's. The firing pulses are blanked out for a short period of time at each 60° switching point.

12. The amplitude and duration of a single firing pulse is shown. Also, note the very short rise time of the pulse which is desirable for firing inverter SCR's.

13. The firing pulses are blanked out for the length of time that the voltage at circuit point 81 is positive. This blanking time will be approximately 90 μ seconds as shown in the picture.

14. This picture shows the firing pulses for the two commutation SCR's. Note how the pulses alternate at each 60° switching point.

15. The commutation time can be measured by putting the adjustable DC bus voltage, circuit 13 to 100, on the top trace and the commutation voltage, circuit 16 to 100, on the bottom trace. The length of time the commutation pulse is above the DC bus voltage will be the commutation time.

16. The voltage across any SCR in the inverter bridge will be a square wave as shown in this picture.

17. This is the waveform of the output line to line voltage supplied to the motor.

18. When a commutating SCR fires, the capacitor voltage suddenly drops to a negative value and then slowly increases to the original positive level. If an SCR or diode in the inverter bridge is shorted, this waveshape will be distorted.

CWS
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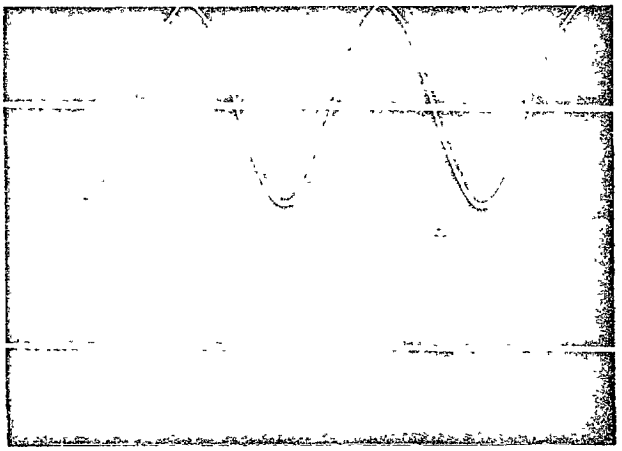
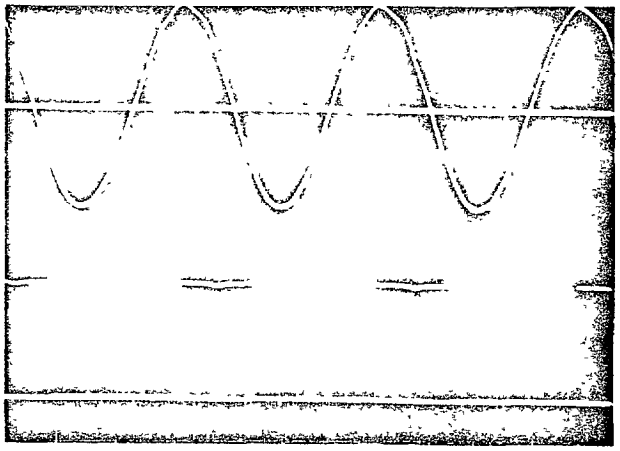
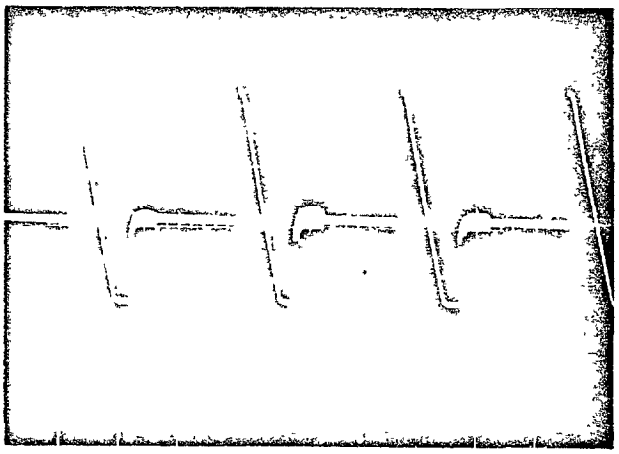


1. TOP TRACE: LINE 1-
100 V/DIV.
BOTTOM TRACE: ACROSS IFC1R,
5V/DIV., 5 MSEC/DIV.
ZERO SPEED



2. SAME AS #1 AT MAXIMUM SPEED.



3. CATHODE OF ISCR SPEED
20 HZ, 20V/DIV.,
2 MSEC/DIV.

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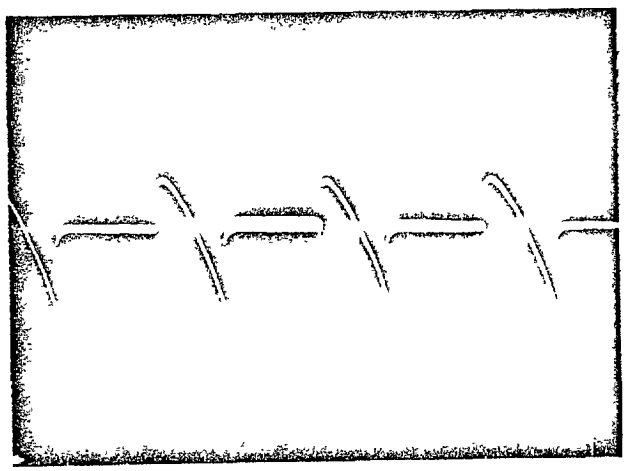
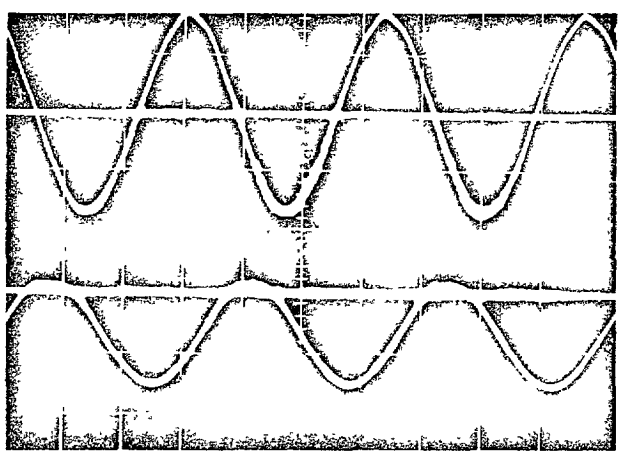
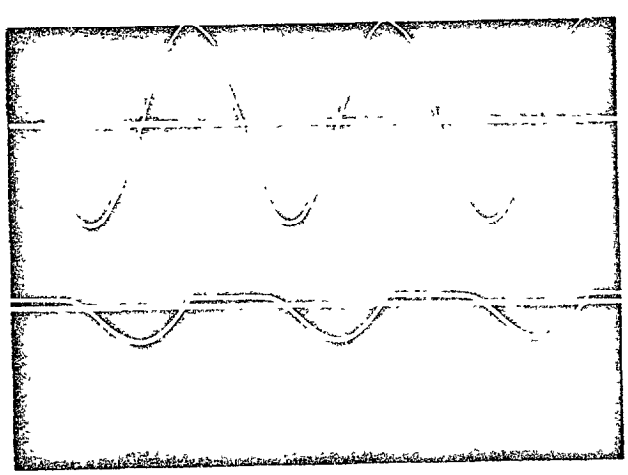


4. SAME AS #3
SPEED - 120 HZ.



5. TOP TRACE: LINE 1
100V/DIV.
BOTTOM TRACE: IS2C
5V/DIV., 5 MSEC/DIV.
ZERO SPEED



6. SAME AS ABOVE, MAXIMUM SPEED.

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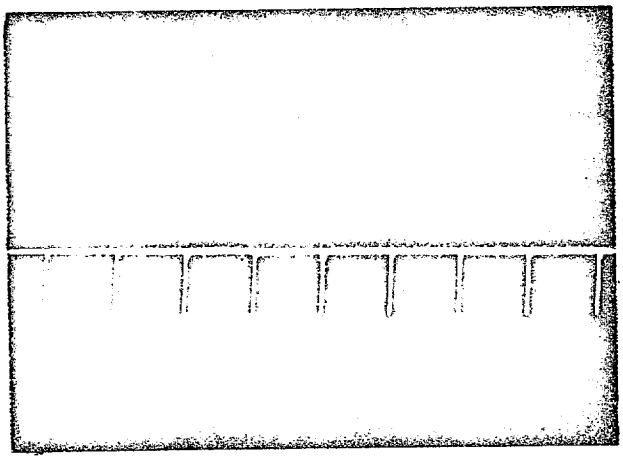
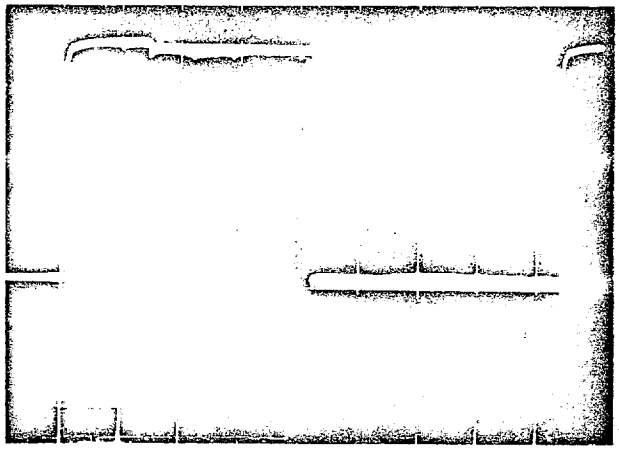
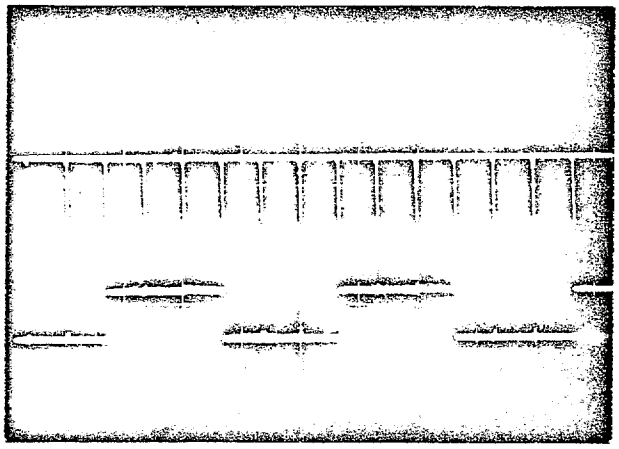


7. POINT 74
MAXIMUM SPEED
5V/DIV., 1 MESC/DIV.



8. COLLECTOR OF RING
COUNTER SPEED - 120 HZ
5V/DIV., 1 MSEC/DIV.



9. TOP TRACE: POINT 74 5V/DIV., 5 MSEC/DIV.: COLLECTOR OF RING COUNTER - 20V/DIV. BOTTOM TRACE

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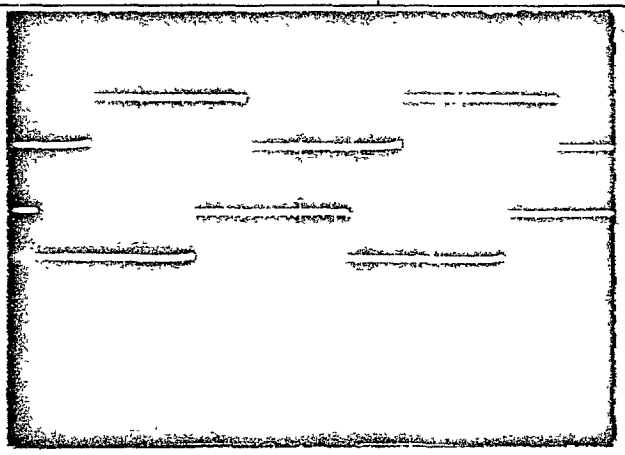
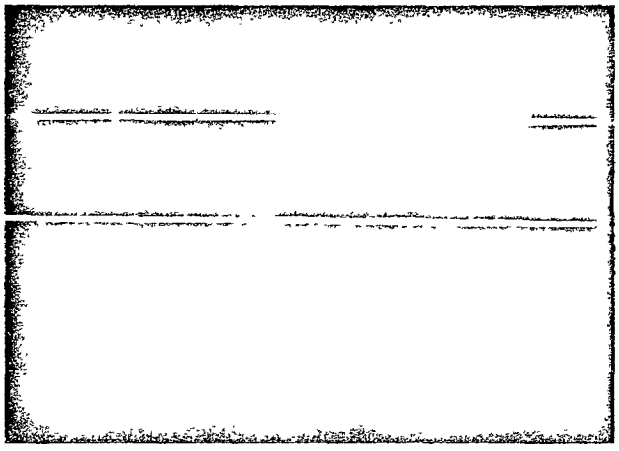
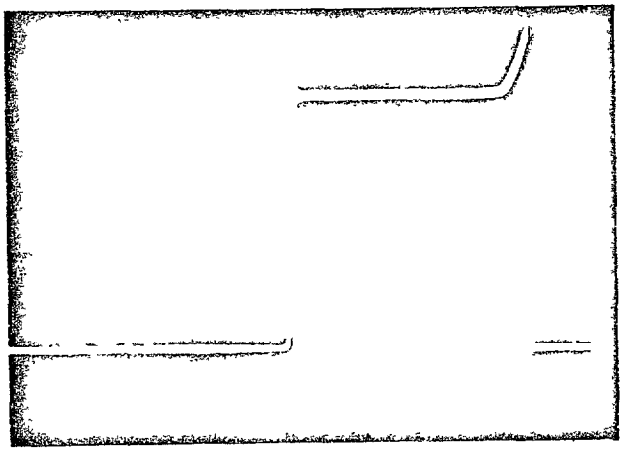


10. TOP TRACE: 4S IQ COLLECTOR
BOTTOM TRACE: 8S IQ COLLECTOR, 20V/DIV., 5MSEC/DIV.



11. VOLTAGE ACROSS FC1R, ANY INVERTER FIRING CIRCUIT - 5V/DIV., 1MSEC/DIV.



12. SINGLE FIRING PULSE. ACROSS ANY FC1R 2V/DIV. 5 μSEC./DIV.

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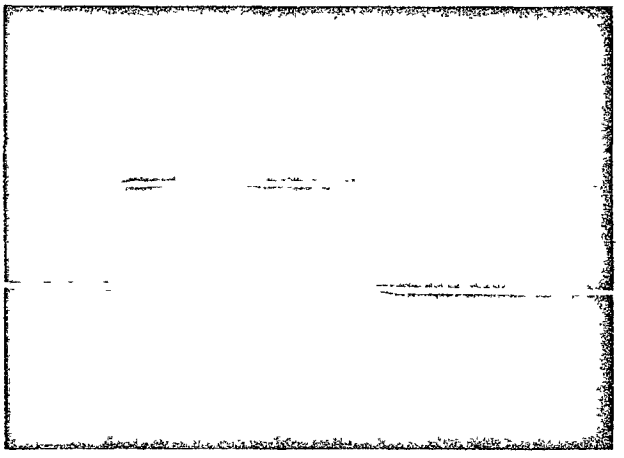
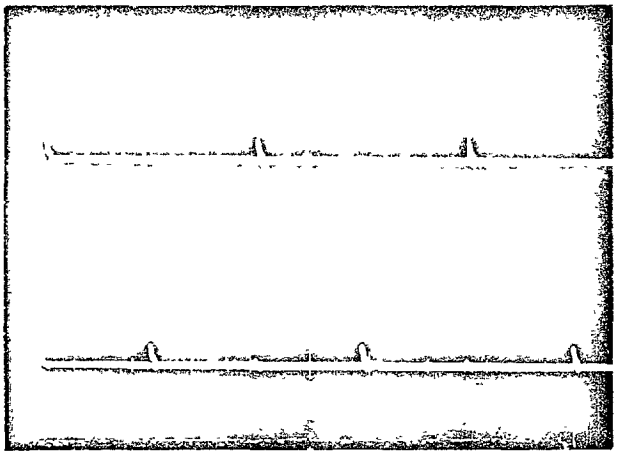
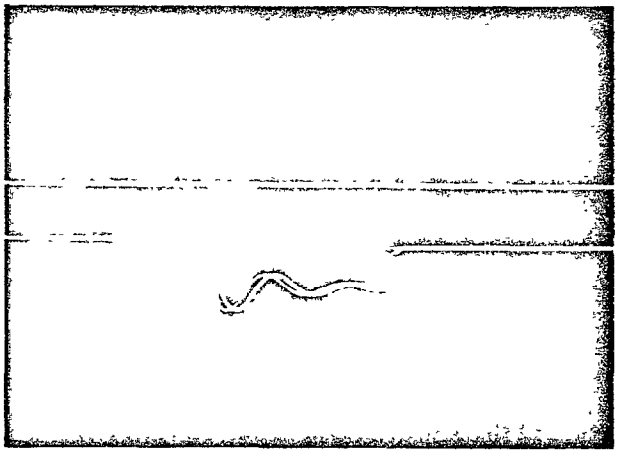


13. CIRCUIT 81 (BLANKING PULSE) 1V/DIV., 20 μ SEC/DIV.



14. TOP TRACE: CIRCUIT 31
BOTTOM TRACE: CKT. 32
1V/DIV., 1 MSEC/DIV.



15. COMMUTATION TIME REFERENCE TRACE: INVERTER BUS.
BOTTOM TRACE: 7 SCR CATHODE. 100V/DIV.
20 μ SEC/DIV.

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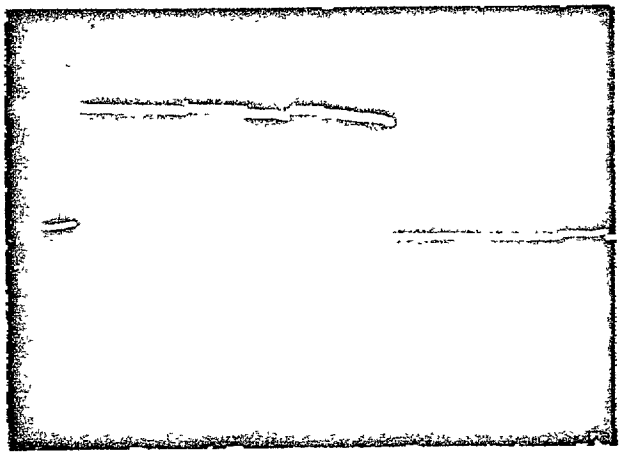
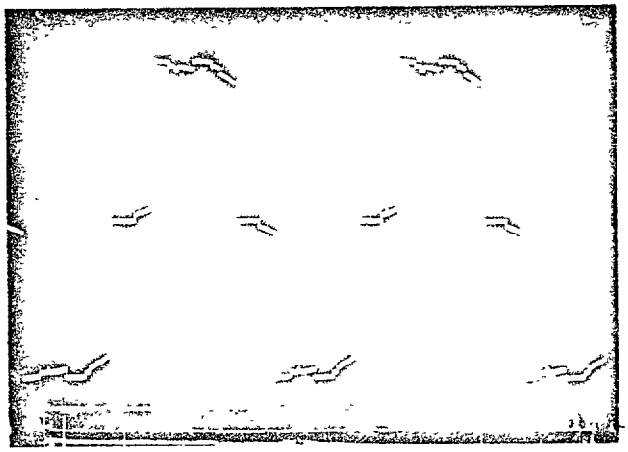
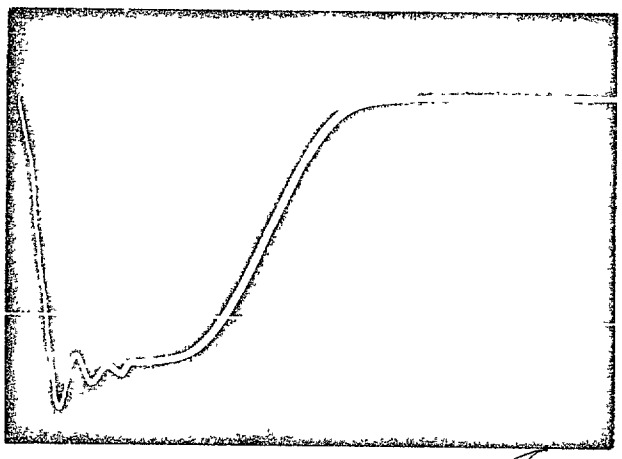


16. ACROSS ANY BRIDGE SCR, SPEED, 90 HZ
1 MSEC/DIV., 20V/DIV.



17. CIRCUIT 151 TO CIRCUIT 152 (OUTPUT TO MOTOR) SPEED 120 HZ.
2 MSEC/DIV., 50V/DIV.



18. ACROSS COMMUTATING CAPACITOR 100V/DIV.
50 μ SEC/DIV.

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