

# *INSTRUCTIONS*

GEK-86638D

TLS1000

## MODULAR RELAY SYSTEM EQUIPMENT INSTRUCTIONS



GENERAL ELECTRIC

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(Front Cover Photo 8043772)

## MODULAR RELAY SYSTEM

## TLS1000

#### INTRODUCTION

The TLS1000 is a comprehensive relaying system for transmission-line protection.

The system is packaged in two four-rack-unit (4 RU) modular cases containing insertable printed-circuit boards, the input magnetics for potential and current, and the high- current output relays. Multi-conductor cables are used to interconnect the two cases.

The TLS relays described in this book include those models that are designed for use in a single zone, two zones, or three zones of protection schemes.

Zones of Protection	Tripping Functions
1	M1/MG1 or MT/MTG
2	M1/MG1 and MT/MTG
3	M1/MG1, M2/MG2 and MT/MTG

Refer to the module location diagrams (Figures 16 and 17) to determine the number and type of tripping functions available in any model of TLS relay.

The TLS system may be set by the user for any of the following relaying schemes.

- 1. Stepped distance
- 2. Zone acceleration
- 3. Permissive overreaching transfer trip
- 4. Permissive underreaching transfer trip
- 5. Directional comparison blocking
- 6. Hybrid tripping

All of the above schemes, except for the stepped-distance scheme, are pilot relaying schemes, and require a communication channel. When a pilot scheme is used, the stepped-distance scheme may also be used to provide backup protection. The directional-comparison-blocking and hybrid-tripping schemes require the addition of the optional blocking units (MB, NB).

These instructions do not purport to cover all details or variations in equipment nor provide for every possible contingency to be met in connection with installation, operation or maintenance. Should further information be desired or should particular problems arise which are not covered sufficiently for the purchaser's purposes, the matter should be referred to the General Electric Company.

To the extent required the products described herein meet applicable ANSI, IEEE and NEMA standards; but no such assurance is given with respect to local codes and ordinances because they vary greatly.

The TLS systems also include other standard features that may be selected by the user, such as:

- 1. Out-of-step blocking
- 2. Switched zone 1 reach
- 3. Fault-detector supervision of the trip bus
- 4. Line pickup (close onto fault) protection
- 5. PT fuse-failure alarm
- 6. Sequential reclosing control
- 7. Channel repeat (echo)
- 8. Weak-infeed tripping
- 9. Direct transfer trip

The various relaying schemes and features are discussed in detail in GE publication GEK-86659, TLS MODULAR RELAY SYSTEM - SCHEME DESCRIPTION. Note that all of these features are not compatible with every scheme. For example, the channel repeat, weak-infeed trip, and direct transfer trip cannot be used with the directional-comparison-blocking scheme.

#### APPLICATION

#### GENERAL

The TLS1000 relay system has been designed so that it may be applied in a broad range of systems without compromising performance or reliability. The TLS system is suitable for use on uncompensated transmission lines, on lines adjacent to seriescompensated lines, and on series-compensated lines. The TLS system may be applied on lines ranging from 2 to 700 kilometers in length. In general, the problems associated with short-line applications are quite different from those associated with long lines (particularly long lines with large-load transfer). Flexibility has been designed into the TLS system to permit relay settings that will achieve maximum performance for each application in terms of speed, security and dependability.

The TLS system is available for both single-pole-tripping and three-pole-tripping applications.

#### OTHER PUBLICATIONS

Because the TLS can be applied in numerous relaying schemes, each requiring different relay settings, two separate publications are available to assist in applying the TLS relay. Refer to GE instruction books **GEK-86659**, TLS **MODULAR RELAY SYSTEM - SCHEME DESCRIPTION**, and **GEK-86668**, TLS **MODULAR RELAY SYSTEM - APPLICATION AND SETTINGS GUIDE**, for further information.

#### RELAY CHARACTERISTICS

The tripping functions in the TLS1000 system are of the variable mho type, developed by multi-input phase-angle comparators. The TLS1000 employs three phase- and three ground-tripping functions per zone of protection. The signals used to derive these characteristics are as follows:

#### PHASE RELAYS (M1, M2, MT)

Operating Signal: Iøø ZR1 - Vøø

No.1:  $(V \phi \phi_1 - I \phi \phi Z' R_1)^M$ Polarizing Signals No.2: IØØZR1  $\phi\phi$  = AB, BC, or CA where: = Positive sequence 1 = Memory Μ  $Z_R = Relay reach$ Z'R = Offset reachGROUND RELAYS (MG1. MG2. MTG)  $(I\phi - I_0)Z_{R1} + K_0I_0Z_{R0} - V\phi_q$ Operating Signal: No.1:  $(V \phi_1 - I \phi Z' R_1)^M$ Polarizing Signals: No.2: Iø2ZR1 No.3: IØZR1

where: Ø = A, B, or C 0 = zero sequence 2 = negative sequence g = ground K0 = zero-sequence-current compensation factor

The phase- and the ground-tripping functions also include the following additional features:

- 1. Zero suppression at the comparator inputs
- 2. Adjustable phase shift in the polarizing circuits
- 3. Characteristic timer pickup angle adjustment
- 4. Adjustable level detector in the operate circuits

In addition, the phase functions also have an optional zero-sequence current restraint for use in single-pole-tripping applications.

#### BLOCKING RELAYS (MB, NB)

The TLS1000 system includes optional blocking functions. These blocking functions are required in all blocking and hybrid tripping schemes.

The first blocking function, MB, is a variation of a positive-sequence polarized mho ground-distance function. Three of these functions are used, one for each phase. The following signals are used to derive this function:

Operating Signal:  $-I \not o ZR1 - K_I I \not o ZR0 - V \not o g + K_V (V \not o 1 - I \not o 1 Z'R1)^M$ Polarizing Signal:  $(V \not o 1 - I \not o 1 Z'R1)^M$ where:  $K_I$  = zero-sequence current-compensation factor  $K_V$  = setting from 0 to 0.45

These blocking functions are designed to operate for all fault types; however, they may be slow in operating for some phase-to-phase faults. To provide for this contingency, a second blocking function, NB, is included.

This second function uses negative-sequence quantities operating through an amplitude comparator to provide a negative sequence directional characteristic. The signals used to derive this characteristic are:

Operating Signal: V2 - KI2ZR2

Restraining Signal: I2ZR2

where: K = negative-sequence-current compensation factor.

#### DESCRIPTION OF HARDWARE

### ALUMINUM CASE ASSEMBLY

#### Construction

The TLS1000 cases are constructed from sheet aluminum. The front cover consists of an aluminum frame with a plate glass window. It is hung from the top of the case on a removable hinge. This allows easy access to all the modules.

The case is painted with a textured-finish baked enamel.

The modules are mounted vertically. The sockets within each case (towards the rear) serve as a mechanical support for each module as well as the means of electrical connection. There are card guides on the top and bottom of each case to allow easy removal and insertion, as well as to provide an extra support for the modules.

#### Electrical Connections and Internal Wiring

External connections are made to each case through six terminal blocks mounted on the rear cover plates. Each block contains 14 terminal points, which consist of a Number 6 screw threaded into a flat contact plate.

Connection to the printed-circuit-board modules is made by means of 60-pin edge connectors. Connection to the MGM module is made by means of two connector sockets: an 8-contact current block and a 104-pin signal block. The current block contacts are rated to handle current transformer (CT) secondary currents.

The cases are interconnected via cables that are terminated with 15-pin subminiature type-D connectors. The one- or two-zone distance relays use five cables, while the three-zone distance relay uses seven cables. An additional socket is included on the logic case, to provide an output port for monitoring twelve additional data points.

#### **Identification**

The TLS system model number label is located on the inside of the front cover.

A marking strip indicating the name and position of every module in a given case is included on the lower inside edge of the front cover. It is placed to be read when the front cover is fully opened. Figures 16 and 17 show the location of the modules and a summary of the functions performed by each.

The terminal blocks located on the rear of the modular case are uniquely identified by a two-letter code that is found directly beneath the outer-most edge of each terminal block. Also, the terminal points (1 through 14) are identified by stamped numbers.

#### PRINTED-CIRCUIT-BOARD MODULES

#### Basic Construction

Each module consists of a printed-circuit board and front panel. Two knobs are provided on the front panel for removing and inserting the module. Electrical connection is made by the contact pads at the back edge of the board. Not all module locations within the case have a printed-circuit board. Some locations have a blank board and front panel.

#### Identification

Each module has its own identification number consisting of a three-letter code followed by a three-digit number. These are found at the bottom of each front panel and may be read when the case cover is opened.

#### MODULE DESCRIPTION

Refer to the TLS1000 MODULAR RELAY SYSTEM APPLICATION AND SETTINGS GUIDE, GEK-86668, for the calculations of module settings.

#### ABM101, ABM102

(See Figure 1)

These modules provide the following functions:

- 1. Reach adjustment for MB units
- 2. Zero-sequence current compensation adjustment for MB units
- 3. Polarizing voltage for MB units
- 4. Operating signal for MB units
- 5. Coincidence logic for MB units
- 6. Positive-sequence-current detector
- 7. Fault detector
- 8. Zero-sequence-current supervision for ground-tripping units
- 9. Negative-sequence-current supervision for ground-tripping units

The ABM101 is used in systems rated for 60 hertz, while the ABM102 is used for 50 hertz systems.

#### Front-Panel Switches:

r These switches adjust the positive-sequence reach of the MB units. The reach of 5-ampere rated relays can be adjusted from 2 to 50 ohms in 0.2 ohm steps by selecting the appropriate switches. The reach is equal to 2 plus the sum of the numbers of the switches whose toggles are to the right, i.e. closed. For example, if the top four switches are positioned to the right, the reach will be five ohms:

(2 + 0.2 + 0.4 + 0.8 + 1.6) = 5.0

For relays rated 1 ampere, the reach will be five (5) times the value determined by the above method.

**On-Board Switches** 

- I1 These switches adjust the pickup level of the positive-sequence-current detector. Pickup current is in per unit of rated current  $(I_N)$  and is adjustable from 0.2 to 3.2 per unit in 0.2 per-unit steps. The per-unit pickup current is equal to 0.2 plus the sum of the numbers of the switches whose toggles are to the right.
- K These switches adjust the zero-sequence-current compensation factor  $[(Z_0 Z_1)/Z_1]$  for the MB units from 1 to 7 in 0.1 steps. K is equal to 1 plus the sum of the numbers of the switches whose toggles are to the right.
- KV These switches adjust the voltage compensation factor for the MB units from Ø to 0.45 per-unit in 0.15 per unit steps. KV is equal to 1 plus the sum of the numbers of the switches whose toggles are to the right.
  On-Board Links
- IO SHIFT This link selects the phase shift in the zero-sequence-current supervision signal for the ground-tripping units. The phase shift can be  $0^{\circ}$ ,  $5^{\circ}$ ,  $10^{\circ}$  or  $15^{\circ}$  lag.
- I2 SHIFT This link selects the phase shift in the negative-sequence-current supervision signal for the ground-tripping units. The phase shift can be  $0^{\circ}$ ,  $5^{\circ}$ ,  $10^{\circ}$  or  $15^{\circ}$  lag.
- **OFFSET** This link determines whether the MB unit characteristics are offset into the protected line ("IN" position) or non-offset ("OUT" position).
- POL This link selects the phase shift in the polarizing voltage for the MB units. The phase shift can be either 0° or 20° leading.

## AFM101, AFM102, AFM103, AFM104, AFM105, AFM106

(See Figure 2)

These modules perform identical functions; however, they are found in different locations in the cases, depending upon how they are to be used. There are two basic qualities that separate these modules one from the other:

- 1. The system frequency for which the AFM module has been designed.
- 2. The minimum and maximum reaches, as well as the smallest increment of adjustment (step), is different on each of the AFM modules.

Table I tabulates these differences. Use it as a reference for the "Front Panel Switches" discussion that follows.

	SYSTEM FREQUENCY	I	REACH (	OHMS)	WHERE USE	D (TYPICAL)	
MODULE	(hertz)	MIN.	MAX.	STEP	1-ZONE TLS	2-ZONE TLS	3-ZONE TLS
AFM101	60	1	25	0.1	M1/MG1 or MT/MTG	M1/MG1	M1/MG1
AFM102 AFM103	60 60	2 3	50 750	0.2 0.3	 	MT/MTG	M2/MG2 MT/MTG
AFM104	50	1	25	0.1	M1/MG1 or MT/MTG	MT/MTG	M1/MG1
AFM105 AFM106	50 50	2 3	50 75	0.2 0.3		MT/MTG	M2/MG2 MT/MTG

TABLE I

These modules provide the following functions:

- 1. Reach adjustment
- 2. Zero-sequence-current compensation adjustment
- 3. Zero-sequence supplementary-angle adjustment
- 4. Operate-circuit filter and signal processing
- 5. Operate-circuit "IZ-V" summation
- 6. Summation of zero-sequence-current and negative-sequence-current supervision signals

#### Front-Panel Switches

**r** These switches adjust the positive-sequence reach of the M1/M2/MG1 units. The reach of 5-ampere rated relays can be adjusted from (MIN.) to (MAX.) ohms in (x-ohm) steps. The reach is equal to (MIN.) plus the sum of the numbers of the switches whose toggles are to the right. See Table I to determine the values of MIN., MAX., and STEP.

For relays rated 1 ampere, the reach will be five (5) times the value determined by the above method.

MULT This switch multiplies the reach set on the r switch by 1, 0.25 or 0.1. For example, if the r switch is set for "10" ohms, and the MULT switch is set for 0.25", the actual reach will be 2.5 ohms.

#### **On-Board Switches**

KO These switches adjust the zero-sequence-current compensation  $(Z_0/Z_1)$  for the MG1 units from 1 to 7 in 0.1 steps. Ko is equal to 1 plus the sum of the numbers of the switches whose toggles are to the right.

**Options** - These switches provide flexibility for different applications by permitting signals to be added, as follows:

- **S** This switch adds the high-level bypass signal into the polarizing signals when the toggle is to the right.
- A FIL This switch adds the output of the A filter to the operate signal when the toggle is to the right.

**O SUP** These switches select the amount of zero suppression in the output of the B filter. The zero suppression can be adjusted from 0.1 to 1.5 per unit in 0.03 per unit steps, and is equal to 0.1 plus the sum of the numbers of the switches whose toggles are to the right.

#### On-Board Links

- **B** FIL The output of the B filter is added into the operate signal when this link is in the "IN" position.
- MULT This link determines the clipping level of the  $I_0Z_{R1}$  signals that are used in the operate signals. THIS LINK SHOULD NORMALLY BE IN THE SAME POSITION AS THE FRONT PANEL MULT SWITCH.
- ∠ZRO This link provides a supplementary phase shift for the zero-sequence-current signal so that MG1, MG2, and MTG can be set for different zero-sequence angles. This supplementary phase shift can be either 0°, 25°, 50° or 75° lagging.

## <u>AFM201, AFM202</u>

(See Figure 3)

These modules provide the following functions:

- 1. Operate-circuit filters and signal processing for M1, M2 or MT units
- 2. High-level bypass signal for M1, M2 or MT units.

AFM201 modules are used for 60-hertz-rated systems, while AFM202 modules are used for 50-hertz-rated systems. One AFM201 (or AFM202) module is needed for each zone of protection in the TLS Modular Relay System.

#### **On-Board Switches**

- **Options** These switches provide flexibility for different applications by permitting signals to be added as follows:
- S This switch adds the high-level bypass signal into polarizing signals when the toggle is to the right.
- A FIL This switch adds the output of the A filter to the operate signal when the toggle is to the right.
- **O SUP** These switches select the amount of zero suppression in the output of the B filter for the M1, M2 or MT units. The zero suppression can be adjusted from 0.1 to 1.5 per unit in 0.03 per unit steps, and is equal to 0.1 plus the sum of the numbers of the switches whose toggles are to the right.

#### <u>On-Board Links</u>

**B** FIL The output of the B filter is added into the operate signal only when this link is in the "IN" position.

(See Figure 4)

#### **ETM101**

This module provides the following functions:

1. Coincidence logic circuitry for the M1/MG1 and M2/MG2 units

2. Polarity detectors for M1/M2 polarizing voltages

#### Front-Panel Switches

 $I \not o - \not o$  These switches set the phase-to-phase current sensitivity of the coincidence-logic circuits. Sensitivity can be set between 0.1 and 1.0 per unit of rated current (IN) in each phase, and is equal to 0.1 plus the sum of the numbers of the switches whose toggles are to the right.

#### <u>On-Board Switches</u>

IO SENS These switches set the ground-current sensitivity  $(3I_0)$  of the MG1/MG2 coincidence-logic circuits. Sensitivity can be set for 0.05, 0.25, 0.45 or 0.65 per unit of rated current  $(I_N)$  and is equal to 0.05 plus the sum of the numbers of the switches whose toggles are to the right.

**PHA. PHB** These switches determine which polarizing signals are used in the

- & PHC coincidence logic for the MG1/MG2 units. Zero-sequence-current polarizing IO will be used for an input to the coincidence logic when the "IO" toggles are to the right. Similarly, negative-sequence polarizing will be used when the
  - I2 "I2" toggles are set to the right, and voltage polarizing will be used when the
  - $V_p$  "Vp" toggles are set to the right. THE TOGGLES FOR PHA, PHB AND PHC SHOULD ALL NORMALLY BE SET IN THE SAME PATTERN.
- **Vp SENS** These switches set sensitivity of the voltage polarizing signals in per unit. The sensitivities can be separately set for 0, 0.05, 0.3 or 0.35 per unit by placing the desired toggle or toggles to the right.
  - $\phi$ -G The toggles labelled " $\phi$ -G" affect the MG1 or MG2 units, and the " $\phi$ - $\phi$ "
  - $\phi \phi$  toggles affect the M1 or M2 units. Use care when making these settings, since the toggles for " $\phi G$ " and " $\phi \phi$ " are located on the same switch package.

#### ETM102

(See Figure 5)

This module provides coincidence logic for the MT/MTG units.

#### Front-Panel Switches

 $I\phi-\phi$  These switches are identical to the corresponding switches on the ETM101 module, except that they affect the MT unit instead of the M1/M2 unit.

### <u>On-Board Switches</u>

**Vp SENS** These switches are identical to the corresponding switches on the ETM101  $\not \phi - \phi$  module except that they affect the MT/MTG units instead of  $\not \phi - G$  the M1/MG1 or M2/MG2 units.

#### IOM101

(See Figure 6)

The IOM module contains the contact converters that provide an isolated input of remote signals into the relay logic. The contact converters consist of a dropping resistor and a sensitive reed relay. Each contact converter has a **voltage-selection** 

link, which must be set to the DC voltage that will be energizing that contact converter.

## 10M201, 10M202, 10M203

These modules provide the contacts for the auxiliary outputs, including alarms, DLA and channel-control contacts. See the **SPECIFICATIONS** section of this book for the different contact ratings.

## ISM101, ISM102

(See Figure 7)

These modules provide the following functions:

- 1. IZ signal interfaces
- 2. Voltage signal interfaces
- 3. Positive-sequence and zero-sequence-characteristic-angle selection
- 4. Blocking-unit coordinating level detectors (IB)
- 5. Tripping-unit coordinating level detectors (IT)
- 6. Undervoltage-unit coordinating level detectors (U/V)

The ISM101 is used in  $6\phi$ -hertz-rated systems, while the ISM102 is used in 50-hertz-rated systems.

Front Panel Switches

- ØZ1 This switch selects the relay's positive- and negative-sequence-impedancecharacteristic angle. Characteristic angles can be selected between 50° and 85° in 5° steps. This angle will be the same for all measuring units.
- ØZO This switch selects the relay's zero-sequence-impedance-characteristic angle for all measuring units; however, this angle can be shifted for the MG1, MG2 and the MTG by means of the supplementary ∠ZRO link on the AFM10(-) modules in 25° lag steps. The ØZO switch selects characteristic angles between 50° and 85° in 5° steps.

<u>On-Board Switches</u>

- IB These switches adjust the pickup level of the blocking-unit coordinating level detectors. Pickup current is in per unit of rated current  $(I_N)$  and is adjustable from 0.1 to 1.0 per unit in 0.05 per unit steps. The per unit pickup current is equal to 0.1 plus the sum of the numbers of the switches whose toggles are to the right.
- IT These switches adjust the pickup level of the tripping unit coordinating level detectors. Pickup current adjustment is identical to that for the IB above.

## MGM114, MGM115

The magnetics module contains the current and potential transformers to couple the TLS measuring elements to the system. The current circuits are rated at 1 or 5 amperes. The current transformer inputs are shorted automatically when the module is removed. This module is rated for either 50 or 60 hertz. Three links must be set on this module to set system frequency.

The TRIP output relays are also mounted in this module, together with their drive interface. The output relays are telephone-type relays, which pass the ANSI trip duty-contact test.

## <u>PSM</u>

This module provides all power to operate the TLS system. The power supply is selfprotecting and will not be damaged by a continuous short circuit. The output voltage will recover when the fault is removed. An output alarm is provided to indicate voltage outside the desired limits. A green light-emitting diode (LED) on the front panel indicates normal output voltage. A switch mounted on the front panel removes the  $\pm$  12 and +24 volt outputs only. A 3 ampere 250 volt fuse is provided on the board to protect the printed-circuit board.

#### CAUTION

Battery voltage is still present when the front-panel switch is off.

## ULM101

(See Figure 8)

The ULM101 module provides the logic and timing for single-pole tripping. Insertion of the ULM101 module automatically switches the scheme from three-pole tripping to single-pole tripping; conversely, removal returns the scheme to three-pole tripping.

The only settings required are the selection of three-pole-tripping options. These are set via switches 101A and 101B. The switches provide the following options (switch closed for condition described, unless otherwise noted):

POSITION

101A-1	2	
0	0	MT does not select 3-pole trip
0	С	Trip 3 pole for CC3 and MT Trip 3 pole for CC1 or CC3 and MT
С	0	Trip 3 pole for CC1 or CC3 and MT
C	С	Trip 3 pole for any MT
3 4 5 6		Key 3-pole trip for any MT A phase open selection B phase open selection C phase open selection
C 0	0 0 C	Single-pole trip after zone 2 or zone 3 time Trip 3 pole after zone 3 time Trip 3 pole after zone 2 time Trip 3 pole after zone 2 or zone 3 time
101B-1 2 3		Trip 3 pole for an input on CC3 Trip 3 pole for all faults 1 pole/3 pole channel keying logic

An amber light-emitting diode on the front panel indicates three-pole tripping has been selected.

## <u>ULM111</u>

(See Figure 9)

This module provides target, contact converter buffers, channel-input logic and the transfer-trip security timer. There are two logic switches: 111A and 111B, and a timer, TL13, which must be set. SWITCHES

- 111A-1 Closed for direct-transfer trip
  - 2 Open for bus-side potential; closed for external phase-selection input
  - 3 Closed to invert CC1
  - 4 Closed to invert CC3
- 111B-1 Open for directional-comparison block and hybrid schemes; close for switch-zone schemes
  - 2 Open: switch zone for CC1 or CC3; closed: switch zone-1 reach to zone-2 reach for CC4
  - 3 Closed for transfer trip
  - 4 Open: transfer trip via CC1 and CC3; closed: transfer trip via CC2.

TIMER

TL13 Direct-transfer-trip security timer. Set by positioning switches to the right to obtain the desired time. The setting is additive, and has a minimum of 1 millisecond.

FRONT	PANEL	TARGET	LAMPS
-------	-------	--------	-------

TABLE II

Panel Marking	Target Color	Meaning
Α	red	Phase A trip
В	red	Phase B trip
С	red	Phase C trip
I	red	Zone 1 trip via M1 or MG1
II	red	Zone 2 trip via TL2
III	red	Zone 3 trip via TL3
IV	red	Zone 4 trip via TL4
СТ	red	Channel trip
LP	red	Line-pickup trip
WI	red	Weak-infeed trip via TL16
TT	red	Transfer via TL13
MOB	amber	Out-of-step block

All red targets will seal in and retain their status, even if DC power is lost. These targets can only be set while the trip bus is active. The MOB target is non-latching.

## NOTE:

A TARGET WILL LIGHT FOR ANY SIGNAL THAT OCCURS WHILE THE TRIP BUS IS ACTIVE, WHETHER OR NOT THE BUS CAUSED THE TRIP.

**RESET** Resets the red sealed-in targets. Once **RESET** is pushed, all red lamps should blink on for 1 to 2 seconds. The **RESET** button only affects the red LED targets. No other relay functions are affected.

#### <u>ULM121</u>

(See Figure 10)

The ULM121 module contains the system clock, clock-failure-detection logic, out-ofstep-blocking timers, and the channel-keying logic.

Logic switches select the rated system-frequency-keying logic, protection scheme and fault-detector-override logic.

## SWITCHES

- **121A-1** Open: 60 Hz; closed: 50 Hz
  - 2 Open: permissive underreaching transfer trip; closed: permissive overreaching transfer trip
  - **3** Block keying for out-of-step
  - 4 Block RI via scheme logic
  - 5 Invert Key 1
  - 6 Invert Key 2
  - 7 Key 1 and 2 for transfer trip
  - 8 Not used (leave in OPEN position)
- 121B-1 Override fault detector for inputs on CC7 or CC8
  - 2 Override fault detector for out-of-step
  - **3** Override fault detector permanently
  - 4 Closed: enable fault-detector override logic

121C-1 & 2	Open:	hybrid	Both toggles are to be in the same
	Closed:	blocking	position, i.e., both open or both closed.

## <u>TIMERS</u>

- **TL6** Out-of-step-operating-time pickup is the sum of the closed switches. Minimum, 1 cycle; maximum, 7.75 cycles in 0.25-cycle steps
- MOB/MOBG Characteristic timer setting. Minimum, 32°; maximum, 126° in 2° steps.

Use the following equation to determine the characteristic timer setting:

TIMER SETTING = SUM OF SWITCHES + B X 32

B = 1 if SW32 and SW64 open B = 0 if SW32 or SW64 closed

- EXAMPLE: SW4 and SW16 closed. Therefore B = 1Timer Setting = 4 + 16 + (1 x 32) = 52
  - $\frac{\text{EXAMPLE}}{\text{Therefore B} = 0}$ Timer Setting = 4 + 16 + 64 + (0 x 32) = 84

(See Figure 11)

### <u>ULM131</u>

The ULM131 module provides measuring-unit-supervision signals, zone-4 time, the blocking-unit dropout timer, and the negative-sequence blocking-unit characteristic timer. SWITCHES

- 131A-1 Open: supervise NB with the AND of the MT units; closed: supervise NB with any MT
  - 2 Block reclose initiate for out-of-step
  - 3 Closed: put zone 4 in service
  - 4 Closed: put line-pickup tripping in service
  - 5 Open: line-side potential; closed: bus-side potential
  - 6 Not used (Leave in OPEN position)

TIMERS

- TL4 Zone 4 timer. Set for desired time. Minimum, 0.4 second; maximum, 6.3 seconds in 0.1-second steps. The operating time is the sum of the closed switches.
- TL24 NB dropout. Set desired time. Minimum, 0.5 cycle; maximum, 7.5 cycles in 0.5-cycle steps. The setting is the sum of the closed switches.
- TL25 MBG dropout. Set desired time. Minimum, 0.5 cycle; maximum, 7.5 cycles in 0.5-cycle steps. The setting is the sum of the closed switches.
- NB Characteristic timer. Minimum, 64°; maximum, 96°, in 2° steps. The characteristic angle is 64° plus the sum of the closed switches.

(See Figure 12)

## <u>ULM141</u>

The ULM141 module provides most of the scheme logic, fuse failure and sequentialreclosing settings for the trip integrator, zone 2 and zone 3 coordination, block repeat, weak-infeed and transfer-trip timer. In addition, 24 logic switches for scheme selection are provided.

## SWITCHES

- 141A-1 Closed: TL3 in service
  - 2 Supervise TL3 with MOB
  - **3** Supervise zone 1 with MOB
  - 4 Closed: TL2 in service
  - 5 Supervise channel trip with MOB
  - **6** Supervise zone 1 with blocking unit
  - 7 Supervise weak infeed with MOB
  - 8 Supervise TL2 with MOB
- 141B-1 Open: repeat out; closed: repeat in
  - 2 Open: add time delay to repeat
    - 3 Closed: weak-infeed tripping

- 141C-1 Sequential-reclose logic
  2 Open: switch zone via TL2; closed: trip via TL2
  3 Sequential-reclose input logic
- 141D-1 Closed: M2 (used only on 3-zone schemes); open: MT
  2 Comparer input logic
- 141E-1 Comparer input logic
  2 Sequential-reclose logic
  3 Closed: TL16 in service
  4 Not used (leave in OPEN position)
  5 Not used (leave in OPEN position)
  6 Block reclose for M2 or MT
- 141F-1 Block-reclose logic
  2 Block-reclose logic
  3 (TL15 input select) repeat logic

TIMERS

- TL1 Trip integrator; set as required. Minimum, 1 millisecond; maximum, 15 milliseconds, in 1-millisecond steps. The time is the sum of the closed switches.
- TL2 Zone 2 timer. Minimum, 0.2 second; maximum, 3.15 seconds, in 0.1-second steps. The time is the sum of the closed switches.
- TL3 Zone 3 timer. Minimum, 0.4 second; maximum, 6.3 seconds, in 0.1-second steps. The time is the sum of the closed switches.
- TL14 Coordination timer. Minimum, 2 milliseconds; maximum 15 milliseconds, in 1-millisecond steps. The time is the sum of the closed switches.
- TL15 Block repeat timer. Minimum, 2 milliseconds; maximum 15 milliseconds, in 1-millisecond steps. The time is the sum of the closed switches.
- TL16 Weak-infeed timer. Minimum 0.5 cycle; maximum, 7.5 cycles in 0.5-cycle steps. The time is the sum of the closed switches.
- TL22 Transfer-trip time. Minimum, 0.4 second; maximum, 6.3 seconds, in 0.1second steps. The time is the sum of the closed switches.

#### **UTM101**

(See Figure 13)

The UTM101 module provides the characteristic timers for the M1, MG1, MT, MTG and MB units. Each unit can be set to pick up from  $64^{\circ}$  to  $127^{\circ}$  in  $1^{\circ}$  steps. The setting is equal to  $64^{\circ}$  plus the sum of the closed switches.

Three switches are provided to select the **MG1 Supervision** for mho or reactance operation. When making this selection, all three toggles must be in the same position, that is, all open or all closed.

A switch at the bottom of the same unit is provided to supervise M1 by MG1 when the switch is in the closed position.

(See Figure 14)

#### <u>UTM102</u>

The UTM102 module provides the characteristic timers for the M2 and MG2 units. Each unit can be set to pick up from  $64^{\circ}$  to  $127^{\circ}$  in  $1^{\circ}$  steps. The setting is equal to  $64^{\circ}$  plus the sum of the closed switches.

#### VMM101, VMM102

These modules provide the following functions:

- 1. Polarizing signals for M1/MG1, M2/MG2 and MT/MTG units
- 2. NB function

(See Figure 15)

- 3. Zone switching of M1/MG1, M2/MG2 reach
- 4. IO supervision for MG1, MG2 and MTG units
- 5. 3IOZ1 restraint signal for M1, M2 and MT units.

The VMM101 is used for 60-Hz-rated systems, and the VMM102 for 50-Hz-rated systems.

Front-Panel Switches

II These switches select the reach of switched zone 2 in multiples of the zone 1 reach, which is set on the AFM101 or AFM104 module. The reach multiplier is adjustable from 1 to 10 in steps of 0.05, and is equal to 1 plus the sum of the numbers of the switches whose toggles are to the right.

## **On-Board Switches**

- I2LD These switches select the pickup current of the negative-sequencecurrent-level detector of the NB function. Pickup is adjustable from 0.05 to 0.5 per unit in 0.05-per-unit steps. Per-unit pickup current is equal to 0.05 plus the sum of the numbers of the switches whose toggles are to the right.
- KI2Z These switches select the compensation factor for negative-sequence current in the NB function. This compensation factor can be adjusted from 0.6 to 1.0 in 0.05 steps, and is equal to 0.6 plus the sum of the numbers of the switches whose toggles are to the right.
- NB These switches select the reach for the NB function. The reach for 5ampere rated relays is adjustable from 5 to 80 ohms in 5-ohm steps, and is equal to 5 plus the sum of the numbers of the switches whose toggles are to the right. For relays rated 1 ampere, the NB reach will be five (5) times the value determined by the above method.
- OFFSET M1/MG1 These switches select the per-unit offset (into the protected line section) of the polarizing voltages for the M1/MG1 units. The offset is adjustable, from 0. to 0.4 per unit, in 0.1 per-unit steps, and is equal to 0 plus the sum of the numbers of the switches whose toggles are to the right.
- OFFSET MT/MTG These switches select the per-unit offset (into the protected line section) of the polarizing voltages for the MT/MTG units. Offset adjustment is identical to that for OFFSET M1/MG1 above.

VP ANG These switches select the phase shift in the polarizing voltages for the MG1 units. The phase shift can be adjusted to 1°, 10°, 15°, 20°, 25°, 30°, 35° or 45° leading, and is equal to 0 plus the sum of the numbers of the switches whose toggles are to the right.

## On-Board Links

- **IOZ REST** This link provides zero-sequence-current restraint for the M1, M2 and MT units only when the link is in the "IN" position.
- MULT This link determines the amount of zero suppression in the zerosequence-current supervision signal for the MG1, MG2 and MTG units, and in the zero-sequence-current-restraint signal for the M1, M2 and MT units. THIS LINK SHOULD NORMALLY BE IN THE SAME POSITION AS THE FRONT PANEL MULT SWITCH ON THE AFM101 OR AFM104 MODULE.
- M1 VP This link phase shifts the polarizing voltages for the M1 units by the same angle as that for the MG1 units if it is in the "SHIFT" position. If this link is in the "NOT SHIFT" position, the M1 polarizing voltages will not be shifted.

#### TESTING

## DIELECTRIC TESTS

Dielectric testing may be performed (1) between all terminals (tied together) and the case, and (2) between independent circuit groups (refer to elementary diagrams, Figures 21-25). The recommended voltage is 2000 volts rms for initial testing and 1500 volts rms for subsequent periodic testing. The test voltage should be applied for one minute.

## CAUTION

When hipot testing, it is necessary to remove the jumpers between terminals AH13 and AH14, and between terminals BH13 and BH14. This removes the grounding connection between the surge capacitors and case ground. Failure to do so could result in damage to the filter capacitors on the PSM module when the DC supply terminals are tested.

## NOTE

ALL OTHER STUDS CAN BE TESTED WITH THE JUMPER IN PLACE WITHOUT DAMAGE; HOWEVER, LEAKAGE WILL BE INDICATED, DUE TO CURRENT FLOWING THROUGH THE SURGE CAPACITORS

## ACCEPTANCE TESTS

The operational tests described in this section should be conducted prior to the installation of the TLS system. These may be done on a "bench-top" basis.

## CAUTION

Remove all power from the TLS before removing or inserting any of the printedcircuit-board modules. Failure to observe this caution may result in damage to the relay.

One method of removing power is to turn off the power switch on the PSM power supply module and then remove both of the connection plugs located in the TPM position on the left side of the case.

## Initial Test Settings

To begin the acceptance tests, the module settings should be as indicated in Tables III and IV. Remove the modules to gain access to the links and switches referred to in Table III. Module locations are shown in Figures 16 and 17.

Module	Figure	Descr	iption	Ì	Switc	h or Link	
Name	Number	Page	Case	Socket	Туре	Name	Setting
ABM10(-)	1	8	Α	С	Switch	I <sub>1</sub>	0.2
4		0	ti -	41	li	K	1
11 		11		"	41 	KV	0.3
H 		11	#1 	11	Link	IO SHIFT	0
65 43		11				I2 SHIFT	0
# 11			•	11		OFFSET	IN
			•			POL	0
VMM10(-)	15	19	11	Ε	Switch	I2LD	0.05
0	-	0	н	II	11	KĪ2Z	1.0
11		11	11	11	II	NB	5
0		11	11	н	U	OFFSET M1/MG1	0.3
			Ð	u	41	OFFSET MT/MTG	0.3
0		ŧ1	u	H	11	VP ANG	0
		H	6	0	Link	IOZ_REST	OUT
11			11	<b>11</b>	11	MULT	1
41		81	H	"	n	M1VP	NOT SHIFT
ETM102	5	12	н	G	Switch	VP SENS Ø-Ø	0
"	-	"	0	ü	"	VP SENS Ø-G	Ō
AFM20(-)	3	11	11	J	н	S	LEFT
"	-	u	11	u .	11	AFIL	RIGHT
<b>\$1</b>		11	н	U	н	0 SUP	0.1
li		11	H	H	Link	BFIL	IN
AFM10(-)	2	9	u	L	Switch	KO	4.0
8		11	H	17	11	Š	LEFT
н		11	15	u –	н	AFIL	RIGHT
11		U U	0	8	H	O SUP	0.1
11		11	н	u	Link	BFIL	IN
U		н	11		0	MULT	1
н		n	H	H	<b>11</b>	∠ZRO	0
ETM101	4	11	Ð	N	Switch	IO SENS	0.05
		41	11	11	(3) Separate	IÕ	RIGHT
н		11	U.	0	Switches	I <sub>2</sub>	0
11		0	11	H	Labelled PHA,PHB,PHC	VP	14
0		H	0	н	Switch	VP SENS Ø-Ø	0
H			H	11	61	VP SENS Ø-G	0
AFM20(-)	3	11	0	R	11	S	LEFT
IF		11	11	H	0	AFIL	RIGHT
11		IL.	14	0	н	O SUP	0.1
80		0	u	11	Link	BFIL	IN
						(Continu	ied)

TABLE III INTERNAL MODULE SETTINGS

Module	Module Figure Description Switch or Link						
Name	Number	Page	Case	Socket	Туре	Name	Setting
AFM10(-)	2	9		T	Switch	Kø	4.0
		6 1	H 11	11 11		S	LEFT
		n		"	40	AFIL	RIGHT
AFM10(-)		11	n	ŧ	0 SUP	0.1	
0		41	H.	11	Link	BFIL	IN
		11		11	11	MULT	1
0		11		11	11	∠ ZRO	0
ISM10(-)	7	13	н	V	Switch	IB	0.2
u i		II		<b>H</b>	11	IT	0.2
ETM101++	4	11	В	Att	Switch	IO SENS	0.05
8		0	H	11	(3) Separate		RIGHT
1		0 0	14 13	H H	Switches	I2	
		U U		н	Labelled	VP	u
11		ł.	u	H	PHA,PHB,PHC Switch		440
0		11		0-	Switch II	VP SENS Ø VP SENS Ø	
AFM20(-)++	3	11	**	C++	Switch	S	LEFT
0		11	11	ti	0	AFIL	RIGHT
11 		11	If	н	0	O SUP	0.1
42		11	11	88	Link	BFIL	IN
AFM10(-)++	2	9	0	E††	Switch	KO	4.0
0		H	U.	0	44	S	LEFT
41 11		11		61 11		AFIL	RIGHT
			11 11	4	14 1. 4 . L	O SUP	0.1
					Link	BFIL	IN
ii		N N	u			MULT ∠ZRO	1 ø
UTM102++	14	18	11	<b>611</b>	C. J.L.a.k		90°
"	14	10	н	G†† "	Switch "	M1 M1G	90 90°
UTM101	13	18	8	к	Switch	M1	<b>9</b> 0°
11		41	u	11	41	M1G	<b>9</b> 0°
		u	0	U	11	MT	<b>9</b> 0°
		u 	#1		11	MTG	<b>9</b> 0°
41		81 11	H H	11	0	MB	90°
11		u U	11	0	11 41	SUPERVISION SUPERVISION	MHO M1 NO SPVI
ULM131	11	16	u	Р	Switch	NB	90°
ULM121	10	16	н	c			
	10	10		S "	Switch "	MOBø MOBG	126° 126°
IOM101	6	12	u	Y	Link	48-125-250	DC VOLTAGE
			- 7 *			signed for pro	

## TABLE III, continued INTERNAL MODULE SETTINGS

tt These modules are included only in those TLS relays designed for providing three zones of protection.

	ch	Description	
Module Name	Name	Setting	Page
ABM10(-)	r	6.0 ohms	8
AFM10()	r	6.0 ohms	9
11	MULT	1.0	9
ETM10(-)	IØ-Ø	0.1	11
ISM10(-)	øZ1	85	13
u	øΖο	85	13
PSM	ÓN/OFF	OFF	13
VMM10(-)	II	1.0	19

TABLE IV FRONT PANEL SWITCH SETTINGS

## Test Equipment

The acceptance tests may be conducted in a conventional manner, using the following test equipment:

Three-phase power source, of rated frequency DC-control-voltage source One phase shifter One phase-angle meter Variable auto-transformer, 3 gang, rated 1 ampere (or greater) Variable auto-transformer, single gang, rated 2 x (two times) rated current (or greater) One test reactor: Tapped for 6/12/24 ohms for 5 amp relays (GE #6054975G1 reactor) Two AC voltmeters One AC ammeter One oscilloscope One card extender (GE #0138B7406G1) One pair XTM test plugs (GE #XTM28R1 and XTM28L1)

The specific requirements for this equipment are given above and in the associated test-circuit diagrams (Figures 18-20).

The three-phase AC sinusoidal voltage must be balanced and undistorted. Similarly, the DC power should come from a good DC source having less than 5% ripple.

As an alternative, a three-phase electronic test source may be used. In many cases, these devices enable the test circuits to be simplified considerably.

## Test Connections

The test-circuit diagrams indicate TLS terminal numbers (rear cover terminals) and the corresponding XTM-test-plug terminal numbers. For the acceptance tests, the test connections should be made to the rear cover terminals. The test plugs are intended for post-installation testing, and are described in a separate subsection under **PERIODIC TESTS**.

The interconnecting cables between the measuring unit and logic cases should be in place for all tests.

## REPLICA IMPEDANCE ANGLE AND REACH TESTS

## CAUTION

Remove all power from the TLS before removing or inserting any of the printed-circuit-board modules. Failure to observe this caution may result in damage to the relay.

#### <u>M1/MG1 Units</u>

- 1. Place the ETM101 module from module location "N" of the measuring unit case in a card extender. Turn on the DC power supply and check that the green light-emitting diode on the PSM module is lit.
- Connect the relay per Figure 18 for the phase to be tested. 2. Connect the oscilloscope to the card-extender pin number shown in Table V for the phase to be tested. Set  $V_T$  at 60 volts rms and adjust the phase angle for 85°. As the current, IT, is raised to approximately IN, observe that the oscilloscope waveform changes from a large to a smaller magnitude. Fine adjustment of the current and the phase angle will result in the oscilloscope waveform being reduced to a null consisting of only third and fifth harmonics. At the adjustments which produce the optimum null, the angle on the phase-angle meter is the replica impedance angle, which should be between 82° and 88°. The current, IT, at this null should be between 4.75 and 5.25 amperes rms for 5ampere-rated relays, or between 0.95 and 1.05 amperes rms for 1-ampere-rated relays.

When doing these tests, the test voltage, VT, is 60 volts phase-to-ground for the phase-to-ground tests, and 60 volts phase-to-phase for the phase-to-phase tests.

If voltage VT remains at 60 volts phase-to-ground for the phase-to-phase tests, the currents will increase by a factor of  $\sqrt{3}$ . If the trip contacts are being observed during this test, tripping will occur within 3% of null current, providing that a scheme logic has been selected that will permit tripping.

Repeat this test for each phase of the M1/MG1 function. When the M1/MG1 testing is completed, remove the card extender from the ETM101 card and replace the ETM101 card back into module location "N" of the measuring unit.

PHASE UNDER TEST	CARD-EXTENDER PIN NO. "TEST POINT"
A-G	6
B-G	49
C-G	28
A-B	7
B-C	50
<u> </u>	26

TABLE V

## M2/MG2 Units (Three-zone TLS only)

Place the ETM101 card from module location "A" of the logic unit on the extender, and repeat step 2 of the "M1/MG1 Units" test for the M2/MG2 units. When the M2/MG2 testing is completed, remove the card extender from the ETM101 module and restore the ETM101 module to its place in the unit.

## MT/MTG Units

Place the ETM102 module, from module location "G" of the measuring unit case, in the card extender. Repeat step 2 of the "M1/MG1 Units" tests for the MT/MTG units. When the MT/MTG testing is completed, remove the card extender from the ETM102 module and restore the ETM102 module to its place in the unit.

#### MB Units

- 1. Place the ABM10(-) module, from module location "C" of the measuring-unit case, in the card extender.
- 2. Repeat step 2 of the "M1/MG1 Units" tests, except:
  - a) Use Table VI for oscilloscope connections.

#### <u>TABLE VI</u>

PHASE UNDER TEST	CARD-EXTENDER PIN NO. "TEST POINT"
A-G	12
B-G	21
C-G	57

- b) Current IT at the null should be between 5.0 and 5.5 amperes rms for 5ampere-rated relays, or between 100 and 1.10 amperes rms for 1-ampererated relays.
- c) Adjust the phase angle for 265° instead of 85°.
- 3. When the MB testing is complete, remove the card extender from the ABM10(-) module and restore the ABM10(-) module to its place into the unit.

#### OFFSET MHO CHARACTERISTIC TESTS

- 1. Place the UTM101 module (module location "K" of the logic case) in the card extender (M1/MG1, MT/MTG and MB).
- 2. Connect the relay per Figure 18. Connect the oscilloscope to the card-extender pin number shown in Table VII for the phase to be tested.

GEK-	866	38
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	FUNCTION	UNDER TEST	PHASE UNDER TEST	CARD EXTENDER PIN NO. "TEST POINT"
Forward	Zones:	MG1	A-G	20
		41	B-G	10
		11	C-G	7
		М1	A-B	9
		11	B-C	8
		11	C-A	8 6
		MTG or MG2	2 A-G	23
		11	B-G	24
		11	C-G	25
		MT or M2	A-B	5
		H	B-C	3
		n	C-A	5 3 4
Blockin	g:	MB	A-G	53
	-	11	B-G	27
		0	C-G	28

TABLE VII

3. Set current IT at rated current (1 ampere rms or 5 amperes rms) and the phaseangle meter at 85°. Reduce VT from approximately 70 volts rms until the measuring unit under test picks up, as indicated by the oscilloscope trace going from approximately 0 to approximately 10 volts. Pickup should occur for VT between 55 and 61 volts rms. This test checks the reach at the replica impedance angle, including the pull-back effect at this current level (approximately 3%).

When doing these tests, test voltage VT is measured phase-to-ground for the phase-to-ground tests and phase-to-phase for the phase-to-phase tests. If VT is measured phase-to-ground for the phase-to-phase tests, the voltage read will be reduced by a factor of  $1/\sqrt{3}$ . Also, all three-phase voltages must go up and down together (voltages are ganged).

Since the M1/MG1, M2/MG2 and MT/MTG values are used for tripping, pickup is defined as the first time a pulse reaches the 10-volt level. The pickup steady-state condition will occur within 1 volt of the onset of the first 10-volt pulse.

4. After the measuring unit picks up, continue reducing VT until the measuring unit drops out again, as indicated by the oscilloscope trace going from approximately 10 to approximately 0 volts. Dropout should occur for VT between 2 and 4 volts rms for MG1 or MTG functions, or between 5 and 7 volts rms for M1 or MT functions. This test checks the amount of forward offset.

Dropout is defined as when the 10-volt level is no longer present. The dropout steady-state condition will occur within 0.5 volt of the onset of the first zero-going pulse.

- 5. Return VT to approximately 70 volts rms, and set the phase-angle meter to  $55^{\circ}$ . Reduce VT until the measuring unit picks up, which should occur for VT between 43 and 54 volts rms. Change the phase-angle meter to 115° and vary VT until the measuring unit again picks up, which should also be for VT between 43 and 54 volts rms. This test checks the shape of the mho circle.
- 6. Repeat tests 3, 4 and 5 for each phase of the M1/MG1 and MT/MTG functions.
- 7. Set current IT at rated current (1 ampere rms or 5 amperes rms) and the phaseangle meter at 265°. Reduce VT from approximately 70 volts rms until the MB under test picks up, as indicated by the oscilloscope trace going from approximately 0 to approximately 10 volts. Pickup should occur for VT between 52 and 58 volts rms. This test checks reach at the replica impedance angle, including the pull-back effect at this current level (approximately 3%).
- 8. After the MB picks up, continue reducing  $V_T$  to 0 volts. The MB should remain picked up.
- 9. Return VT to approximately 70 volts rms, and set phase-angle meter to 235°. Reduce VT until the MB picks up, which should occur for VT between 46 and 54 volts rms. Change the phase-angle meter to 295° and vary VT until the MB again picks up, which should also be for VT between 46 and 54 volts rms. This test checks the shape of the mho circle.
- 10. Set the phase angle to  $85^{\circ}$  and return VT to approximately 70 volts rms. Reduce VT until the MB under test picks up, which should occur for VT between 0.3 and 1.5 volts rms.
- 11. Repeat tests 7 through 10 for each phase of the MB functions.
- 12. Remove the UTM101 module from the card extender and reinsert it into module location "K" of the logic unit. Steps 13, 14 and 15 apply only to those TLS models having three zones of protection.
- 13. Remove the UTM102 module (module location "G" of the logic case) and place it on the card extender.
- 14. Repeat steps 2 through 6 of the OFFSET MHO CHARACTERISTIC TESTS, except now test for the M2/MG2 functions.
- 15. Remove the card extender from the UTM102 module and restore the UTM module to its place in the unit.

## NB UNIT TESTS

- 1. Place the ULM131 module in the card extender. Connect the oscilloscope probes to pin 3 and pin 22 on the card extender.
- 2. Directional Check:
  - a) Connect the relay per Figure 19. Set  $V_T$  to  $3\sigma$  volts rms,  $V_B$  and  $V_C$  to 67 volts rms, and  $I_T$  to rated current (I<sub>N</sub>). Set the phase angle to  $95^{\circ}$ , current leading voltage ( $265^{\circ}$  current lagging voltage). Check for +10 to +12 volts DC at pin 3. The signal at pin 22 should be a series of blocks approximately one-half cycle in duration; the off time should be less than 1.5 milliseconds.

- b) Change the phase angle to 85°, current lagging voltage. Check for less than 1 volt DC at pin 3. The response at pin 22 is a pulse having a width of 0.0 milliseconds to 1.0 millisecond. If no pulse is detected, it may be concluded that the pulse width is 0.0 milliseconds, and meets the intent of this test.
- c) Remove the ULM131 module from the card extender and reinsert the module into the case.
- 3. Reach Check:
  - a) Move the card extender to the VMM101/102 module in the analog case. Connect the oscilloscope to test loop TP7 on the board. <u>NOTE</u>: This is **not** card edge connector pin 7.
  - b) Connect the relay per Figure 19. Set VT to 30 volts rms and IT to 1.45 times rated current (1.45 IN). Set the phase angle to  $85^{\circ}$ , current lagging voltage. Check for a null at TP7 (the "null" voltage is a signal with a peak fundamental-frequency signal of less than 0.5 volt). The phase angle may be varied  $\pm 3^{\circ}$ , and the current  $\pm 5\%$  to achieve the null signal.
  - c) Remove the VMM101/102 module from the card-extender and restore the module to its place the case.

## FAULT-DETECTOR TESTS

- 1. Place the ABM10(-) module from module location "C" of the measuring-unit case in the card extender. Connect the oscilloscope to card extender pin 52. Set the oscilloscope for external trigger.
- 2. Set current IT at 0.09 IN. Close the pushbutton test switch for approximately 1 second. When the pushbutton test switch opens, the oscilloscope trace should go to approximately 10 volts, and remain there momentarily, after which it should return to approximately 0 volts.
- 3. Increase IT to 0.45 IN and repeat test 2; at this level the oscilloscope trace should remain at approximately 10 volts except when the pushbutton test switch is closed.
- Remove the card extender from the ABM10(-) module and restore the module to its place.

## LEVEL-DETECTOR TESTS

- 1. Connect the relay to test "I1" level detector per Figure 20. Increase the current until the oscilloscope trace goes from approximately 0 to approximately 10 volts, at which point the current should be between 0.54 and 0.66 times  $I_N$ .
- 2. Place the ISM10(-) module from module location "V" of the measuring-unit case in the card extender. Connect the relay to test phase A undervoltage per Figure 20. Reduce voltage VT until the oscilloscope trace pulses from approximately 0 to approximately 10 volts, at which point the voltage should be between 41 and 45 volts rms. The trace should remain high at no less than 30 volts rms.

- 3. Change relay connections to those shown for phase B undervoltage per Figure 20. Repeat step 2.
- 4. Change relay connections to those shown for phase C undervoltage per Figure 20. Repeat step 2.
- 5. Change relay connections to those shown for phase A IB unit per Figure 20. Increase current ITEST until the oscilloscope trace goes from approximately 0 to approximately 10 volts. Current should be within 10% of 1 ampere rms for 5-amp-rated relays, or 0.2 ampere rms for 1-amp-rated relays.
- 6. Repeat step 5 for IB phases B and C and for IT phases A, B and C connections, as shown in Figure 20.

#### TESTING THE TLS OPERATION WITH DIFFERENT SETTINGS

Because of the level of sophistication of the TLS modular relay system and the large number of selections that may be made, it is impossible to present one or two equations that will satisfy every condition. This section makes an attempt, however, to allow for the calculation of the pickup voltages for the MHO function when using the test circuits described in the corresponding section of the TESTING portion of this instruction book, but with different settings than those listed in Tables III and IV. This will permit some testing to be done using settings other than those specified as part of the acceptance tests.

To test with different settings, refer to the corresponding section of ACCEPTANCE TESTS. For instance, if the M1 function is being tested, use the same test setup and settings as described in the M1 portion, but use the equations and notes given below to modify the expected test results. Only those settings identified in the equations are allowed to be varied; otherwise, the expected results may be different than calculated.

#### NOTE:

BECAUSE OF SATURATION EFFECTS, IF A REACH MULTIPLIER (RM) OF 0.1 IS USED, THE TEST VOLTAGE AT PICKUP MUST BE LESS THAN 40% OF RATED.

M1/M2/MT (Phase-to-Phase Tests)

The effective forward reach may be calculated by the following equation:

### $Z_F = 2 \times Z_{NP} \times RM$

where:

ZF = effective forward reach ZNP = set nameplate reach RM = reach multiplier

#### Example:

If the current equals 5 amperes, the reach multiplier equals 1, and the set nameplate reach is 6 ohms, the nominal phase-to-phase pickup voltage at the angle of maximum reach is:

where:  $V_{NOM} = I \times Z_F = 5 \times 2 \times 6 \times 1 = 60 V_{\emptyset-\emptyset}$  $V_{NOM} = nominal phase-to-phase pickup voltage$ I = current

The offset reach in the TLS is based on positive-sequence voltage and current and is not affected by the reach multiplier. The instruction-book test setup uses a balanced three-phase voltage and single phase-to-phase current. For this test, V1 = V $\phi$ N and I1 = I $\phi/\sqrt{3}$ . Note that the voltmeter is connected phase-to-phase and V1 = V $\phi-\phi/\sqrt{3}$ . Therefore, the effective forward offset is:

$$Z_{FO} = Z_{NP} \times (per unit offset)$$

where: ZFO = effective forward offset reach

or in terms of ZF

$$ZFO = \frac{ZF}{2 \times RM} \times (Per unit offset)$$

Example:

If the current is 5 amperes, the set nameplate reach 6 ohms, and the per-unit offset is 0.3, the nominal phase-to-phase pickup voltage at the angle of maximum reach is:

 $5 \times 6 \times 0.3 = 9$  volts

MG1/MG2/MTG (Phase-to-Ground Tests)

The test circuit uses a balanced three-phase voltage and a single phase-to-ground current. Note that for the instruction-book tests it is assumed that  $\emptyset Z_1 = \emptyset Z_0$ . The effective forward reach is a function of K<sub>0</sub> as well as the nameplate reach, and is equal to:

$$ZF = ZNP \times \frac{2 + K_0}{3} \times RM$$

where:  $K_0 = zero-sequence$  compensation factor

Example:

If the current equals 5 amperes, RM equals 1, the set nameplate reach is 6 ohms and  $K_0$  equals 4, the nominal phase-to-ground pickup voltage at the angle of maximum reach is:

$$VNOM = 5 \times 6 \times \frac{2+4}{3} = 60 \text{ volts}$$

Because the offset reach is positive-sequence ohms, it is not affected by the K0 setting. The test circuit produces  $V_1 = V_{ON}$  and  $I_1 = I_0//3$ ; the effective forward offset reach is therefore:

$$ZFO = \frac{Z_{NP} \times (Per unit offset)}{3}$$

or, in terms of ZF

$$ZFO = \frac{ZF \times (Per unit offset)}{(2 + K_0) \times RM}$$

Example:

If the current equals 5 amperes, RM equals 1, the set nameplate reach is 6 ohms and KO equals 4, and the per-unit offset is 0.3, the phase-to-ground pickup voltage at the angle of maximum reach is:

$$\frac{5 \times 6 \times 0.3}{3} = 3$$
 volts

MB

The test circuit uses a balanced three-phase voltage and a single phase-to-ground current. Note that in the instruction book tests it is assumed that  $\emptyset Z_1 = \emptyset Z_0$ . The effective blocking reach is a function of the set nameplate reach, K (current compensation) and KV (voltage constant). The reverse, or blocking direction, reach is:

$$ZBLK = ZNP \times \frac{3 + K}{3} \times \frac{1}{1 - KV}$$

where: K = current compensation
 KV = voltage constant
 ZBIK = blocking-direction reach

Example:

If the test current equals 5 amperes, the nameplate reach is 6 ohms, K equals 1 and KV equals 0.3, the phase-to-ground voltage at pickup at the angle of maximum reach will be:

5 x 6 x 
$$\frac{3+1}{3}$$
 x  $\frac{1}{1-0.3}$  = 57.14 volts

The forward (tripping direction) reach is not affected by K or KV. For the test circuit  $V_1 = V \phi_{-N}$  and  $I_1 = I \phi //3$ , the effective offset reach will be:

 $ZBO = \frac{ZNP \times (Per unit offset)}{3}$ where: ZBO = effective blocking offset reach

or, in terms of the blocking-direction reach:

ZBLK x 
$$\frac{1 - KV}{3 + K}$$
 x (Per unit offset)

Example:

If the current equals 5 amperes, the nameplate reach is 6 ohms and the per-unit offset is 0.1, the nominal phase-to-ground pickup voltage will be:

$$\frac{5 \times 6 \times 0.1}{3} = 1$$
 volt

#### PERIODIC TESTS

A periodic test program should be developed that checks all of the TLS functions employed in the scheme under consideration. It is left to the user's discretion to choose, from among the Acceptance Tests given in the previous section, those tests that may be applicable as Periodic Tests for a particular installation scheme.

## XTM TEST PLUGS

#### Description

The XTM test plugs are designed specifically for post-installation testing of the TLS system. There are two plugs; XTM28L1 (left-hand plug) and XTM28R1 (right-hand plug), each providing access to fourteen relay and fourteen system points. The system points are located on the outer edge. The plugs are keyed by the contact-

finger arrangement so that there may be no accidental interchange between the lefthand and right-hand plugs.

The plugs are fitted with a sliding handle that swings out to facilitate wiring to the terminals. The terminals consists of number 8 screws threaded into flat contact plates. The handles each have a tab on the outside edge to guide the wire dress of the test leads.

#### NOTE:

NOT ALL THE EXTERNAL CONNECTIONS TO THE TLS ARE WIRED THROUGH THE TEST RECEPTACLE.

#### <u>Terminal Designation</u>

The test receptacle and connection plugs are located to the left of the magnetics module (extreme left-hand position). Their terminals are labeled 1 through 28, with 1 through 14 corresponding to the left-hand side and 15 through 28 corresponding to the right-hand side. These points are designated on the elementary diagram (Figures 21 through 25) as TP1 through TP28.

The left-hand-test-plug (XTM28L1) terminals are labeled 1R through 14R and 1S through 14S for the relay side and system side, respectively, with the system side labeled in red. Similarly, the right-hand-test-plug (XTM28R1) terminals are labeled 15R through 28R and 15S through 28S.

#### XTM Test-Circuit Connections

Test-circuit connections, designated as TP points in the elementary diagrams, should be made to the relay side of the test plug. Where it is desired to use available system quantities for testing, e.g., DC control power, jumpers may be inserted between the corresponding system-side and relay-side test-plug terminals.

Appropriate precautions should be taken when working with station battery DC. Connections should be made to the test plugs prior to insertion into the TLS.

## Test Plug Insertion

To insert the test plugs, the two connection plugs must first be removed. In so doing, electrical continuity is broken between the power system and the TLS for those signals that are wired through the test receptacle (refer to TP points on elementary diagrams, Figures 21 through 25). For the terminals connected to the current-transformer secondaries, shorting bars are included on the system side of the test receptacle. These are clearly visible through the transparent plastic face plate on the receptacle. The shorting bars make contact before the connection-plug contacts break during removal, so that the CT secondaries are never open-circuited.

Both test plugs may be inserted at the same time. Otherwise, if using only one test plug, the connection plug may remain in the other half of the receptacle.

When the test plugs are inserted into the receptacle, parts of the power system become isolated from the TLS. Refer to the TLS elementary diagrams (Figures 21-25) for the TP points associated with each of the test plugs.

## WARNING

IT IS CRITICAL THAT JUMPERS BE INSERTED ON THE SYSTEM-SIDE TEST-PLUG TERMINALS THAT ARE CONNECTED TO THE CT SECONDARIES. IF THESE JUMPERS ARE LEFT OUT, THE RESULTING HIGH VOLTAGES DEVELOPED PRESENT A SERIOUS HAZARD TO PERSONNEL AND MAY SEVERELY DAMAGE EQUIPMENT.

#### CARD EXTENDER

The card extender (GE #0138B7406G1) is used to obtain information about the operation of an individual module. The extender may be inserted in the place of any of the printed-circuit-board modules. The module can then be inserted into the connector on the card extender.

The extender has 60 test points, which are identified by numbers 1 through 60.

#### CAUTION

Remove power from the TLS before removing or inserting any of the printedcircuit-board modules. Failure to observe this caution may result in damage to the relay.

One method of removing power for certain cases is to turn off the power switch on the PSM power-supply module and then remove both of the connection plugs located in the TPM position on the left side of the case.

## WARNING

CAUTION MUST BE EXERCISED WHENEVER A CARD EXTENDER IS <u>INSERTED INTO AN IOM OR</u> <u>PSM POSITION</u>, SINCE STATION BATTERY POTENTIAL WILL BE PRESENT AT SOME POINTS. FAILURE TO OBSERVE THIS WARNING MAY RESULT IN PERSONAL INJURY OR DAMAGE TO EQUIPMENT. TURNING OFF THE POWER SWITCH ON THE PSM MODULE AND REMOVING BOTH CONNECTION PLUGS DOES <u>NOT</u> REMOVE <u>ALL</u> EXTERNAL POWER TO THE RELAY.

## BLOCK DIAGRAM OF MEASURING-UNIT CIRCUITRY

Block diagrams for various portions of the measuring-unit circuitry are given in Figures 26 through 31, as referenced in Table VIII. These block diagrams indicate module pin numbers in the measuring-unit case, with the letter being the module location letter given in Figure 13. For example, signal "IAI" is shown in Figure 27, (sheet 2), as being on "V14" and "V6", which means that this signal is on pins "14" and "6" of module (ISM10(-) in module location "V" of the measuring-unit case.

TAE	BLE	٧I	II

TYPE OF CIRCUITRY	FIGURE NO.
Voltage-Processing Circuits	26
Current-Processing Circuits	27
Polarizing Voltage Circuits	28
Reach Adjustment and Operate Circuits	29
M1, MG1, MB Coincidence Logic and Timers	30
MT, MOBø, MTG and MOBG Coincidence Logic and Timers	31

## RECEIVING, HANDLING AND STORAGE

#### CAUTION

This relay contains electronic components that could be damaged by electrostatic-discharge currents if those currents flow through certain terminals of the components. The main source of electrostatic-discharge currents is the human body, and the conditions of low humidity, carpeted floors and isolating shoes are conducive to the generation of electrostatic-discharge currents. Where these conditions exist, care should be exercised when removing and handling the modules to make settings on the internal switches. The persons handling the module should make sure that their body has been discharged, by touching some surface at ground potential, before touching any of the components on the modules.

Immediately upon receipt, the equipment should be unpacked and examined for any damage sustained in transit. If injury or damage resulting from rough handling is evident, file a damage claim at once with the transportation company and promptly notify the nearest General Electric Sales Office.

If the equipment is not to be installed immediately, it should be stored indoors in a location that is free from moisture, dust, metallic chips, and severe atmospheric conditions.

#### INSTALLATION

#### ENVIRONMENT

The location should be clean and dry, free from dust and excessive vibration, and well lighted to facilitate inspection and testing.

#### MOUNTING

The TLS cases have been designed for standard rack mounting. Each case measures four rack units (4 RU) in height. The units may also be flush-mounted on a panel. Refer to Figures 32 and 33 for the outline and mounting dimensions.

Provision has been made for surface-panel mounting as well. This is accomplished by removing and reversing the side brackets so that the mounting wings are in the rear. For surface mounting, cutouts must be made in the panel to allow for the terminal blocks and interconnection cables.

## EXTERNAL CONNECTIONS

External connections are made according to the elementary diagram, Figures 21 through 25. These are general diagrams incorporating all of the available options. Connection need not be made to those terminals associated with options that will not be used.

## INTERCONNECTION CABLES

Interconnection cables are included as part of the TLS units. The cable sockets located on the back of the cases are marked, and should be connected like-mark-tolike-mark, i.e. PL4 measuring unit to PL4 logic unit. All cables are the same, and the length is such that the cases must be mounted one on top of the other. The No.6 socket on the logic unit is the output port for optional monitoring points. The connection plugs snap into the sockets, which are keyed for proper polarity.

## SPECIFICATIONS

## RATINGS

Rated	Frequency	0	50 or 60 hertz
	Voltage		
	5	0	100 to 120 volts AC
Rated	Current	0	$I_N = 1$ or 5 amperes
DC Cor	ntrol Voltage	0	48 VDC - Operating Range: 34- 60 VDC 110/125 - Operating Range: 88-150 VDC 220/250 - Operating Range: 176-300 VDC
Cont Thre	um Permissible Currents tinuous se Seconds Second	0	2 x IN 50 x IN 100 x IN
Cont	m Permissible AC Voltage inuous Minute (one per hour)		2.0 x rated 3.5 x rated
For	t Temperature Range Storage Operation	0	-40° to +65° Celsius The TLS has been designed for continuous operation between -20°C and +55°C per ANSI Standard C37.90. In addition, the TLS will not malfunction, nor be damaged by, operation at temperatures up to +65°C.
Insula	tion-Test Voltage	0	2 kV 50/60 hertz, one minute
Impuls	e-Voltage Withstand	0	5 kV peak, 1.2/50 milliseconds, 0.5 joule
Interf	erence-Test Withstand	0	ANSI/IEEE C37.90 and IEC 255-5
<b>BURDENS</b>			
Curren	t Circuits	0 0	0.03 ohm $\angle$ 5°, IN = 5 amps 0.14 ohm $\angle$ 30°, IN = 1 amp
Voltag	e Circuits	0 0	0.2 VA ∠ 49°, 60 hertz 0.24 VA ∠ 48°, 50 hertz
DC Bat	tery (for contact converters)	0	1.4 milliamperes each
and	tery (for Power Supply Telephone Relays) LL VOLTAGE RATINGS		<u>Normal Tripped</u> 13 watts 40 watts
<u>Contact Da</u>	<u>ta</u>		·
Trip O	utputs	0	Continuous rating = 3 amperes Make and carry for tripping duty (per ANSI C37.90) 30 amps Break 180 VA resistive at 125/250 VDC
## SPECIFICATIONS

(Continued)

Auxiliary Outputs (including Alarms)	0 0 0 0	Break 60 VA inductive at 125/250 VDC Continuous rating = 3 amperes Make and carry for 30 seconds 5 amperes Break 25 watts inductive at 125/250 VDC Make and carry continuously 50 watts Maximum of 250 volts or 0.5 ampere
DLA and Channel Control Contacts	0	10 watts 250 VDC maximum 0.5 amp maximum

Reach Settings in Ohms

FUNCTION	MODULE	RANGE	RESOLUTION	MULTIPLIERS
M1/MG1	AFM101/104	(1 to 25) x $\frac{5}{IN}$	$0.1 \times \frac{5}{IN}$	0.1, 0.25, 1.0
M2/MG2 (1)	AFM102/105	(2 to 50) x $\frac{5}{IN}$	0.2 x $\frac{5}{IN}$	0.1, 0.25, 1.0
MT/MTG	AFM103/106	(3 to 75) x $\frac{5}{10}$	0.3 x $\frac{5}{IN}$	0.1, 0.25, 1.0
SWITCHED(2)	VMM101/102	(1 to 10 x Z1	0.05	0.1, 0.25, 1.0
МВ	ABM101/102	(2 to 50) x <u>5</u> IN	$0.2 \times \frac{5}{IN}$	
NB	VMM101/102	(5 to 80) x $\frac{5}{IN}$	5 x <u>5</u> IN	

#### NOTES: (1) AFM102/105 may be used as:

MT/MTG in two-zone units

M2/MG2 in three-zone units

(2) Switched distance function based on M1/MG1

#### Replica Impedance Angle Settings

FUNCTION	MODULE	RANGE	RESOLUTION
∠ZR1(3)	ISM101	50° to 85°	5°
∠ZR0(3)	ISM101	50° to 85°	5°

NOTE:

(3) One replica impedance angle adjustment is used for all zones of protection

# Characteristic Timer Settings

FUNCTION	MODULE	RANGE	RESOLUTION
M1/MG1	UTM101	64° to 127°	1°
M2/MG2	UTM102	64° to 127°	1°
MT/MTG	UTM101	64° to 127°	1°
NB	ULM131	64° to 96°	2°
MOB/MOBG	ULM121	32° to 126°	- 2°

## Adjustable Logic Timers

TIMER	MODULE	PU/DO	RANGE	RESOLUTION	DESCRIPTION
TL1	ULM141	PU	1 - 15 ms	1 ms	Trip Integrator
TL2	ULM141	PU	.2 - 3.15 sec	0.05 sec	Zone 2
TL3	ULM141	PU	.4 - 6.3 sec	0.1 sec	Zone 3
TL4	ULM131	PU	.4 - 6.3 sec	0.1 sec	Zone 4
TL6	ULM121	PU	1 - 7.75 cyc	0.25 cyc	Out of Step
TL13	ULM111	PU	1 – 15 ms	1 ms	DTT
TL14	ULM141	PU	2 – 15 ms	1 ms	Coordination
TL15	ULM141	PU	2 – 15 ms	1 ms	Repeat Block
TL16	ULM141	PU	.5 - 7.5 cyc	0.5 cyc	Weak Infeed
TL22	ULM141	PU	.4 - 6.3 sec	0.1 sec	DTT Reclose Block
TL24	ULM131	DO	0.5 - 7.5 cyc	0.5 cyc	NB Dropout
TL25	ULM131	DO	0.5 - 7.5 cyc	0.5 cyc	MB Dropout

## <u>ACCURACY</u>

Distance Measuring Units	o Reach: ± 5% of setting at angle of maximum reach
	o Angle of Maximum Reach: ± 30 of setting
Zone Timers	o ± 3% of setting
Characteristic Timers	o ± 10
DIMENSIONS	
Standard rack-mounted unit	o 6 15/16 inches (176 millimeters) high o 19 1/16 inches (484 millimeters) wide (Standard 19-inch rack) o 14 inches (356 millimeters) deep (including terminal blocks

# <u>WEIGHT</u>

Standard rack-mounted unit weighs approximately 33 pounds (15 kilograms) net.

#### GEK-86638

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\* Figure 1 (0285A8279 [3]) Internal Switches, Links and Front Panel, ABM101, ABM102 Modules



\* Figure 2 (0285A8274 [2]) Internal Switches, Links and Front Panel, AFM10(-) Module



Figure 3 (0285A8270-1) Internal Switches, Links and Front Panel, AFM201, AFM202 Modules



\* Figure 4 (0285A8280 [2]) Internal Switches and Front Panel, ETM101 Module Indicates revision

\*



\* Figure 5 (0285A8275 [2]) Internal Switches and Front Panel, ETM102 Module Indicates revision

\*



Figure 6 (0285A8888) Internal Links and Front Panel, IOM101 Module



\* Figure 7A (0285A8273 [3]) Internal Switches and Front Panel, ISM101, ISM102 Modules



Figure 7B (0286A2547) Internal Fuse and Front Panel, PSM12(-) Module



\* Figure 8 (0285A8271 [3]) Internal Switches and Front Panel, ULM101 Module



\* Figure 9 (0285A8272 [4]) Internal Switches and Front Panel, ULM111 Module Indicates revision

\*



Figure 10 (0285A8281-1) Internal Switches and Front Panel, ULM121 Module



Figure 11 (0285A8276-1) Internal Switches and Front Panel, ULM131 Module



\* Figure 12 (0285A8277 [3]) Internal Switches and Front Panel, ULM141 Module
\* Indicates revision



Figure 13 (0285A8278-2) Internal Switches and Front Panel, UTM101 Module



Figure 14 (0285A9114) Internal Switches and Front Panel, UTM102 Module



\* Figure 15 (0285A8282 [3]) Internal Switches, Links and Front Panel, VMM101, VMM102 Module

			•	0000			
					ZONE MI/MGI	ZONE MI/MGI; MT/MTG	THREE MI/MGI;MZ/MG2;MT/MIG
MODULE LOCATION	FUNCTION	ON BOARD Switches	ON BOARD LINKS	FRONT PANEL SWITCHES	RATED FREQUENCY + 50H2 + 50H2	19 20 14 19 19 19 19 19	+ 50 HZ
∢	DLA	NONE	NONE	W NON	10M 202 202	=	=
υ	MB FAULT DET I L D I CPH SHIFT I CPH SHIFT	<u> </u>	IO SHIFT IZ SHIFT OFFSET POL	/D(REACH)	A6M 101 102	=	=
ш	OLARIZING ZONE SW NB 10 SUP'V 310Z REST	I <sub>2</sub> L D KI <sub>2</sub> E NB OFFSET MI/MGI OFFSET MT/MTG	IC REST MULT MI VP	11	VMM -00- -05	z	2
ა	MT/MTG F COINCIDENCE LOGIC	VP SENS Q-Q V P SENS Q-G		φ-φ[	ETM 102 08 08 BLANK	E T M 102 102	-
ر	MT OPERATE CIRCUIT	S A FIL O SUP	12 อ	NONE	AFM 201 202 202 202 202 202 8LANK	4FM 201 202	=
L	M TG OPERATE CIRCUIT	KO A FIL O SUP	ם 117 איערד גבוס	12 (REACH) MULT	AFM 102 105 Blank	4FM 102 105	201 201 201
z	MI/MGI COINCIDENCE LOGIC	IO SEAS PHA PHA PHA PHA PHA SEAS CPS SEAS CPS SEAS		τφ-φ	E 101 101 101 08 101 101	₩.10 101 101	=
æ	MI OPERATE CIRCUIT	S A FiL O Sup	BFIL	NONE	AFM 201 202 08 08 BLANK	AF M 201 202	=
	CIRCUIT	KO S FIL O SUP	B FIL MULT L ZRO	J. (REACHU MULT	AFM 101 104 104 104 104	0101 01 01	=
>	INTERFAC	1	NOM	& ₹ 0 5 0	15M 101 102	15M 101 102	=
	MAGNETICS AND TRIPPING RELAYS				MGM114 + (IN = 1 AMP) OR 15 + (IN = 5 AMP) MGM115 + (IN = 5 AMP)		
- - -	TEST PLUG				N A F		
	T R N L J G E C A	V     T     R     N     L     J     G     E     C     A       MAGNETICS     INTERFACE MGI     MI     MI/MGI     MT     MT/MTG     MB     MB       MAGNETICS     INTERFACE MGI     MI     MI/MGI     MT     MT/MTG     MB     MB       TPIPPING     UV LU     OFERATE OPERATE OPERATE CONCIDENCE POERATE CONCIDENCE TO BASHIT     MB     MB     MB       TPIPPING     18     LD     CFRCUIT     CIRCUIT     CIRCUIT     CIRCUIT     CIRCUIT     CIRCUIT     DLA       RELAYS     17     LD     CFRCUIT     CIRCUIT     CIRCUIT <td>NAGNETICS     V     T     R     N     L     J     G     E     C     A       MAGNETICS     INTERACE     MGI     MI/MGI     MI     MI/MGI     MT     MT/MG     MT/MTG     ME     M       AND     U/V LU     OPERATE     OPERATE<!--</td--><td>V     T     R     N     L     J     G     E     C     A       MAGNETICS     U/V LU OPERATE MGI     MI MI/MGI     MI/MGI     MI/MGI     MI/MGI     MI/MGI     MI/MGI       TPIPPING     U/V LU OPERATE CONNECTENCE ME IN MI/MGI     IN MI/MGI     MI/MGI     MI/MGI     MI       TPIPPING     U/V LU OPERATE OPERATE CONNECTENCE OPERATE CONNECTENCE     NI/MGI     MI/MGI     MI/MGI     MI/MGI       TPIPPING     IB     KO     IB     KO     IB     MI/MGI     IB     MI/MGI       TPIPPING     IIT     LO     CTRCUT     LOGIC     CIRCUT     CIRCUT     IIL     DLA       TPIPPING     IIT     L     LO     CIRCUT     CIRCUT     CIRCUT     IIL     DLA       TPIPPING     IIT     L     LOGIC     CIRCUT     CIRCUT     CIRCUT     IIL     DLA       IIT     L     L     LOGIC     CIRCUT     CIRCUT     CIRCUT     CIRCUT     CIRCUT     CIRCUT       IIT     L     L     A     L     A     L     DLA       IIT     L     L     L     L     L     L     L     L       IIT     L     L     A     L     A     L     L</td><td>V     T     R     N     L     J     G     E     C     A       TPIPPING     U/V LU OPERATE MGI     MII     MI/MGI     MTG     MT     MT/MTG     FOUTUTET     FOUTUTET       TPIPPING     U/V LU OPERATE CONCIDENCE OFERATE CONCIDENCE NS     U/V LU OPERATE CONCIDENCE OFERATE CONCIDENCE NS     NI/MT/MTG     FOUTUTET     &lt;</td><td>V         T         R         N         L         J         G         E         C         A         MOULE           TPIPPING         IT L0         IT L0         MITMIGI         MT         MT/MTG         RQUENT         Location           TPIPPING         TPIPUG         IFL         D         G         E         C         A         MOULE           TPIPPING         TPIPPING         IFL         DOSIC         CREATE         CREAT</td><td><math display="block"> \begin{array}{ c c c c c c c c c c c c c c c c c c c</math></td></td>	NAGNETICS     V     T     R     N     L     J     G     E     C     A       MAGNETICS     INTERACE     MGI     MI/MGI     MI     MI/MGI     MT     MT/MG     MT/MTG     ME     M       AND     U/V LU     OPERATE     OPERATE </td <td>V     T     R     N     L     J     G     E     C     A       MAGNETICS     U/V LU OPERATE MGI     MI MI/MGI     MI/MGI     MI/MGI     MI/MGI     MI/MGI     MI/MGI       TPIPPING     U/V LU OPERATE CONNECTENCE ME IN MI/MGI     IN MI/MGI     MI/MGI     MI/MGI     MI       TPIPPING     U/V LU OPERATE OPERATE CONNECTENCE OPERATE CONNECTENCE     NI/MGI     MI/MGI     MI/MGI     MI/MGI       TPIPPING     IB     KO     IB     KO     IB     MI/MGI     IB     MI/MGI       TPIPPING     IIT     LO     CTRCUT     LOGIC     CIRCUT     CIRCUT     IIL     DLA       TPIPPING     IIT     L     LO     CIRCUT     CIRCUT     CIRCUT     IIL     DLA       TPIPPING     IIT     L     LOGIC     CIRCUT     CIRCUT     CIRCUT     IIL     DLA       IIT     L     L     LOGIC     CIRCUT     CIRCUT     CIRCUT     CIRCUT     CIRCUT     CIRCUT       IIT     L     L     A     L     A     L     DLA       IIT     L     L     L     L     L     L     L     L       IIT     L     L     A     L     A     L     L</td> <td>V     T     R     N     L     J     G     E     C     A       TPIPPING     U/V LU OPERATE MGI     MII     MI/MGI     MTG     MT     MT/MTG     FOUTUTET     FOUTUTET       TPIPPING     U/V LU OPERATE CONCIDENCE OFERATE CONCIDENCE NS     U/V LU OPERATE CONCIDENCE OFERATE CONCIDENCE NS     NI/MT/MTG     FOUTUTET     &lt;</td> <td>V         T         R         N         L         J         G         E         C         A         MOULE           TPIPPING         IT L0         IT L0         MITMIGI         MT         MT/MTG         RQUENT         Location           TPIPPING         TPIPUG         IFL         D         G         E         C         A         MOULE           TPIPPING         TPIPPING         IFL         DOSIC         CREATE         CREAT</td> <td><math display="block"> \begin{array}{ c c c c c c c c c c c c c c c c c c c</math></td>	V     T     R     N     L     J     G     E     C     A       MAGNETICS     U/V LU OPERATE MGI     MI MI/MGI     MI/MGI     MI/MGI     MI/MGI     MI/MGI     MI/MGI       TPIPPING     U/V LU OPERATE CONNECTENCE ME IN MI/MGI     IN MI/MGI     MI/MGI     MI/MGI     MI       TPIPPING     U/V LU OPERATE OPERATE CONNECTENCE OPERATE CONNECTENCE     NI/MGI     MI/MGI     MI/MGI     MI/MGI       TPIPPING     IB     KO     IB     KO     IB     MI/MGI     IB     MI/MGI       TPIPPING     IIT     LO     CTRCUT     LOGIC     CIRCUT     CIRCUT     IIL     DLA       TPIPPING     IIT     L     LO     CIRCUT     CIRCUT     CIRCUT     IIL     DLA       TPIPPING     IIT     L     LOGIC     CIRCUT     CIRCUT     CIRCUT     IIL     DLA       IIT     L     L     LOGIC     CIRCUT     CIRCUT     CIRCUT     CIRCUT     CIRCUT     CIRCUT       IIT     L     L     A     L     A     L     DLA       IIT     L     L     L     L     L     L     L     L       IIT     L     L     A     L     A     L     L	V     T     R     N     L     J     G     E     C     A       TPIPPING     U/V LU OPERATE MGI     MII     MI/MGI     MTG     MT     MT/MTG     FOUTUTET     FOUTUTET       TPIPPING     U/V LU OPERATE CONCIDENCE OFERATE CONCIDENCE NS     U/V LU OPERATE CONCIDENCE OFERATE CONCIDENCE NS     NI/MT/MTG     FOUTUTET     <	V         T         R         N         L         J         G         E         C         A         MOULE           TPIPPING         IT L0         IT L0         MITMIGI         MT         MT/MTG         RQUENT         Location           TPIPPING         TPIPUG         IFL         D         G         E         C         A         MOULE           TPIPPING         TPIPPING         IFL         DOSIC         CREATE         CREAT	$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$

Figure 16 (0164B9687 Sh 1 [2]) Module Location and Setting Diagram, Measuring Unit Case (A)

	MODULE	FUNCTION	ON BOARD SWITCHES			Dri Board Links		FRONT PANEL SWITCHES	ONE OR THO ZONE (NJ/MG) OR (NJ/NTG); (MJ/NE) AHD MJ/NTG) THREE ZONES (NVVNI; WZ/M37; NT/NTG)
	A	COINCIDE NGE LOGIC	10.SENS PH-A PH-B	S S S S S S S S S S S S S S S S S S S		ENON		Ιφ-φ	ETMI01
M2 / MG2	υ	M2 OPERATE CIRCUIT	S A FIL O SUP			B FiL		NONE	BLANK AFM202
M2/	Е	MG2 OPERATE CIRCUIT	KO S A FIL	O SUP		B FIL MULT ERO		A (REACH) MULT	BLANK AFMIO5
	6	CHARACTERISTIC TIMER (FOR M2/MG2)	MG2 MG2			NONE		NONE	BLANK UTMIO2
	×	CHARACTERISTIC CHARACTERISTIC TIMERS (FOR M2/MG2)	TIMERS MI CHAR MGI CHAR	MT CHAR MG CHAR MG CHAR DGIC LOGIC SWITCH MI UNIT SUPERVISION		NONE		NONE	UTMIOI
	2	LOGIC CONE 243 TIMERS	TLIMERS TLI TL2	TL3 TL15 TL15 TL15 TL16 TL16 TL22 SMITCHES SMITCHES	1444 10 11 1	BNON		NONE	0LMI41
	٩	SUPERVISION NB ZONE 4	TIMERS TL4 TL24	TL25 NB CHAR LOGIC SWITCH 131A		NONE		NONE	NLMI31
	s	KEYING MOB	TIMERS TL6 MOB CHAR	MOEG CHAR LOGIC SWITCHES 121A 1218 1218 1216 1216 1216		NONE		NOtIE	121WISI
	5	TARGETS	TIMER TLI5 LOGIC	5% TCHES 11A		NONE		RESET	ULMIII H
	*	SINGLE POLE POLE	LOGIC SWITCH IOIA	80 0		3 N CN		NONE	
	¥	CONTACT CONVERTERS	NONE			VOLTAGE SELECT124		NONE	100W001
	ZA	AUX OUTPUT RELAYS	NONE	RELAY FUNCTION FUNCTION K1-1 K1-2 K2-1 K2-2 IR-1 K1-9 IR-1 R1-9 LR-2 R1-92 LR-2 R1-92 LR-2 R1-92 LR-2 BT-92-1	671-08-3 871-08-3 871-00-3	6F1-0C-3	NONE	MONE	10M203
	zc	AUX OUTPUT RELAYS	NONE	FUNCTION FUNCTION K1 - 1 K2 - 1 IR - 2 IR - 2 LR - 1 LR - 2 LR - 1	R13-01 BF1-04-1	EFFI CLOCK	NONE	NONE	10M203
	35	POWER SUPPLY	NONE			VOLTAGE SELECTION LINK		ON/OFF	PSM21
		TEST PLUG	NONE			NONE		NONE	WdL.

Figure 17 (0164B9687 Sh 2 2) Module Location and Setting Diagram, Logic Unit Case (B)



Figure 18 (0183B3657 Sh 2 [2]) Test Circuit for Replica Impedance Angle and Reach Tests



Figure 19 (0183B3657 Sh 3 [2]) Test Circuit for NB and Fault Detector Tests

					+						
CARD EXTENDER PIN NC.		48	12	=	2	37	42	20	21	4	35
NODULE	EXTENCER	ABUIO-1	ISMIO(-)								
	rh W	TP9	1	1	1	TP 9	IPH	TP13	TPI3	TPII	6 d 1
XTM TERMINAL NO.	×	ı ı	TP22	r P23	1 P 24	1	1	ł	I	ł	1
MINAL	nji	АНГ	1	ı	I	АНІ	АН 2	AH 3	AH3	AH 2	1 HY
TERMINAL BOARD NO.	×	!	AG2	AG3	AG4	1	1	1	1	1	1
	TEST	1	A	63	ပ	A	æ	U	υ	8	۲
FUNCTION UNDER	TEST	-1	> 1	2	7	18	18	18	11	11	11



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Figure 20 (0183B3657 Sh 4 [2]) Test Circuit for Level Detector Tests



Figure 21 (0138B7776 Sh 1 [1]) Elementary Diagram for TLS1000 System





Figure 23 (0138B7776 Sh 3 [2]) Elementary Diagram for TLS1000 System



Figure 24 (0138B7776 Sh 4 [2]) Elementary Diagram for TLS1000 System



Figure 25 (0138B7776 Sh 5 [2]) Elementary Diagram for TLS1000 System



Figure 26 (0179C7137 Sh 1 [1]) Block Diagram of Voltage Processing Circuit



Figure 27 (0179C7137 Sh 2 [1]) Block Diagram of Current Processing Circuit



Figure 28 (0179C7137 Sh 3) Block Diagram of Voltage Polarizing Circuit



Figure 29 (0179C7137 Sh 4 [1]) Block Diagram of Reach Adjustment and Operate Circuits



Figure 30 (0179C7137 Sh 5 [1]) Block Diagram of M1, MG1 and MB Coincidence Logic and Timers



Figure 31 (0179C7137 Sh 6 [1]) Block Diagram of MT, MOBØ and MOBG Coincidence Logic and Timers



Figure 32 (0138B7600 Sh 3) Outline & Mounting Dimensions and TB Locations for Modular Case (TLS 1 & 2 Zone)



Figure 33 (0138B7600 Sh 4 [1]) Outline & Mounting Dimensions and TB Locations for Modular Case (TLS 3 Zone)



GEK-86638

Figure 34 (8043769) Photograph, TLS Measuring Unit - Front View



Figure 35 (8043771) Photograph, TLS Logic Unit - Front View



Figure 36 (8043773) Photograph, TLS Measuring and Logic Units - Back View (3/92)(200) GENERAL ELECTRIC METER AND CONTROL BUSINESS DEPT., MALVERN, PA 19355