Digital Relays and Capacitive Voltage Transformers: Balancing Speed and Transient Overreach

DISTANCE RELAYS AND
CAPACITIVE VOLTAGE TRANSFORMERS —
BALANCING SPEED AND TRANSIENT OVERREACH

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1. Introduction

Capacitive Voltage Transformers (CVTs) are the predominant source of the voltage signals for distance relays in High Voltage (HV) and Extra High Voltage (EHV) systems.

CVTs provide a cost-efficient way of obtaining secondary voltages for EHV systems. They create however, certain problems for distance relays. During line faults, when the primary voltage collapses and the energy stored in the stack capacitors and the tuning reactor of a CVT needs to be dissipated, the CVT generates severe transients that affect the performance of protective relays.

The CVT caused transients are of significant magnitude and comparatively long duration. This becomes particularly important for large Source Impedance Ratios (SIR — the ratio of the system equivalent impedance and the relay reach impedance) when the fault loop voltage can be as low as a few percent of the nominal voltage for faults at the relay reach point. Such a small signal is buried beneath the CVT transient making it extremely difficult to distinguish quickly between faults at the reach point and faults within the protection zone.

Electromechanical relays can cope with unfavorable CVT transients due to their natural mechanical inertia at the expense of slower operation.

Digital relays are designed for high-speed tripping and therefore they face certain CVT-related problems.

CVT transients can affect both the transient overreach (a relay operates during faults located out of its set reach) and the speed of operation (slow tripping for high SIRs) and directionality.

This paper begins with analysis of the CVT transients (Section 2). The influence of the CVT transients on the performance of digital distance relays follows (Sections 3 and 4). A new algorithm balancing transient overreach and speed of operation, its hardware implementation and the results of testing are presented in Section 5. The paper discusses transient overreach issues rather then directionality as the latter is effectively controlled with the memory polarization.

2. CVT Transients

2.1. Equivalent circuit of a CVT

A generic CVT consists of a capacitve voltage divider, tuning reactor, step-down transformer and ferroresonance suppression circuit (the additional communication equipment is not siginificant in these considerations).

Under line fault conditions, when the voltage drops and there is no threat of exceeding the knee-point of the magnetizing characteristic of the step-down transformer, a CVT can be represented by the equivalent linear circuit as shown in Figure 1. The analyzed CVT contains a particular ferroresonance suppression circuit. The analysis, however, is similar to other types of ferroresonance circuits. In this paper we will follow the CVT model shown in Figure 1.

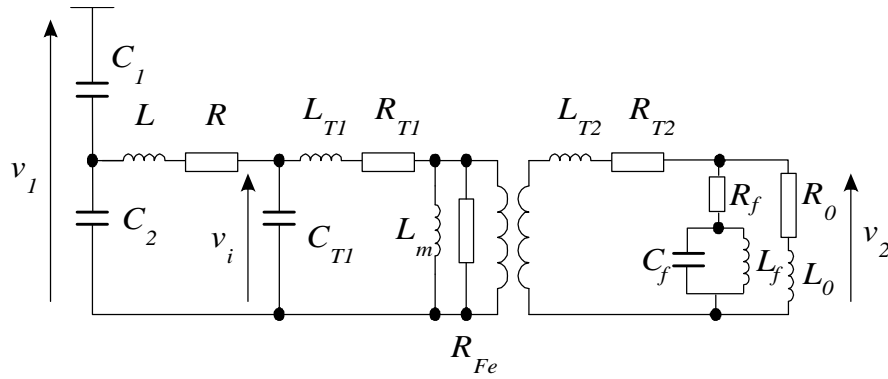The linear circuit of Figure 1 can be further simplified as shown in Figure 2.

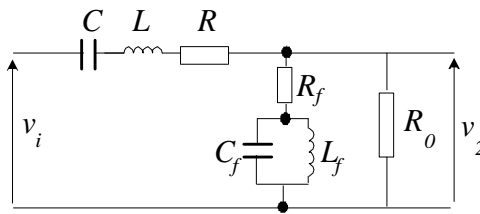Figure 1. Equivalent circuit diagram of a CVT.

Figure 2. Simplified model of a CVT from Figure 1.

The parameters in the circuit of Figure 2 are:

C	sum of the stack capacitances,
L, R	equivalent inductance and resistance, respectively, of the tuning reactor and the step down transformer,
R_0	burden resistance,
f	subscript for parameters of the anti-resonance circuit.

For illustration, in this paper we will follow a numerical example of the following two sample 500kV CVTs (all the secondary parameters are re-calculated for the intermediate voltage level):

- CVT-1 ("high-C CVT"):

$$
\begin{aligned}
R_0 &= 1.03997 \cdot 10^5 && \text{— load resistance, } \Omega \\
L_f &= 315.3 && \text{— suppression inductance, H} \\
C_f &= 0.0285 \cdot 10^{-6} && \text{— suppression capacitance, F} \\
R_f &= 77379 && \text{— suppression resistance, } \Omega \\
R &= 3289 && \text{— resistance, } \Omega \\
C &= 9.1605 \cdot 10^{-8} && \text{— sum of dividing capacitances, F} \\
L &= 76.136 && \text{— inductance, H}
\end{aligned}
$$

- CVT-2 ("extra high-C CVT"):

$$
\begin{aligned}
R_0 &= 2.08584 \cdot 10^5 && \text{— load resistance, } \Omega \\
L_f &= 616.35 && \text{— suppression inductance, H} \\
C_f &= 0.01134 \cdot 10^{-6} && \text{— suppression capacitance, F} \\
R_f &= 148519 && \text{— suppression resistance, } \Omega
\end{aligned}
$$

R	=	1536	— resistance, Ω
C	=	$0.162442 \cdot 10^{-6}$	— sum of dividing capacitances, F
L	=	48.136	— inductance, H

2.2. CVT transients – sample waveforms

Figures 3 and 4 present examples of CVT operation during a fault occurring at the zero crossing and maximum of the primary voltage, respectively.

As seen from the figures, the CVT transients can last for up to two cycles and reach the magnitude of up to 40% of the nominal voltage.
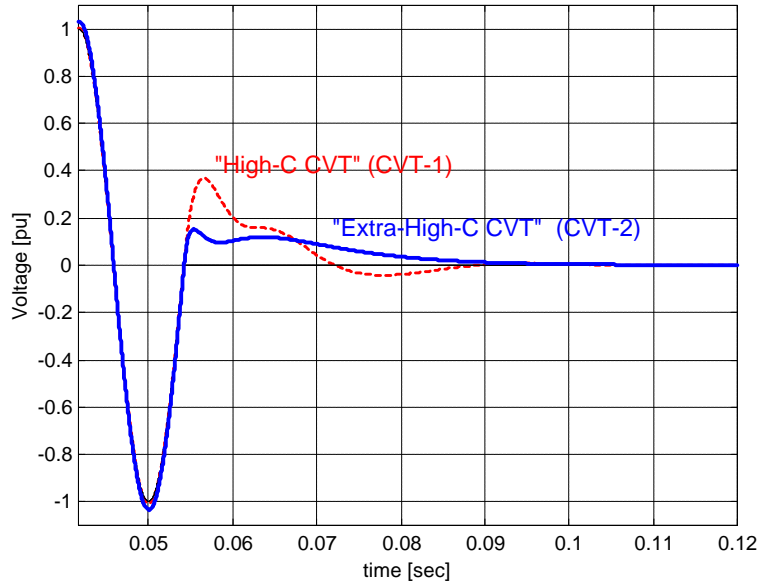

Figure 3. Sample transients for high- and extra-high-C CVTs.
The primary voltage drops to zero at the zero crossing.

Subsection 2.3 provides a detailed mathematical model of the CVT induced noise. Subsection 2.4 discusses the factors that control the CVT transients in detail.

2.3. Transfer function and eigenvalues of a CVT

The transfer function derived for the model of Figure 2 is:

$$G_{CVT}(s) = \frac{A_3 s^3 + A_2 s^2 + A_1 s}{B_4 s^4 + B_3 s^3 + B_2 s^2 + B_1 s + B_0} \tag{1}$$
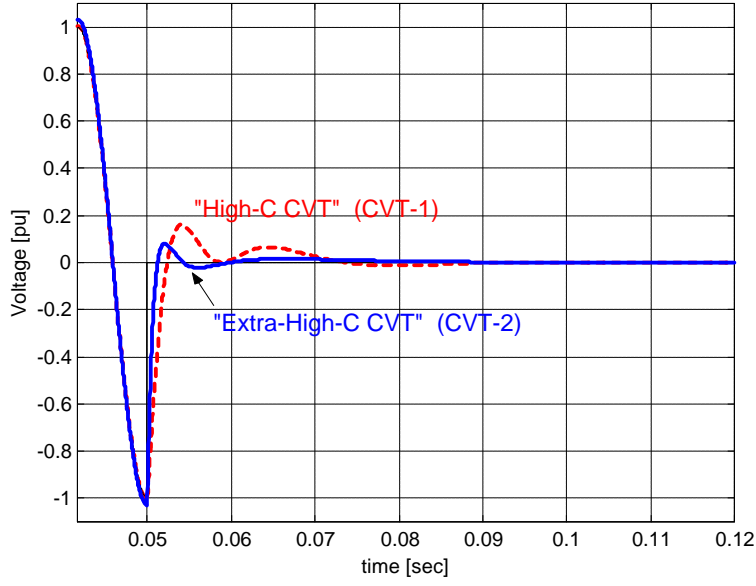
where:

$$A_3 = L_f C_f R_f R_0 C \; ;$$

Figure 4. Sample transients for high- and extra-high-C CVTs.
The primary voltage drops to zero from the voltage peak.

$A_2 = L_f R_0 C$;

$A_1 = R_f R_0 C$;

$B_4 = L_f C_f (R_f + R_0) LC$;

$B_3 = LCL_f + RCL_f C_f (R_f + R_0) + L_f C_f R_f R_0 C$;

$B_2 = LC(R_f + R_0) + RCL_f + L_f C_f (R_f + R_0) + L_f R_0 C$

$B_1 = RC(R_f + R_0) + L_f + R_f R_0 C$;

$B_0 = R_f + R_0$

For example, for CVT-1 (example of a high-C CVT) one obtains:

$$G_{CVT(s)} = \frac{582.739\,s\left(s^2 + 453.5s + 1.113 \cdot 10^5\right)}{\left(s^2 + 192.5s + 4.401 \cdot 10^4\right) \cdot \left(s^2 + 626.9s + 3.626 \cdot 10^5\right)} \tag{2a}$$

and for CVT-2 (example of a extra high-C CVT):

$$G_{CVT(s)} = \frac{1784.245\,s\left(s^2 + 593.8s + 1.431 \cdot 10^5\right)}{(s + 993.8) \cdot (s + 725) \cdot (s + 238.6) \cdot (s + 105.4)} \tag{2b}$$

The eigenvalues determining the nature of the transient induced by the CVT can be calculated now from the transfer function. For the two considered CVTs the eigenvalues are:

- CVT-1 (high-C CVT):

$$-313.43 + j514.13$$
$$-313.43 - j514.13$$
$$-96.27 \; + j186.39$$
$$-96.27 \; - j186.39$$

The above values determine two aperiodically decaying oscillatory components with the following time constants and frequencies, respectively:

$$T = 3.1905 \;\; [ms] \quad \text{and} \quad f = 81.8261 \; [Hz]$$
$$T = 10.3876 \; [ms] \quad \text{and} \quad f = 29.6647 \; [Hz]$$

- CVT-2 (extra high-C CVT):

$$-993.8011$$
$$-724.9701$$
$$-238.6495$$
$$-105.3577$$

The above values determine four aperiodically decaying dc components with the time constants respectively:

$$1.0062 \; [ms]$$
$$1.3794 \; [ms]$$
$$4.1902 \; [ms]$$
$$9.4915 \; [ms]$$

An extra-high-C CVT has all its eigenvalues real. This results in a decaying non-oscillatory distortion (see Figure 5 for illustration). A high-C CVT has all its eigenvalues complex (pairs of conjugate values) resulting in decaying oscillatory distortion (see Figure 6 for illustration).

From the digital signal processing point of view, the values of parameters of the CVT noise do not make the filtering easy. The frequencies of the oscillatory components (high-C CVT) are quite close to 60Hz where the information signal is. In addition, their time constants are in the order of the power cycle. The time constants of the dc components (extra high-C CVT) are of the same order (maximum-to-minimum ratio is about 10) — this means that none of the components can be neglected and an estimator would have to trace and suppress all four decaying dc components.

Based on the above observations it is justified to assume the following signal model for the secondary voltage of a CVT:

$$v_{(t)} = v_{CVT(t)} + V_1 \cos(w_1 t + j_1) + v_{noise(t)} \tag{3}$$

where:

v_{noise} is a high frequency noise including harmonics and decaying high frequency oscillatory components,

V_1, φ_1 are parameters of a fundamental frequency phasor to be filtered or estimated,

v_{CVT} is a CVT induced transient assuming one of the following forms:

$$v_{CVT(t)} = \sum_{k=1}^{4} A_k \exp\left(-\frac{t}{T_k}\right) \tag{4a}$$

or

$$v_{CVT(t)} = \sum_{k=1}^{2} A_k \cos(\omega_{0k} t + \varphi_{0k}) \exp\left(-\frac{t}{T_k}\right) \tag{4b}$$

or

$$v_{CVT(t)} = A_1 \cos(\omega_0 t + \varphi_0) \exp\left(-\frac{t}{T_1}\right) + \sum_{k=2}^{3} A_k \exp\left(-\frac{t}{T_k}\right) \tag{4c}$$

Equations (4) mean that the CVT induced transient can be:

- combination of four aperiodically decaying dc components (extra high-C CVT),
- combination of two oscillatory decaying components (high-C CVT),
- combination of one oscillatory decaying component and two aperiodically decaying dc components (general case).

Certainly, the parameters of the voltage signal model are unknown. The presented numerical examples can be used as some indication of the range and relations between the time constants and frequencies. The initial magnitudes and angles in (4) depend on the pre-fault conditions and the fault inception angle.

Ideally, the signal model (3)-(4) should be used to design either a filter or a phasor estimator for the voltage signal for a digital distance relay.

2.4. CVT transients – the contributing factors

The mathematical relations given by the signal model of the "CVT noise" (3)-(4) have the following explanation.

As the CVT-generated transients result from the energy stored in the stack capacitors and the tuning reactor, the transients are basically controlled by the parameters of the CVT itself and the point on wave at which the fault occurs.

The compensating reactor is tuned by a CVT manufacturer to ensure zero phase shift between the primary and secondary voltages, and from this perspective, the inductance of the reactor is a constant value dependent only on the capacitances used to set-up the divider.

The shunt parameters of the step-down transformer practically do not contribute to the CVT transients during fault conditions when the voltage collapses.

Consequently, the transients are basically controlled by the following factors:

- Sum of the stack capacitances.
- Shape and parameters of the ferroresonance suppression circuits.
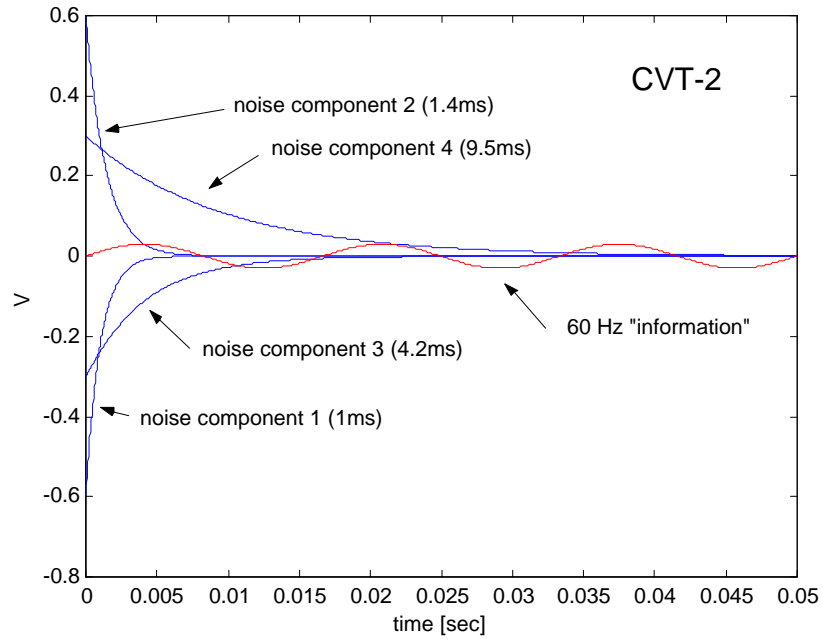- CVT burden.
- Point on wave when a fault occurs.

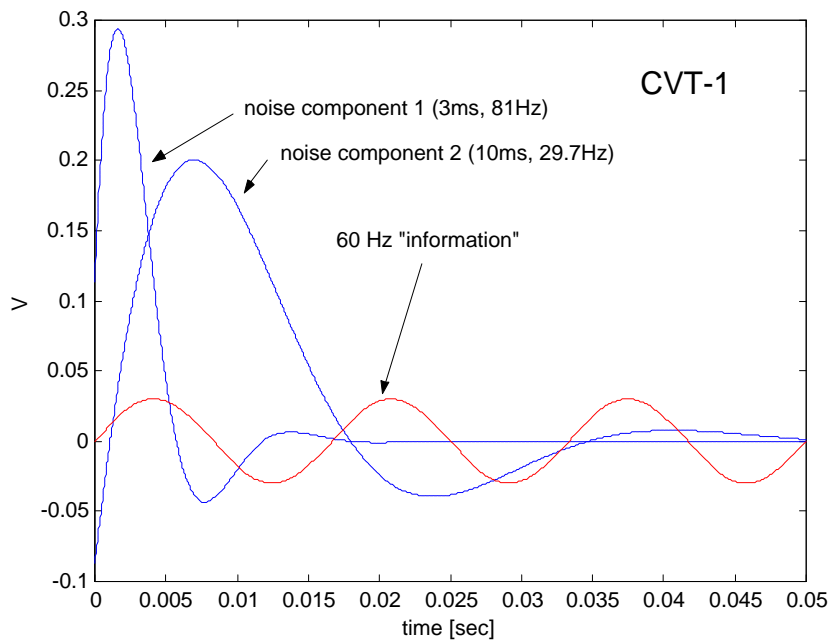Figure 5. Comparison of the components of the CVT noise with a low 60Hz signal (extra high-C CVT).

Figure 6. Comparison of the components of the CVT noise with a low 60Hz signal (high-C CVT).

Sum of stack capacitances

The higher the sum of the stack capacitances, the lower the magnitude of the transients. Therefore, judging only from the magnitude of the CVT transient, one should recommend CVTs with higher sum of the stack capacitances to be used to feed distance relays with the voltage signals.

On the other hand, the CVTs with larger capacitors are more expensive. Also, the behaviour of a distance relay depends on the applied filtering and measuring algorithms. In many instances the magnitude **alone** of the CVT transient is of a secondary importance for transient overreach and speed of operation.

Typically, the sum of the stack capacitances is in the range of 100nF. From this perspective, CVTs are classified as of "normal-C", "high-C" and "extra-high-C" types. The threshold values are rather fuzzy. For example, the CVT-1 used in this paper has its stack capacitances summing to 91.6nF, while the CVT-2 – to 162.4nF.

When testing distance relays one should consider a CVT model of the high-C type first. It is, however, necessary to test a given relay using different types of CVTs as the magnitude alone of the CVT transient may be of a secondary importance for some algorithms.

Ferroresonance suppression circuit

A ferroresonance suppression circuit is designed to prevent subsynchronous oscillations due to saturation of the core of a step-down transformer during overvoltage conditions.

The ferroresonance circuit loads a CVT and creates an extra path — apart from the burden — for the dissipating energy. Therefore, the damping circuit has significant impact on the characteristic of the CVT transients.

A specific design of a ferroresonance damping circuit is often treated as proprietary information and is seldom available. However, there are two generic models of a ferroresonance suppression circuit that will be considered.

One design consists of a resistor in series with a parallel LC branch. The LC subcircuit is tuned to the nominal frequency (60Hz or 50Hz) and behaves as an open circuit at the nominal frequency. Under off-nominal frequencies the LC circuit draws some current and the energy dissipates in the series resistor. We will refer to this RLC band-pass filter as a **type 1** ferroresonance suppression circuit (sometimes it is called an "active suppression circuit").

Another design uses a resistor and saturable inductor connected together with a flash-over air gap. The RL circuit burdens the CVT permanently. In addition, the inductor saturates at about 150% of the nominal voltage. The air gap may trigger above that level inserting yet another resistor into the circuit to provide more damping. We will refer to this anti-resonance circuit as a **type 2** ferrorezonance suppression circuit (sometimes it is called a "passive suppression circuit").

As a rule, the CVT with a type 2 circuit has a less distorted output voltage.

If the details of the ferroresonance suppression circuit are unknown, one should, consider the more severe case and assume the type 1 ferroresonance circuit when testing distance relays.

CVT burden

The CVT burden is one of the dissipating paths for the energy accumulated in the CVT circuitry. Therefore, better CVT performance is obtained when the CVT is fully loaded.

Electromechanical relays can load CVTs naturally due to their higher burden. Digital relays, in turn, create a very small load compared with the rated burden of CVTs (100-400VA). Therefore, when using digital relays it is recommended that the CVT be fully loaded, using artificial load if necessary, to avoid extensive transients.

When testing distance relays one should consider not only the rated burden of a CVT, but also test distance relays with CVTs operating on a small load.

Fault inception angle (point on wave)

The most severe transients are generated when a fault occurs at the zero crossing of the primary voltage (compare Figures 3 and 4). The accumulated energy is then at its maximum resulting in larger magnitudes of the transient components. The least severe transient occurs during faults initiated at the maximum wave point.

From a statistical point of view faults appear more often at voltages large enough to initiate the insulation breakdown (i.e. close to the maximum point on wave). However, when testing distance relays one must not neglect faults initiated at the zero crossing as they may "occur" when switching onto a fault.

2.5. CVT transients and high SIRs

CVT transients can create drastic problems for distance relaying in conjunction with high SIRs.

Considering solid faults at the reach point one may approximate the voltage at the relay location using the following equation:

$$V_{fault} \cong \frac{V_{nominal}}{1 + SIR} \qquad (5)$$

Using the above equation Table 1 gives the voltage magnitudes for a range of SIRs. As the SIR increases the fault voltage at the reach point drops to very small values. The magnitude of the CVT transient, in turn, remains constant (independent from the SIR) as the energy accumulated in the CVT is a straight function of the pre-fault voltage.

This results in extremely unfavorable signal to noise ratios (as for the protection-oriented measurements when the speed counts). As illustrated in Figure 7, for example, the magnitude of the noise components may be 10 times larger than the magnitude of the 60Hz operating signal. The noise dominates the signal for 1.5 to 2 cycles.

Table 1. Fault voltage as a function of SIR.

SIR	0.1	1	5	10	20	30
V_{fault} [pu]	0.91	0.50	0.17	0.09	0.05	0.03

The unfavorable signal to noise ratio contributes to both transient overreach and slow operation of distance relays.

Certainly, such extreme proportions occur for high SIRs. Traditionally, vendors specify their distance relays up to the SIR of 30 (sometimes 50 or 60). Such high values are not applicable for

longer lines in heavily interconnected systems. There are, however, situations when the high SIRs are a fact. They include:

- Short lines adjacent to busbars in a long corridors linking the generation and load areas.
- Lines in weak systems such as in developing countries.
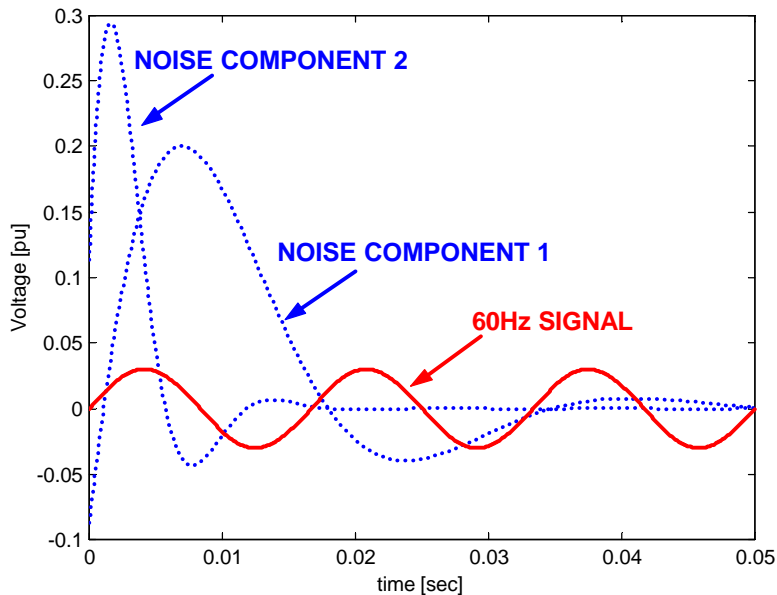- Distance back-up on short lines for current differential or phase comparison schemes.

Figure 7. Illustration of the signal-to-noise ratio for the CVT transients (CVT-1 fault at zero crossing) and high SIRs (30).

3. Distance Relays and CVTs — Transient Overreach

For faults located at the reach point the impedance must be measured precisely in order to ensure proper relay operation. Particularly, the impedance must not be underestimated. If the impedance is underestimated, the relay could maloperate if the impedance appears to be in the operating region although it is an external fault. This holds true for relays that calculate the impedance explicitly and for those that use phase or magnitude comparators.

Generally, transient overreach may be caused by:

- overestimation of the current (the magnitude of the current as measured is larger than its actual value, and consequently, the fault appears closer than actually located),
- underestimation of the voltage (the magnitude of the voltage as measured is lower than its actual value),
- combination of the above.

Overestimation of the current magnitude can happen due to the dc component in the current waveform and can be prevented by using a mimic filter (either classical mimic filter or a band-pass differentiating filter).

Underestimation of the voltage can happen due to CVT transients and is much more difficult to control.

3.1. Voltage estimation

To illustrate the problem Figures 8 and 9 present sample voltage waveforms (CVT-1, SIR=30) and the estimates of the magnitude obtained using the Fourier algorithm with the window of 1/8th of a power cycle, half-, and full-cycle.

Analysis of a large number of simulations similar to the presented samples leads to the following observations:

(a) Underestimation of the voltage magnitude can be significant (contributing up to 80-90% of the error). Assuming the current magnitude is being measured correctly at the moment when the voltage is underestimated, the impedance becomes underestimated proportionally to the voltage magnitude (80-90% of transient overreach).

(b) Underestimation of the voltage magnitude occurs 20-40msec after the fault initiation. This may lead to the idea of introducing security counts (deliberate delay) some time after the fault occurrence to prevent transient overreach. This solution, however, is not robust since the danger of transient overreach may occur as early as 20msec – the security counts introduced so early would slow down a relay significantly for high SIRs.

(c) At some point in time, the noise or some of its components assume the magnitude close to the 60Hz voltage but opposite phase (see Figure 7 – the noise component 1 resembles the inverted 60Hz signal during the 18-25msec time interval). The 60Hz signal and the noise components cancel mutually to certain extent, and therefore, the phasor estimator tends to underestimate the magnitude.

(d) Underestimation of the voltage magnitude is independent from the window size of the phasor estimator and the fault inception angle. Unexpectedly, larger errors may occur for long data windows during less severe transients (see Figure 9). This reinforces the call for thorough testing and negates some of the common assumptions that the fault at the zero crossing always causes the most trouble for distance relays, for example.

3.2. Impedance estimation

Underestimation of the voltage magnitude translates directly (assuming the current being measured accurately) into the negative error in the measured impedance — a fault would seem to be closer.

In addition, the phase of the voltage signal may show significant transient errors due to the CVT noise — the phase may flip by 360 degrees before settling to its correct value. This causes the impedance trajectory to orbit the origin of the Z-plane as shown in Figure 10. This phenomenon is very dangerous for relay stability because even if the impedance is not underestimated by the magnitude, relays using expanded mho characteristics will maloperate due to the impedance entering the expanded zone 1 characteristic, especially for high SIRs.

3.3. Relay reach

The situation shown in Figure 10 is an ultimate case and shows that unless the measuring algorithm of a distance relay (both a digital filter and phasor estimator) is designed specifically to cope with CVT transients under high SIRs, the relay would overreach significantly.
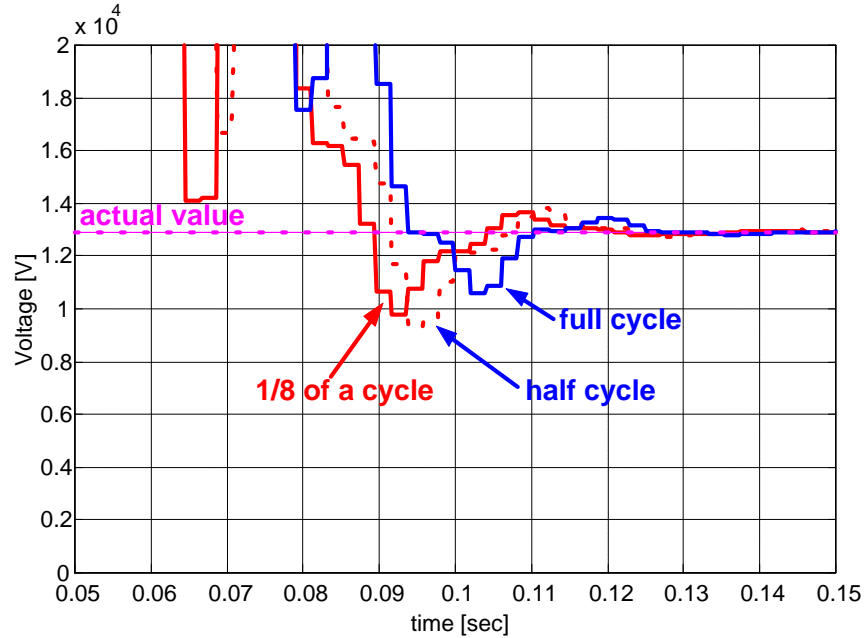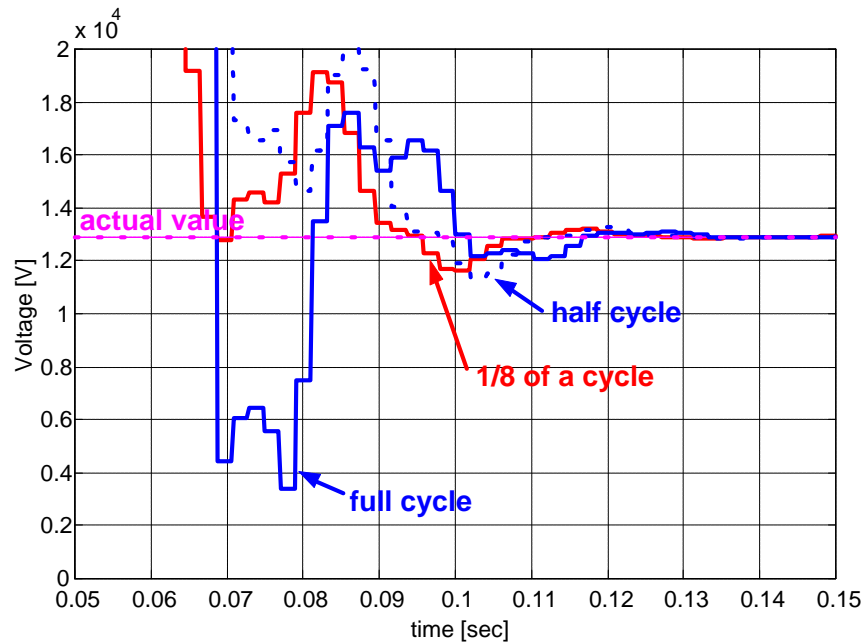

Figure 8. Voltage magnitude estimated using various window lengths for a fault at the reach point under the SIR of 30 and CVT-1 as a voltage source (0 deg inception angle, fault at 54 msec).

Figure 9. Voltage magnitude estimated using various window lengths for a fault at the reach point under the SIR of 30 and CVT-1 as a voltage source (90 deg inception angle, fault at 50 msec).
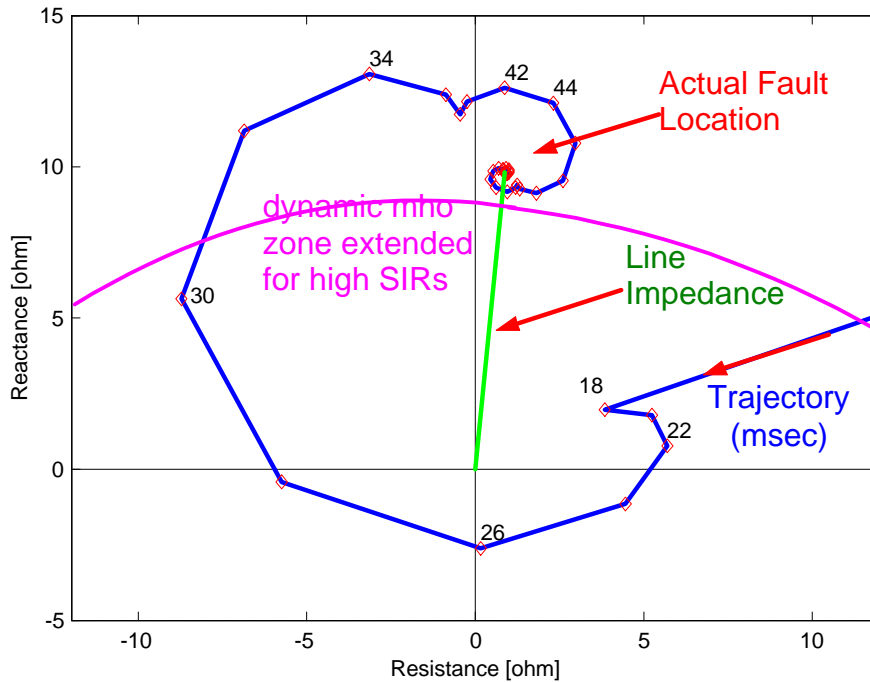
Figure 10. Impedance locus may pass below the line impedance vector
(CVT-1, SIR=30, 90 deg fault inception angle).

For a given measuring algorithm, type of operating characteristic (static or dynamic mho, quadrilateral) and some extra means of stabilizing the relay (such as security counts), the maximum reach vs. SIR curve may be created. Figure 11 presents two examples of such curves.

The reach reduction curves in Figure 11 provide application guidelines. They call, however, for drastic reduction of the zone 1 reach. This, in turn, means that the relay relies entirely on pilot schemes and the overreaching zone 2 for tripping internal faults.

3.4. Accuracy requirements

One may reverse the line of thinking of the previous subsection and find the accuracy requirements for both the voltage and current signals assuming the maximum encountered SIR and the maximum transient overreach to be guaranteed.

For example, assuming the SIR of 30, one finds the voltage at the relay location for a fault at the reach point to be about 3% of the nominal (Table 1). If 5% is the maximum assumed transient overreach, then the total voltage underestimation and current overrestimation at all times should not exceed 0.05 * 0.03 = 0.15% of the nominal.

This presents a significant challenge since we are attempting to attain metering accuracy in the transient domain. Figure 12 illustrates this observation.
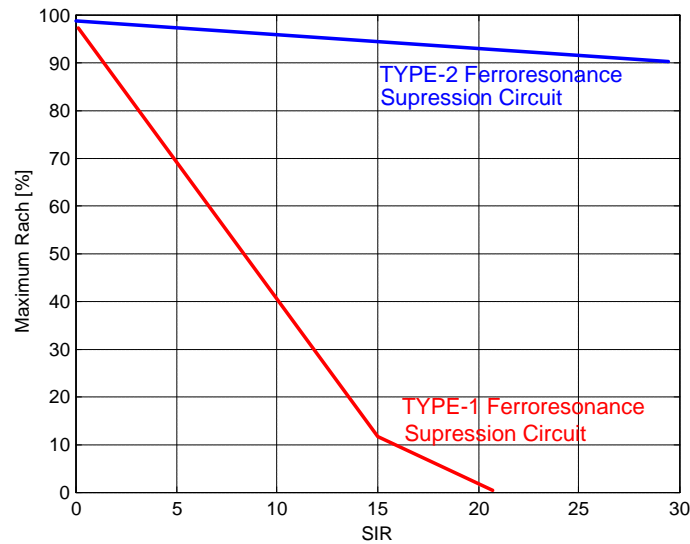
Figure 11. Sample generic reach reduction curves.

4. Distance Relays — Speed

CVT-generated transients under high SIRs cause not only transient overreach of distance relays for out of zone faults, but also slow down the relays for in zone faults as explained in this section.

As illustrated in Figure 7 the 60Hz voltage signal carrying the information as to the fault location (the current does not bring any new information for high SIRs) is buried beneath the CVT noise for a long time. In order to distinguish faults at the reach point for the considered situation (SIR=30) and faults, say at 75% of the reach, the relay must set apart the voltage of 3%*0.75 = 2.2% of the nominal (tripping) and 3% of the nominal (blocking). The difference of 0.8% of the nominal must be sensed in the situation when the noise assumes the level of 30% of the nominal. Practically, a relay would not trip until the CVT-generated transients die out and the 60Hz signal emerges from beneath the noise. If a relay trips much faster, it often shows significant transient overreach as well.

What is worth emphasizing is that using phasor estimators with short data windows does not improve the situation. As illustrated in Figures 8 and 9, the magnitude estimated using 1/8th cycle window still requires about 25-35msec to get close to the actual value of the voltage magnitude.

Yet another issue related to speed is the use of security counts (deliberate delay) in order to cope with the transient overreach. Even if the delay is introduced some time after the fault, the delay is practically in effect when the relay is about to trip under high SIRs. This slows down the operation even more.
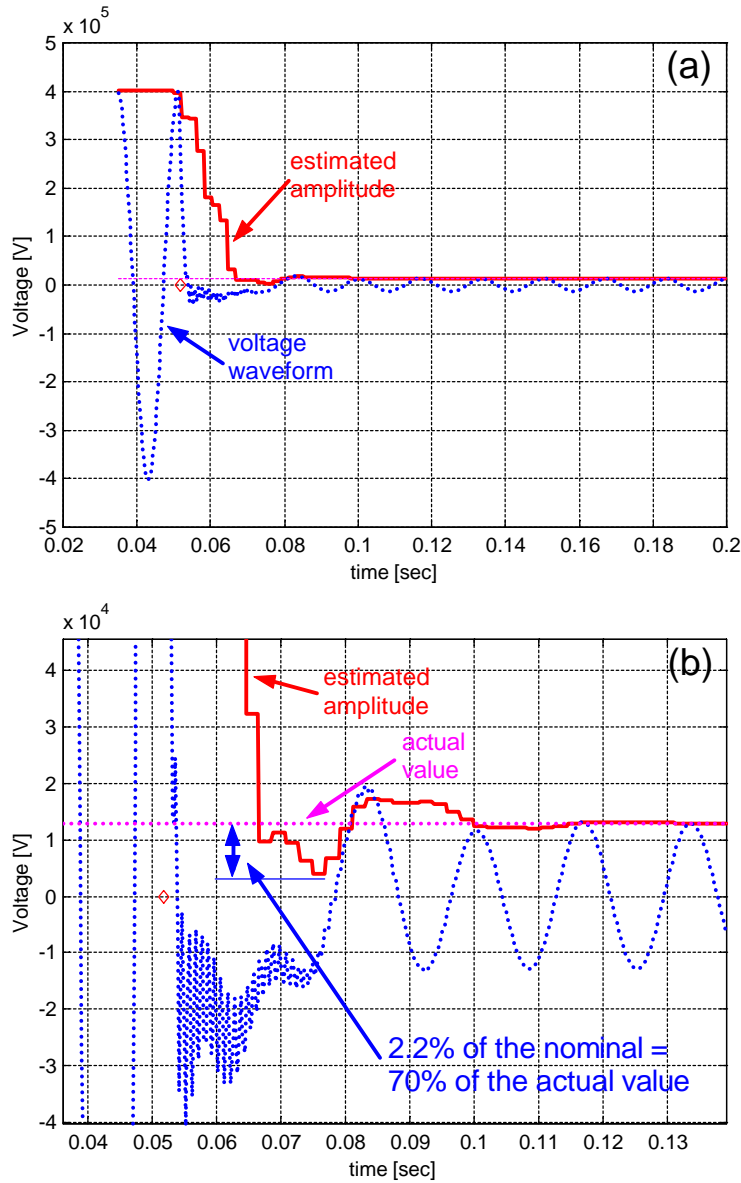
Figure 12. Estimated voltage magnitude (CVT-1, 90deg inception angle, SIR of 30). The magnitude ramps down quickly (a), but gets underestimated by 2.2% of the nominal contributing to 70% transient overreach (b).

5. New Algorithm

This section summarizes the highlights of a new distance algorithm for excellent CVT transient control.

5.1. Pre-filtering

In order to suit best the needs of voltage and current signals, different filters have been used voltage-wise and current-wise.

The currents are pre-filtered using a "modified mimic" filter. The filter is a stationary Finite Impulse Response (FIR) filter which has a much better frequency response compared to the classical mimic filter.

The voltages are pre-filtered using a special, designed to cope with CVT transients, non-symmetrical FIR filter with the window length of approximately $3/2^{nd}$ of a power cycle. Due to its optimal design, the delay introduced by the filter is much lower than a power cycle. The filter performs very well for both CVT transients and high frequency noise.

5.2. Phasor estimation

Likewise, different phasor estimators are used for the voltage and current signals. The current phasors are measured using the full-cycle Fourier algorithm. The voltage phasors are estimated using the half-cycle Fourier algorithm.

The combination of the pre-filtering and phasor estimation algorithms ensures the following accuracy:

- **Currents**: less than 3% transient overshoot due to the dc components.
- **Voltages**: less than 0.6% (of the nominal) transient underestimation due to the CVT transients.

The combination of the above accuracy result in transient overreach ranging from 1% (for SIRs up to 5) to about 20% (SIR = 30).

In order to reduce the transient overreach further, a double zone 1 has been implemented as shown in Figure 13.
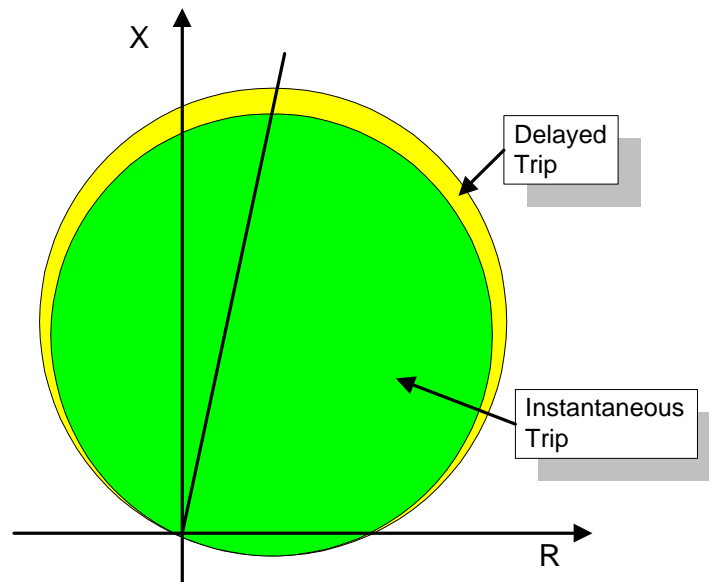

Figure 13. Instantaneous and delayed zones 1.

The inner zone 1 has its reach dynamically adjusted using the voltage magnitude. The dynamic reach varies from 80% of the actual (set) reach for the SIR of 30, up to 95% for the SIR of 0.1. The inner zone is completely secure and therefore no delay is applied there. It ensures fast

operation for faults located at 0-80% of the reach for high SIRs, and for 0-95% of the reach for low SIRs.

The outer zone 1 has its reach fixed at 100% of the actual (reach setting) and applies some delay to prevent maloperation.

As a result, the transient overreach has been reduced to a very small value (~1-5% over the SIRs up to 30) at the expense of slowing down the relay only for faults close to the reach point.

5.3. Distance comparators

Let us use the mho characteristic to illustrate the concept of double-reach zone 1 in more detail. The mho distance element uses dynamic (memory polarized) characteristics with "self-tilting" reactance and memory-polarized zero- and negative-sequence directional supervision.

Tables 2 and 3 summarize the operating equations for ground and phase elements, respectively. The tables identify the comparators that work in a double-reach mode. The reach is reduced on per-element basis (i.e. separately for each element) using a multiplier. The multiplier for a given element is controlled by the voltage of that element (for example, the AG voltage is used for the ground distance phase A multiplier; the AB voltage for the phase distance AB multiplier, etc.). Figure 14 presents the relation between the voltage and the reach multiplier.
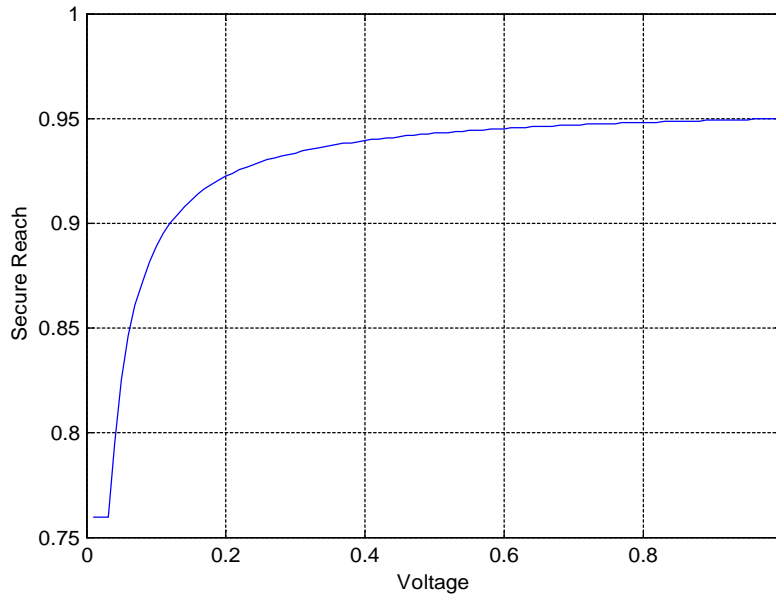

Figure 14. Inner zone 1 reach as a function of the voltage magnitude.

Zones 2, 3 and 4 do not apply the double-reach approach as they are delayed and/or used by overreaching pilot schemes where communication solves many problems transient problems.

Table 2. Ground distance elements.

Characteristic	Phase Comparator	Double Reach (Y/N)
Dynamic mho	IZ-V vs. $V_{mem\,(pos)}$	Y
Reactance	IZ-V vs. I_0Z	Y
Zero-sequence directional	I_0Z vs. $V_{mem\,(pos)}$	N
Negative-sequence directional	I_2Z vs. $V_{mem\,(pos)}$	N

Table 3. Phase distance elements.

Characteristic	Phase Comparator	Double Reach (Y/N)
Dynamic mho	IZ-V vs. $V_{mem\,(pos)}$	Y
Reactance	IZ-V vs. IZ	Y
Directional	IZ vs. $V_{mem\,(pos)}$	N

5.4. Hardware implementation

The described algorithm has been implemented using the concept of a "universal relay" — a modular, scaleable and upgradable engine for protective relaying. Figure 15 presents the basic hardware modules of the relay; while Figure 16 — the actual implementation.
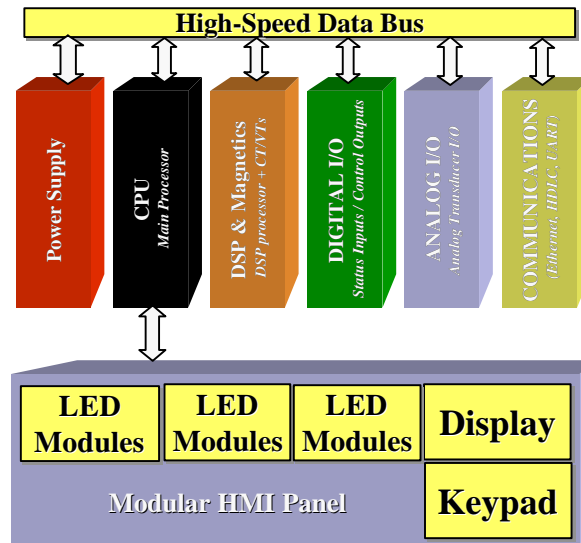

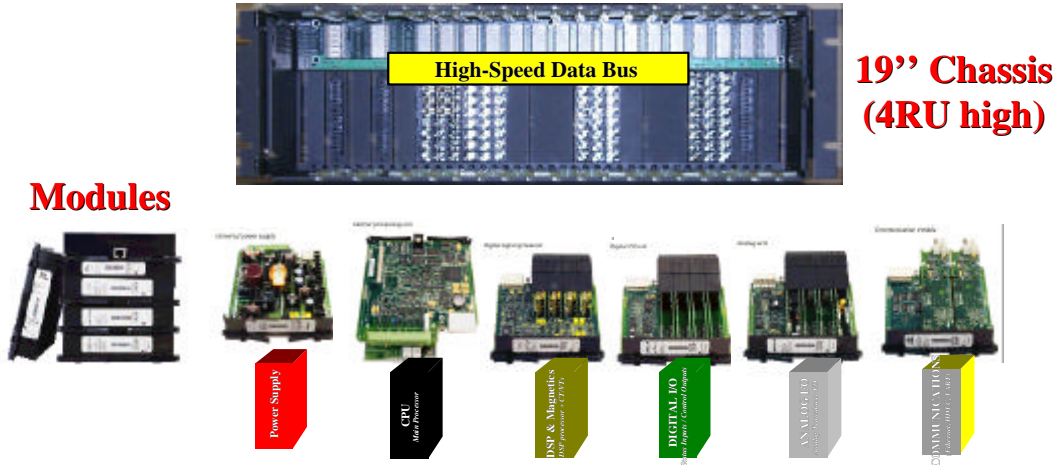Figure 15. Modular hardware architecture.

Figure 16. Actual relay architecture.

5.5. Testing and results

Initial versification of the algorithm has been performed using Real-Time Digital Simulator (RTDS) generated waveforms and MATLAB simulations. Several thousand cases have been analyzed at this stage.

The following definition of a transient overreach has been adopted in testing:

$$TO_{\%} = \frac{reach\ of\ solid\ operation - reach\ of\ no\ operation}{reach\ of\ no\ operation} \cdot 100\% \tag{6}$$

The testing showed that the transient overreach is well controlled (less than 5% - using definition (6)). Figure 17 presents the average operating times versus the fault location (fault characteristic) and SIR (system characteristic) obtained from this stage of testing.

The final stage of testing has been performed using actual relays, RTDS (Figure 18) and high accuracy, high-power voltage and current amplifiers. The anticipated operating times and transient overreach have been successfully validated.

6. Conclusions

New insights into the distance relaying problems caused by CVTs have been given. As explained, various CVT configurations (value of the stack capacitances, type of the ferroresonance circuit and amount of load) affect the relay performance to a different degree.

Transient overreach specifications of relays available on the market are very imprecise. Definition of transient overreach and test conditions (type of a CVT, primarily) are not specified by the vendors. This relates to type of a CVT, type of a ferroresonance circuit, CVT burden, fault inception angle, etc.

Tests performed by the authors on selected relays using the CVT-1 and CVT-2 models delivered much worse performance characteristics than those published by vendors. In many instances comparatively short operating time independent from the fault location is a sign of a very poor

CVT transient control under high SIRs. In response to that, a new algorithm has been presented in this paper that ensures superior performance in terms of transient overreach without significant sacrificing the speed of operation.
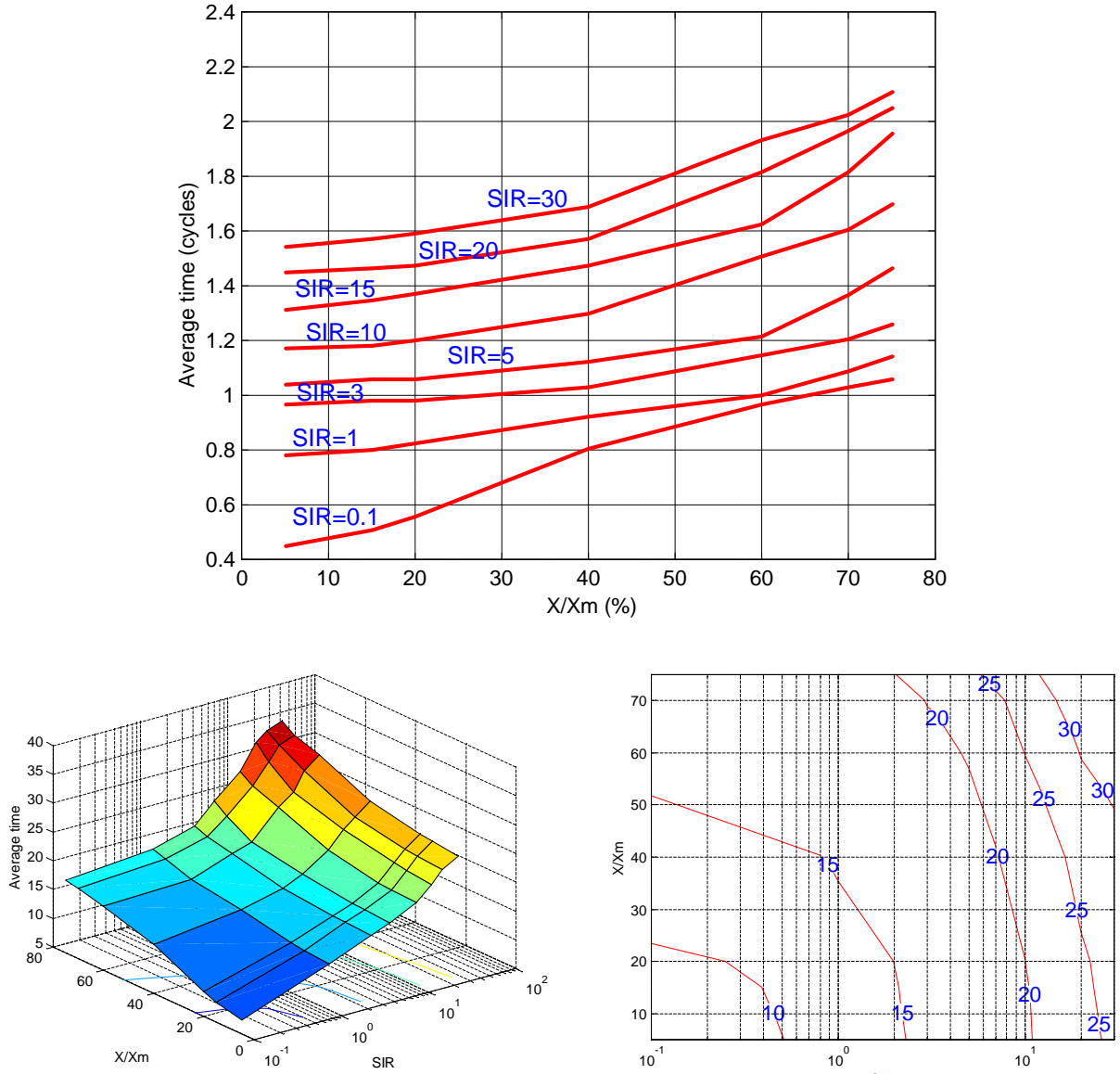

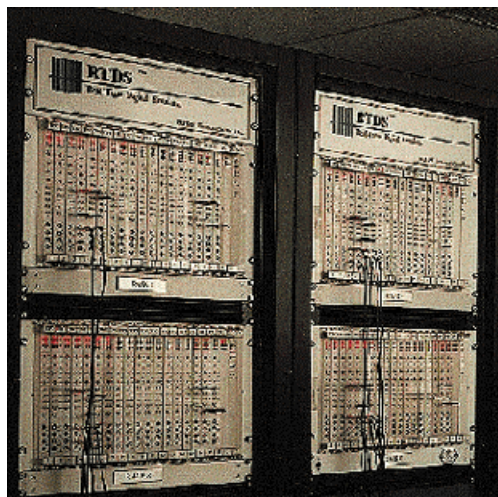Figure 17. Average operating times of the new algorithm (MATLAB).

Figure 18. RTDS hardware used in testing.

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Biographies

Bogdan Kasztenny received his M.Sc. (89) and Ph.D. (92) degrees (both with honors) from the Wroclaw University of Technology (WUT), Poland. In 1989 he joined the Department of Electrical Engineering of WUT. In 1994 he was with Southern Illinois University in Carbondale as a Visiting Assistant Professor. From 1994 till 1997 he was involved in applied research for Asea Brown Boveri in the area of transformer and series compensated line protection. During the academic year 1997/98 Dr.Kasztenny was with Texas A&M University as a Senior Fulbright Fellow, and then, till 1999 - as a Visiting Assistant Professor. Currently, Dr.Kasztenny works for General Electric Company as a Senior Application/Invention Engineer. Dr.Kasztenny is a Senior Member of IEEE, holds 2 patents, and has published more than 90 technical papers.

Dave Sharples after early experience with the Electricity Authority in the UK graduated from the University of Manchester (UK) with a M.Sc. (Tech) degree in 1963. After experience with the English Electric Meter Relay and Instrument Division he emigrated to Canada to join Ontario Hydro. Following early retirement in 1993 he has acted as a protection consultant, most recently with GE Power Management.

Vince Asaro graduated from Ryerson Polytechnical Institute, Toronto, Ontario Canada, in 1988 with a Bachelor of Electrical Engineering Technology specializing in control systems. He then worked for Perkin Elmer Photovac designing hardware and firmware for gas analytical equipment. . In 1997 he joined General Electric - Power Management and is now the lead firmware designer for the D60 distance relay and is responsible for firmware development for new products.

Marzio Pozzuoli graduated from Ryerson Polytechnical Institute, Toronto, Ontario Canada, in 1987 with a Bachelor of Electrical Engineering Technology specializing in control systems. He then worked for Johnson Controls designing industrial automation systems. He was involved in the design of Partial Discharge Analysis systems for large rotating electric machinery with FES International. In 1994 he joined General Electric – Power Management and is the Technology Manager responsible for the engineering and development of new products.