GET-8031

PLS1 Polyphase Line Relaying System

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DESCRIPTION

The PLS1 MOD10 relaying system uses sequence components as does its' predecessors, the SLYP/SLYN and SLYP/SLCN schemes, both of which have enjoyed many years of successful service. Further information on the SLYP/SLCN scheme can be found in GET-6456 and GET-6652. Improvements in performance have been achieved in the PLS system in the following areas:

- Security
- Sensitivity to high resistance ground faults
- Reduced sensitivity to load without increase in operating time through use of "energy comparators"
- Phase selection for single-pole tripping schemes
- Monitoring (through continuous monitoring module)

The PLS1 System is a complete transmission line protection system that may be applied on series compensated transmission lines, uncompensated lines and on lines adjacent to compensated lines. It may be used for any or all of the following conditions:

1. Single-pole or three-pole tripping
2. High resistance ground faults
3. Zero sequence mutual coupling with parallel lines
4. Weak infeed conditions at one terminal of the transmission line
5. Single-pole tripping for intercircuit faults (requires two communication channels)

The settings for the various functions in the PLS system can be determined using common system knowledge such as source and transmission line parameters, fault studies, etc. For series compensated line applications, it is necessary to know the gap flashing levels when gaps are used to protect the capacitors, or the MOV protective levels when MOV's are used for capacitor protection. No other special information or studies are required.

The following functions are included in the system:

Permissive Tripping

PDT - positive sequence distance
NDD - negative sequence distance
NT & IT - negative sequence directional and overcurrent

Blocking

PDB - positive sequence distance
NB & IB - negative sequence directional and overcurrent

Direct Tripping

PD1 - Positive sequence distance
ND - Negative sequence distance
IDT - Zero sequence overcurrent with positive sequence restraint
ITOC - Time overcurrent backup (zero sequence with positive sequence restraint)

Phase Selectors (current operated)

ϕA SEL Phase A current plus positive, negative and zero sequence current phase selector

ϕB SEL Phase B current plus positive, negative and zero sequence current phase selector

ϕC SEL Phase C current plus positive, negative and zero sequence current phase selector

Backup Tripping and/or Reclosing Control

PDX Positive sequence distance

Out-of-step Blocking

POSB Positive sequence distance

Overcurrent Functions

FD Fault detector (positive, negative and zero sequence)
I1T Positive sequence for line pickup
IT Permissive trip supervision, negative and zero sequence current with positive sequence current restraint
IB Permissive block supervision, negative and zero sequence current with positive sequence current restraint
IMA,B,C Phase overcurrent

Undervoltage Functions

VA,VB,VC Phase undervoltage

Details on the operation of these functions are provided later.

SCHEME LOGIC

The PLS1 system is configured as a hybrid scheme. It can be applied with a single communication channel, with two separate communications channels or with one three-frequency channel.

CHANNEL LOGIC

1. Single Communications Channel (frequency shift power line carrier or audio tone)

The Communications channel is used only with the permissive relaying functions to establish pilot tripping for all internal faults. The phase selectors are used with some of the relaying functions to trip only the faulted phase for SLG faults and to trip all three phases for multi-phase faults.

2. One Three-frequency or two Separate Communications Channels (frequency shift power line carrier or audio tone)

The two separate communications channels or the three-frequency channel are used to:

a. transmit a permissive trip signal to the remote terminal of the line

b. transmit faulted phase identification to the remote terminal of the line.

The channels are keyed as shown in Figure 1.

Phase-identified channels must be used when single-pole tripping is required for intercircuit faults on double circuit lines. For improved performance, they should also be considered when single-pole tripping is used in the following situations:

1. Series compensated lines

2. Weak infeed conditions

3. High resistance faults.

DIRECTIONAL COMPARISON LOGIC

Simplified logic for the hybrid portion of the scheme is shown in Figure 1. For an internal fault, one or more of the permissive tripping functions will operate and apply one of the inputs to the comparer AND16 and will key the appropriate permissive transmitter via OR10, AND15, OR18 and the channel keying logic. Receipt of the trip signal via any receiver will apply another of the inputs to the comparer while the NOT input will be absent because the blocking functions will not have operated, or will be prevented from operating, for this internal fault. A trip permission output will then be produced via AND16, OR14, TL1, OR15 and AND17.

A priority system is used between the tripping and blocking functions to establish transient blocking during fault current reversals following clearing of an external fault on a parallel line, or for voltage reversals that can occur when series capacitors are present. For an external fault PDB or NB will operate and:

1. Apply the NOT input to AND15 to block transmitter keying.

2. Apply the NOT input to AND16 to block pilot tripping.

3. Apply the NOT input to AND11 to block zone 1 direct tripping by PD1.

4. Energize timer TL30/24 or TL25 respectively.

These timers are set with a long dropout time (delay dependent on the application) so that when the fault is cleared the NOT inputs to AND11, AND15 and AND16 will not be removed immediately. Consequently, transmitter keying and pilot tripping will be prevented even if one or more of the tripping functions were to operate during a current or voltage reversal. Note that the operation of the tripping functions will cause the blocking functions to reset by applying a NOT input to AND2 and/or AND65 but that the reset will not be complete until the dropout time of the respective blocking function. The NOT inputs to AND2 and AND65 are required during an internal fault. For this condition the blocking functions must not produce an output or else tripping will be blocked. For example, for a close-in internal three-phase fault, the blocking function (PDB) may try to operate because it is offset to include the relay location within its operating characteristic. The tripping function (PDT) will also operate however, and by virtue of its design will operate faster than the blocking function. PDT will block PDB operation by applying the NOT input to AND65 and will also block NB operation by applying one of the NOT inputs to AND2. Note that NB may try to operate on the negative sequence quantities produced

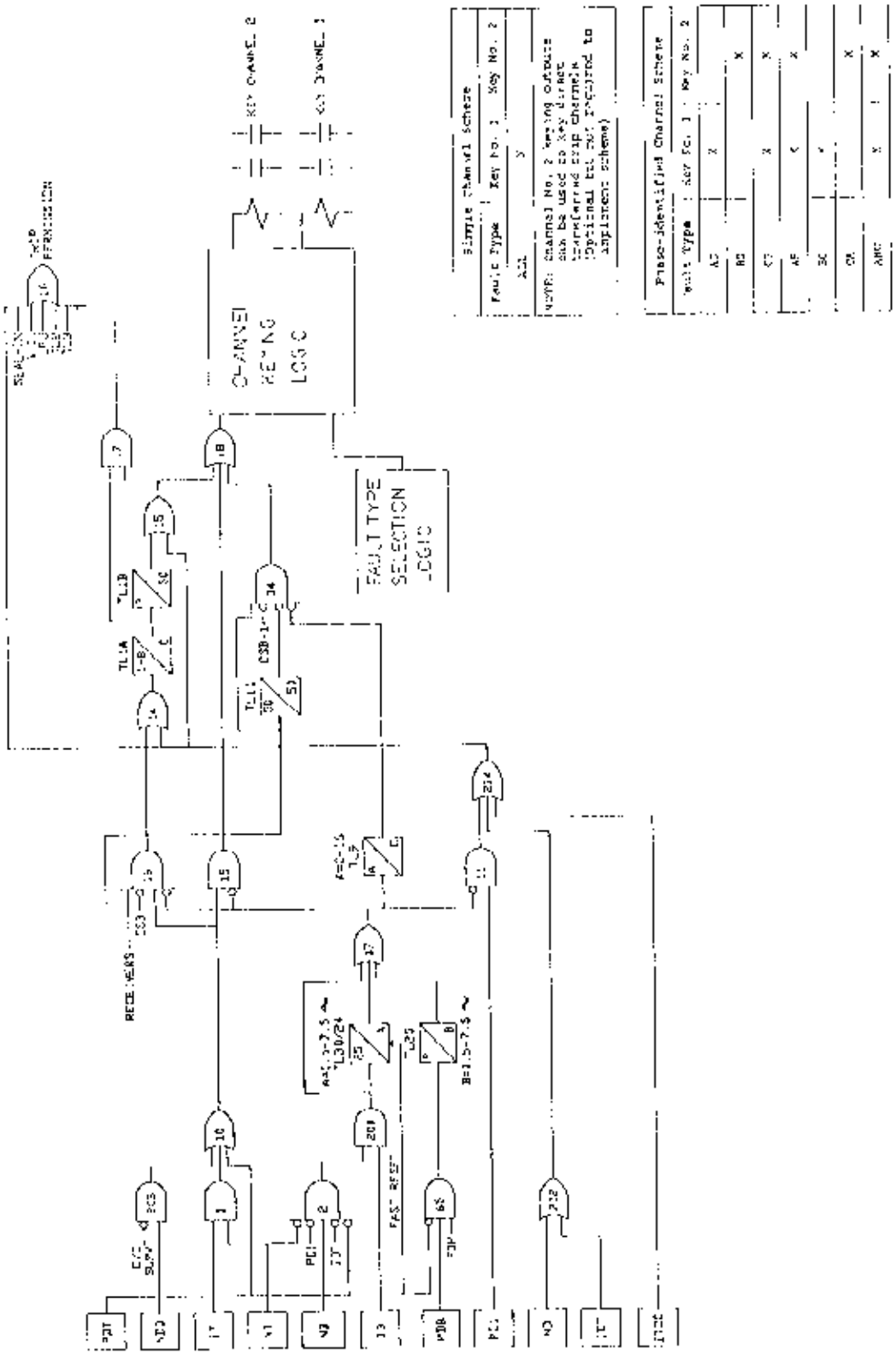


Figure 1 (0171C8788 Sh.1) Logic Diagram, Directional Comparison

at the inception of the three-phase fault (occurs asymmetrically), thus the reason for inhibiting it with PDT. A similar priority system is established between NT and NB.

The PDX function is used with a separate timer to provide an independent zone 2 function that can be set to coordinate with zone 1 functions in adjacent lines. PDX is also used as part of the reclosing (inhibit and cancel) schemes.

The direct tripping functions (PD1, ND, IDT and ITOC) operate to trip directly and independently of the pilot portion of the scheme. The output of any of these functions will initiate trip permission directly through OR214, OR14, OR15 and AND17.

WEAK INFEED, REPEAT KEYING, LINE PICKUP TRIP, OUT-OF-STEP LOGIC AND LOSS OF POTENTIAL

The channel echo (repeat) circuitry, made up of the receiver, TL11 and AND34 works as follows: if a trip signal is received at CC1 and there is no output from the blocking functions the NOT input to AND34 will be absent. Thus, AND34 will produce an output to key the permissive transmitter (see above) for the 50 millisecond pickup time of timer TL11. After 50 milliseconds, no further keying will be permitted because timer TL11 will time out and apply a NOT input to AND34 to stop keying. Thus TL11 and AND34 perform a knockdown circuit to prevent the keying circuits of all transmitters from being locked in.

Simplified logic for the weak infeed trip circuitry is shown in Figure 2 and is composed of AND14, any receiver (via OR12), OR11, OR37 and TL16. Assume that an internal fault has been detected at the remote terminal of a transmission line and that the local blocking functions have not operated. Therefore, there will be a signal received at the local terminal and there will be no output from OR37 because none of the blocking functions are up. If the fault detector (FD), or the overcurrent blocking supervision function (IB), or the overcurrent tripping supervision function (IT) are picked up, or if all three voltage detectors are dropped out, then OR11 will produce an output. Consequently, AND14 will have all of its upper inputs present, and if it is assumed for the moment that the lower input to AND14 is present, then AND14 will produce an output. This output is applied to security timer TL16 which will issue a trip permission when it times out.

The lower input to AND14 comes from the open-pole sequencing circuitry which is required in single-pole tripping applications. It allows the weak infeed circuitry to perform at the inception of a fault, removes it from service during the open-pole period following a single-pole trip, and re-inserts it on the inception of a fault during or following this period. The circuitry works as follows. At the inception of a fault, NOT4 will be producing an output thus the lower input to AND14 will be present, and tripping will be as described above. When the faulted phase is tripped, timer TL26 will time out to apply the middle input to AND214 via OR211 and to inhibit any phase selector output which in turn applies the upper input to AND214 via NO1212 and OR212. When the faulted phase is cleared by opening the breaker, the respective open-pole detector (AND7, AND8, or AND9) will pick up and apply the lower input to AND214 via OR32. AND214 will thus produce an output which will be sealed in on the open-pole detector via OR211 and OR212. The output of AND214 without a concurrent phase selector output will allow AND71 to produce an output which will reset NOT4 and thus remove the lower input from AND14 so that weak infeed tripping will be blocked. If a subsequent fault occurs during the open pole period, one of the phase selectors will pick up and apply the NOT input to AND71 via OR210. NOT4 will then produce an output which will apply the lower input to AND214 thus re-instating weak infeed tripping. If no fault occurs, weak infeed tripping will be re-instated when the open-pole detector resets after the breaker is successfully reclosed.

Timer TL27 (following AND214) will be energized during the open-pole period and its output is used to arm the three-pole tripping circuitry so that any faults occurring during the open-pole period, or during reclosure of the breaker will be tripped three-pole.

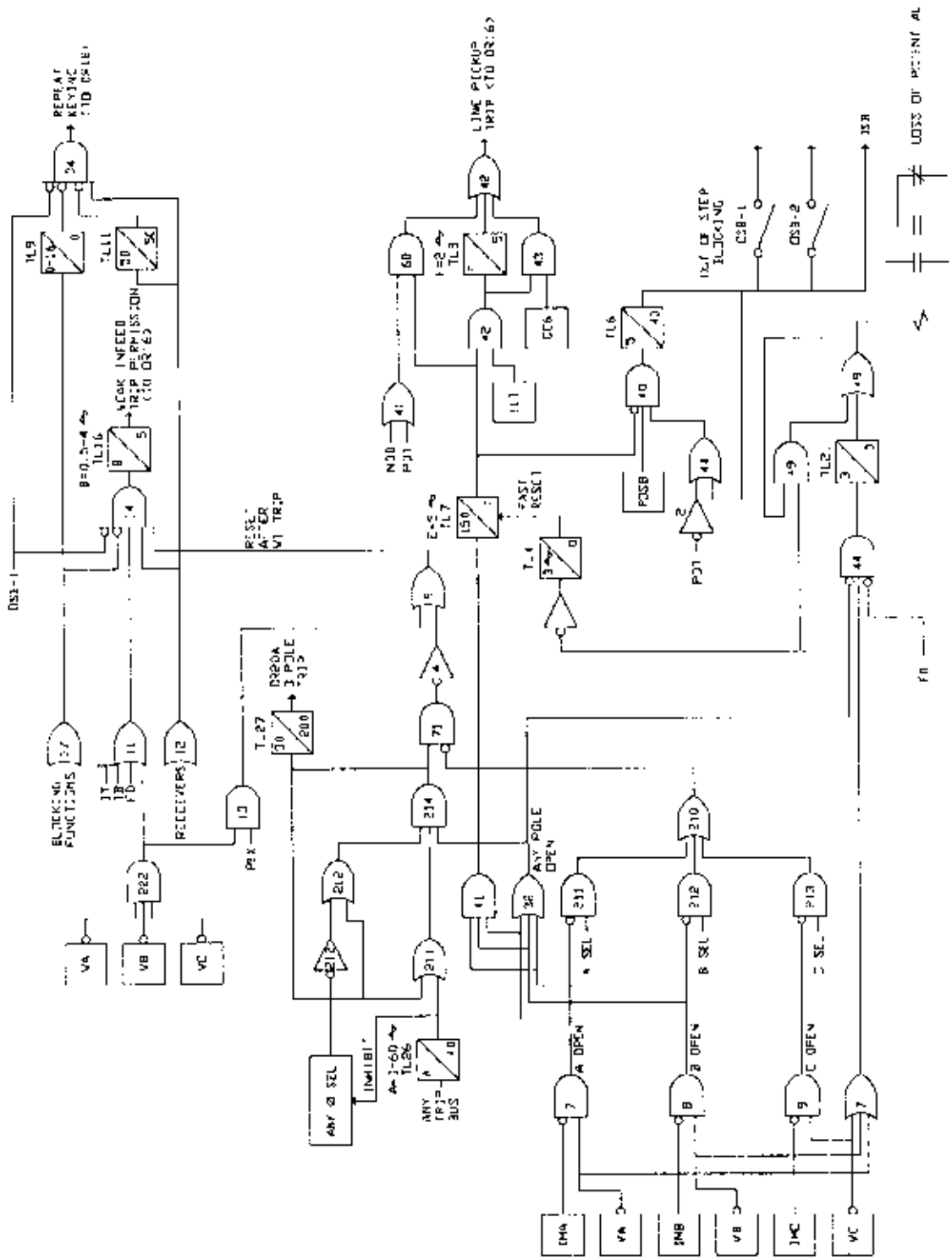


Figure 2 (0179C8269 Sh.3 [2]) Logic Diagram,
Weak Infeed, Repeat Key, Line Pickup, Out-of-Step

The line pickup logic is used to initiate tripping when a line is energized by a manual closure or on reclosing following a three-pole trip. The circuitry is composed of AND41, TL4, TL7, AND42, TL8, OR42, OR41, AND60, AND43 and CC6. The circuitry works as follows. AND41 will produce an output when the line is de-energized as indicated by outputs from all three open-pole detectors. At that time, timer TL7 will be energized and when it times out 150 milliseconds later, it will apply the top input to AND42 and the bottom input to AND60. The line pickup circuit is now armed and ready to trip if any of the following functions pick up when the line is energized:

1. PDT - positive sequence tripping function
2. NDD - negative sequence tripping
3. I1T - positive sequence overcurrent function

If none of these functions operate when the line is returned to service then timer TL7 will be fast reset 3 cycles (TL4 pickup time) after all three phase voltages return to normal as indicated by no output from OR7.

Note that NDD or PDT will not pick up when closing into a bolted three-phase fault (such as when the grounding chains are left on the line), hence the need for the I1T function. It is desirable to set this function above the maximum load current, however, it must be set below the maximum load current if conditions require it. Timer TL8, contact converter CC6 and AND43 are provided for use in those applications where I1T must be set below full load current and where high speed reclosing is used at each terminal of the transmission line. This timer allows time for the voltage to return to normal and remove line pickup tripping from service before load current can initiate a trip following a simultaneous high speed reclose. If simultaneous reclosing is not used at each end of the line, then faster tripping can be attained on closing into a fault by applying a continuous input to CC6 which allows timer TL8 to be continuously bypassed via AND43. Timer TL8 should be bypassed if I1T can be set above full load regardless of whether or not simultaneous high speed reclosing is used.

Out-of step blocking circuitry is provided and the output is routed through 2 switches (OSB-1 and OSB-2).

The output of OSB-1 is used to block zone 1 and pilot tripping along with zone 2 and zone 3 time-delayed tripping. Transmitter keying is also blocked. Direct tripping by the IDT, ND and ITOC functions is left in service.

The output of OSB-2 is used to block all tripping. With this switch closed, the position of OSB-1 is irrelevant.

The loss of potential (LOP) logic is made up of AND44, TL21, AND49 and OR49. If potential is lost without a concurrent output from the open-pole circuitry or the fault detector (FD) then AND44 will produce an output to start timer TL21. If the loss lasts for three milliseconds, then a loss of potential output will be produced. The output will be sealed in via AND49, OR49 and the output of any of the voltage detectors (OR7) so that the LOP contacts will remain closed until the voltage returns to normal. Note that the LOP circuitry will operate for both a total loss as well as a partial loss of potential. If the drop in potential occurs as the result of a fault, the fault detector will operate to prevent LOP from being set up. Similarly, LOP will not be set up when any of the breakers are open because one or more of the open-pole detectors will operate.

TRIP LOGIC

The trip logic is used to determine which pole or poles of the breaker should be tripped when trip permission is received from the directional comparison logic. The simplified trip logic is shown in Figure 3. The logic works as follows. Trip permission from the directional comparison logic is applied to AND21, AND22 and AND23 via OR16. For single-line-to-ground (SLG) faults, the faulted phase will only be selected. An output from the phase selection logic will apply the second input to its associated AND circuit (21, 22 or 23) and initiate tripping through its associated logic chain. For example, if phase "A" is faulted, then phase "A" will be selected and an input will be

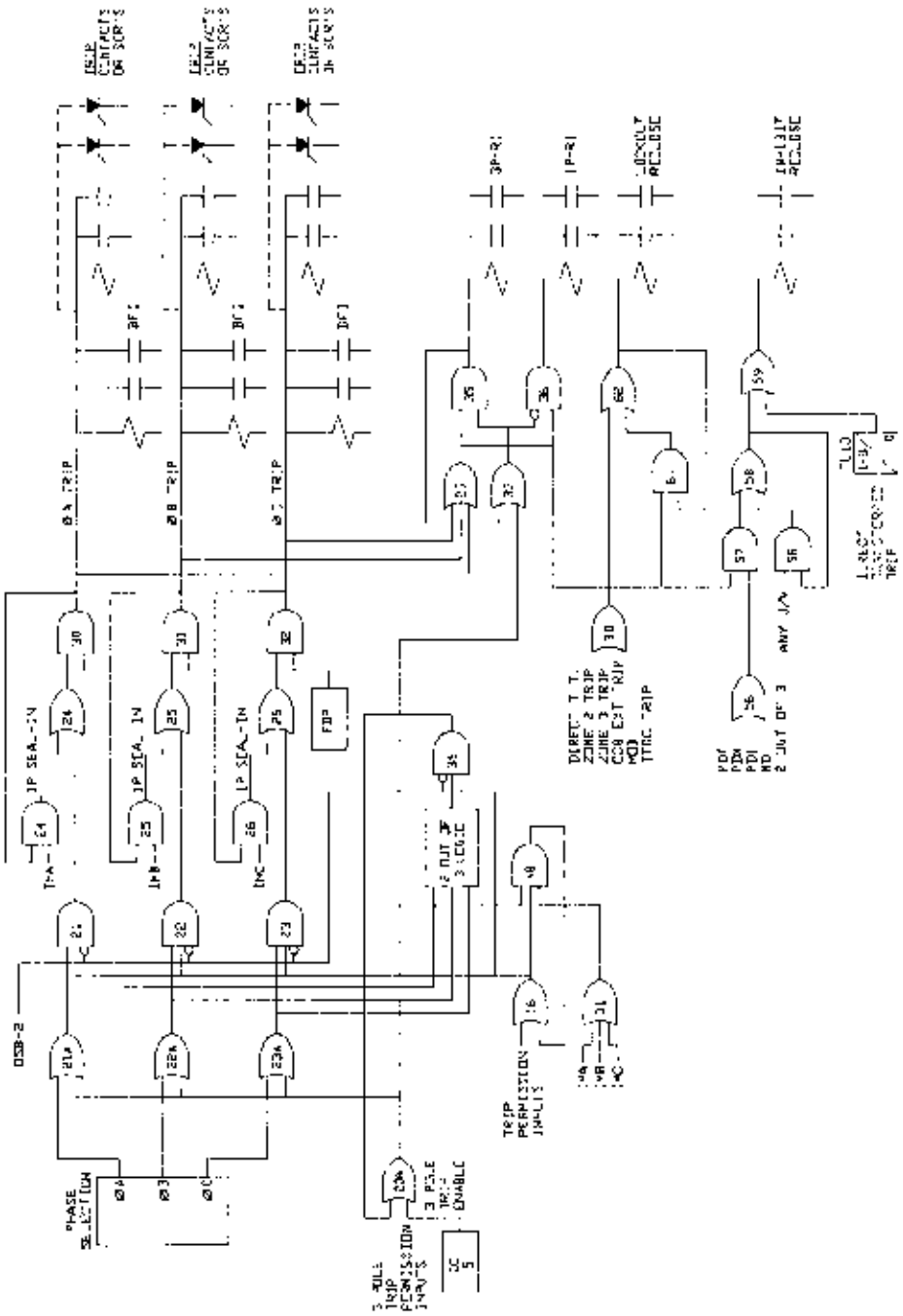


Figure 3 (0179C8269 Sh.2 [1]) Logic Diagram, Trip and Reclose Logic

applied to AND21 via OR21A. The output of AND21 will initiate tripping via OR24 and AND30. Note that the second input to AND30 comes from the fault detector (FDP) that is an integral part of the PLS scheme. The fault detector will operate only for faults on or in the vicinity of the protected line and provides security by insuring that tripping cannot be initiated unless a fault has occurred. For multi-phase faults, the phase selector circuitry will issue a three-pole trip output which will be applied to AND21, AND22 and AND23 concurrently. If trip permission is given, then all three poles of the breaker will be tripped simultaneously.

Simplified phase A selection logic for the phase-identified scheme is shown in Figure 4. Tripping of phase A can be initiated only if the ϕA receiver has produced an output thus indicating that the remote terminal has detected a phase A fault. For example, assume the case of simultaneous faults shown in Figure 5. The fault will be detected at all terminals of the line and a permissive trip signal will be produced at all terminals. However, at the terminal near the fault, the fault looks like a Phase A fault in line 1 and a Phase B fault in line 2. At the remote terminals, the fault looks like an A-to-B-to-ground fault in both lines. Without proper precautions, single-pole tripping would occur at the terminals near the fault while three-pole tripping would occur at the remote terminals.

Sensitive overcurrent detectors (IMA, IMB AND IMC) are provided as part of the scheme to provide seal-in circuits in the event of a breaker failure. The seal-in is required to maintain the input to the breaker failure scheme in the event a failure did occur. The seal-in circuits work as follows.

For a three-pole trip, at least one of the overcurrent detectors will be up thus OR31 will be producing an output which is applied to the bottom input of AND48. The top input to AND48 comes from OR20A initially and this input will be sealed in from AND39 which will be energized for any three-pole trip. The middle input to AND48 and the bottom input to AND39 will initially be a trip permission input from OR16, but these inputs will be sealed in by an output from AND48. Thus, once a three-pole trip occurs, the trip buses will be sealed in by the sensitive overcurrent detectors, and will not be reset until all three of the detectors are reset. Note that the fault detector input is also sealed in once a trip has occurred.

For a single-pole trip, only the faulted phase will be tripped. In this situation, the trip output associated with the faulted phase only will be sealed in. For example, assume a phase "A" trip. The output of AND30 will be sealed in via AND24, OR24 and the current detector IMA and will remain sealed in until IMA resets.

RECLOSING LOGIC

Reclose Initiate - A single-pole reclose initiate (1P-RI) output will be produced whenever a single-pole trip is called for. If three-pole tripping is called for, then a three-pole reclose initiate (3P-RI) output will be produced.

Inhibit Reclose - An inhibit reclose output will be produced if a trip is initiated and there is an output from any or all of the following functions which may be independently selected via switches provided in the system.

1. PDX, positive sequence distance function, zone trip
2. PDT, positive sequence distance function, pilot trip
3. PD1, positive sequence distance function, zone 1 trip
4. ND, negative sequence distance function, direct trip
5. Any multi-phase fault as indicated by the two-out-of-three selection logic
6. A direct transferred trip input from external equipment (if used, not selectable by switch)

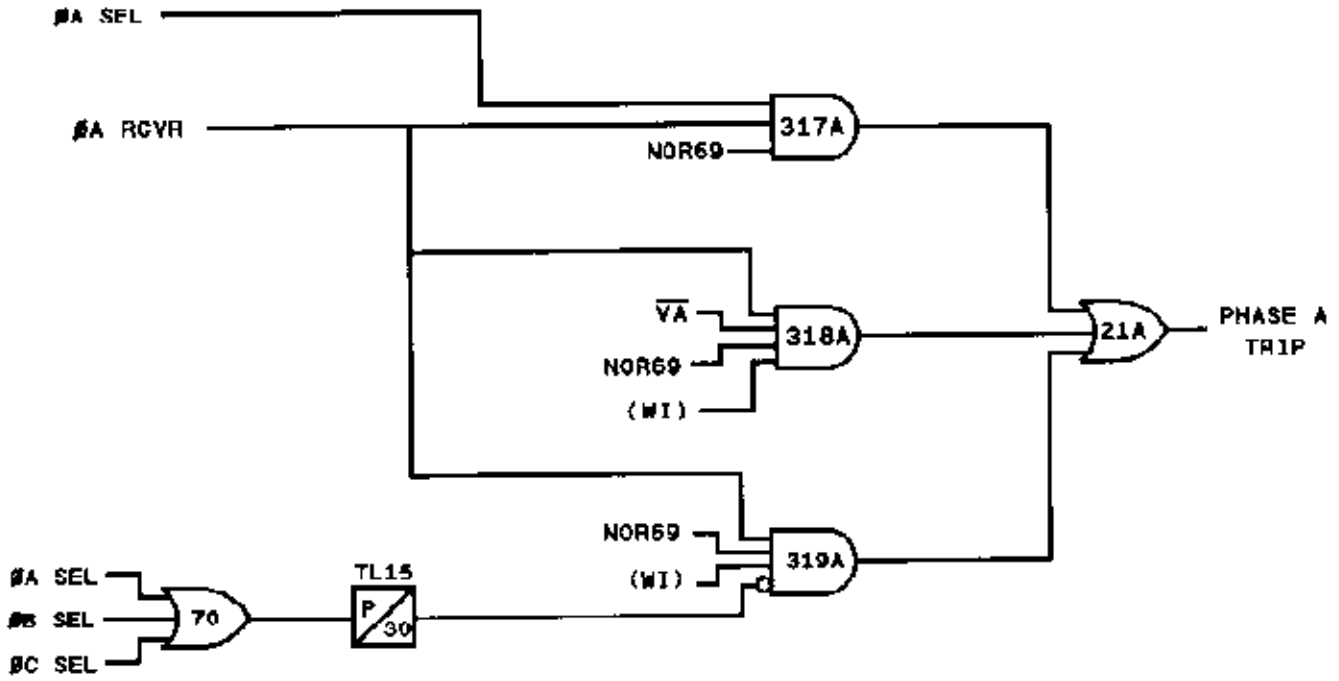


Figure 4 - Simplified Faulted Phase Selection Logic

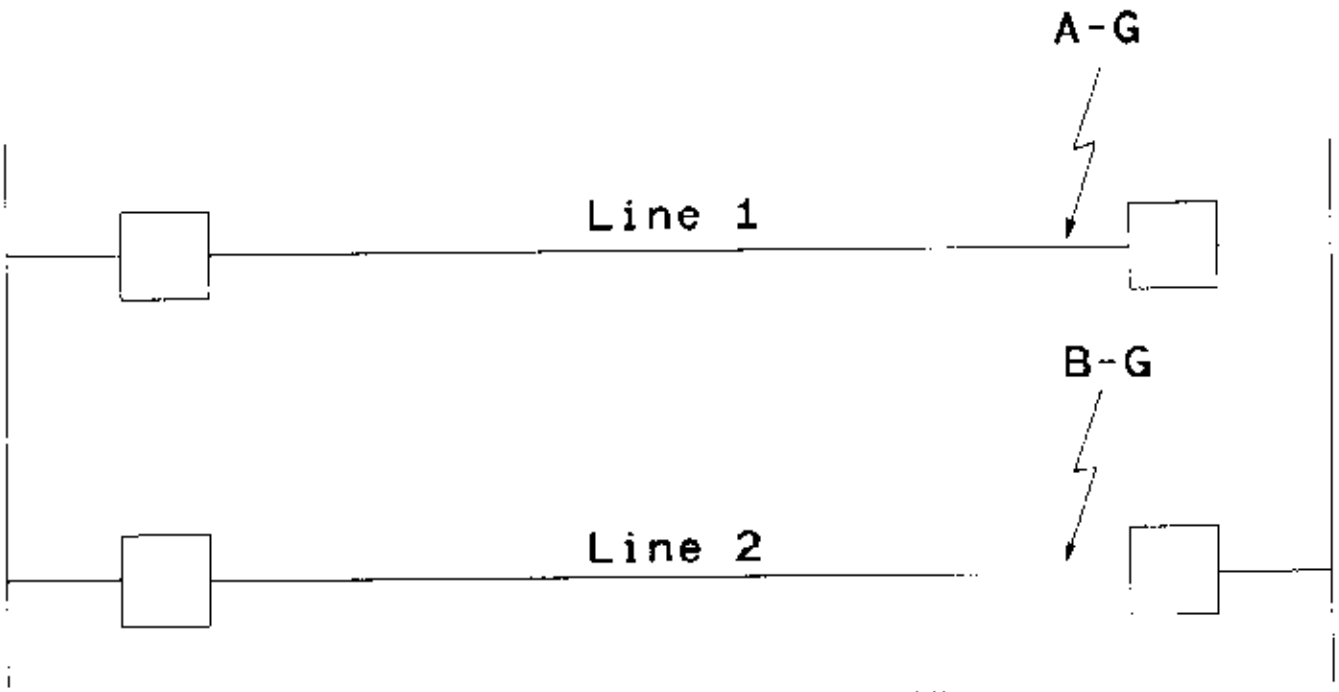


Figure 5 - Simultaneous faults on parallel lines

The inhibit reclose outputs are sealed in via a loss of voltage and are provided for use in sequential reclosing schemes; i.e., reclosing would be inhibited via this output until the voltage returns to normal at which time reclosing would then be permitted. The basic premise behind sequential reclosing is to allow the end where the fault is the least severe to reclose first and then allow the other end to follow if the reclosure is successful as indicated by the return of voltage.

The PLS System will initiate three-pole tripping for all multi-phase faults, but can not identify that the trip was initiated specifically by a three-phase fault as opposed to other fault types. However, the following can be ascertained. The PDX and PDT functions will operate for all three-phase faults on the line and may operate for some severe unbalanced faults, including single-line-to-ground (SLG) faults if they are severe enough. Of the two functions, the PDT is the least likely to operate for SLG faults (see description of PDT and PDX functions). The PD1 function will operate for all three-phase faults within its reach, for some severe line-to-line (L-L) and line-to-line-to-ground (L-L-G) faults but it will not operate for any SLG faults. Therefore, if it is desired to block reclosing for all three-phase faults and if it is acceptable to block reclosing for some severe L-L and L-L-G faults then the inhibit reclose contacts can be used. Note that blocking of reclosing for the severe L-L and L-L-G faults may be beneficial to the power system.

Lockout Reclose

A lockout reclose output will be produced if a trip is initiated and there is an output from any or all of the following functions:

1. Zone 2 timer, time-delayed trip
2. Zone 3 timer, time-delayed trip
3. TTOC, time overcurrent trip
4. CC8 (external three-pole trip)
5. Direct Transferred Trip

These outputs are not sealed in by an undervoltage condition as are the inhibit reclose outputs, and persist only as long as a trip output is produced. They can be used to cancel reclosing by energizing the appropriate input in the reclosing relay.

AMPLITUDE (ENERGY) COMPARATORS

The measuring functions in the PLS1 system use amplitude (energy) comparators, rather than the traditional phase angle comparator, to make their measurement. A simplified amplitude (energy) comparator is shown in Figure 6.

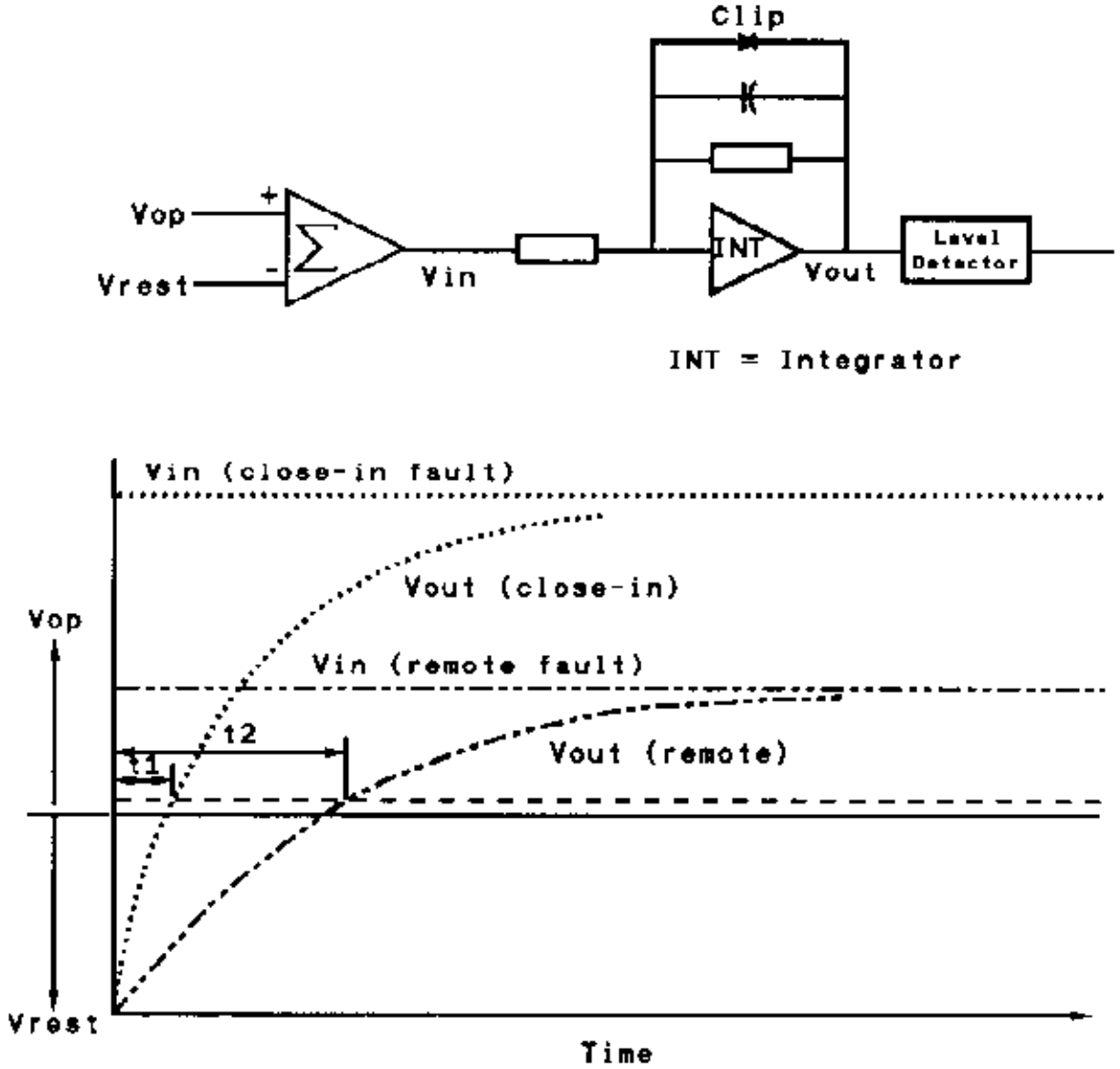


Figure 6 - Simplified Energy Comparator

In quiescent conditions, the input to the comparator is a restraint signal. When operation of the function is called for, the input signal becomes large enough to overcome the restraint input and an output is produced. How fast the function operates is dependent on the magnitude of the input signal. Larger input signals will be integrated faster than smaller signals, thus the larger the signal, the faster will be the operation as shown in Figure 6. The clip circuit is provided to limit the amount of energy stored in the integrator when very large input signals occur, such as for a close-in heavy fault condition. By limiting the energy storage, the function can be made to reset faster than would otherwise occur without the clip.

Actual input signals to an energy comparator are shown in Figure 7.

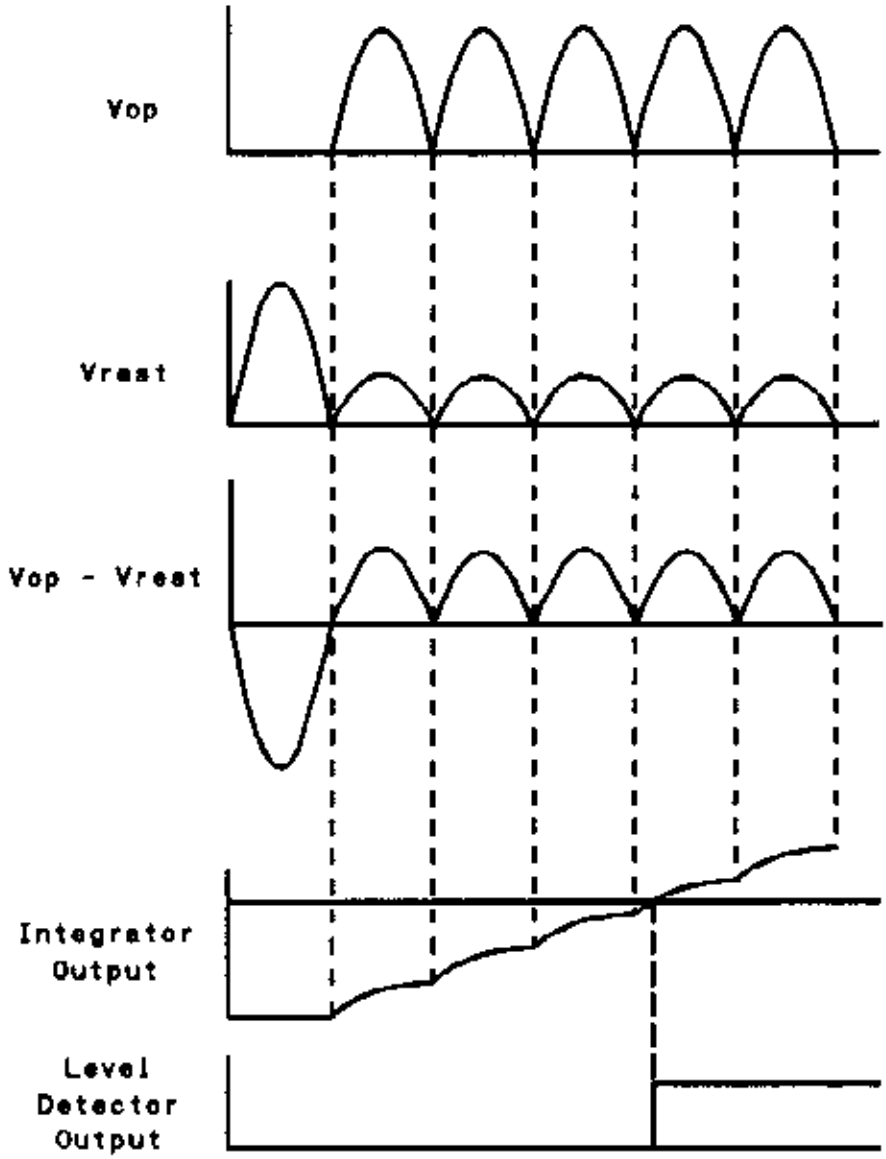


Figure 7 - Typical Input Signals to Energy Comparator

The signals shown would be similar to the operate (Vop) and restraint (Vrest) obtained from PDT, the positive sequence overreaching distance function.

POSITIVE SEQUENCE DISTANCE FUNCTIONS

The following positive sequence distance functions are included in each PLS1 transmission line relaying system:

1. PDT - Forward Looking Overreaching Tripping function
2. PD1 - Zone 1 direct tripping function
3. PDB - Reverse Looking Blocking function
4. PDX - Auxiliary tripping function
5. POSB - Out-of-step blocking function

All of the functions operate through the amplitude/energy comparator described earlier. Each function performs a different duty in the logic, therefore the operation of each will vary slightly, but each uses the same basic operating principles.

BASIC OPERATION

The basic operation of the positive distance functions in the PLS1 system can be explained by referring to Figure 8.

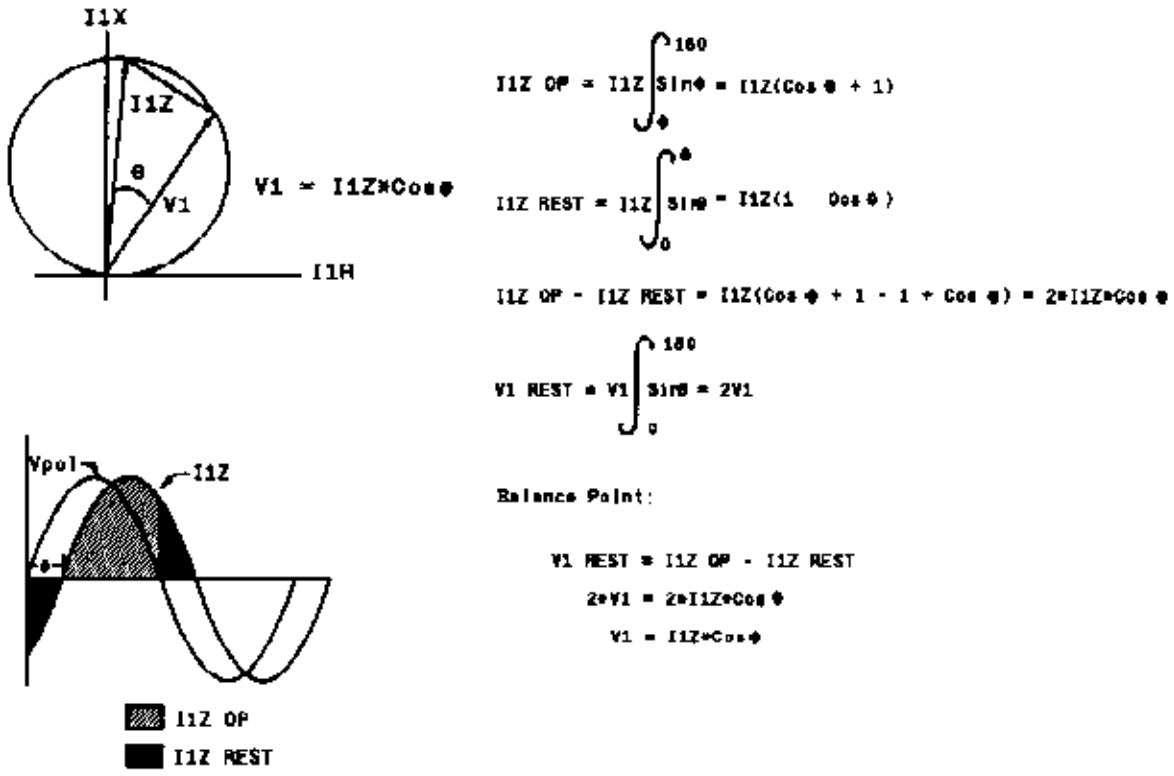


Figure 8 - Balance point conditions for positive sequence distance functions

The operating signal **I1Z OP** and the restraining signal **I1Z REST** are derived as a function of the polarizing signal Vpol, which, for steady-state operation is equal to V1, the positive sequence

voltage at the relay. When Vpol and I1Z are coincident, **I1Z OP** energy is produced whereas **I1Z REST** energy is produced when the signals are non-coincident. This is shown in Figure 9.

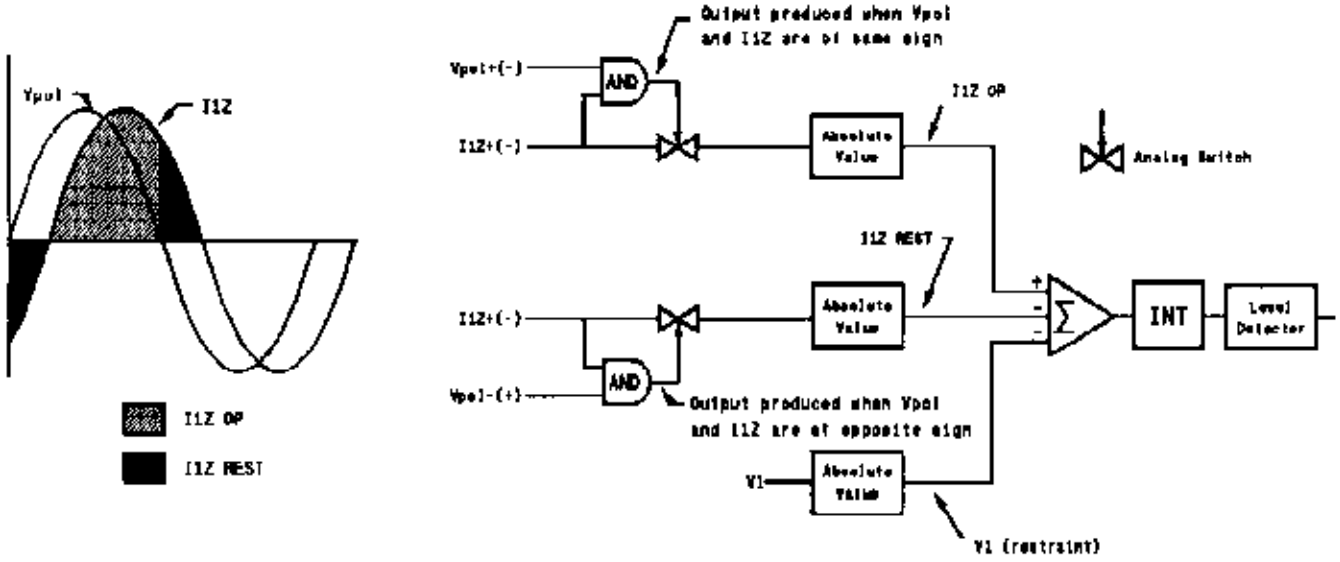


Figure 9 - Derivation of **I1Z OP** and **I1Z REST**

Operation occurs when the energy difference between the **I1Z OP** and **I1Z REST** signals is greater than the energy provided by the restraining voltage, V1. The function is at the balance point when the I1Z energy difference equals the V1 restraint energy. For faults outside of the reach, the V1 restraint energy predominates and the function will be in a restraint condition. To better understand this phenomena, refer to Figures 10 and 11.

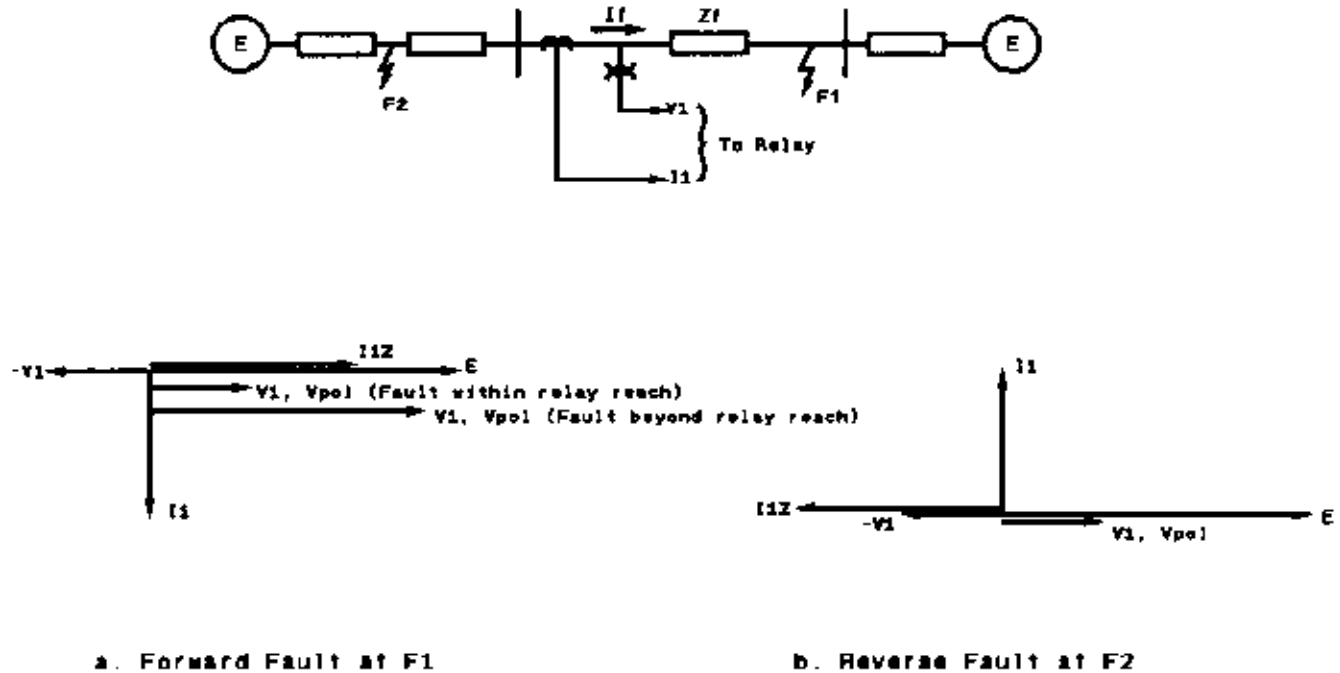
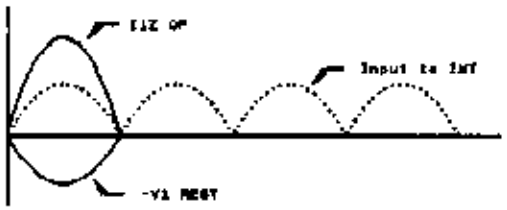


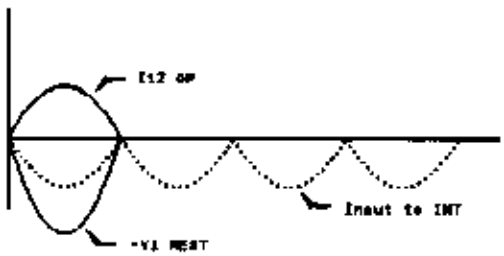
Figure 10 - Phasor Diagrams for Forward and Reverse Faults

Figure 10 shows the phasor diagrams for the forward and reverse faults shown in the simple system of that Figure. The phasors are drawn with the assumption that the fault impedance angle and the relay reach angle are equal. The important thing to note for this condition is the relationship of the polarizing voltage phasor Vpol to the relay reach phasor I1Z. For forward faults Vpol and I1Z are in phase therefore, per Figure 9, there will only be an **I1Z OP** signal produced. On the other hand, Vpol and I1Z are out of phase for reverse faults thus there will only be an **I1Z REST** signal produced.

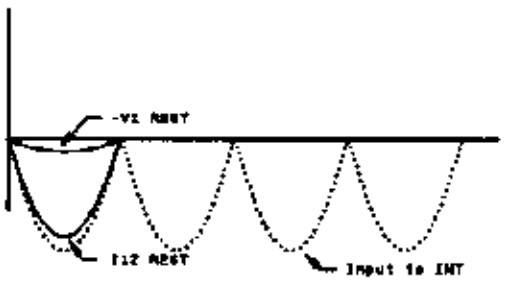
Figure 11 shows the **I1Z OP** and **V1 REST** signals seen by the SUMMER of Figure 9. **-V1 REST** is shown because that is how it is treated by the SUMMER. Also shown is the resultant output of the SUMMER which is the input to the INTEGRATOR.



a. Forward Fault Within Relay Reach



b. Forward Fault Beyond Relay Reach



c. Reverse Fault

Figure 11 - Inputs and Output of SUMMER of Figure 9

The signals are shown for three different fault conditions. For simplicity, **I1Z OP** and **V1 REST** are shown only during the first half cycle, but do exist during the succeeding half cycles wherein only the INTEGRATOR input is shown. The following observations can be made:

1. For faults within the reach of the function (Figure 11a) the **I1Z OP** signal will increase relative to the **V1 REST** signal as the fault is moved toward the function, and vice versa. Consequently, the input to the INTEGRATOR will increase in magnitude as the fault gets closer to the relay location. This will tend to lead to faster operating times for close-in faults and somewhat slower operating times for remote faults.

For large **I1Z OP** signals (long Z reaches and strong sources) operating times in the order of 3 to 4 milliseconds have been measured. Note that security will not be jeopardized for these conditions because the **I1Z OP** signals are large enough to swamp out any transients that might exist at the time of the fault.

2. For forward faults beyond the reach of the function (Figure 11b) the **V1 REST** signal is larger than the **I1Z OP** signal and gets relatively larger as the fault is moved farther away from the function. This results in a larger and larger negative (restraining) input to the INTEGRATOR which provides increased security for these remote faults.

3. For faults behind the function, there is only **I1Z REST** (no **I1Z OP**) which adds to any **V1 REST** to make the function very secure for reverse faults.

Impedance and reach angles of 90° were used in the previous analysis to simplify the explanation. A similar type of analysis can be used to show that the functions will work properly when angles other than 90° are encountered.

The steady-state and dynamic characteristics for a 90° function are shown in Figure 12.

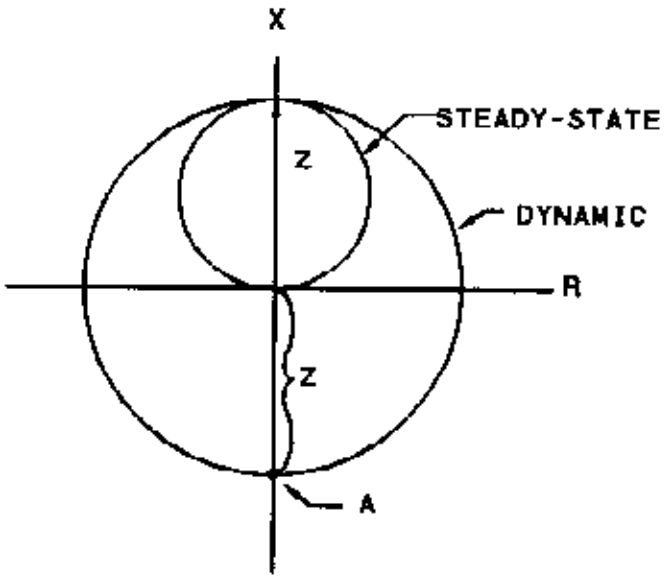


Figure 12 - Steady-state and Dynamic Characteristics of Positive Sequence Distance Function

The steady-state characteristic is self-explanatory, but the dynamic characteristic requires some explanation. The reach shown in the third and fourth quadrants does not mean that the function is non-directional. This area applies for capacitive faults in the forward direction, a condition that only arises on series compensated lines. To better understand this phenomena, refer to Figure 13, which shows a simple system with series compensation.

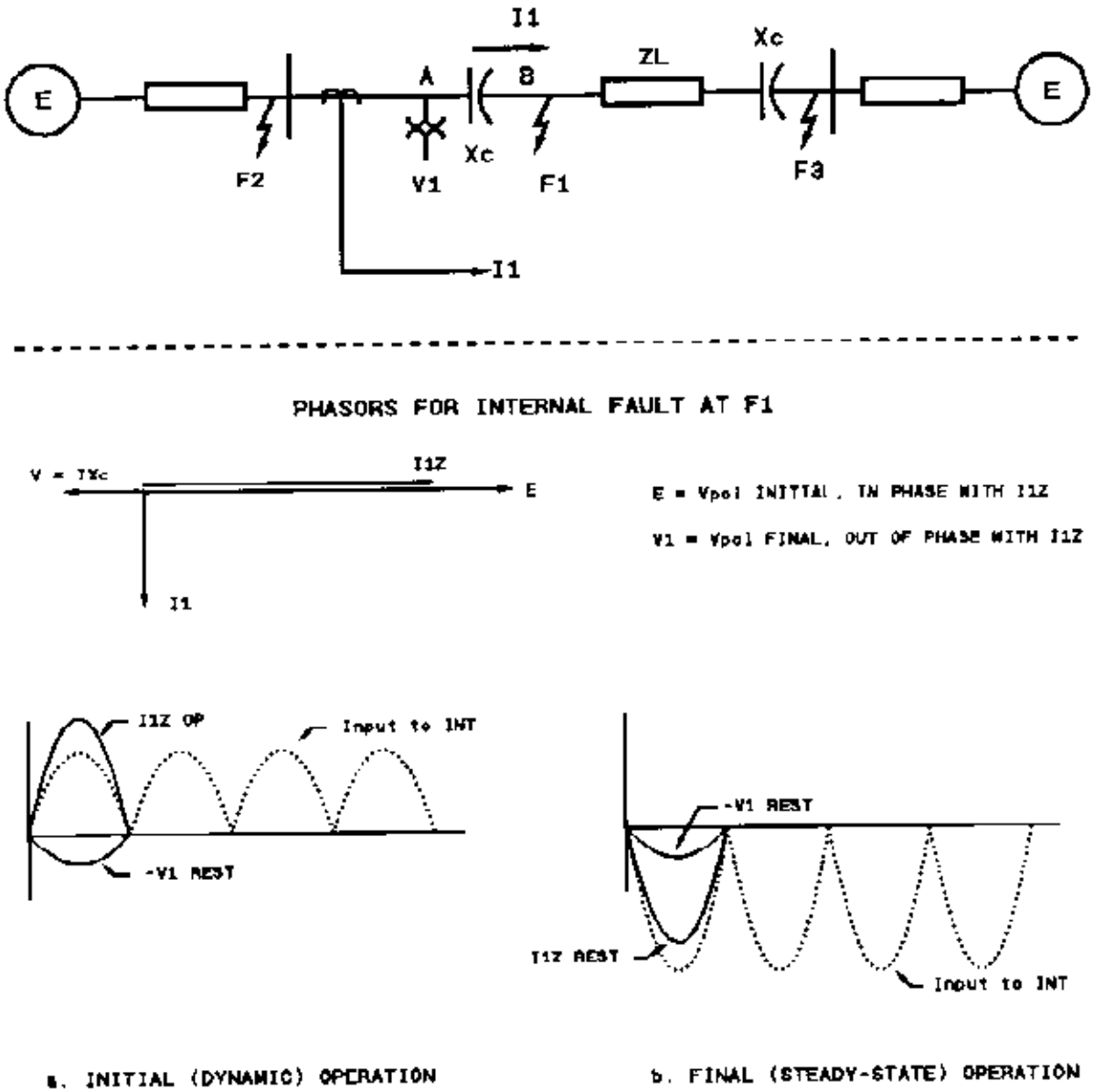


Figure 13 - System with Series Compensation

The phasor diagram for a fault at F1 is also shown in the Figure. Of import is the phase relationship of the I1Z phasor to the initial (remembered) polarizing voltage E and the final (steady-state) polarizing V1. Initially, I1Z and E are in phase thus an I1Z OP signal will be produced. If the reach Z of the function is greater than the capacitive reactance Xc of the capacitor, the function will operate because the input to the INTEGRATOR will be positive as shown in Figure 13a. After the memory has died out, and assuming the steady-state condition is reached (unlikely, unless fault clearing is delayed), the function will reset because I1Z and the final polarizing voltage V1 will be out of phase at that time, and an I1Z REST signal will be produced. This will add to the -V1 REST signal to produce a negative input into the INTEGRATOR as shown in Figure 13b. Note that if Xc = Z then the voltage V1 will be exactly equal to I1Z and the relay will be in balance at the point A shown in Figure 12. If Xc is greater than the reach Z, the impedance will plot outside of the characteristic, and the function will not operate because the input to the INTEGRATOR will go negative at that time. Thus, the characteristic does indeed have a dynamic reach along the negative X axis that is equal to the

forward reach Z of the function. For a reverse fault (F2 in Figure 12) the function will not operate because the signals produced will have the same relative relationship as shown in Figure 11c, a non-operate condition.

The basic operation of the positive sequence distance functions has just been described. Other refinements are included in the functions to provide improved performance during load flow, single-pole tripping, etc.

For example, the coincidence circuitry shown in Figure 14 is used to lessen the effects of load flow.

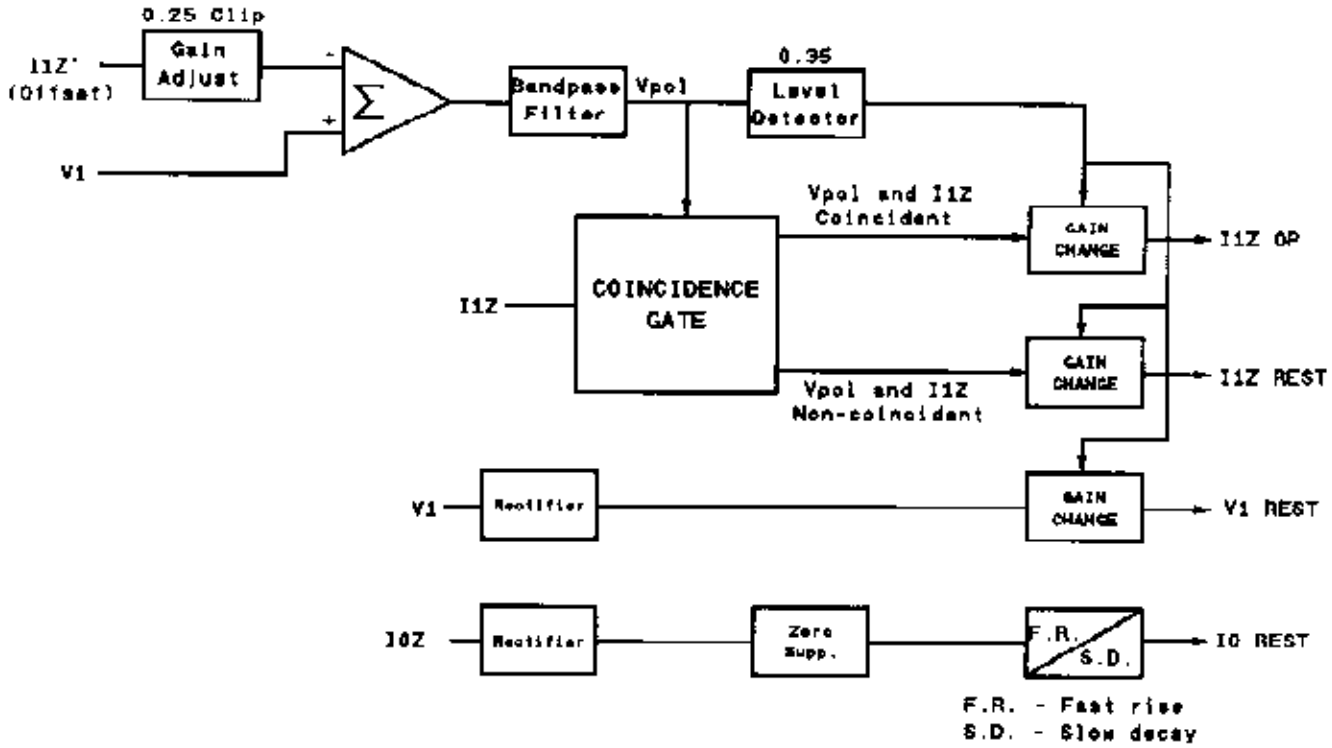


Figure 14 - Coincidence Circuitry

The output of this circuitry for fault and load conditions is shown in Figure 15a and 15b respectively. Two things should be noted about these Figures:

1. The I1Z and Vpol signals are in phase for the fault condition (a realistic condition) whereas they are significantly shifted in phase for the load condition.

2. The I1Z OP signal is much greater for the fault condition than for the load condition, which will generally be the case, especially for moderate to heavy faults.

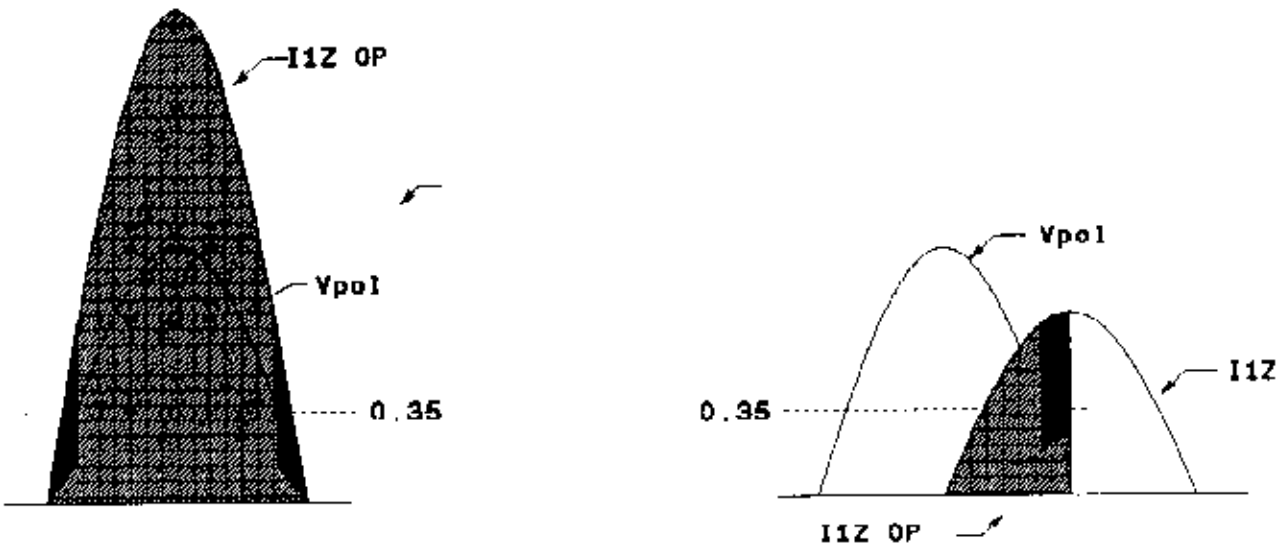


Figure 15 - I1Z OP Output of Coincidence Circuitry Shown in Fig. 12

The shaded area in these Figures represents the I1Z OP signal (operating energy) for fault and load conditions. The darkened area shows the reduction in the signal level (energy) that results from the level detector and gain change circuitry of Figure 14. For polarizing voltage signals Vpol less than 0.35 per unit, the gain is low so that the I1Z OP signal will be less as shown in Figure 15. When Vpol exceeds 0.35 per unit, the gain is increased to provide a corresponding increase in the magnitude of the I1Z OP signal. Note that the effect on the I1Z OP signal is much greater for the load condition which is desirable because it makes the function less susceptible to operation on load flow; i.e., there is less energy available for operation. For the fault condition, the overall reduction is much less, thus the operation of the function will be affected to a much lesser extent, also a desirable condition.

PDT AND PDB FUNCTIONS

To further reduce the effect of load flow, the positive sequence overreaching function PDT is provided with forward offset as shown in Figure 16.

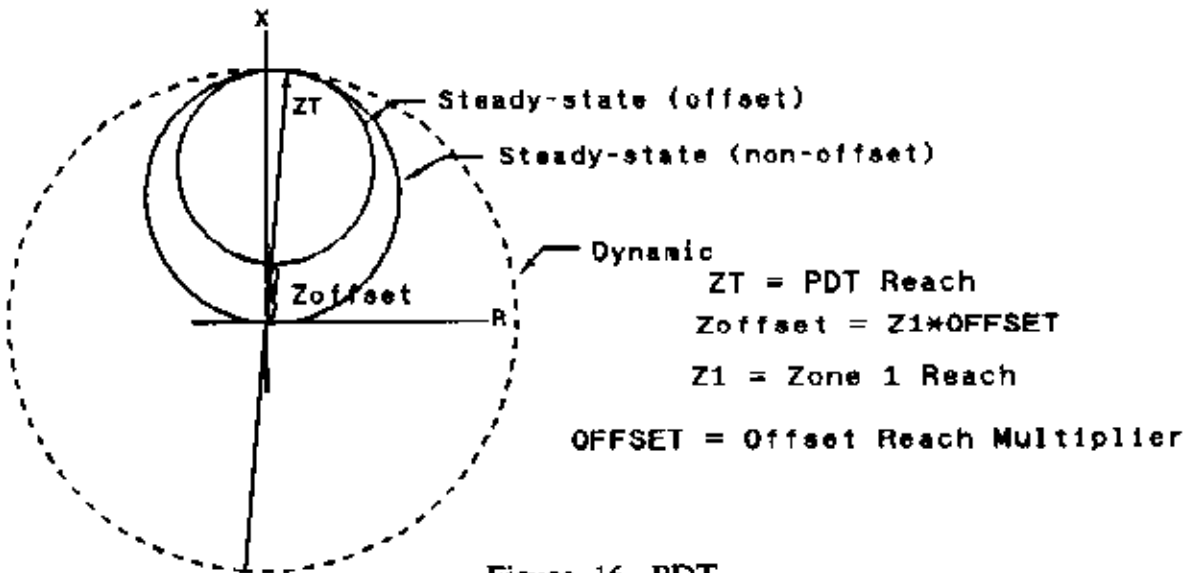


Figure 16 - PDT

As can be seen, the forward offset reduces the steady-state area of the characteristic in the region where the load impedance would normally plot. Note that the function will operate dynamically for those faults that fall in the area of the forward offset. The offset is formed in the voltage polarizing circuit by subtracting the I1Z' offset signal from the remembered positive sequence voltage (see Figure 14, upper left corner). The clip circuit is provided to limit the magnitude of the offset signal under fault conditions so that it will not override the remembered voltage during heavy faults and cause it to change to quickly.

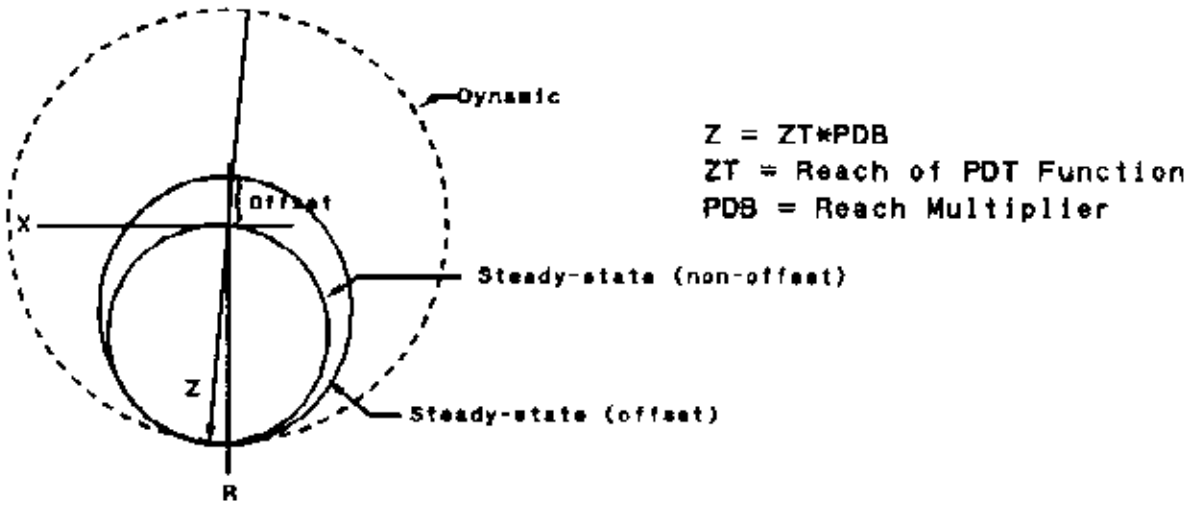


Figure 17 - PDB Function

The positive sequence blocking function PDB has a characteristic similar to the PDT function, except it has a reverse offset equal to the offset set on the PDT function. PDB has no offset when PDT is set without offset. PDB looks in the other direction from PDT as shown in Figure 17.

The block diagram in Figure 18 shows the inputs used to derive the PDT and PDB functions. There are several inputs shown on this diagram that need further discussion.

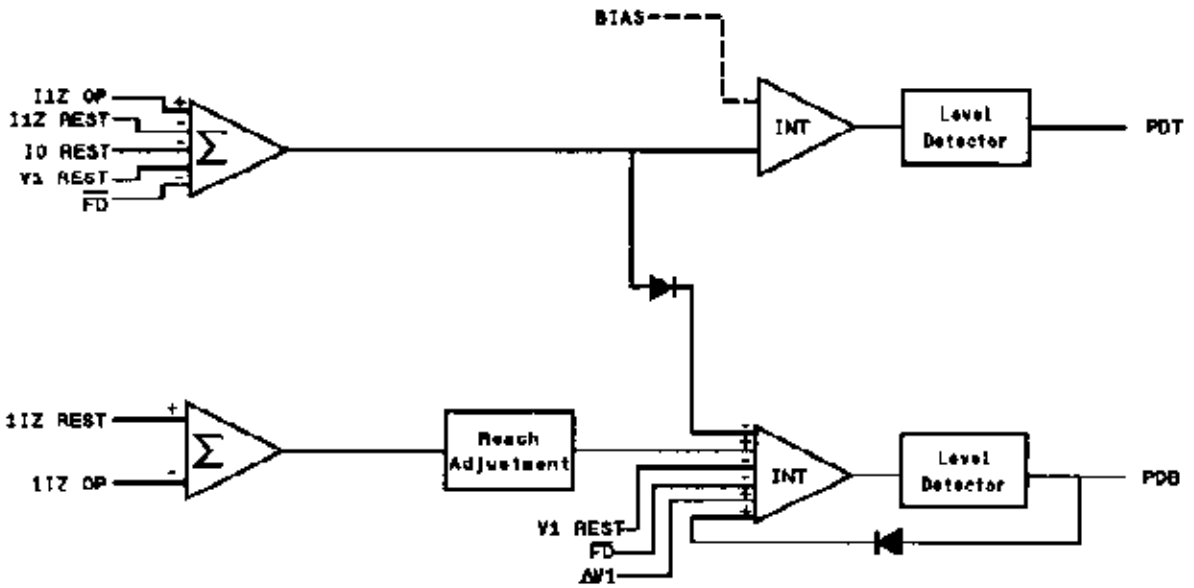


Figure 18 - Block Diagram for PDT and PDB Functions

PDT and PDB are supervised by the fault detector FD which provides a restraining signal when it is NOT picked up. When FD operates, the NOT FD input removes the negative restraint thus allowing operation of the respective function if the other conditions are met. Fault detector supervision is used to prevent operation of the functions for other than fault conditions, such as loss of potential, etc.

The PDT function has a restraint input (IO REST) that is proportional to the zero sequence current present during faults involving ground. It is intended to prevent the PDT function from operating for single-line-to-ground faults to prevent three-pole tripping from being initiated when the scheme is operated in the single-pole tripping mode.

The PDB function has an operating input that is related to the change in the positive sequence voltage ($\Delta V1$). This input is meant to speed up the operation of PDB at fault inception to enhance coordination with the PDT function at the remote terminal of the transmission line.

When offset is used on the PDT function, the PDB function is offset in the reverse direction thus making it liable to operation for some internal faults (within the offset reach) on the transmission line. The PDT function will operate for the same faults, thus the output of the PDT summing amplifier is used as a restraint signal to the PDB function to prevent it from operating for those faults.

Some applications (depending on reach settings and load) do not require offset of the PDT function, thus there will be no offset on the PDB function. Without offset, the PDB function will operate dynamically for an external zero-voltage fault and will set up blocking for that condition. The function must not be allowed to reset immediately when the memory dies out otherwise incorrect tripping could be initiated in adjacent lines if the fault had not been cleared by that time. The feedback loop shown in Figure 13 is used to seal-in the output of the PDB function to keep it picked up until the fault is cleared and voltage is returned to reset the function via the V1 REST input.

PD1 FUNCTION

The block diagram for the PD1 function is shown in Figure 19.

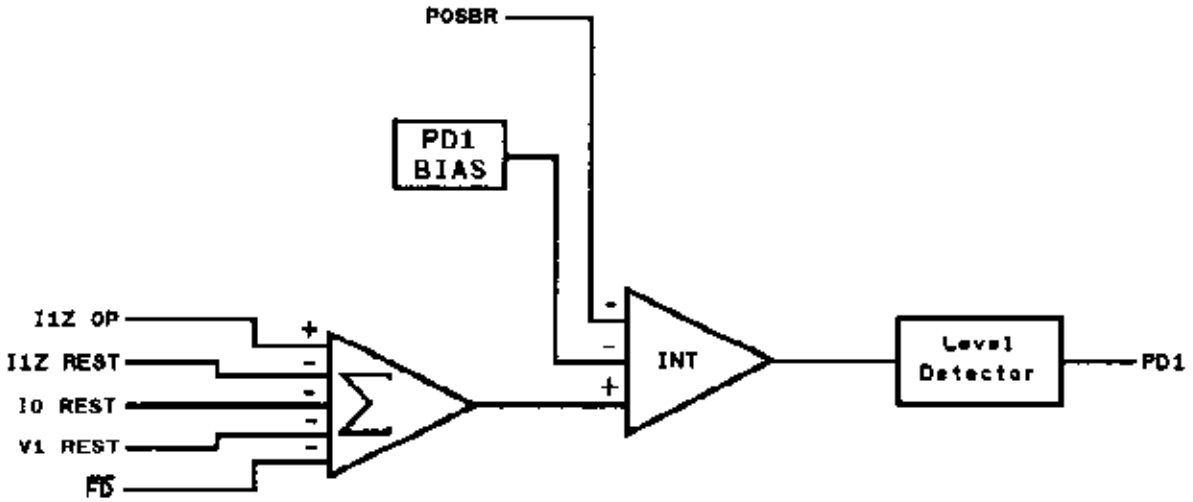


Figure 19 - Block Diagram for PD1 Function

The fault detector (NOT FD) and zero sequence restraint (IO REST) inputs to the PD1 function are used for the very same reasons described for the PDT function.

The PD1 function is restrained by an output from the out-of-step blocking function POSBR to prevent it from operating during a swing condition.

The PD1 BIAS input to the PD1 function is required when the scheme is applied on series compensated lines. The I1Z OP input to the INTEGRATOR must exceed the PD1 BIAS setting before the PD1 function can produce an output. The PD1 BIAS setting is related to the type of protection used around the series capacitor (gaps or MOV's) and is selected so that the function won't operate on transients produced by the capacitors. Refer to the following PLS1 instruction book for further details:

1. GEK-90671, Hybrid Scheme for Series Compensated Lines, Single FSK Channel

3. GEK-90669, Hybrid Scheme For Series Compensated Lines, Dual FSK (phase-identified) Channels

The PD1 bias setting is set to the minimum when the scheme is applied on uncompensated lines.

PDX FUNCTION

The PDX function is an auxiliary function that can be used to provide time-delayed backup tripping or it can be used to provide control in a sequential reclosing scheme (refer to respective instruction book for further details). The block diagram for the PDX function is shown in Figure 20.

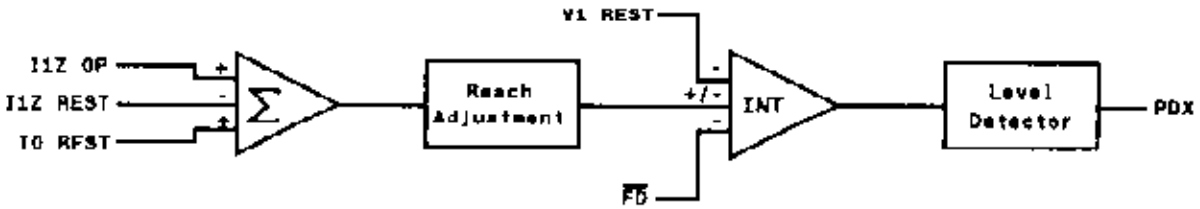


Figure 20 - Block Diagram of PDX Function

Fault detector supervision is also included with this function to prevent operation for other than fault conditions.

The IO REST signal is actually used to assist operation in this function (+ at input to SUMMER) rather than restrain as is done in the PDT and PD1 functions. This input is intended to cause operation of the PDX function for close-in heavy single-line-to-ground faults, especially near a generating station. If a sequential reclosing scheme is used, the output of the PDX function can be used to inhibit reclosing.

POSB FUNCTION

The POSB function is used to provide an out-of-step blocking output during swing conditions.

The function is restrained by the change (DELTA) in zero and/or negative sequence currents to prevent operation during unbalanced faults. Another restraint input is provided by the change (DELTA) in the operate signal (I1Z - V1) to prevent operation during three-phase faults. The DELTA restrain inputs make the function very secure against operation for other than a swing condition.

The block diagram for the POSB function is shown in Figure 21.

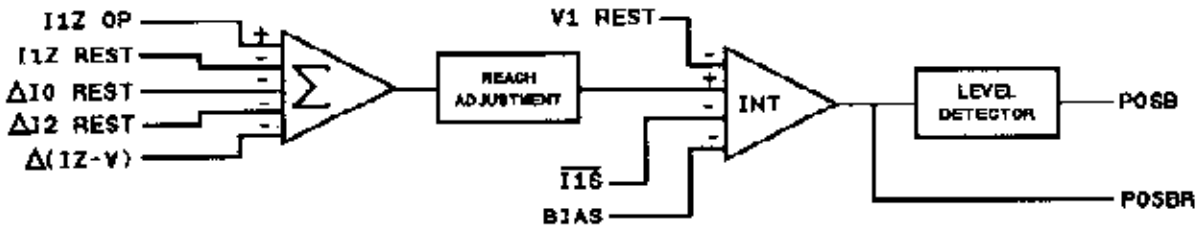


Figure 21 - Block Diagram of POSB Function

Overcurrent supervision is provided by the I1S function, a sensitively set positive sequence overcurrent function. The fault detector can not be used to provide supervision to this fault because it will not operate during a swing which is a balanced three-phase condition.

NEGATIVE SEQUENCE DISTANCE FUNCTIONS: ND and NDD

The negative sequence distance elements, ND and NDD, are primarily intended to provide protection for phase to phase faults. These functions utilize negative and positive sequence currents and voltages extracted from the line currents and voltages to develop their operating and restraining quantities. The ND and NDD use an energy comparator form of amplitude comparator as the basic discriminating unit. Operation occurs when the magnitude of the negative sequence operating quantity is greater than that of the positive sequence restraining quantity. The ND unit is used for direct tripping; the NDD unit has the same reach as the ND unit but has a shorter time constant and is used the directional comparison scheme. The ND and NDD are used as standard distance functions when they are applied on systems without series capacitors; but, similar to the PD1, ND and NDD must be used as a combined overcurrent - distance function when applied on series compensated lines, or on lines adjacent to series compensated lines. The negative sequence distance functions have a switched reach. The normal reach is equal to the Zone 1 reach setting of the PLS. When the Zone 2 or Zone 3 timers (TL2 and TL3) produce an output, the reach is increased by the reach multiplier setting.

BASIC OPERATION

The basic operating and restraining quantities for the ND and NDD functions are:

Operating: $Vop = |V2 - I2 \cdot Zr1|$ EQ. 1

Restraining: $Vrt = |V1 - I1 \cdot Zr1|$ EQ. 2

where,

Zr1 is the reach setting of the Zone 1 distance functions.

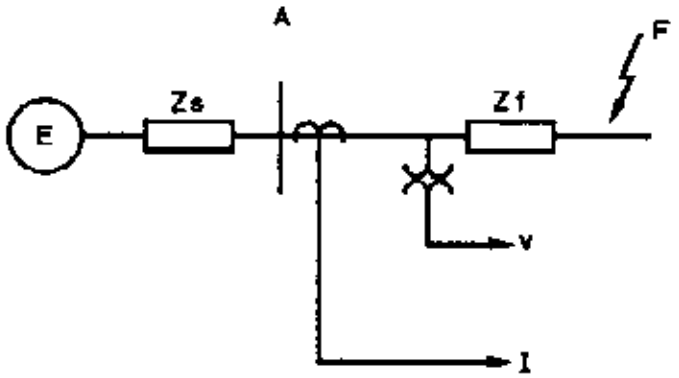


Figure 22 - Simple Power System

For a fault at the balance point, the operating and restraining quantities are equal in magnitude. The operating quantity is equal to the negative sequence voltage at the fault and the restraining quantity is equal to the positive sequence voltage at the fault. Consider a simple radial system as shown in Figure 22. Figure 23 is the sequence network for a phase to phase fault at Zf ohms from terminal A. Assume that the reach of the ND, Zr1, is set equal to Zf so that a balance point exists at the fault location.

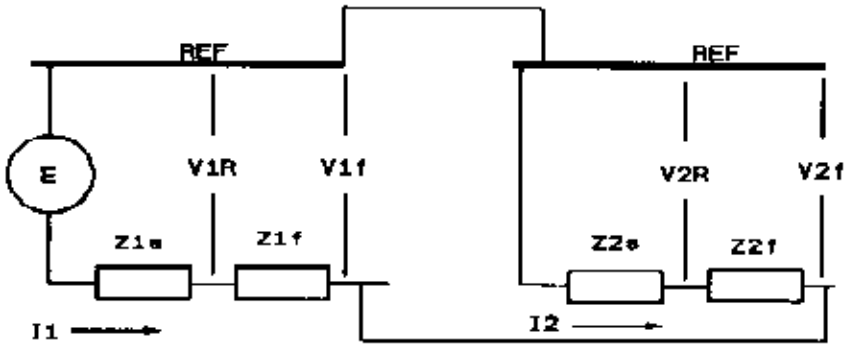


Figure 23 - Sequence Network Connections for Phase-to-phase Fault

The PLS relay system includes sequence networks that extract the positive and negative sequence currents and voltages at the relay location from the phase quantities. The sequence currents are multiplied by a replica impedance, Zr1, which for this example is equal in magnitude and angle to the impedance to the fault Zf. The IZ quantities are then combined with the sequence voltages to produce the operating and restraining quantities.

From Figure 23 it can be seen that:

$$V1R = V1f + I1 \cdot Zf \qquad \text{EQ. 3}$$

$$V2R = V2f + I2 \cdot Zf \qquad \text{EQ. 4}$$

Substituting Eq. 3 and 4 into Eq. 1 and 2 yields:

$$Vop = V2f + I2 \cdot Zf - I2 \cdot Zr1 \qquad \text{EQ. 5}$$

$$Vrt = V1f + I1 \cdot Zf - I1 \cdot Zr1 \qquad \text{EQ. 6}$$

Since Zr1 is set equal to Zf, the input quantities for the fault of Figure 23 are:

$$Vop = V2f \qquad \text{EQ. 7}$$

$$Vrt = V1f \qquad \text{EQ. 8}$$

Again from Figure 23:

$$V1f = V2f \qquad \text{EQ. 9}$$

Therefore:

$$Vop = Vrt \qquad \text{EQ. 10}$$

Figure 24 shows a convenient means to construct and view the relative magnitudes of the operating and restraining quantities for a system where the source, line, and replica impedance angles are the same. Using this graphical approach, the operating quantity is equal

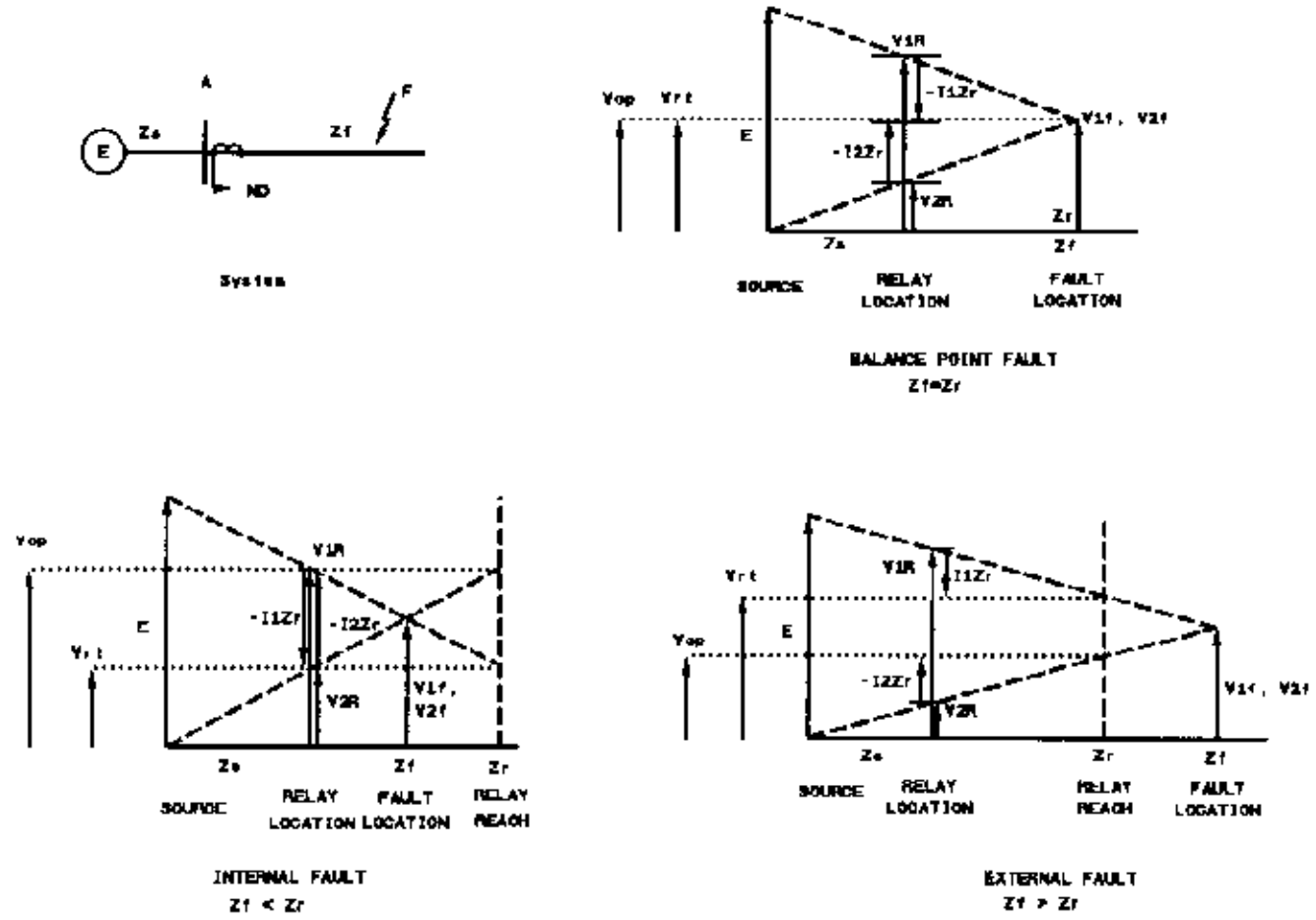


Figure 24 - Negative Sequence Distance Function Phasor Analysis

to the negative sequence voltage at a point equal to Zr1 ohms from the relay location; the restraint quantity is equal to the positive sequence voltage at the same point. (Refer to Figure 24). Figure 25 shows a numerical sample of a balance point phase to phase fault, an internal phase to phase fault, and a phase to phase fault beyond the reach of the ND unit.

IMPEDANCE TO FAULT	SOURCE IMPEDANCE	ND REACH	OPERATE SIGNAL	RESTRAINT SIGNAL
3.0	6.0	3.0	33.5	33.5
1.5	6.0	3.0	40.2	26.8
4.5	6.0	3.0	28.7	38.3

Figure 25 - Numerical Analysis

The characteristic of the ND unit is shown on an R-X diagram in Figure 26. Even though the characteristic includes area in the reverse direction (below the R axis), the unit is directional.

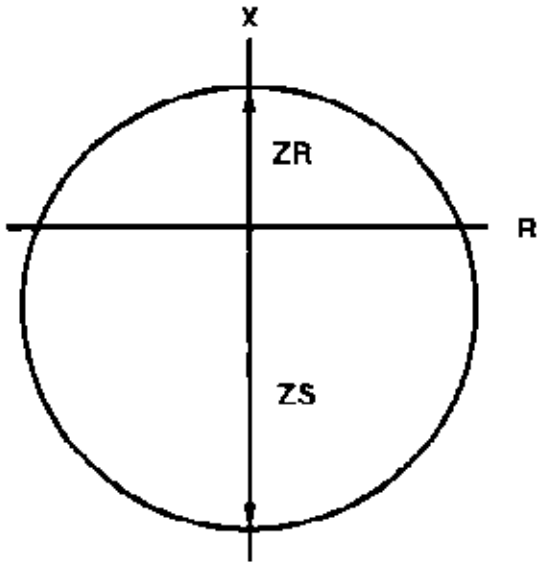
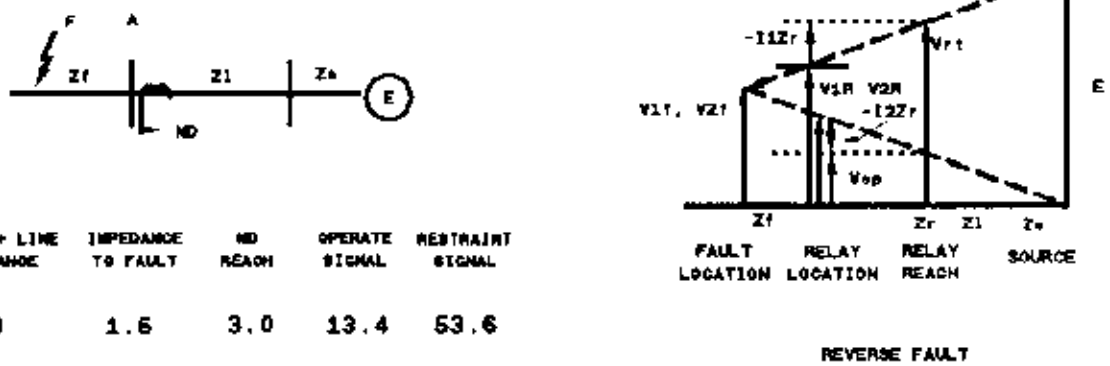


Figure 26 - Negative Sequence Distance Function Characteristic

Figure 27 illustrates this directional property by establishing that for a phase to phase fault behind the relay (on an uncompensated system), the restraint signal is always larger than the operate signal. This information is presented both graphically and with a

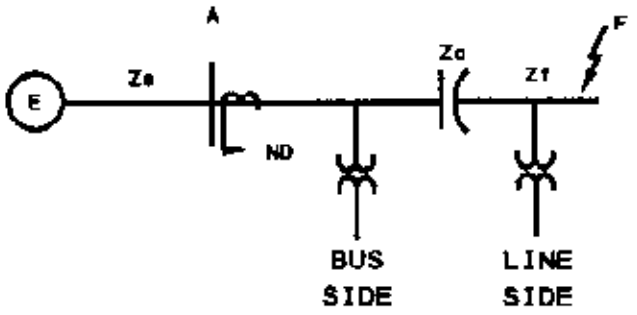


SOURCE + LINE IMPEDANCE	IMPEDANCE TO FAULT	ND REACH	OPERATE SIGNAL	RESTRAINT SIGNAL
6.0	1.6	3.0	13.4	53.6

Figure 27 - Response to Reverse Fault

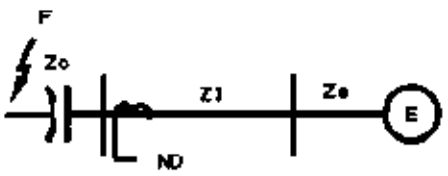
numeric example. If the fault below the R axis is actually a capacitive fault in the forward direction (i.e., net capacitive reactance between the relay and the fault), then the ND will operate as shown in Figure 28. The magnitude of the operating quantity is calculated both for a potential source located on both the line-side of the series capacitor and on the bus-side of the series capacitor.

Figure 29 shows a simple radial system with a capacitive fault located behind the relay. The table on Figure 29 shows the calculated operating and restraining quantities for three values of capacitor impedance: $Zc < Zr$, $Zc = Zr$, and $Zc > Zr$. When the impedance of the capacitor is greater than the reach of the ND unit, the ND unit operates; that is, the ND unit is no longer directional. Note that in order for the capacitive impedance to be greater than the reach setting, the line behind the relay must be considerably longer than the protected line. Two solutions exist



IMPEDANCE TO FAULT	SOURCE IMPEDANCE	CAPACITOR IMPEDANCE	ND REACH	OPERATE SIGNAL	RESTRAINT SIGNAL	POTENTIAL LOCATION
0.0	6.0	1.5	3.0	66.9	1.95	BUS
0.0	6.0	1.5	3.0	55.8	11.2	LINE

Figure 28 - Numerical Analysis for Forward Capacitive Fault



SOURCE + LINE IMPEDANCE	CAPACITOR IMPEDANCE	ND REACH	OPERATE SIGNAL	RESTRAINT SIGNAL
6.0	1.5	3.0	22.3	44.7
6.0	3.0	3.0	33.5	33.5
6.0	4.5	3.0	64.1	16.8

Figure 29 - Numerical Analysis for Reverse Capacitive Fault

for this possible operation: one is to provide directional supervision of the ND unit, the second is the use of a level detector. Both of these approaches will be discussed.

PLS IMPLEMENTATION

Figure 30 shows a block diagram of the ND and NDD negative sequence distance functions as implemented in the PLS relay. The basic operating and restraining quantities are as described previously, but there are additional inputs to enhance the performance of the function.

The inputs to the negative sequence distance unit are:

Operating quantities:

$V_{op}: | V2 - I2 \cdot Zr1 |$

Supplemental operating signal:

$K \cdot | V2 - I2 \cdot Zr1 | - X \cdot | Vnom |$

Restraining quantities:

$V_{rt}: | V1 - I1 \cdot Zr1 |$

Supplemental restraining signals:
- Switched Fault Detector bias
- Ripple attenuator
- Out of Step restraint: POSBR
- I0· Z restraint
- Open pole restraint*
- ND bias**

*Used only in ND unit.
**Used only in ND unit on series compensated lines

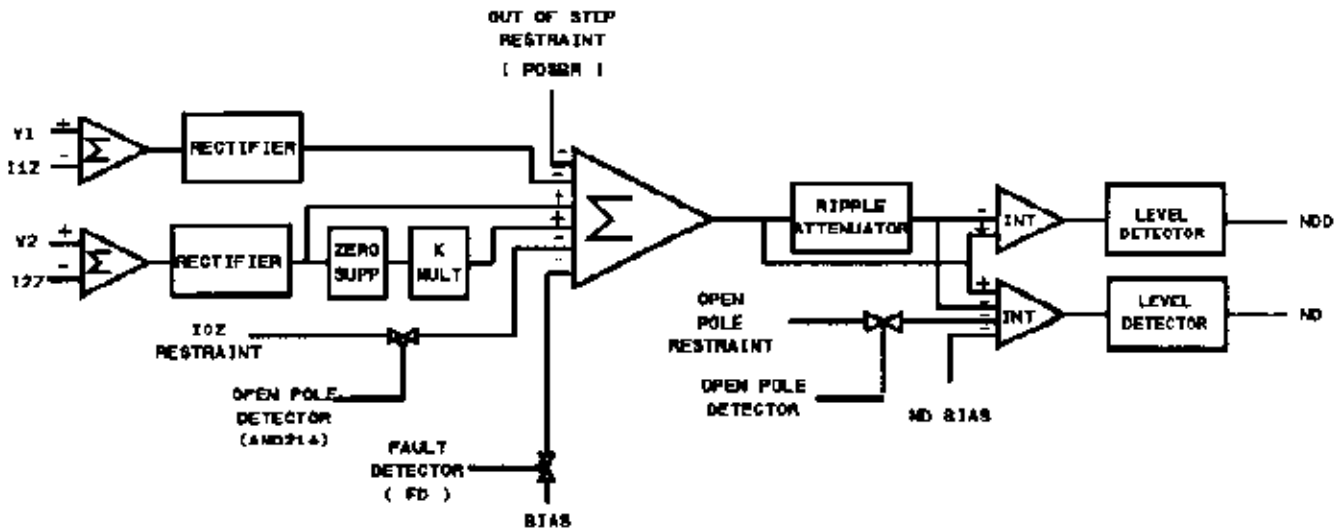


Figure 30 - Negative Sequence Distance Operating Circuit

Supplemental operating signal

K· | V2 - I2· Zr1| -X· | Vnom|

This quantity is intended to provide faster operating times for the ND unit for high magnitude faults. The magnitude of the operating signal, V2 - I2· Zr1, must be greater than 0.5 per unit volts in order for the supplemental signal to be effective. The maximum value of the operating signal for an external fault is 0.5 per unit. There are no customer adjustments on the supplemental operating signal.

Supplemental restraining signals

Switched Fault Detector Bias - The Switched Fault Detector Bias provides a pre-disturbance restraint signal for security. When the fault detector operates, this bias is removed and does not affect the performance of the relay. One of the main purposes of the Switched Fault Detector Bias is to provide a restraint signal when the line is de-energized to prevent misoperations due to transients when the breaker is closed. Under normal operating conditions, the positive sequence voltage and current provide a restraint signal to the ND unit. There are no customer adjustments on the Switched Fault Detector Bias.

Ripple Attenuator - The Ripple Attenuator consists of a bandpass filter tuned to the 2nd harmonic frequency. This circuit is used to substantially reduce the 2nd harmonic in the net operating signal without increasing the time constant of the integrator. The Ripple Attenuator does not introduce the time delay that would result from a longer integrator time constant. There are no customer adjustments on the Ripple Attenuator.

Out of Step Restraint (POSBR) - The Out of Step Restraint signal, POSBR, is derived from the OSB (Positive Sequence Out of Step Blocking unit) operating signal, and is used to desensitize the ND and NDD during out of step conditions to prevent misoperation of the negative sequence distance elements during the swing. This is required when the swing impedance passes through the ND characteristic near the forward reach point. The magnitude of the restraint signal, V1 - I1· Zr1, approaches zero for this condition. The operate signal, V2 - I2· Zr1, will have some magnitude which will be determined by the system unbalances and errors in voltages and currents and may be larger than the positive sequence restraint signal. The POSBR signal provides the needed security for this condition. There are no customer adjustments for the Out of Step Restraint.

I0· Z restraint - The I0 restraint signal is used in single pole tripping applications to prevent the ND unit from operating on close-in single line to ground faults. During the open pole period following a single pole trip, the restraint is removed to make the ND more sensitive to a second single line to ground fault which might occur during the open pole period. There are no customer adjustments on the I0 restraint signal.

Open Pole Restraint - The Open Pole Restraint signal is used in single pole tripping applications to add restraint during the open pole period following a single pole trip. During the open pole period negative sequence currents and voltages exist on the power system due to the open phase rather than from fault conditions. This signal prevent misoperation caused by these quantities and is also used to prevent operation of the ND functions for faults external to the protected line. There are no customer adjustments on the Open Pole Restraint signal.

ND Bias - The ND Bias is used in those applications on series compensated power systems. It is similar to the PD1 Bias used in the Positive Sequence Zone 1 Distance unit. The Bias is used to prevent operation on external faults in which the protective devices on the series capacitors (triggered gaps or MOV's) may not bypass.

PERFORMANCE ON OTHER FAULT TYPES

Single line to ground faults - Theoretically the ND unit can see some single line to ground faults. The PLS scheme logic is designed to either prevent the ND from operating, or if it does operate, to slow the unit to allow proper single pole tripping.

Double line to ground faults - Theoretically the ND unit will measure the correct impedance on double line to ground faults; however, the net operating signal energy will be less than for a phase to phase fault at the same location. On close in double line to ground faults, it is possible that the I0· Z restraint signal may prevent the ND unit from operating. For these faults, the positive sequence zone 1 unit, PD1, will operate and select three pole tripping.

Three phase faults - Theoretically the ND unit will not operate for three phase faults since the operating signal is base on negative sequence quantities.

NEGATIVE-SEQUENCE DIRECTIONAL FUNCTIONS: NT and NB

The NT trip and the NB block directional functions are negative-sequence voltage polarized. Like the other measurement functions in the PLS, NT and NB are implemented using the "energy comparator" described earlier. Simply stated, these directional functions determine if an unbalanced fault is in the trip or block direction by determining if the operate quantity is greater than the restraint quantity. Both the operate and restraint quantities are formed from a combination of negative-sequence current and voltage.

Since the PLS directional functions are based on implementations from the earlier SLYP/SLCN relay scheme (see GET-6456), the PLS theory of operation will be developed by first reviewing the "phase angle comparator" approach used in that scheme, then showing the theoretical conversion from the phase angle comparator approach to the amplitude comparator approach, and finally describing the energy comparator design used in the PLS.

PHASE ANGLE COMPARATOR APPROACH

A phase angle comparator compares the phase angle between phasor quantities to determine if the relay function should operate or not. The phasors are commonly termed the operate and polarize quantity. As the name implies, the polarize quantity for a directional function must be a stable reference quantity that will not reverse direction regardless of whether the fault is in the trip or block direction. Negative-sequence voltage provides a superior directional function polarizing quantity for ground faults as compared to zero-sequence current and/or voltage particularly when zero-sequence mutual coupling is present.

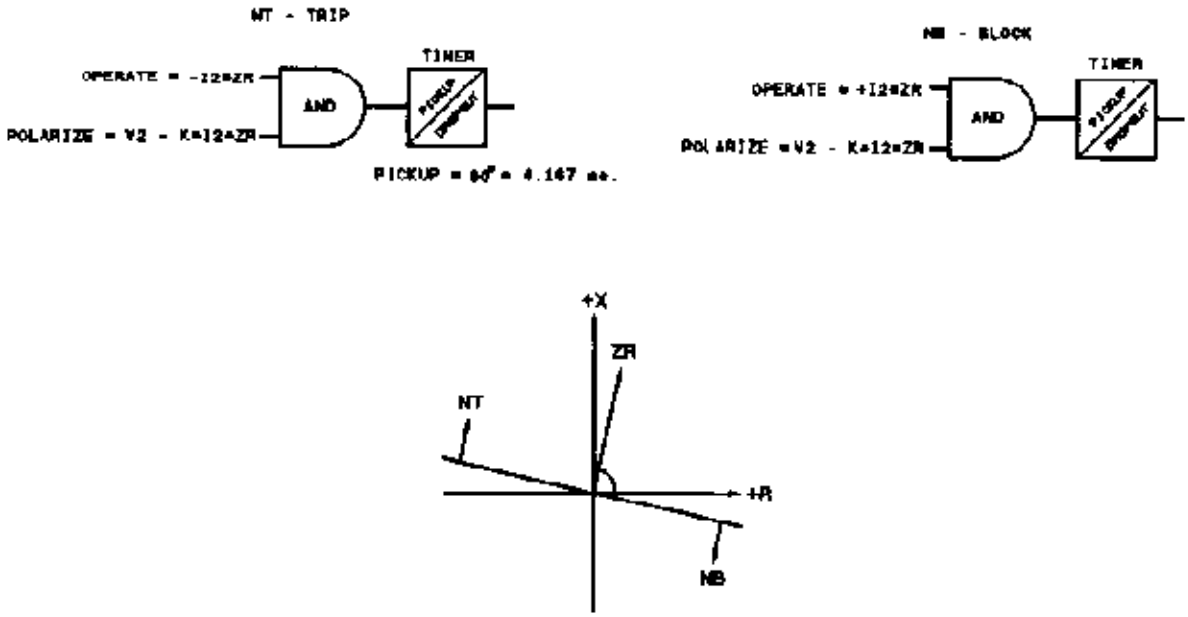


Figure 31 - NT and NB Using Basic Phase Angle Comparator

NT and NB can be derived by using a basic phase angle comparator as shown in Figure 31. The operate and polarize quantities for NT and NB using this technique are listed below:

	NT	NB
OPERATE	-I2*ZR	+I2*ZR
POLARIZE	V2 - K*I2*ZR	V2 - K*I2*ZR

where:

I2 = negative-sequence current at relay
V2 = negative-sequence voltage at relay
ZR = relay replica impedance

The operate and polarize quantities are phasors, and the phase angle comparator shown in Figure 31 produces an output when these two phasors are coincident for 90 or more electrical degrees as indicated by the timer pickup being set at 90° (or 4.167 ms. for a 60 Hz power system). The directional characteristics for these functions are shown on an R-X diagram at the bottom of Figure 31.

The use of a compensated polarizing quantity, V2 - K*I2*ZR, instead of just V2 serves two purposes. For lines without series capacitor compensation, an adequate polarizing quantity magnitude is assured even for an infinite bus. For lines with series capacitor compensation, a correct reference for faults in front of the series capacitors is assured. This will be illustrated when the PLS energy comparator design is discussed. For the PLS, the scalar value K can be set over a range of 0 to 1 with a resolution of 0.05.

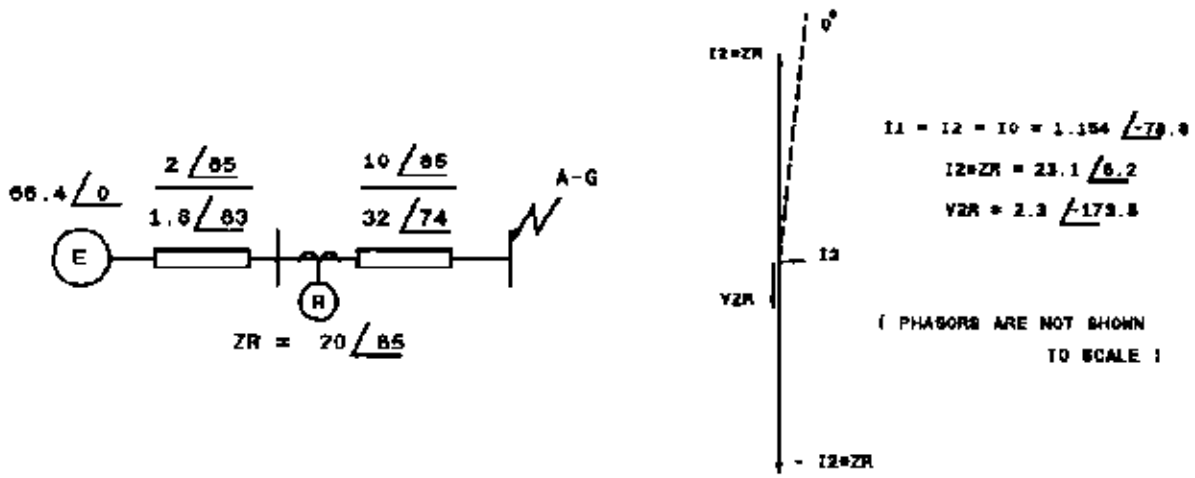


Figure 32 - Trip Function Phasors for Forward Fault

Figure 32 shows the phasor relationships for an NT directional function with an a-g fault on a simple radial system. In this example, the source and line impedance angles are 85°, and the relay replica impedance, ZR, angle is also 85°. Regardless of whether the polarize quantity is V2 or V2 - K*I2*ZR, the operate quantity, -I2*ZR, is in phase (coincident for 180°) with the polarize quantity and the NT function will operate.

AMPLITUDE COMPARATOR AND PHASE ANGLE COMPARATOR EQUIVALENCY

An amplitude comparator, in its simplest implementation, compares the magnitude of an operate quantity versus the magnitude of a restraint quantity to determine if the relay function should operate or not. If the operate quantity is larger than the restraint quantity, then the relay function operates. It can be shown that given A and B as the two phasor inputs to a phase angle comparator an equivalent relay function can be implemented as an amplitude comparator provided $|A + B|$ and $|A - B|$ are used as the two inputs to the amplitude comparator. For the NT and NB functions of Figure 31 to be implemented as an amplitude comparator, the following quantities must be used:

	NT	NB
OPERATE	$\lvert V2 - (1+K)*I2*ZR \rvert$	$\lvert V2 + (1-K)*I2*ZR \rvert$
RESTRAINT	$\lvert V2 + (1-K)*I2*ZR \rvert$	$\lvert V2 - (1+K)*I2*ZR \rvert$

The basic amplitude comparator circuitry for NT and NB is shown in Figure 33. Figure 31 and Figure 33 depict different designs for NT and NB that theoretically yield identical functional response.

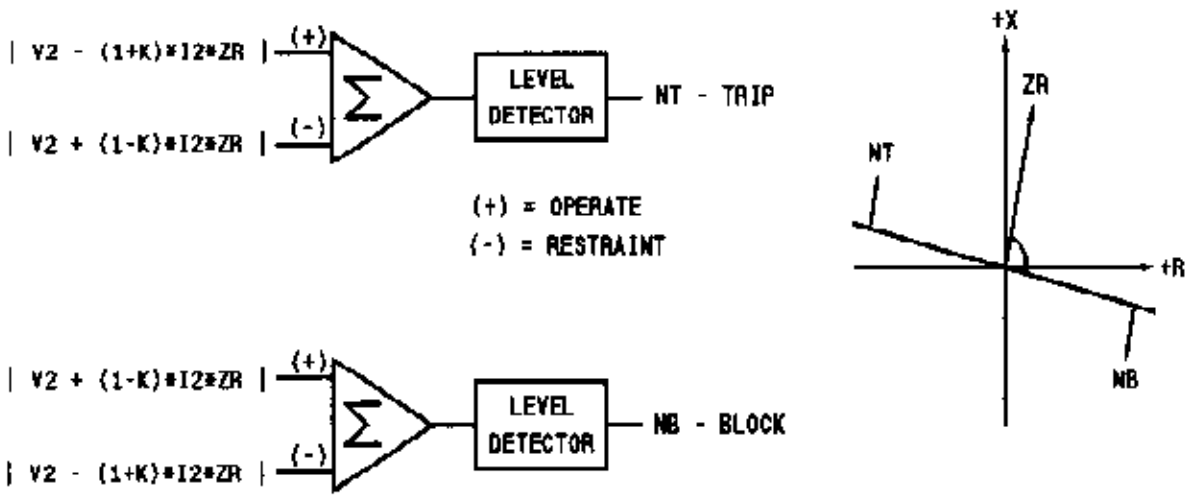


Figure 33 - NT and NB using Basic Amplitude Comparator

Figure 34 shows the phasor relationships for an amplitude comparator NT directional function with an a-g fault on the same system from Figure 32. A K value of 0.1 is assumed for this example. Since $|Vop| > |Vrest|$, the NT function operates for the assumed fault and system conditions.

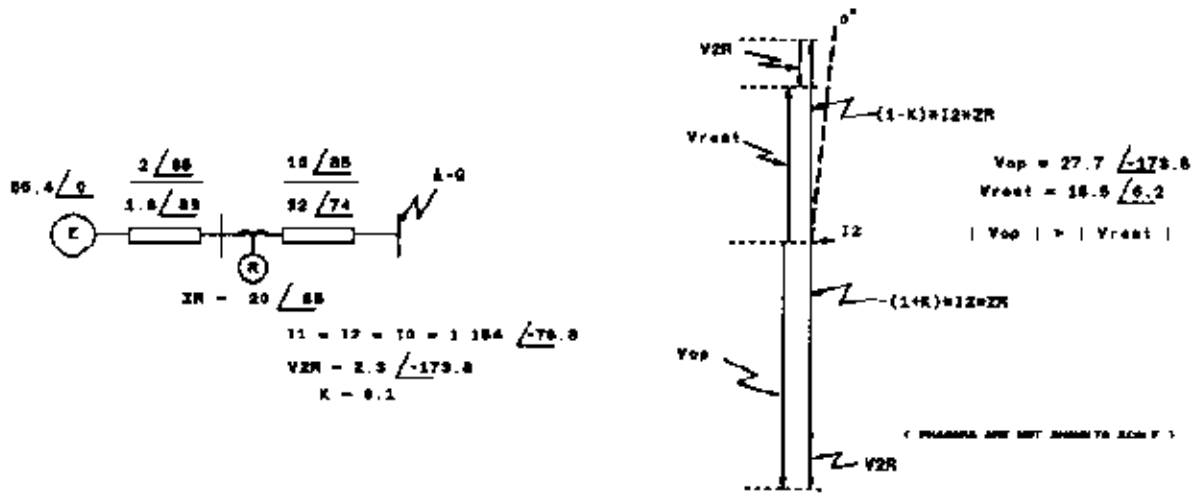


Figure 34 - Phasors for Trip Function Using Energy Comparator

ENERGY COMPARATOR IMPLEMENTATION

A simplified representation of the NT and NB circuitry as implemented in the PLS is shown in Figure 35. As noted before, an energy comparator is utilized rather than a simple amplitude comparator. The PLS design also uses different operate and restraint quantities for NT and NB as compared to the theoretical quantities described previously.

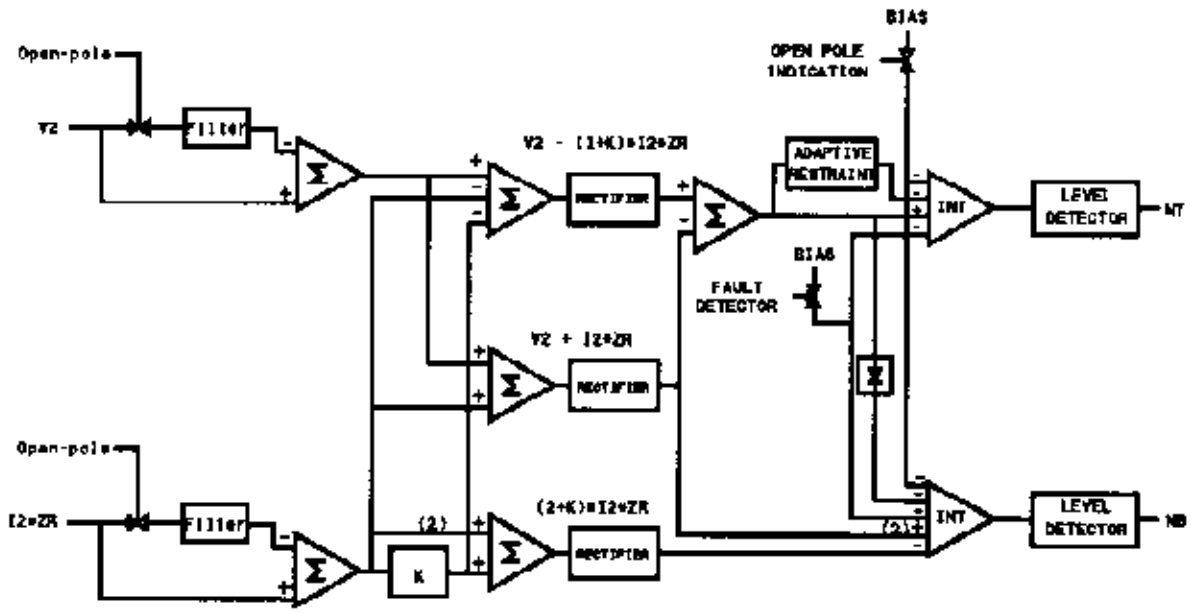


Figure 35 - NT and NB Circuitry using Energy Comparator

The actual PLS operate and restraint quantities are tabulated below:

	NT	NB
OPERATE	| V2 – (1+K)*I2*ZR|	| 2*V2 + 2*I2*ZR|
RESTRAINT	| V2 + I2*ZR|	| (2+K)*I2*ZR|

The NT restraint quantity is | V2 + I2*ZR| rather than the theoretical | V2 + (1−K)*I2*ZR| . The elimination of the (1−K) factor creates a larger magnitude restraint quantity for increased security.

For the NB function, both the operate and restraint quantities are essentially doubled in magnitude compared to the corresponding NT values. NB is a blocking function and NT is a tripping function. A blocking function at one end of a protected line should operate as fast as or faster than the tripping function at the other end for a through fault condition. Doubling the NB operate and restraint quantities compared to NT assures more energy in NB and consequently a faster operate time compared to NT at the other end for the through fault condition.

Other than the factor of two mentioned above there are other differences in the NB operate and restraint quantities compared to the theoretical quantities shown in Figure 33. The restraint quantity is | (2+K)*I2*ZR| rather than the theoretical | 2*V2 − 2*(1+K)*I2*ZR| . Elimination of 2*V2 creates a smaller restraint quantity that increases dependability and speed of operation. The operate quantity is | 2*V2 + 2*I2*ZR| rather than the theoretical | 2*V2 + 2*(1−K)*I2*ZR| . Elimination of the (1−K) factor creates a larger operate quantity for dependability and speed.

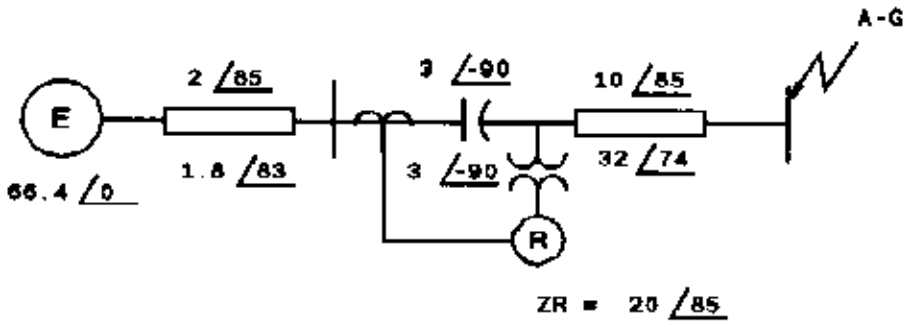
Figure 36 is the same system from Figure 32 with 30% series capacitor compensation added at the relay location. Note that the potential supply is located on the line-side of the series capacitor bank. This system will be used to illustrate that the offset factor, K, provides reliable operation of NT for a forward a-g fault even when the series capacitor bank protective gaps do not operate to short out the capacitive reactance. As noted on Figure 36, V2 at the relay is virtually reversed from the V2 at the fault. This would result in non-operation of NT if K = 0 as indicated below.

$$\begin{aligned} \text{OPERATE} &= |\, V2 - I2*ZR \,| \\ &= |\, 1.39 \angle 23^\circ - (1.36 \angle -76.8^\circ)*(20 \angle 85^\circ) \,| \\ &= |\, 25.86 \angle -172.6^\circ \,| \\ \text{RESTRAINT} &= |\, V2 + I2*ZR \,| \\ &= |\, 28.54 \,| \end{aligned}$$

Since RESTRAINT > OPERATE, NT will not operate if K = 0. If K is set according to the formula given below, then NT will operate.

$$K = \frac{2*Xc}{ZR}$$

where: Xc = reactance of series capacitor bank
ZR = NT reach = 20 ohms



I1 = I2 = I0 = 1.36 /-76.8

V2 (AT FAULT) = 12.3 /173.5

V2 (AT RELAY) = 1.39 /23

Figure 36 - Series Compensated System

For the example of Figure 36, K = 2*3/20 = 0.3. A margin of 10% is suggested making K = 0.33. Since the PLS setting resolution for K is 0.05, the actual value used would be K = 0.35. The calculations below illustrate that NT will operate with K = 0.35.

$$\begin{aligned} \text{OPERATE} &= |\, V2 - (1+K)*I2*ZR \,| \\ &= |\, 1.39\angle 23^\circ - (1.35)*(1.36\angle -76.8^\circ)*(20\angle 85^\circ) \,| \\ &= |\, 35.37 \,| \\ \text{RESTRAINT} &= |\, V2 + I2*ZR \,| \\ &= |\, 28.54 \,| \end{aligned}$$

Since OPERATE > RESTRAINT, NT will operate if K = 0.35.

The basic advantage of the energy comparator is that an integrator (an integrating op-amp) replaces the magnitude comparator of the simple amplitude comparator. If the difference between the operate signal and restraint signal is positive, then the energy comparator integrates "up" toward the trip threshold level. If this difference is negative, then the energy comparator integrates "down" away from the trip threshold level. This allows for modifying the response of NT and NB by adding additional restraint inputs based on what other measuring functions and the scheme logic are indicating.

As shown on Figure 35, both NT and NB have restraint "energy" added when one pole is open and when the fault detector is not operated. Both of these restraint levels, shown as "BIAS" on Figure 35, are fixed by design. With one pole open it is necessary to desensitize NT and NB to prevent operation on the resulting negative-sequence current and voltage. The open-pole detector also switches in the filter circuits shown in the V2 and I2*ZR inputs shown in Figure 35. This cancels out the V2 and I2*ZR signals so that NT and NB cannot operate on the negative sequence quantities produced with a pole open. Both functions will operate transiently, however, because the output of the filter will not change instantly for a concurrent change in the input.

Under normal power system conditions the fault detector is not picked up. This fact switches in a level of restraint energy for security biasing. When the fault detector picks up indicating a system fault or disturbance, this restraint is removed, and if either NT or NB begins to integrate "up" toward operation the integration must overcome the initial restraint energy. Simply stated, at the instance a fault occurs both NT and NB are biased toward non-operation.

NT also incorporates an "adaptive restraint" which provides a restraint input based on the NT output signal (difference between the NT operate and restraint signals). The purpose of this arrangement is to prevent NT from operating if the negative-sequence current and voltage change slowly over time. Many transmission lines are untransposed, and this dissymmetry coupled with normal load flow results in the presence of negative-sequence current and voltage at the relay. As the load flow across the untransposed line increases, the level of negative-sequence quantities at the relay increases. The adaptive restraint feature prevents any possible operation of NT for this condition by supplying a restraint signal to balance the operate signal provided the operate signal is changing slowly. Adaptive restraint has virtually no effect during fault conditions.

NB is restrained by the NT operate signal. This is indicated on Figure 35 by the diode symbol within a box. This is a representation that restraint energy is only applied to NB when the NT output signal is positive (operate signal greater than restraint signal). This arrangement gives the local NT priority over the local NB.

OVER-CURRENT FUNCTIONS

The PLS relay scheme uses a variety of over-current functions for supervision, coordination, and tripping. A list of the functions along with a brief description is provided below.

FD - Fault Detector
IMA, IMB, IMC - Sensitive phase current detectors
3I0 - Zero sequence current detector
IB - Over-current blocking function
IT - Over-current tripping function
I1T - Positive sequence over-current function
IDT - Direct tripping over-current function
ITOC - Time over-current function

FD - FAULT DETECTOR FUNCTION

The Fault Detector (FD) is a sensitive current disturbance detector. The main duty of this function is to supervise the trip output from the PLS scheme. No trip outputs are permitted unless the FD function operates. The purpose of the Fault Detector is to increase the security of the relay system against misoperations due to component failures. A block diagram of the Fault Detector is shown in Figure 37. The function responds to

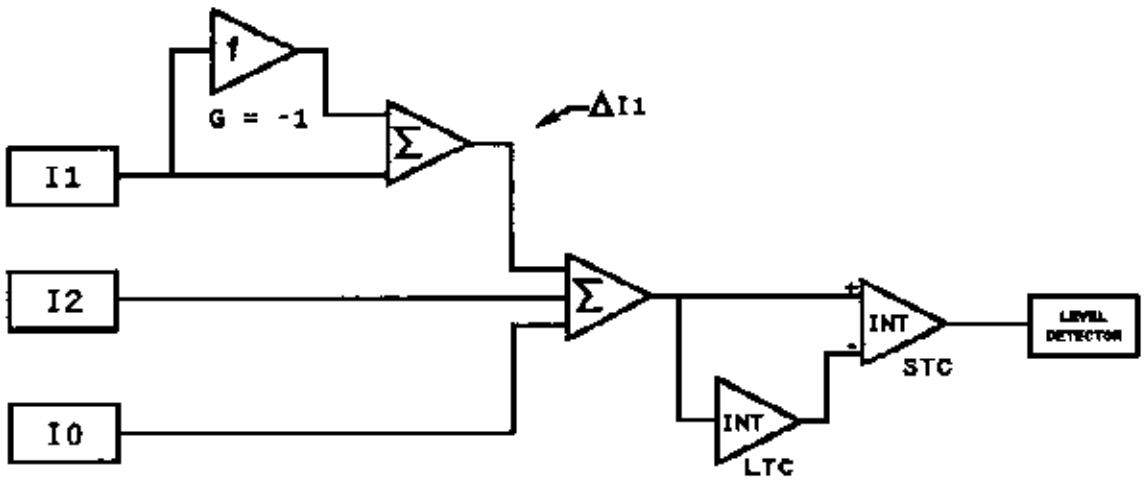


Figure 37 - Fault Detector Function

the summation of the magnitudes of the zero sequence current, the negative sequence current, and the change in the positive sequence current. The change in positive sequence current is produced using a bandpass filter with a gain of -1, as shown in Figure 35. The Δ I1 signal is a transient signal whose duration depends upon the magnitude of the change in current. The Fault Detector circuit uses the integrator approach and incorporates two integrators of different time constants. For low level signals, the output of the long time constant integrator (LTC) is used to cancel the output of the current summer. Thus for low level signals the output of the Fault Detector will be transient. This allows the Fault Detector to adapt to different levels of current unbalance on the transmission line. There is a clamp on the long time constant integrator that limits its output to low level signals. Thus for higher fault currents the output of the fault detector is steady state.

In addition to supervising the trip outputs, the Fault detector output is also used to switch various signals in the PLS measuring functions and as an input to the Continuous Monitor logic module (if supplied).

IMA, IMB, IMC - PHASE CURRENT DETECTORS

The IM functions are sensitive phase current detectors. These functions are used in the open pole detection circuits and also to seal-in the trip and BFI (Breaker Failure Initiate) outputs. The IM functions are typically set to a level equal to 150% of the positive sequence charging current of the line.

3I0 - ZERO-SEQUENCE CURRENT DETECTOR

The 3I0 function as a supervision signal for the Negative Sequence Distance functions; specifically if the 3I0 function picks up, the Negative Sequence distance functions are prevented from initiating a three pole trip. Thus, if the Negative Sequence Distance functions operate for a close in single line to ground fault, they can not initiate incorrect three pole tripping.

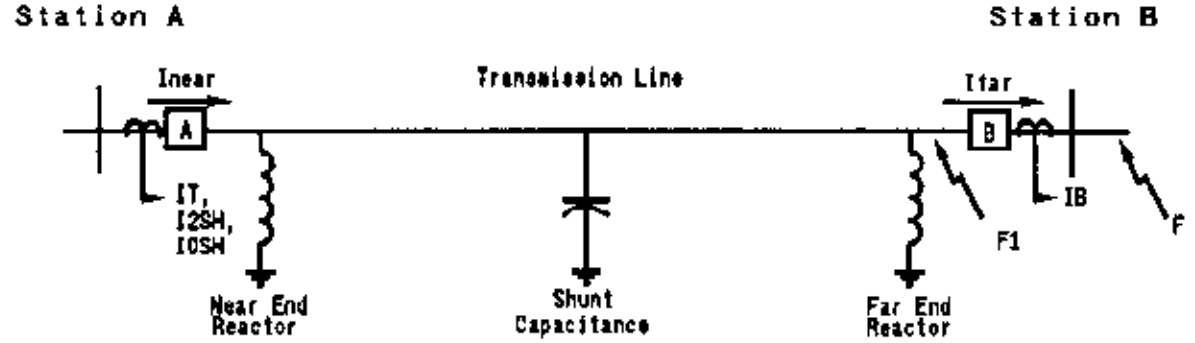
IT - OVER-CURRENT TRIPPING FUNCTION
IB - OVER-CURRENT BLOCKING FUNCTION

The IT (tripping) and IB (blocking) functions are used in the directional comparison scheme along with the negative sequence directional functions to provide sensitive tripping for ground faults. The following operating signals are used:

IT operate signal = $(2|I0| + |I2| - 0.3|I1|)$

IB operate signal = $(2|I0| + |I2| - 0.2|I1|)$

IT and IB must coordinate with each other. This coordination is achieved via the settings placed on the functions, with the requirement that IB at one terminal of the line be more sensitive than



Transmission Line:
XL2 = negative sequence reactance
XL0 = zero sequence reactance

Far End Reactor:
XRF2 = negative sequence reactance
XRF0 = zero sequence reactance

Near End Reactor:
XRN2 = negative sequence reactance
XRN0 = zero sequence reactance

Shunt Capacitance:
XC2 = negative sequence reactance
XC0 = zero sequence reactance

Figure 38 - Sample Power System

IT at the other terminal, and by the lower positive sequence current restraint in the IB. For example, IB at Station B in Figure 38 below must be more sensitive than IT at station A.

Note that the negative and zero sequence currents entering the line will be greater than the respective currents leaving because of the charging current. This must be taken into account. In Figure 38 for example, the negative and zero sequence currents at Station A (I near) will be greater than the respective current at Station B (I far). How much the current will differ will be affected by any shunt compensation used on the line (such as the far end and near end reactors shown in the figure). It is possible to compensate for the effect of the charging current by simply setting IT greater than IB by the amount of the charging current. However, this would entail a fixed difference in setting which would limit the sensitivity of IT. To overcome this limitation, the IT function is provided with an adaptive restraint via the I2 SHUNT and the I0 SHUNT inputs as shown in the block diagram of Figure 38. For example, for a phase-to-phase fault at F in Figure 37, the negative sequence voltage will be relatively large, which in turn will produce a large restraining quantity which is desirable in this instance to assure positive coordination. On the other hand, consider a high resistance fault at F1. For this condition, the negative and zero sequence voltages will be quite low, thus the restraining effect of I2 SHUNT and I0 SHUNT on the IT function at Station A will be minimized thus allowing greater sensitivity for resistive faults.

When bus-side potential is used, bypassing of one or two phases of the capacitor bank could cause the related unbalance (due to load) to appear as an internal fault to the negative sequence directional functions. To prevent tripping, the IT function must be set above the unbalanced current produced during this condition.

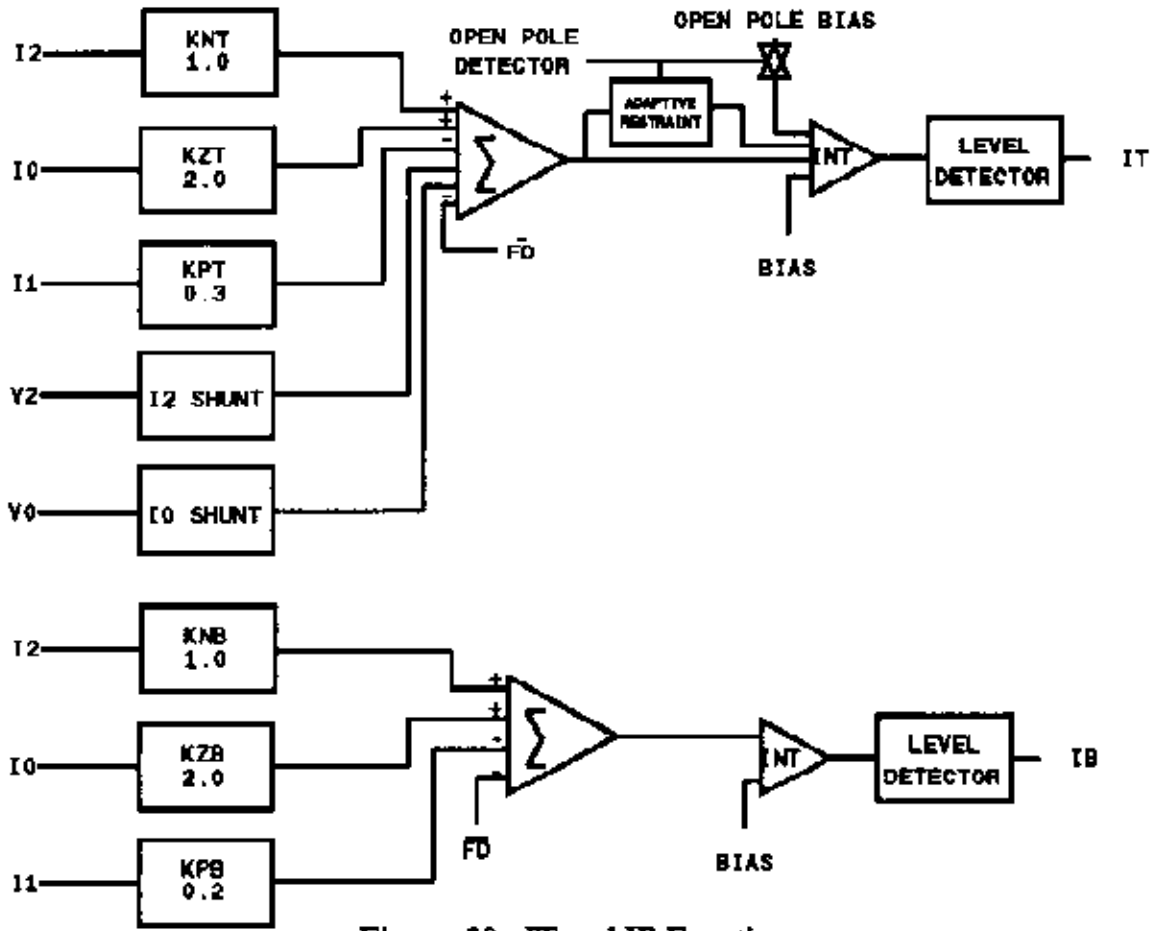


Figure 39 - IT and IB Functions

in addition to the I2 SHUNT and I0 SHUNT, the IT function also has an adaptive pickup feature. As shown in Figure 39, the output of the IT operating signal summer goes to an adaptive restraint circuit. This circuit is similar to that used in the Fault Detector. For low levels of unbalanced currents, the output of the adaptive restraint circuit will cause the IT function to reset after a time delay, during the open pole period following a single phase trip, the limit on the output of the adaptive circuit is raised, thus preventing the IT function to pickup on the unbalanced current due to the open phase. An additional bias, which increases the IT pickup level, is also added at this time.

I1T - POSITIVE-SEQUENCE OVERCURRENT FUNCTION

The I1T function is a positive sequence over-current function that is used in the Line Pickup (Switch onto Fault) Logic.

IDT - OVERCURRENT DIRECT TRIP FUNCTION

The IDT direct tripping overcurrent function uses zero sequence current and may be applied with or without positive sequence current restraint. The IDT operating quantity is:

IDT(operate) = (3I0 - K1I1)

Where:

K1 = 1 or 0

Positive sequence current restraint is recommended (K1 = 1) because it makes the function less sensitive to external faults, while providing excellent sensitivity for close-in internal faults. A block diagram of the IDT function is shown in Figure 40.

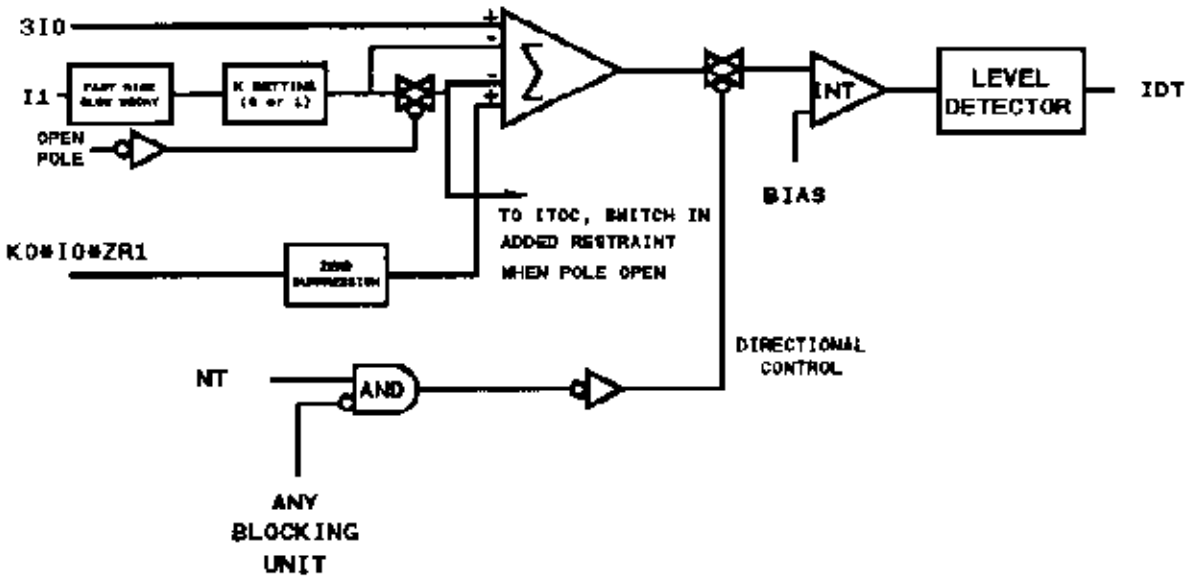


Figure 40 - IDT Function

For example, with K1 = 1, consider the following three cases for the system shown in Figure 41.

Case 1, SLG fault at F1, all breakers closed

I1 = 1180A I0 = 540A

IDT(operate) = [3(540) - 1180] = **440A**

Case 2, SLG fault at F4, breaker B open

I1 = 1023A I0 = 1023A

IDT(operate) = [3(1023) - 1023] = **2046A**

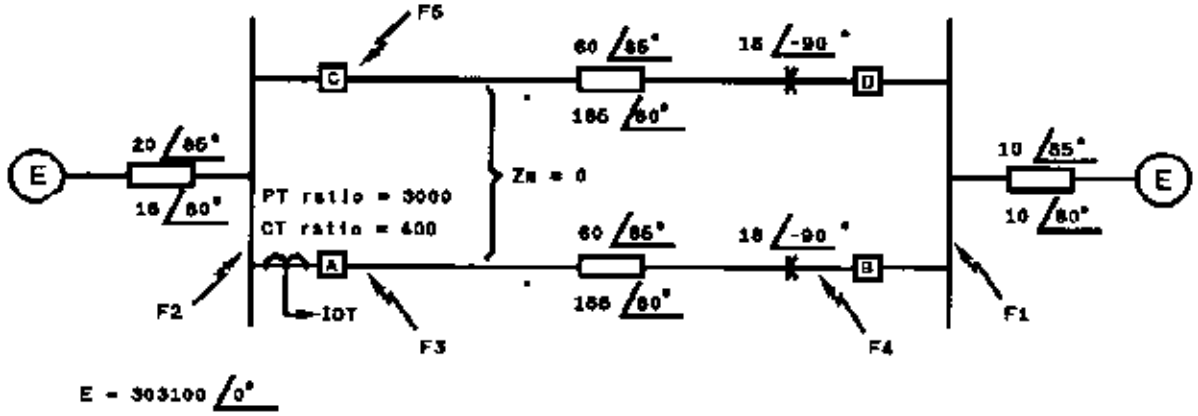


Figure 41 - Sample Power System

Case 3, SLG fault at F3, all breakers closed

I1 = 6187A I0 = 7073A

IDT(operate) = [3(7073) - 6187] = **15032A**

NOTE: If K1 is set to zero, the operating quantity is simply equal to three times (3x) the zero sequence current given above. This must be remembered in determining an appropriate IDT setting if positive sequence current restraint is not used.

Assume for this example that K1 = 1 and that the IDT function is set to pick up at 0.5 per unit amperes. For a 5 ampere rated relay, and for the CT ratio of 2000:5, this transposes to a pickup of 1000 primary amperes. The following can be noted:

1. The function will not operate for Case 1.

2. The function will operate for Case 2, but only after breaker B opens. This will be a sequential trip because operation of IDT follows the opening of breaker B.

3. The function will operate for Case 3. It will be very fast because the operating quantity is 15 times the pickup setting.

Another input is also applied to the energy comparator in addition to the operate signal described above. This signal which uses zero sequence current is effective for close-in heavy faults, and is used to speed up operation of IDT. This input is further described in the setting example provided below.

The IDT function can be directionally controlled by the negative sequence directional functions if desired. Directional control is best used in those applications where the maximum operating quantity that is developed for external faults directly behind the function is greater than the maximum operating quantity developed for external faults at the remote terminal. If the maximum operating quantities are approximately equal for external faults at each end of the line then directional control is not necessary, and its use may be detrimental. For example, consider a fault that occurs at F5 in Figure 41 and then evolves into an internal SLG fault at F3 that is sufficient to operate IDT. If directional control is used, then tripping at F3 cannot occur until the

transient blocking time (established by reset time of blocking function) has elapsed. On the other hand, tripping will occur immediately if directional control is not used.

During the open pole period following a single phase trip, the I1 restraint is increased to provide additional security against trips due to the unbalanced currents.

When using directional control, it is only necessary to evaluate the effects of faults just beyond the remote terminal in determining an appropriate setting. If directional control is not used, then it will be necessary to evaluate the effects of faults directly behind the function as well as at the remote terminal.

ITOC - TIME-OVERCURRENT UNIT

The ITOC very inverse time overcurrent function uses zero sequence current and may be applied with or without positive sequence current restraint. The function is used to provide time-delayed backup tripping for faults involving ground. A block diagram of the function is shown in Figure 42.

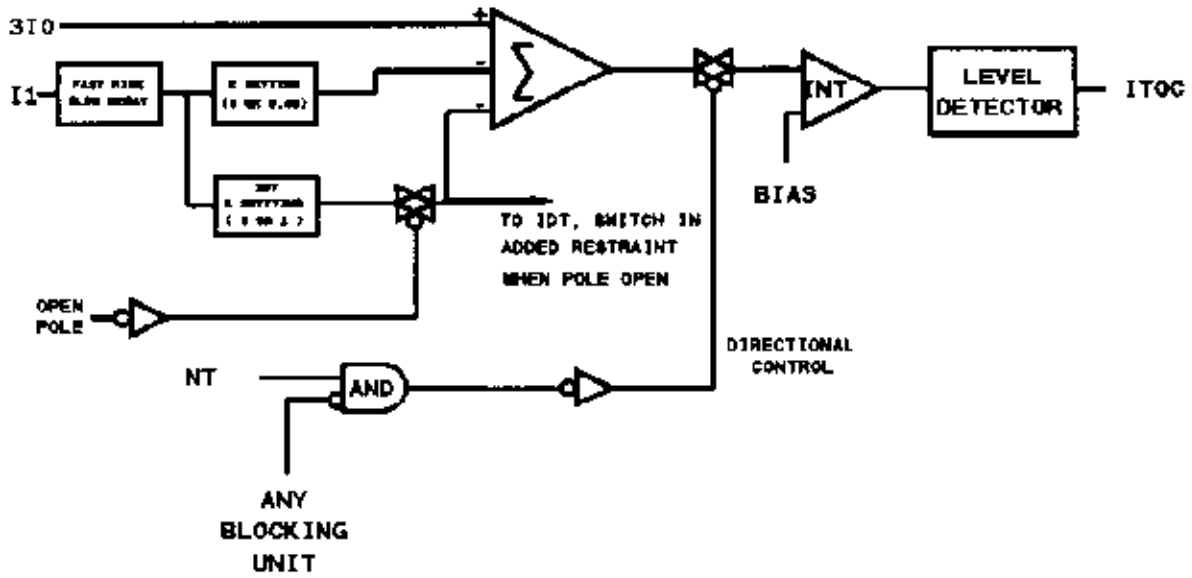


Figure 42 - ITOC Function

It uses the following operating quantity:

$$ITOC(operate) = 3|I0| - K1|I1| \quad (3I0)$$

Where: K1 = 0 or 0.45

Positive sequence current restraint is used to make the function less sensitive to external ground faults. In selecting the settings for ITOC, consideration should be give to:

a. Coordination with other ITOC functions in adjacent lines

b. Coordination with conventional ground TOC functions on adjacent lines

c. Coordination with the zero sequence current produced as a result of an open pole in an adjacent line section

If coordination with conventional ground TOC functions is required, then the suggested approach is to calculate the pickup and time dial settings assuming no positive sequence restraint, but to then use positive sequence restraint in the application. The use of this restraint will provide an additional coordinating margin for ITOC and increase security by preventing undesired operation due to zero sequence error current resulting from load flow over untransposed lines, unsymmetrical gap flashing across series capacitors. During the open pole period following a single phase trip, additional I1 restraint is added to increase security during while the system is unbalanced.

The ITOC function can be directionally controlled by the negative sequence directional functions if so desired. Directional control should be considered if it becomes difficult to coordinate the ITOC function with similar functions in adjacent line sections.

PHASE SELECTORS

The phase selectors in the PLS system are used in the selection of the phase or phases to be tripped during the various types of faults. The phase selectors operate on current only and have no settings or adjustments to be made. The overall block diagram for the "A" phase selector is shown in Figure 43. Identical logic is provided for the phase "B" and phase "C" selectors.

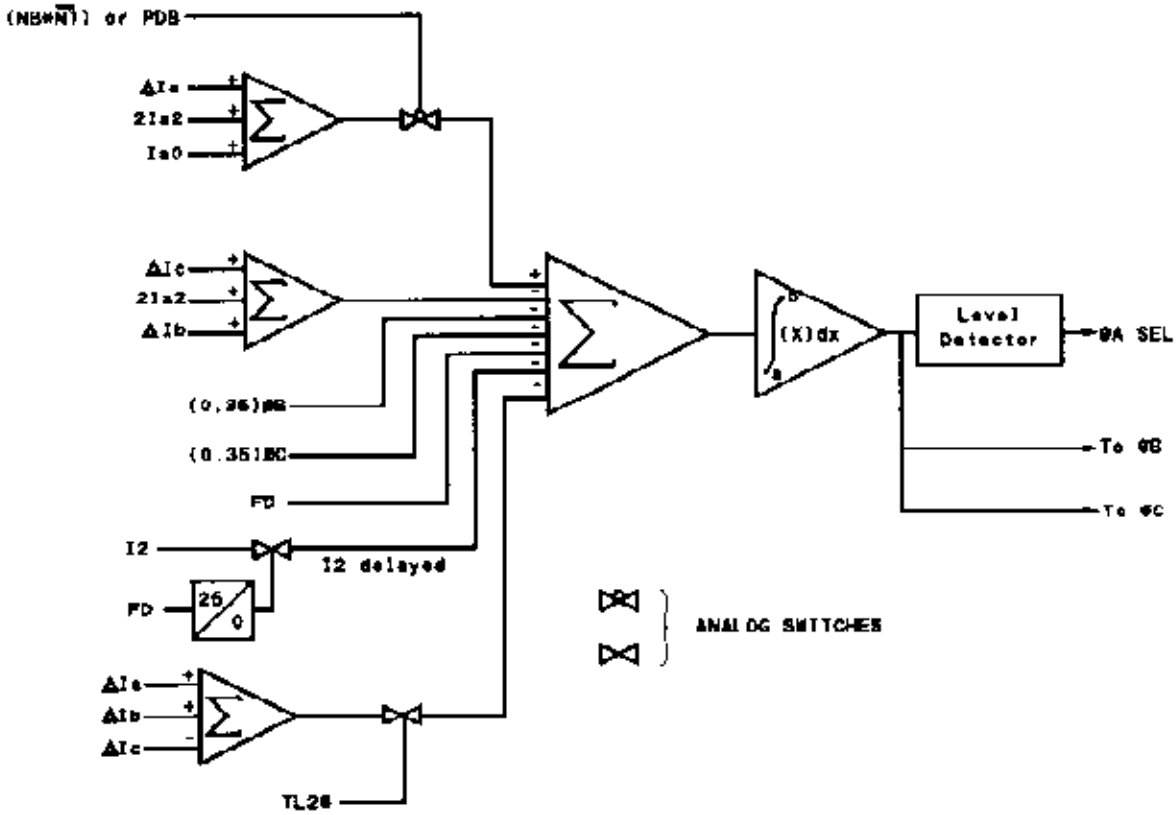


Figure 43 - Phase A Phase selector

Figure 44, taken from Figure 43, shows the basic selection process.

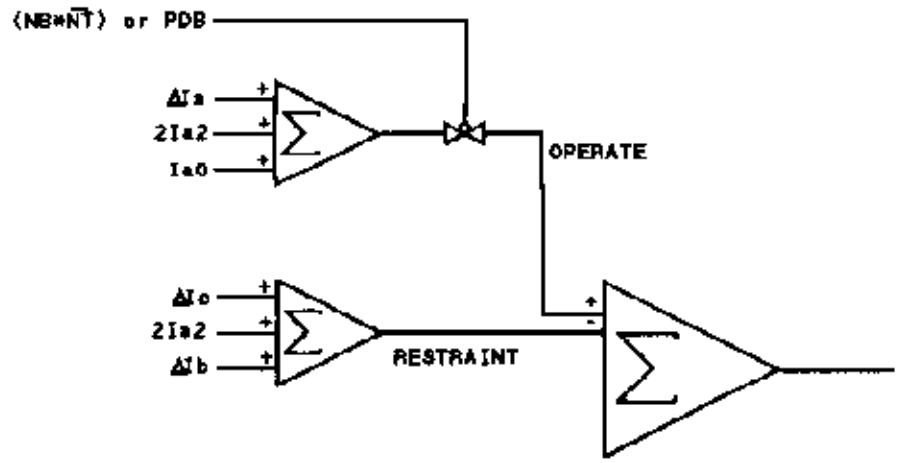


Figure 44 - Phase A Selector, Basic Operation

Operation of the phase A selector occurs when the operate quantity exceeds the restraint quantity. Note that the operate quantity will not be applied to the summing amplifier if the fault is in the reverse direction because an output from the PDB or NB functions will turn the analog switch off. In other words, the phase selector can only operate for faults in the forward direction.

Some of the restraint inputs to the summing amplifier are shown in Figure 45 with the remainder being shown in Figure 46.

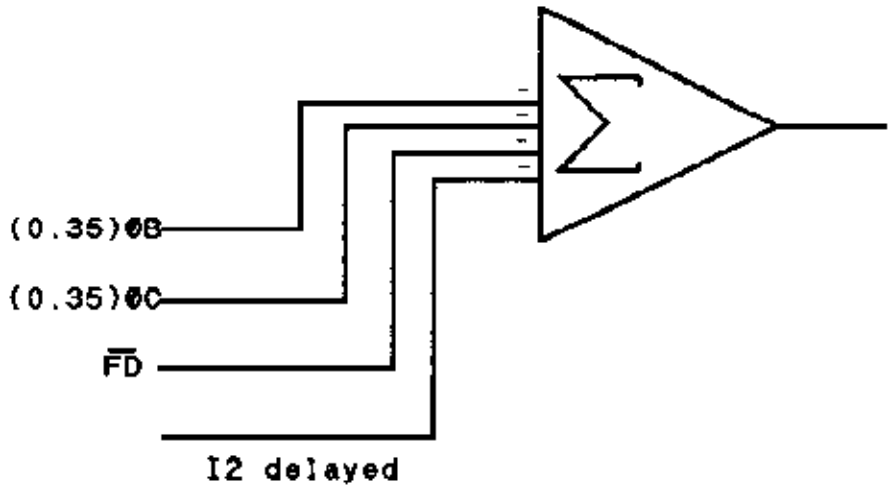


Figure 45 - Restraint Inputs to Phase A Selector

Thirty five percent (0.35) of the output of the phase B and phase C selectors is used to provide restraint to the phase A selector. Similarly, phase A will provide 35 percent of its output to restrain the phase B and phase C selectors. The input from the fault detector (NOT FD) prevents the phase selectors from operating during steady-state conditions when the fault detector will not be picked up. The I2 delayed input provides additional restraint 25 milliseconds after the fault detector operates. This input is used to prevent operation of the unfaulted phase selectors because of the low frequency transients that could be present when series capacitors are used on the power system.

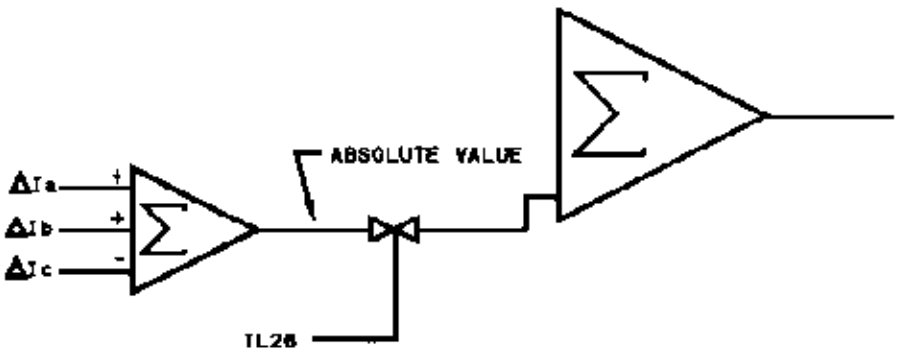
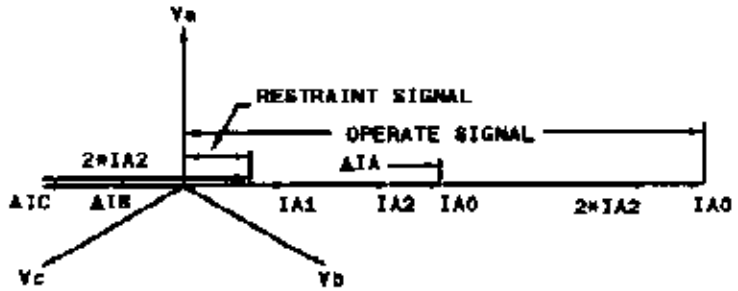


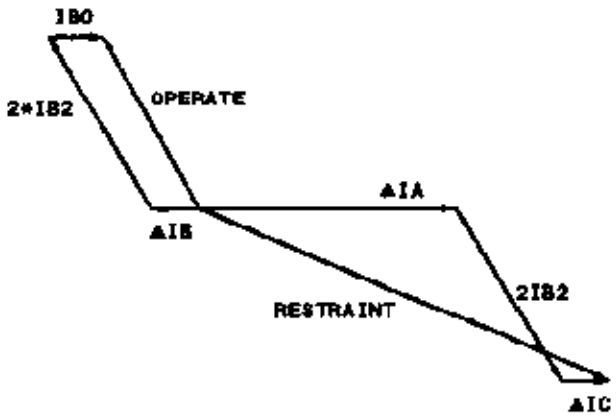
Figure 46 - Restraint Inputs to Phase A Selector

The restraint input shown in Figure 46 is applied only after timer TL26 times out. This restraint input is used to block operation of the phase selectors during the change in current that can occur when the breaker operates to clear the fault. Timer TL26 is energized when a trip output is produced and is set so that it will time out just before the breaker poles open to clear the fault.

Operation of the phase selectors can be analyzed via the phasor diagrams shown in Figures 47 and 48.

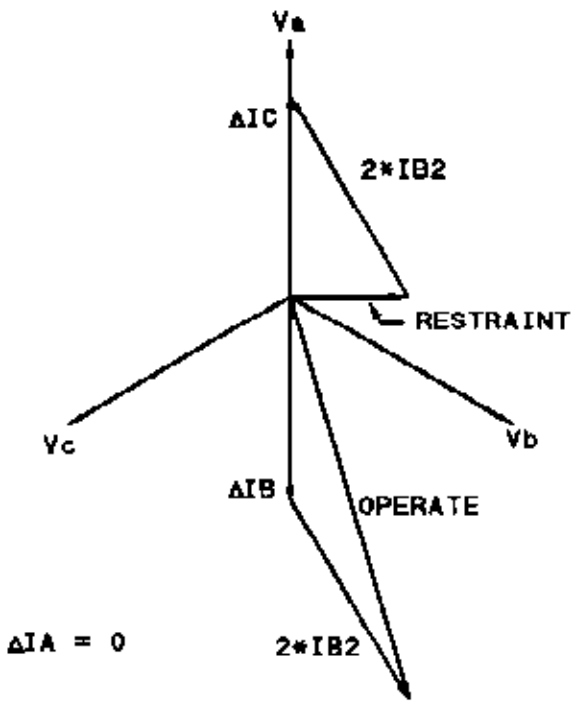


PHASE A SELECTOR

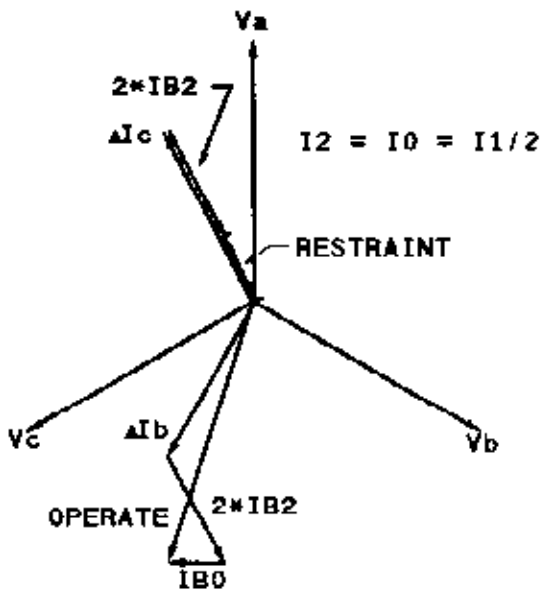


PHASE B SELECTOR

Figure 47 - Phase A and B Selectors for A-G fault



a. BC FAULT



b. BCG FAULT

Figure 48 - Phase B Selector for BC and BCG Faults

For each fault type shown in the Figures, it can be seen that the operate signal is greater than the respective restraining signal for the selector associated with the faulted phase. On the other hand, the restraint signal is greater than the operate signal for the selectors associated with the unfaulted phase as shown in Figure 47.

It is often asked why the negative sequence signal (2*IA2 for the A phase selector for example) is used in both the restraint and operate circuits. Careful examination of the operate signal and restraint signal of Figure 47 will show the reason why. For the faulted phase selector, the negative sequence signal adds a component to the operate signal that increases its magnitude significantly. On the other hand, the negative sequence component of the restraint signal cancels out the changes (deltas) in the IB and IC components to reduce the restraint signal significantly. Since the operate signal is much greater than the restraint signal, operation of the function is enhanced.

For the unfaulted phase selector (Figure 47), the negative sequence components effectively cancel so that the remaining restraint inputs predominate to prevent operation.

CONTINUOUS MONITOR

The continuous monitor is used to monitor up to 40 points in the PLS1 system. It recognizes a change in state of one or more of up to 40 monitored points as an abnormal relay condition if this change in state occurs without a concurrent output from the fault detector described earlier. The module operation can be described functionally with the aid of Figure 49.

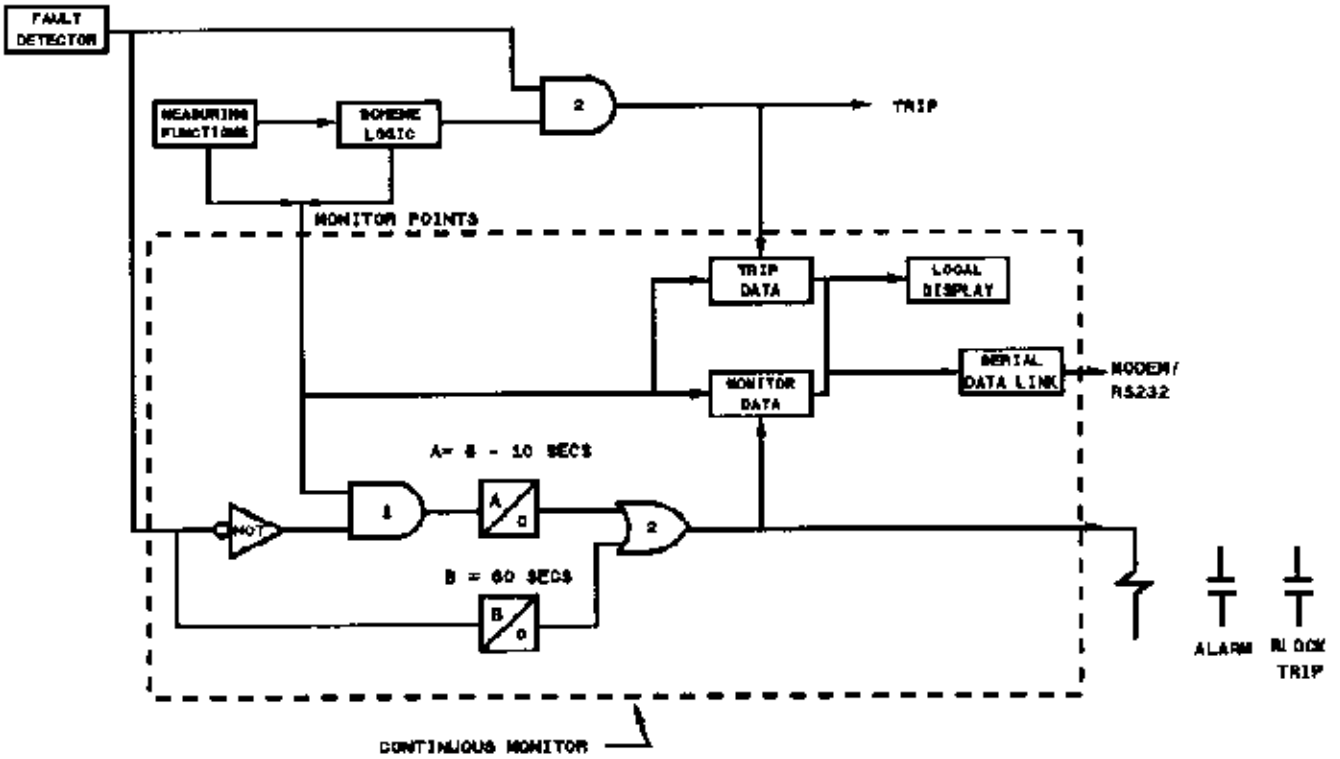


Figure 49 - Continuous Monitor Logic

If one or more of the monitored points changes state (either logic level 0 to 1 or logic level 1 to 0) without a concurrent output from the fault detector, and if this condition persists for 5-10 seconds, then the Continuous Monitor module issues an output to indicate that an abnormal condition has occurred. An output is also produced if a fault detector output persists for 60 seconds. This would be an indication that the fault detector itself had failed or that the power system itself had a significant load current imbalance. Once an abnormality has been detected, the information is stored in non-volatile memory. Since non-volatile memory is used, the data is not lost if the DC power supply is turned off or the DC is removed externally.

The primary function of the Continuous Monitor module is to detect and to alarm for a relay-system abnormality. The other function is to store in non-volatile memory those monitored points that have changed state during a PLS1 relay system trip output. Following a trip output, the Continuous Monitor module scans the monitored points for 10 milliseconds. Any points that change state within this 10 millisecond interval are accumulated in memory as trip data. This can be useful in analyzing relay system response to particular faults. This function and its memory are separate and distinct from the primary function of detecting relay system abnormalities. The Continuous Monitor module can have both "trip data" and "monitor data" in memory at the same time.

Data for five (5) trip events will be stored sequentially. If a sixth trip event occurs prior to the memory being cleared, then the data for the first trip event will be overwritten by the data for the sixth trip event. Thus the data for the five most recent trip events will be retained.

For local access, the two LEDs on the front panel of the module indicate that monitor data and/or trip data are stored in memory. A DATA SELECT toggle switch is used to select which data are to be accessed. A step display pushbutton is then pushed repeatedly to cause the stored points to be displayed via the two-digit point number LED numeric display.

For remote access, a serial data link must be supplied. The Continuous Monitor module includes the necessary software to operate with a serial data link and the chassis backplane wiring connects the input/output ports to a 25-pin connector on the rear of the chassis. This connector resembles an RS-232 connector, but it does **not** provide an RS-232 interface. To provide serial data transmission, an optional, small, fiber-optic transmitter/receiver module can be supplied.

The serial data link option provides the user with the capability of remotely interrogating the Continuous Monitor module to read the data in memory and to clear the memory.

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